EE-677: Foundation of CAD for VLSI

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Introduction





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VLSI Realization Process

Customer's need

Determine requirements

Write specifications

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer





Conventional SoC Design Flow

Bug Fix

Bug Localization

Verification/Sim ulation

Pre-Silicon RTL Verification

High-Level Description

High-Level Synthesis

Machine-Generated RTL

Logic Synthesis Place & Route



Design

75% of the whole development time [Source: Intel 2007]

Respin



Need to Understand RTL **Bug Fix**

Bug Localization

Error Detection

Post-Silicon RTL Validation



Design Optimization Parameters

- Area
- Performance
- Testability
- Power
- Security
- Intelligence





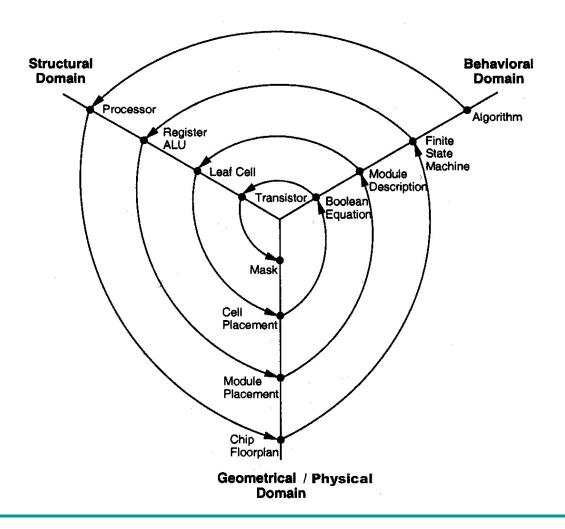
Structured Design

- **Hierarchy**: Divide and Conquer
 - Recursively system into modules
- Regularity
 - Reuse modules wherever possible
 - Ex: Standard cell library
- Modularity: well-formed interfaces
 - Allows modules to be treated as black boxes
- Locality
 - Physical and temporal





Gajski Y-Chart







Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.





Thank You



