Computer Aided Design

An Introduction

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EE-677: Foundations of VLSI CAD

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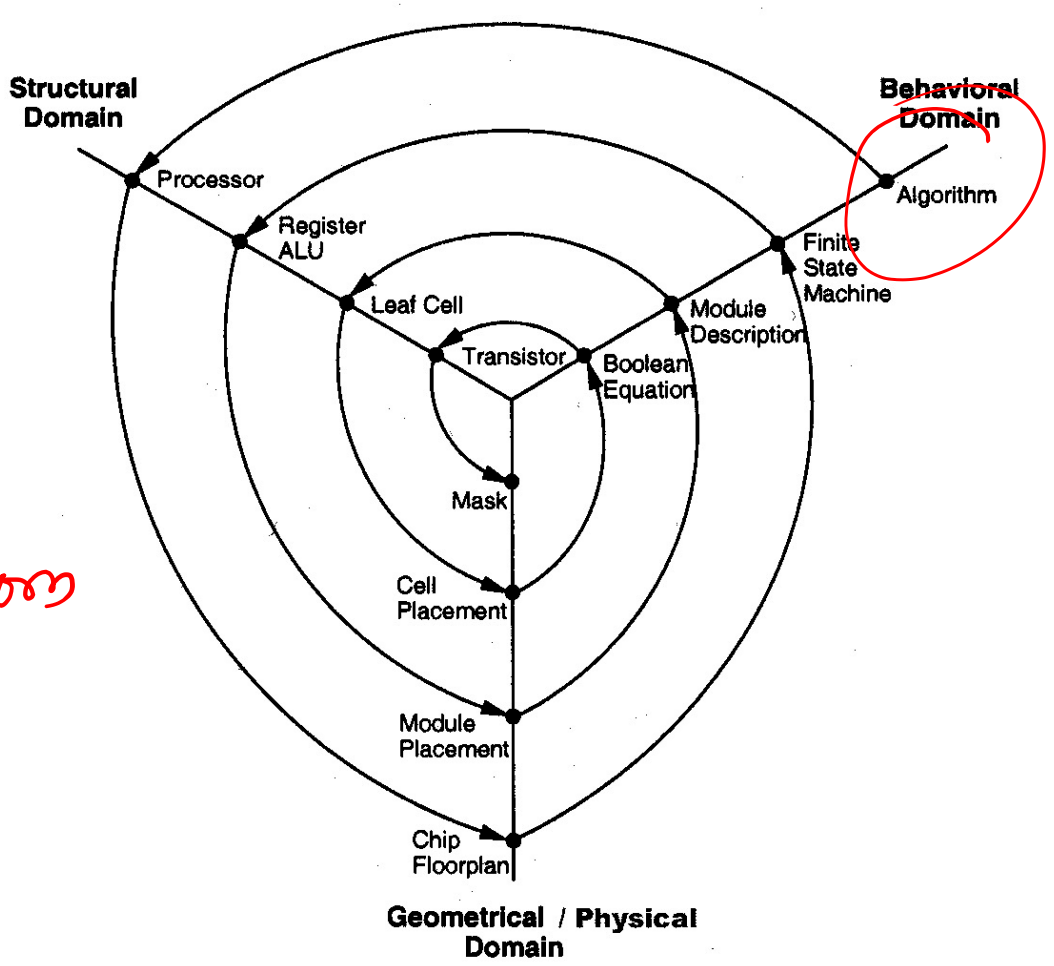
CADSL

Coping with Complexity

- How to design System-on-Chip/ System-of-systems?
  - Billions of transistors
  - Tens to hundreds of engineers
- Structured Design
- Design Partitioning

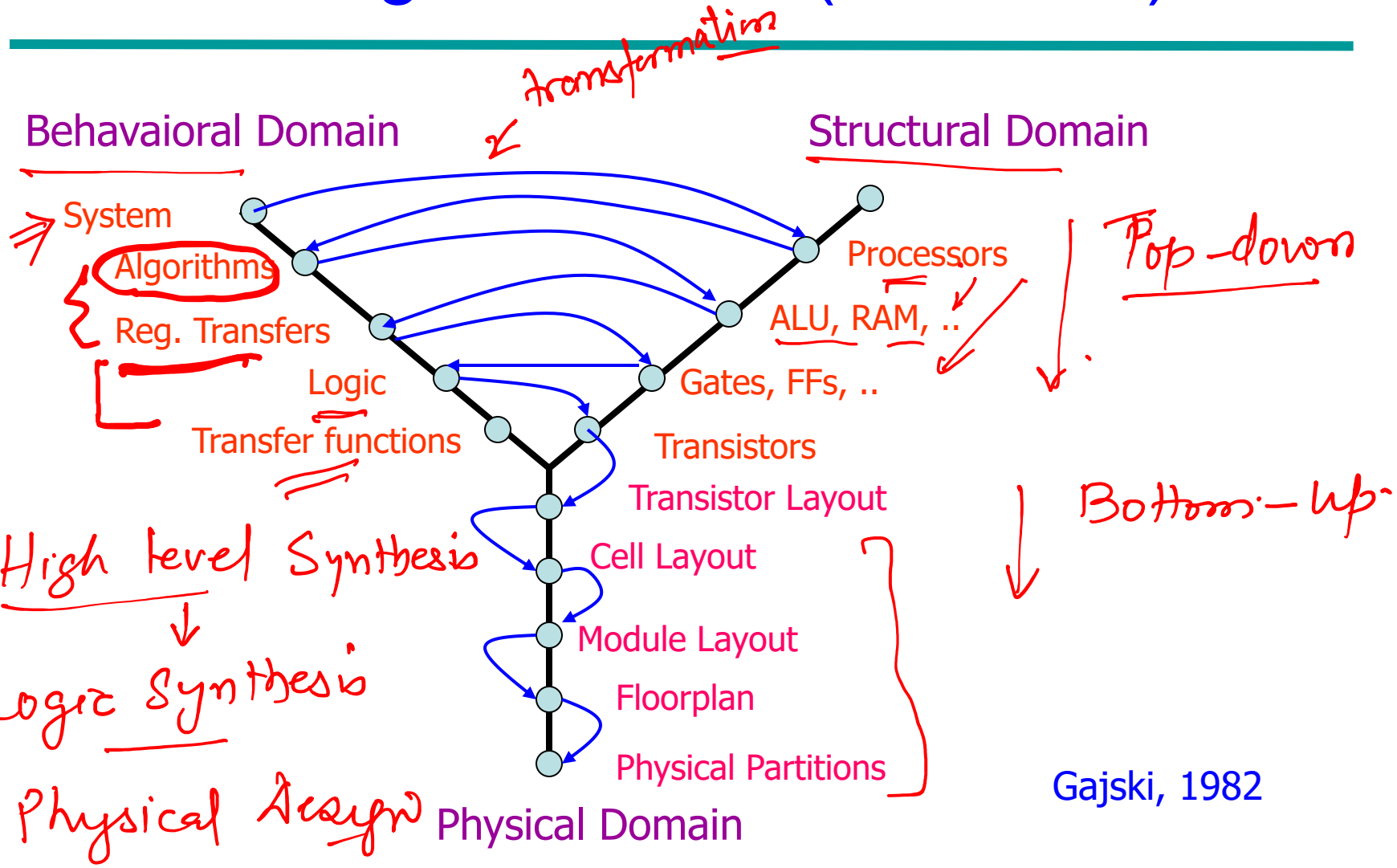
Gajski Y-Chart



Top. down

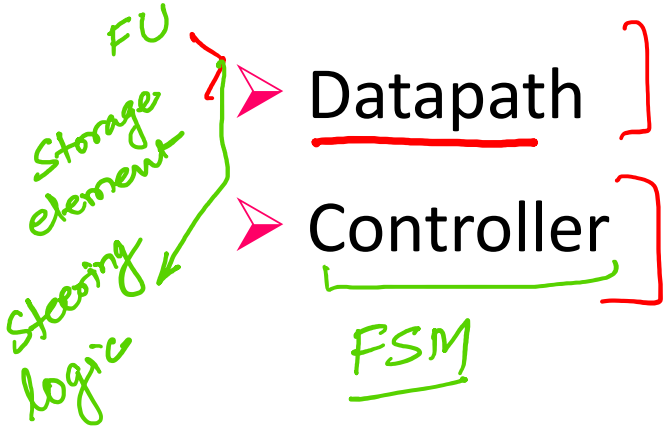
Bottom up

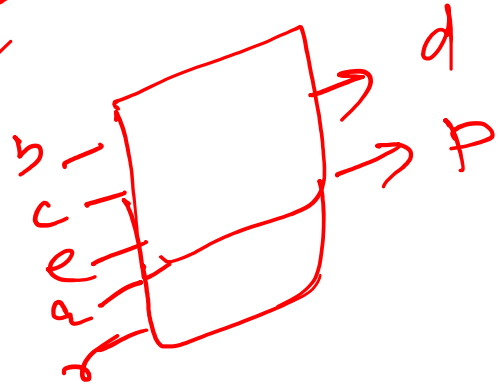
Design Domains (Y - Chart)

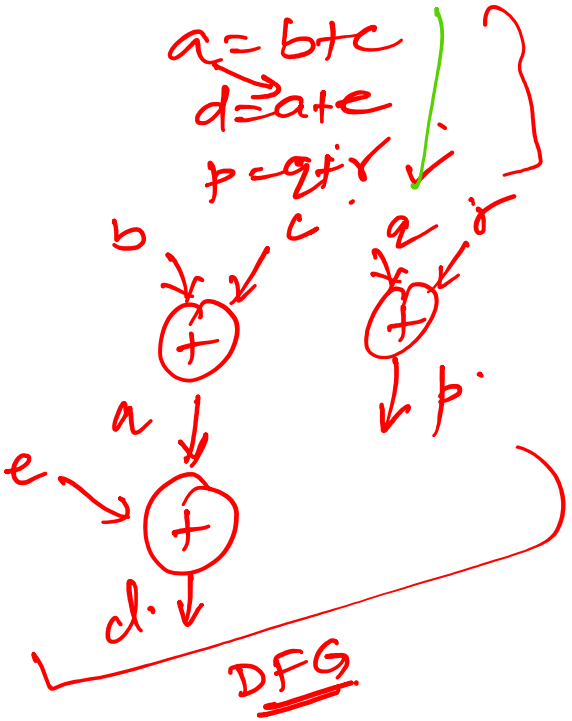


High Level Synthesis

Architectural Level Abstraction



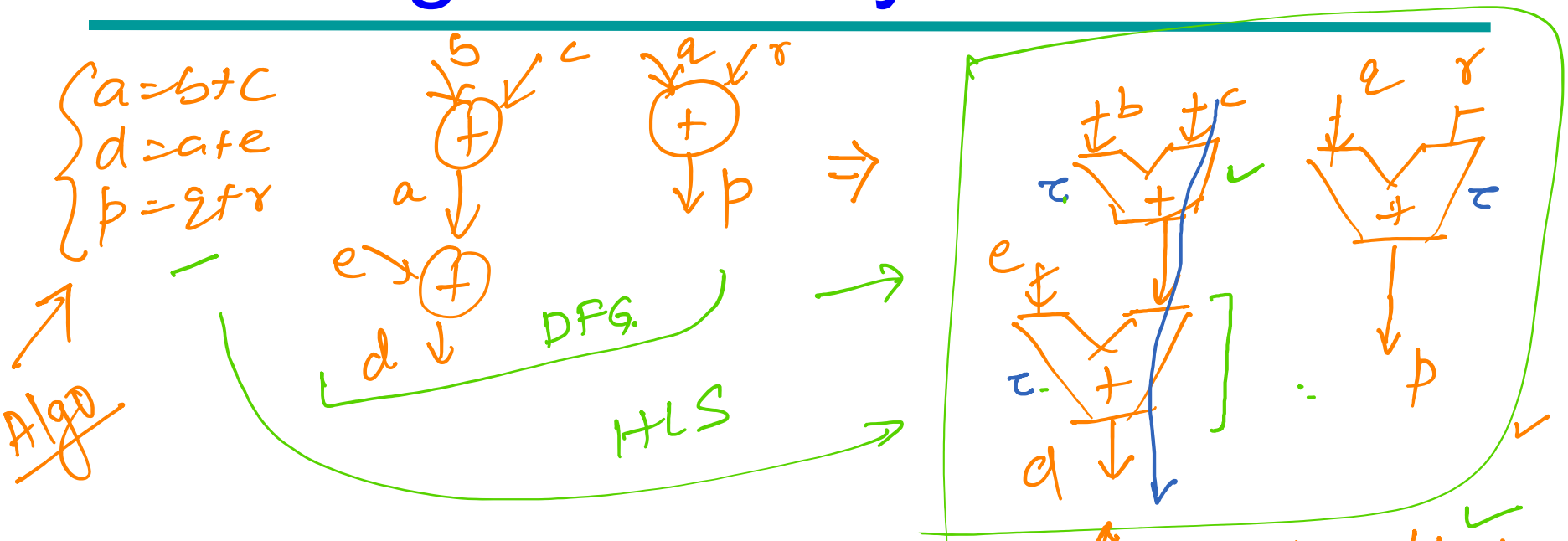




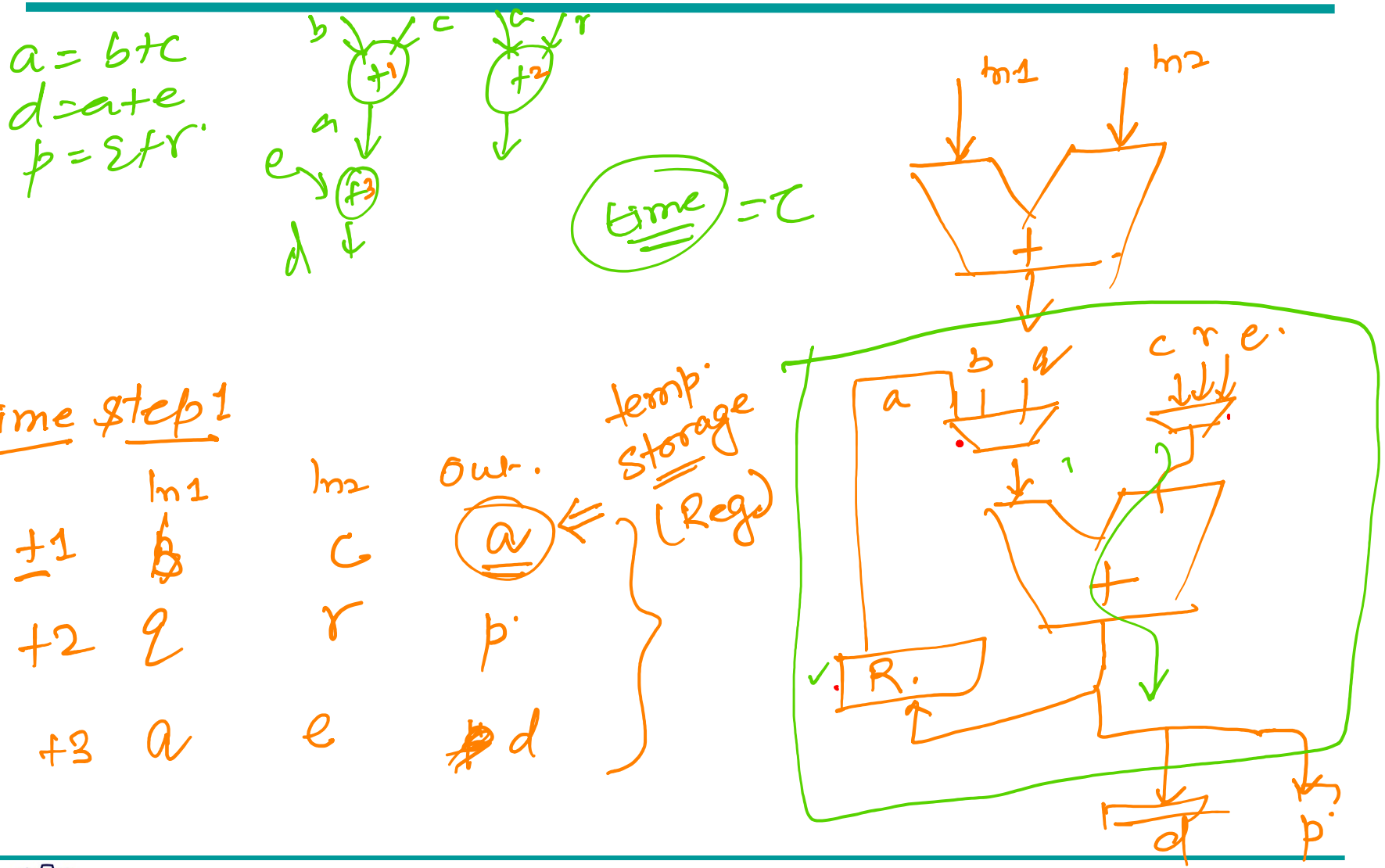
Architectural/High Level Synthesis

- Constructing the macroscopic structure of a digital circuit starting from behavioural models that can be captured from Data flow or Sequencing Graph

High Level Synthesis



High Level Synthesis



High Level Synthesis

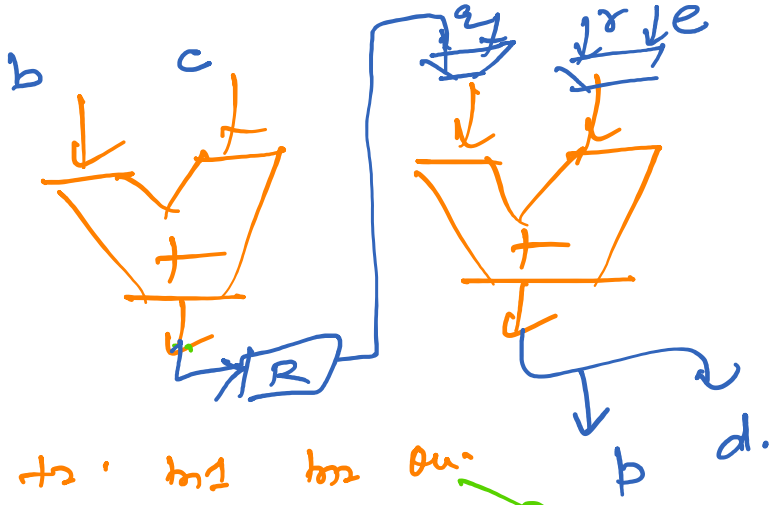
Cost = $x + \delta$

delay = 3τ = 3τ

Power = $x + \delta$

High Level Synthesis

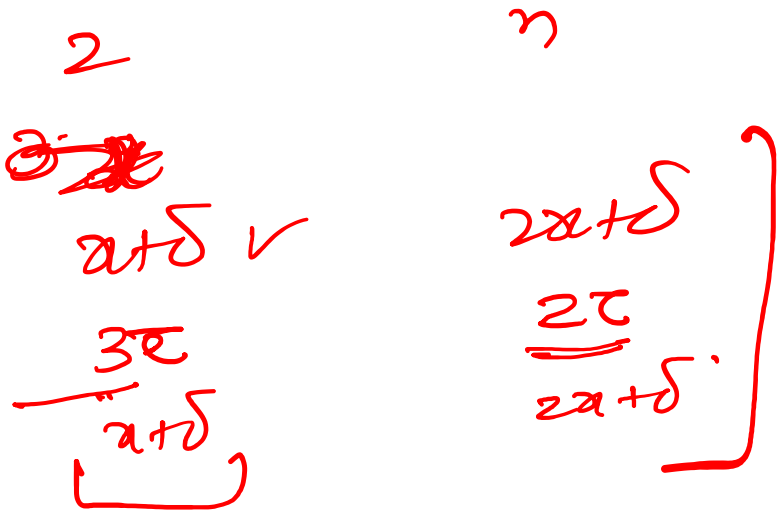
$a = b + c$ ✓
$d = a + e$
$p = q * r$ ✓



Step	fu	in1	in2	out	in1	in2	out
1	+	b	c	a	q	r	p
2	+	a	e	d			

Cost = $2x + \delta$
delay : 2τ
power : $2n + 5$

High Level Synthesis



Thank You