High Level Synthesis

$\Rightarrow$ Testability

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EE-677: Foundations of VLSI CAD

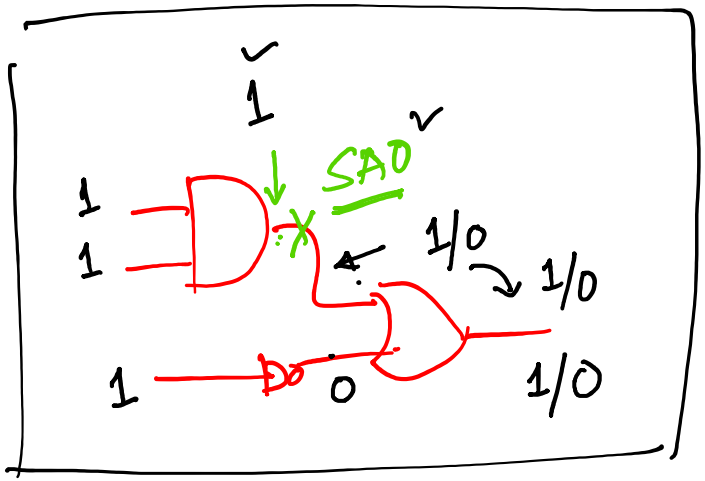
Lecture 13 on 31 August 2021

CADSL

TESTABILITY

↓

{Controllability
Observability}



[TESTING → ensures quality of hardware.]

↓

{Test each & every circuit}

DEFECT

↓

[FAULT] ← SSAF

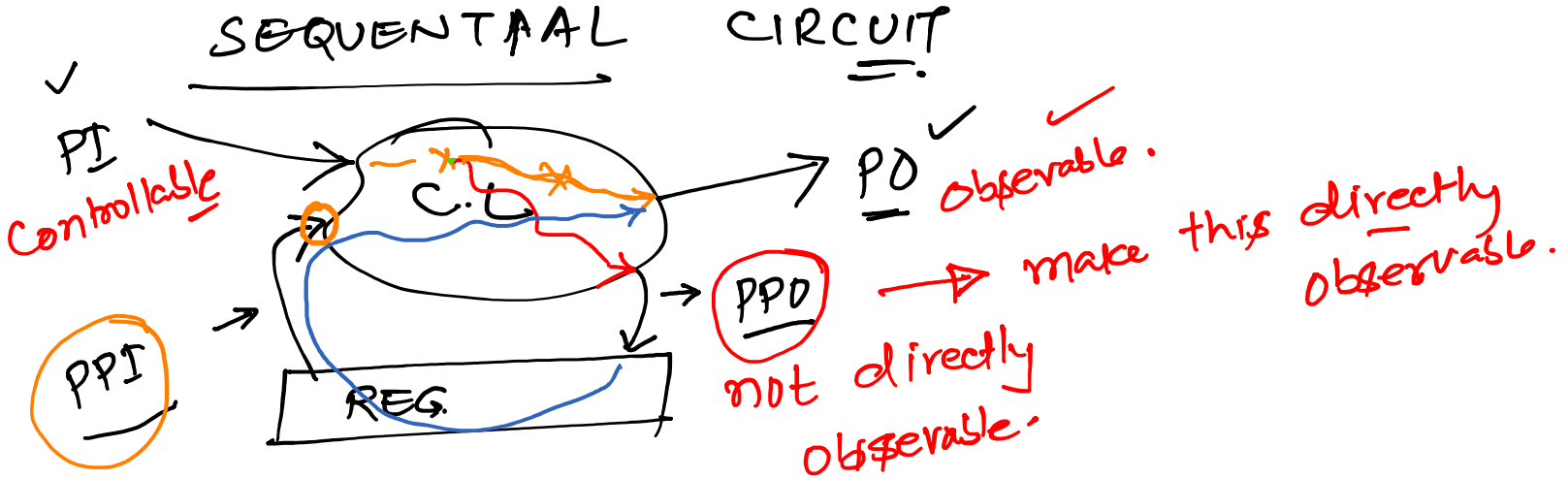
[s-a-0
s-a-1]

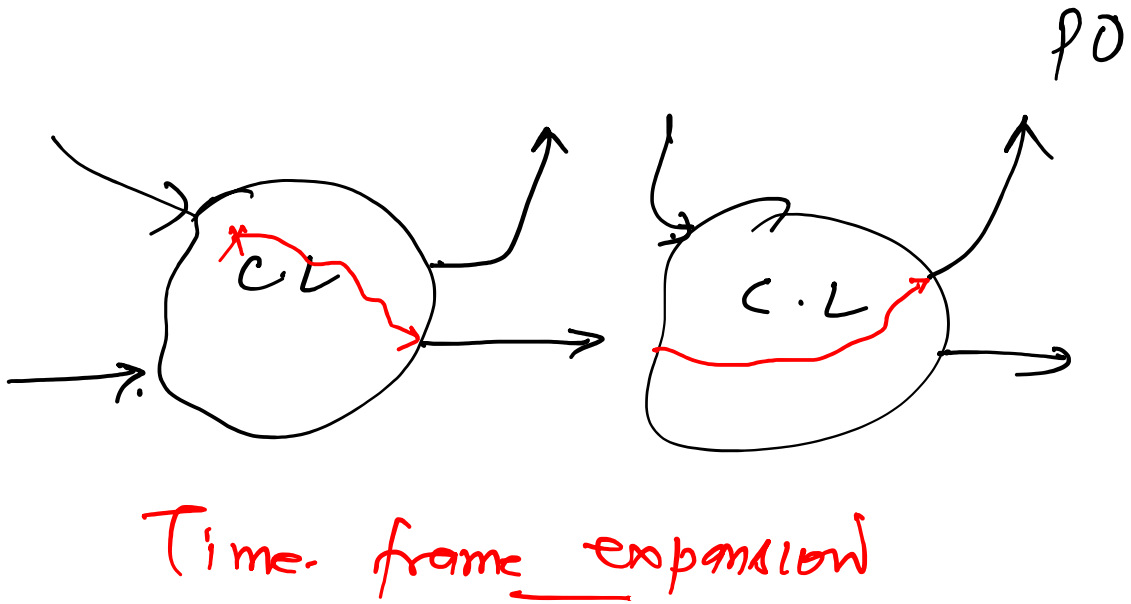
{#test ∝ # nets
∝ # gates}

High Level Synthesis

Objective

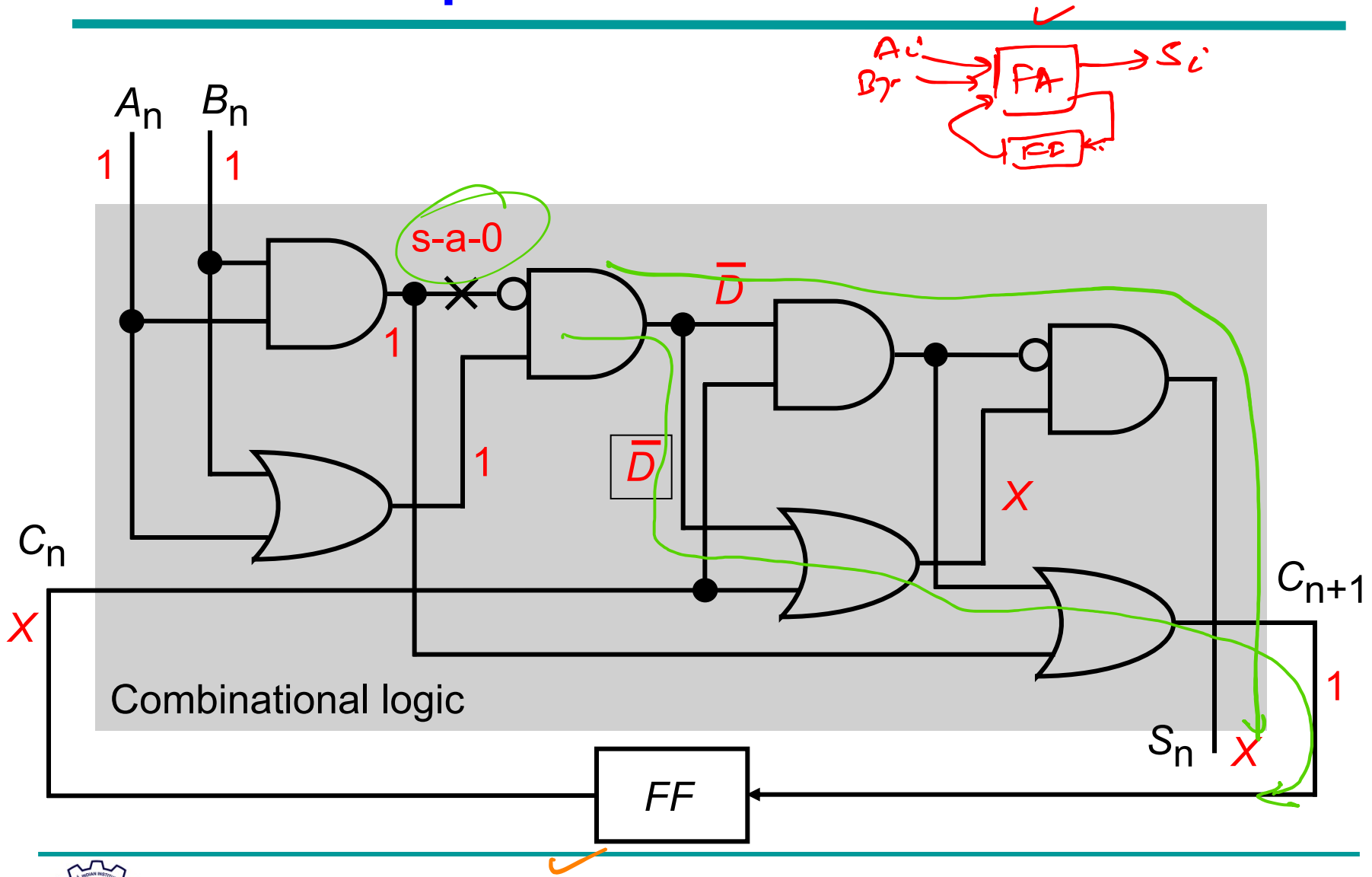
- Area
- Performance
- Power
- Reliability



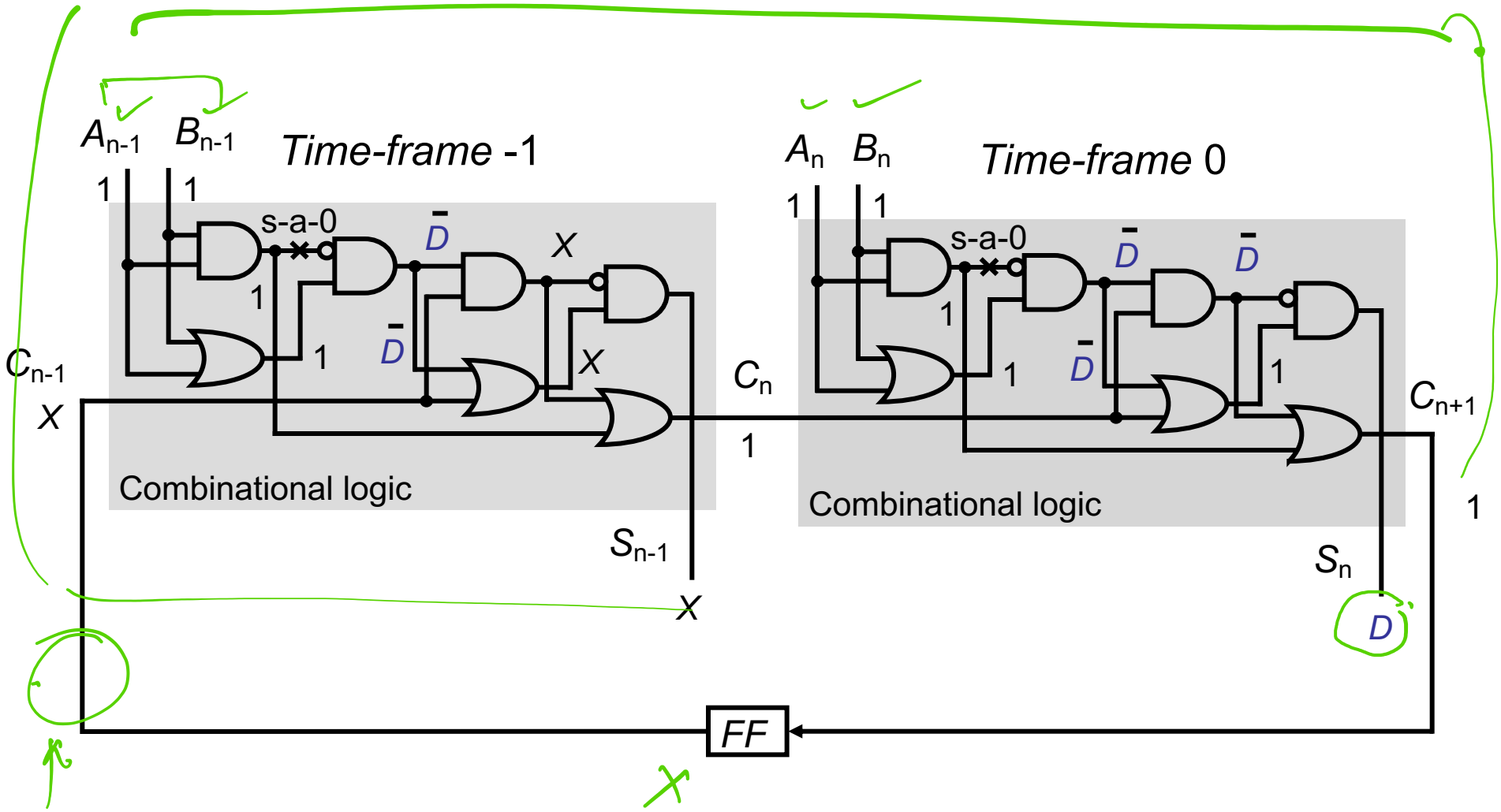


Time frame expansion

Example: A Serial Adder

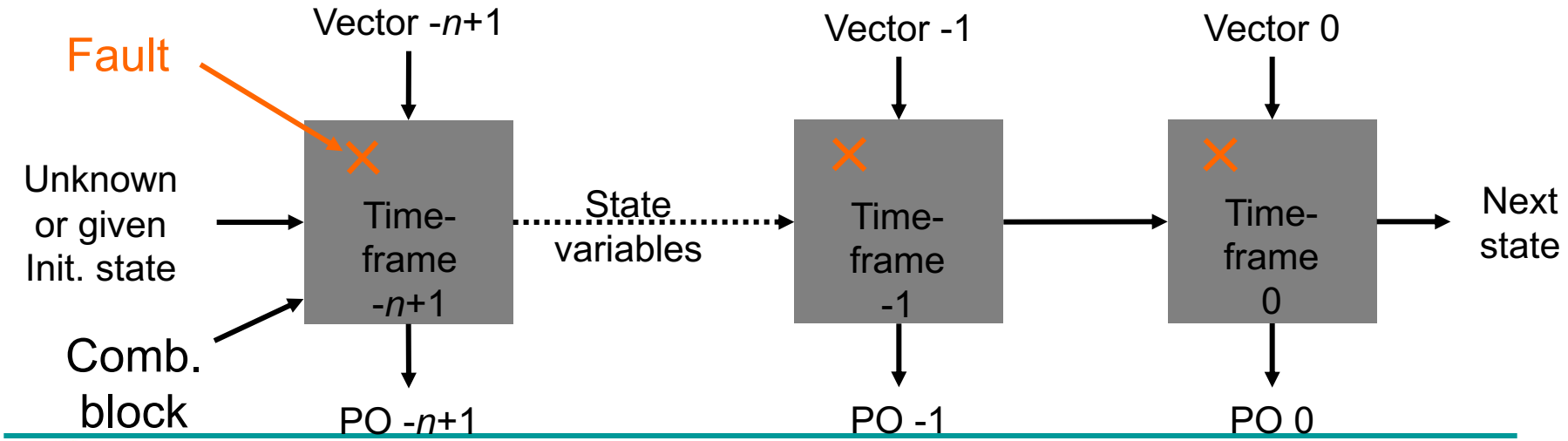


Time-Frame Expansion

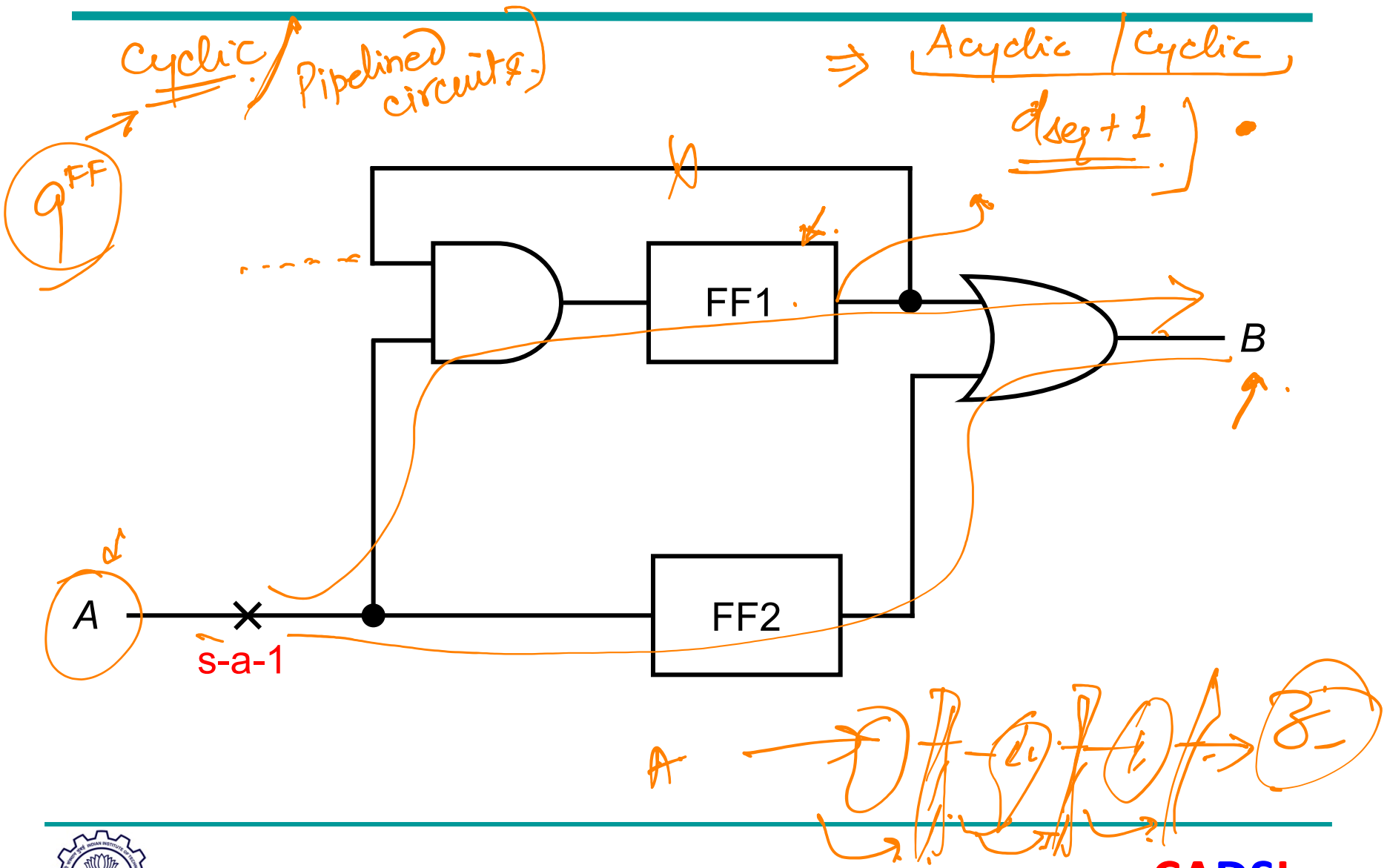


Concept of Time-Frames

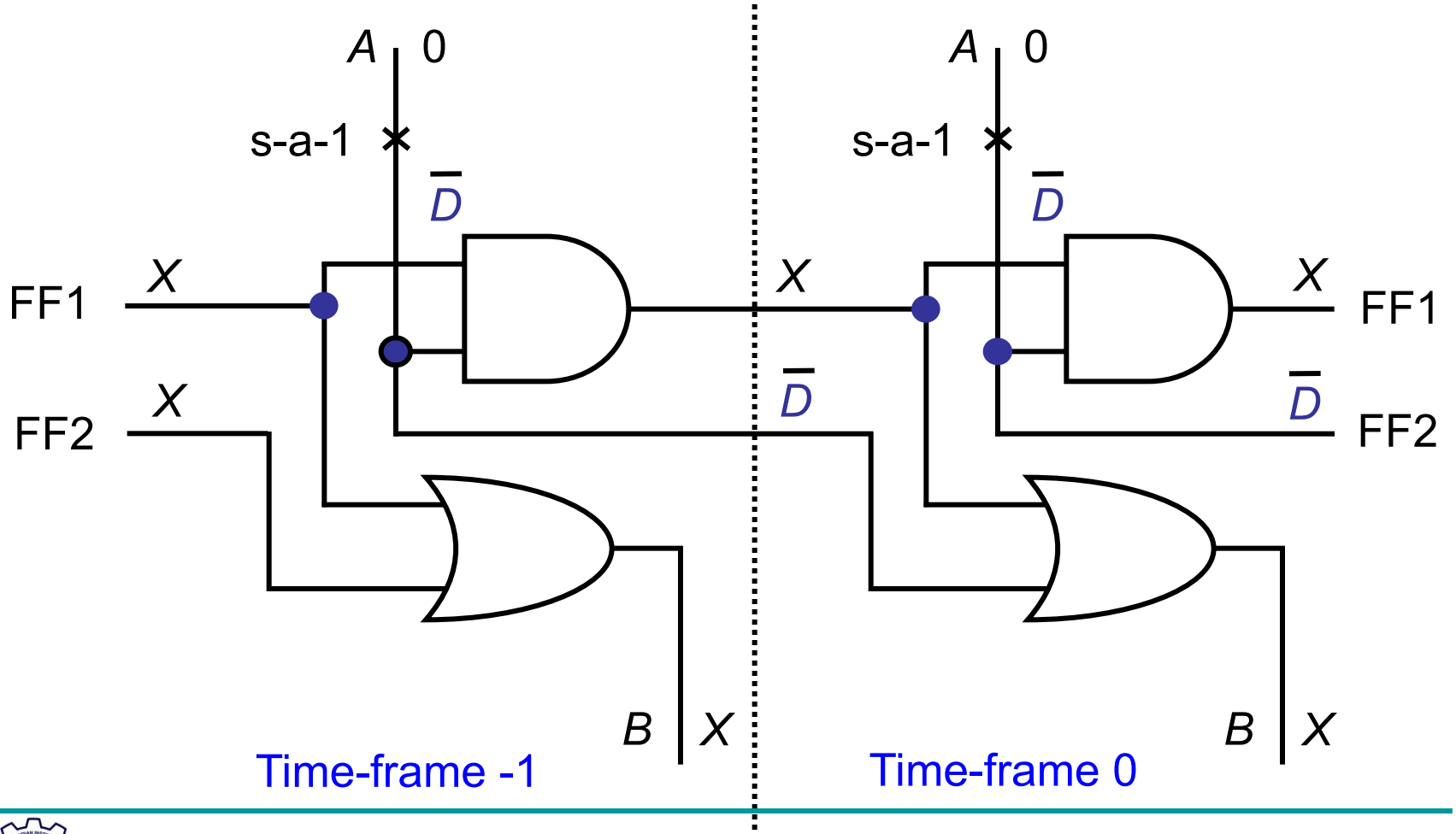
- If the test sequence for a single stuck-at fault contains *n* vectors,
  - Replicate combinational logic block *n* times
  - Place fault in each block
  - Generate a test for the multiple stuck-at fault using combinational ATPG with 9-valued logic



Example for Logic Systems



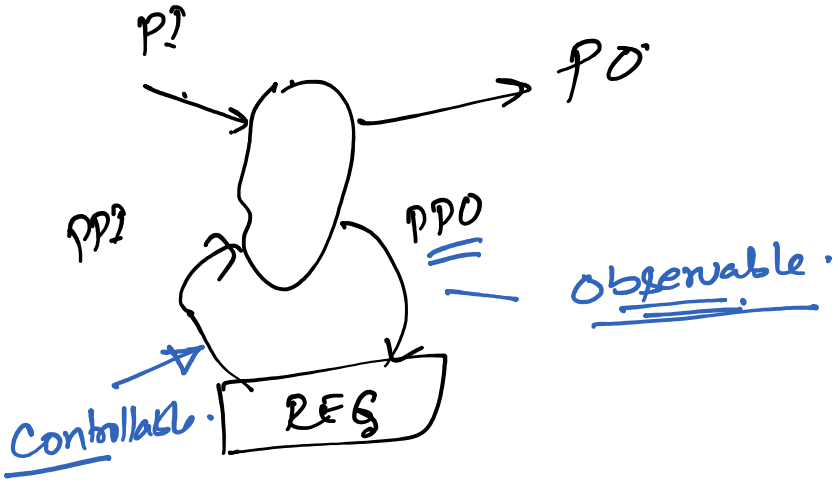
Time Frame Expansion



Testability

Objective

- To improve
  - Controllability
  - Observability
- Reduction in sequential depth → Reduces complexity of test generation

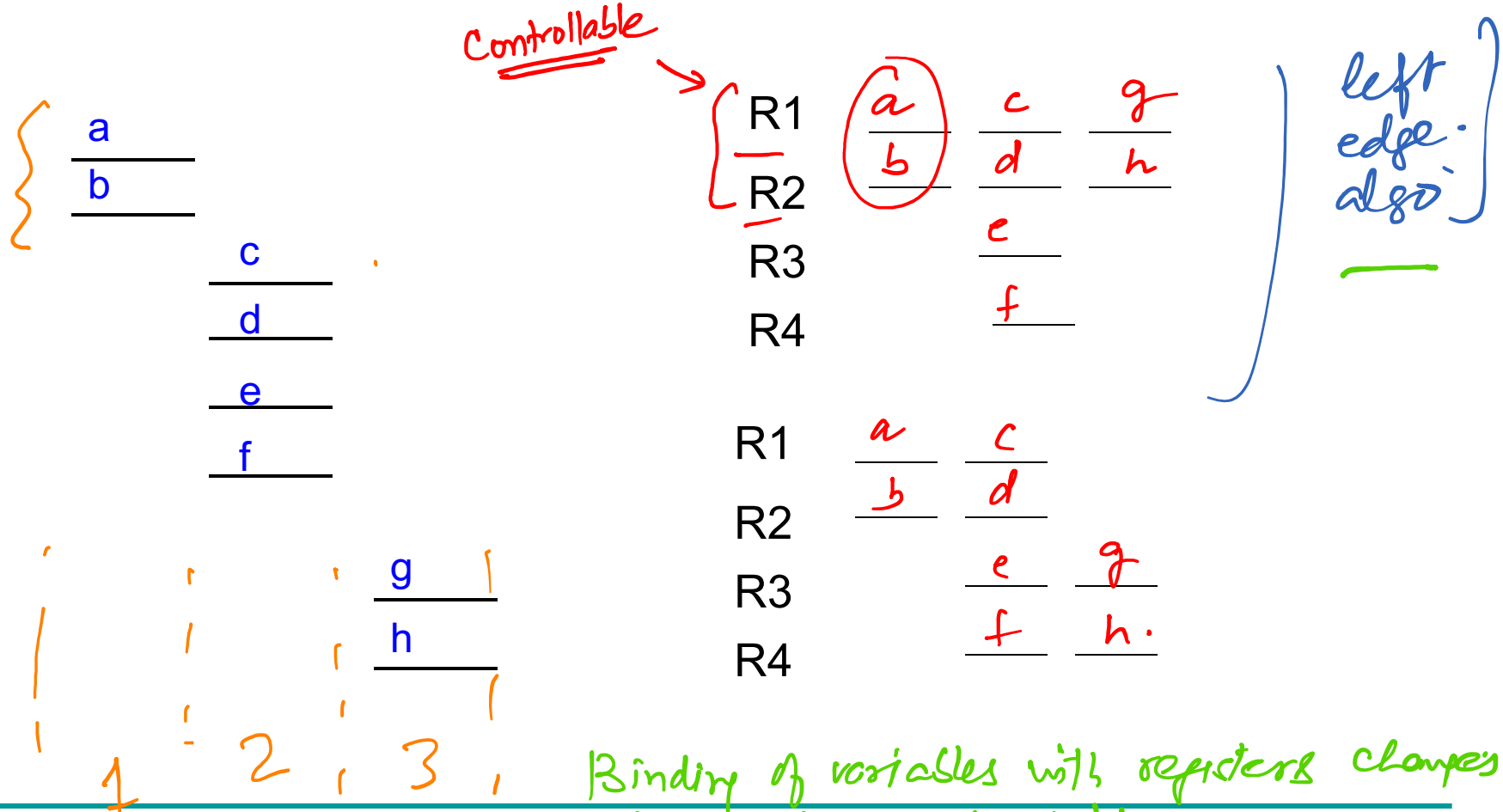


OPERATIONS / VARIABLES.

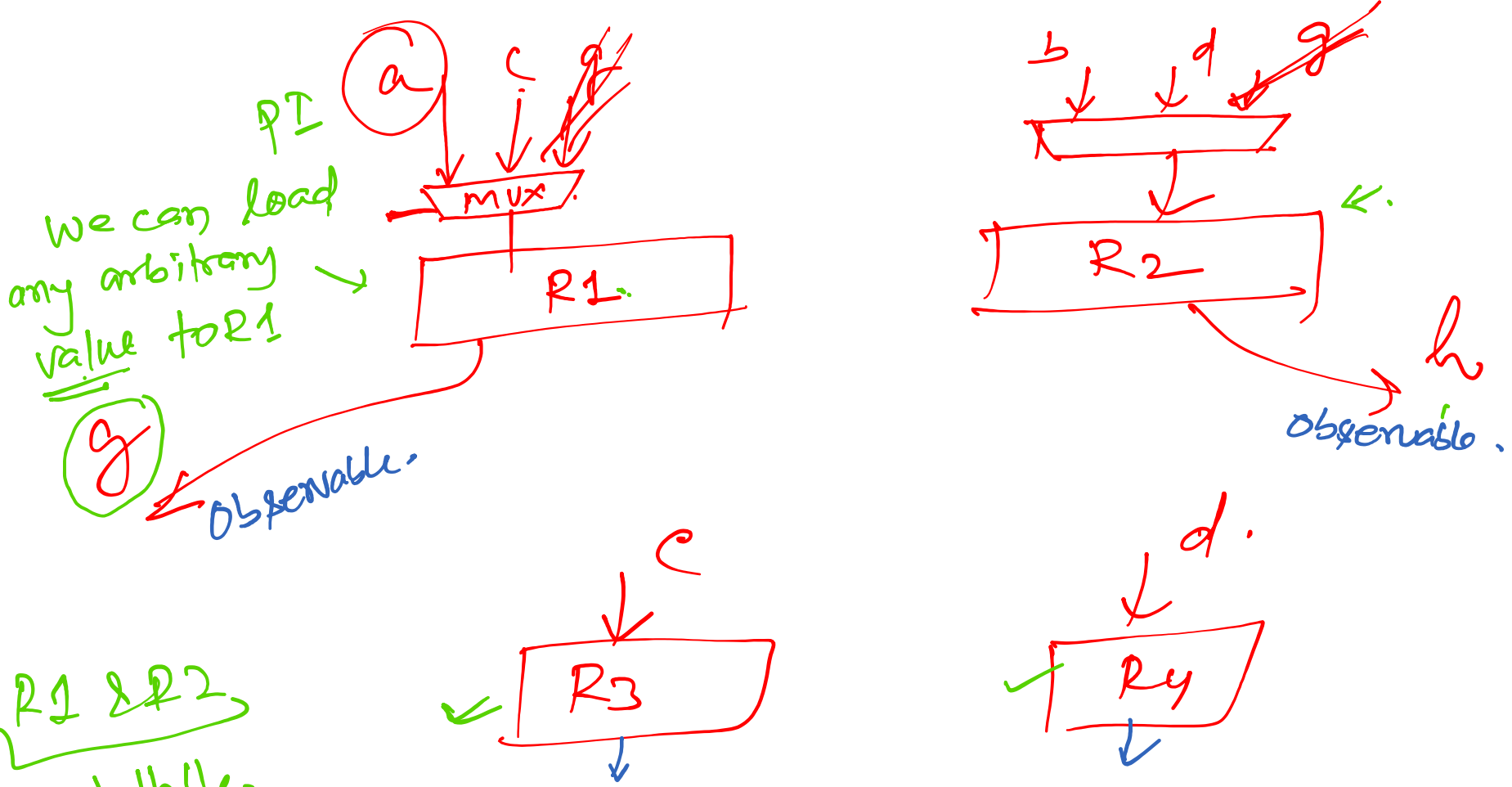
Controllability and Observability

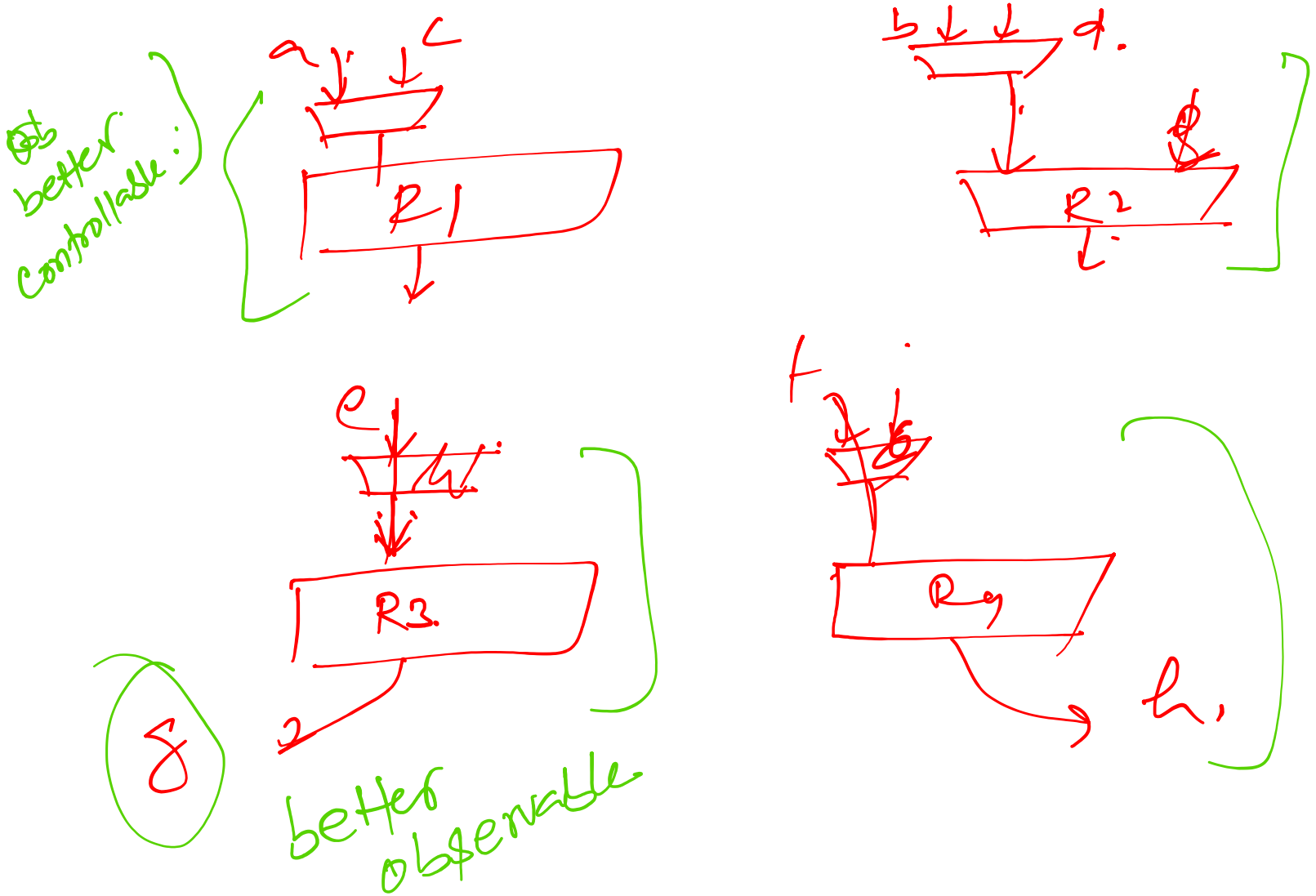
PI : a, b PO : g, h DFG

Controllable →



Binding of variables with registers changes the observability & controllability of the circuit.

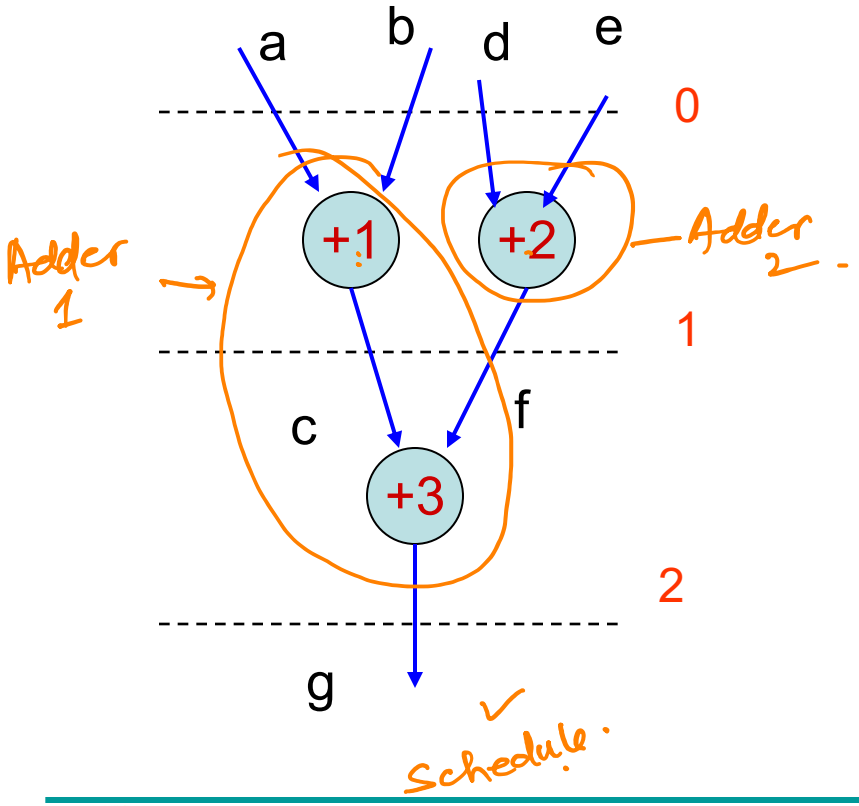

PI
a
c
MUX
R1
we can load any arbitrary value to R1
g
observable.
b
d
g
R2
h
observable.
c
R3
d.
R4
R1 & R2
controllable
R3 & R4
not
R1 & R2
observable.
R3 & R4
not observable.

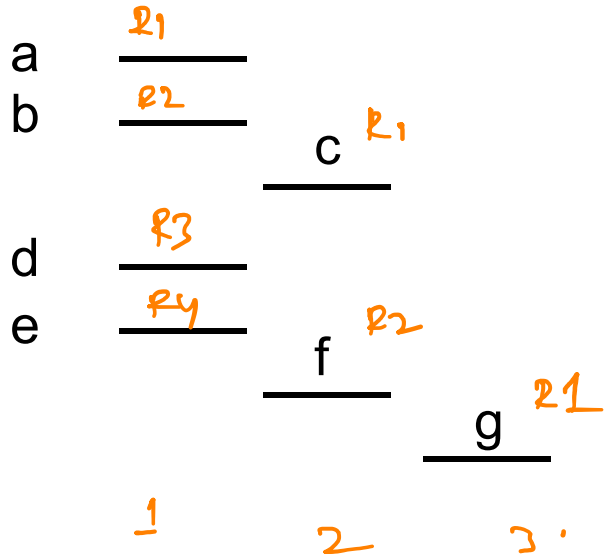

better controllable
R1
R2
R3
R4
better observable

Sequential Depth

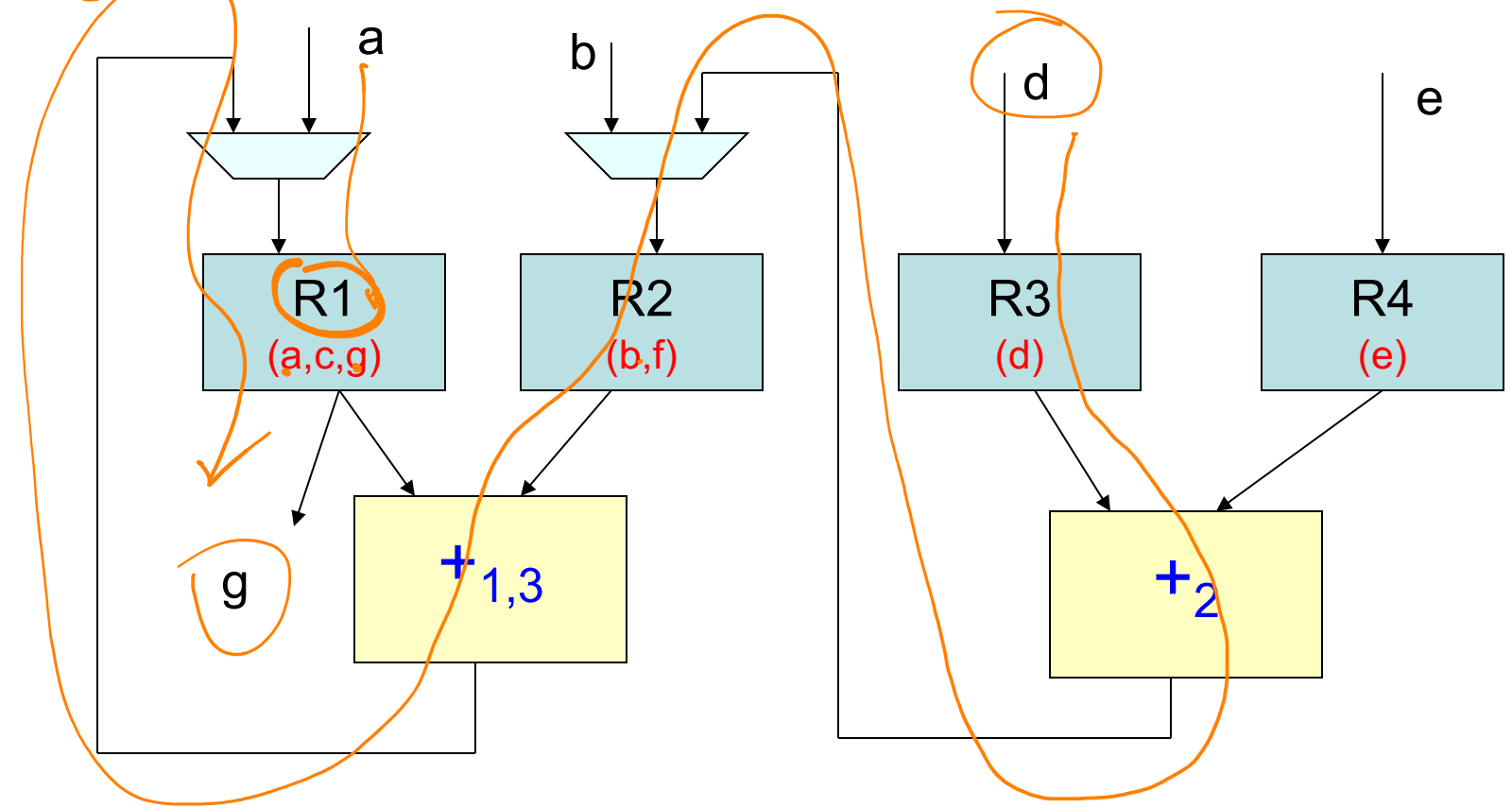
DFG.

c = a+b
f = d+e.
g = c+f

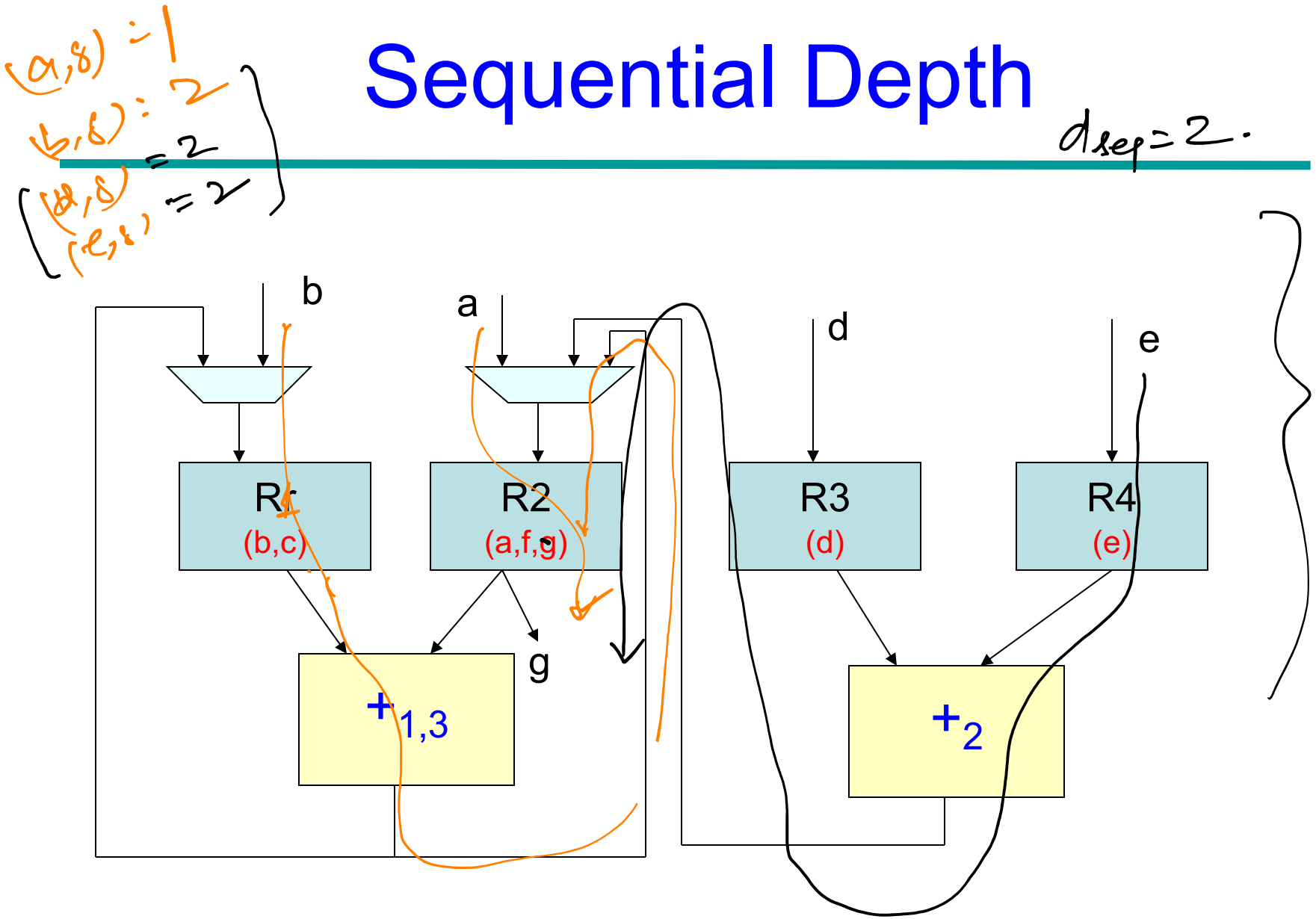




Sequential Depth



Sequential Depth



Thank You