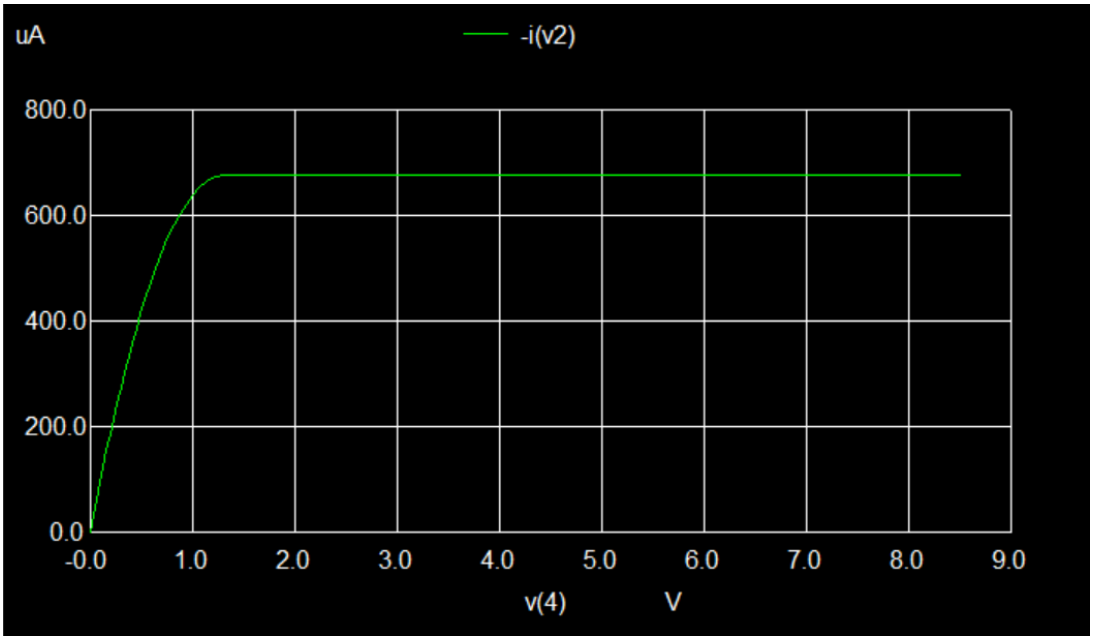
Sheel Shah, 19D070052, Expt5

Q1.

Code:

```
Sheel Shah 19D070052 NMOS Characteristics

.model NM1 nmos Level=1 Vto=0.7 KP=80u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.0

v_dd 2 0 10
r_1 2 3 2.2k
v_gs 3 0 2
v2 1 0
r_d 1 4 2.2k
mn1 4 3 0 0 NM1

.dc v2 0 10 0.1
.control
run
plot -i(v2) vs v(4)
.endc
.end
```



Learnings:

1. I learned about implementing NMOS models and using them in a circuit
2. I revised what the characteristic looked like

Q2.

Code:

```
Sheel Shah 19D070052 CS Amp Biasing

.model NM2 nmos Level=1 Vto=1 Kp=100u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.0

v_dd 2 0 12
r1 2 1 8.2k
r2 1 0 3.3k
v0 2 5 0
** for current
r_d 5 3 3.3k
r_s 4 0 1k
mn1 3 1 4 0 NM2

.op
.control
run
print i(v0), v(3), v(1), v(4)
.endc
.end
```

Results:

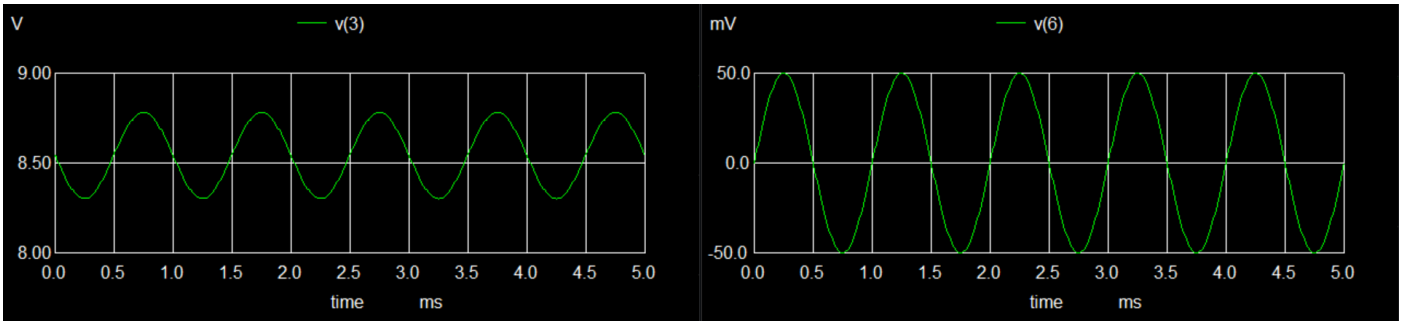
```
i(v0) = 1.017173e-03
v(3) = 8.643329e+00
v(1) = 3.443478e+00
v(4) = 1.017173e+00
```

Learnings:

I looked at the biasing circuit and saw that simulation results matched fairly well with analytical ones.

Q3.
Code:

```
Sheel Shah 19D070052 CS Amplifier

.model NM3 nmos Level=1 Vto=1 Kp=100u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.01

v_dd 2 0 12
r1 2 1 8.2k
r2 1 0 3.3k
r_d 2 3 3.3k

mn 3 1 4 0 NM3
r_s 4 0 1k
c_s 4 0 100u
c1 6 1 10u

v_in 6 0 sin(0 0.05 1k 0 0 0)

.tran 0.01ms 5ms
.control
run
plot v(3)
plot v(6)

meas tran v_in_max max v(6)
meas tran v_out_max max v(3)
meas tran v_in_min min v(6)
meas tran v_out_min min v(3)

print (v_out_max - v_out_min) / (v_in_max - v_in_min)
.endc
.end
```




```
v_in_max                =   4.999226e-02 at=   4.252800e-03
v_out_max               =   8.781442e+00 at=   7.528000e-04
v_in_min                =   -4.999226e-02 at=   4.752800e-03
v_out_min               =   8.301758e+00 at=   4.252800e-03
(v_out_max - v_out_min) / (v_in_max - v_in_min) = 4.797583e+00
```

Learnings:

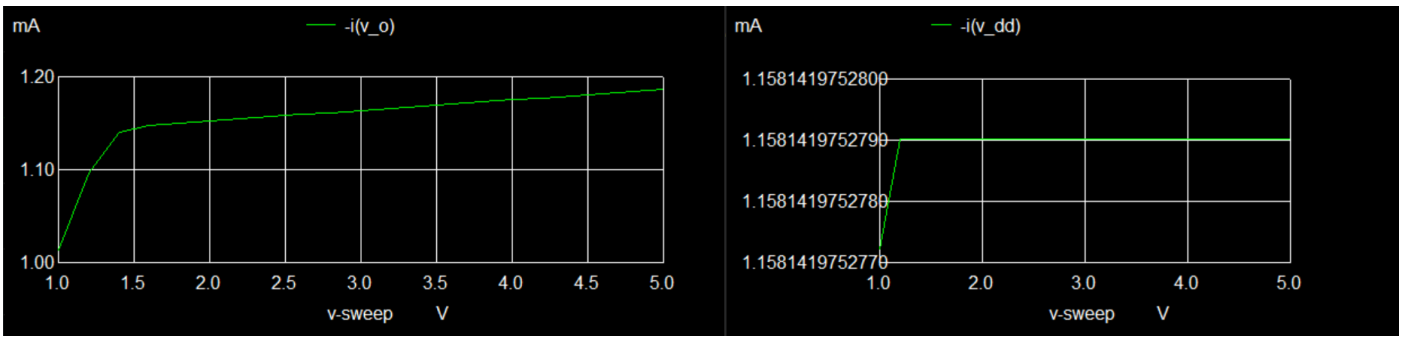
I understood the working of he common source NMOS amplifier and saw the gain matching well with our simulations.

Q4.

Code:

```
Sheel Shah 19D070052 Current Mirror NMOS

.model NM3 nmos Level=1 Vto=1 Kp=100u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.01

mn1 2 2 0 0 NM3
mn2 3 2 0 0 NM3
v_dd 1 0 12
r1 1 2 8.2k
v_o 3 0

.dc v_o 1 5 0.2
.control
run
plot -i(v_o)
plot -i(v_dd)
.endc
.end
```

Results:



Learnings:

I learned about the NMOS equivalent of a current mirror, about its design and its implementation.