Logic Testing

ATPG

Virendra Singh

Professor

Department of Electrical Engineering &

Dept. of Computer Science & Engineering

Indian Institute of Technology Bombay

http://www.ee.iitb.ac.in/~viren/

E-mail: viren@{ee, cse}.iitb.ac.in

EE-677: Foundations of VLSI CAD

Lecture 23 on 04 Oct 2021

CADSL

Boolean Algebra

(Boolean Difference Method)

x_i

$$f(V) \oplus f_{\bar{x}}(V) = 1$$

SA0

$$x_i \cdot (f_{x_i} \oplus f_{\bar{x}_i}) = 1$$

SA 1

$\bar{x}_i$

$$(f_{x_i} \oplus f_{\bar{x}_i}) = 1$$

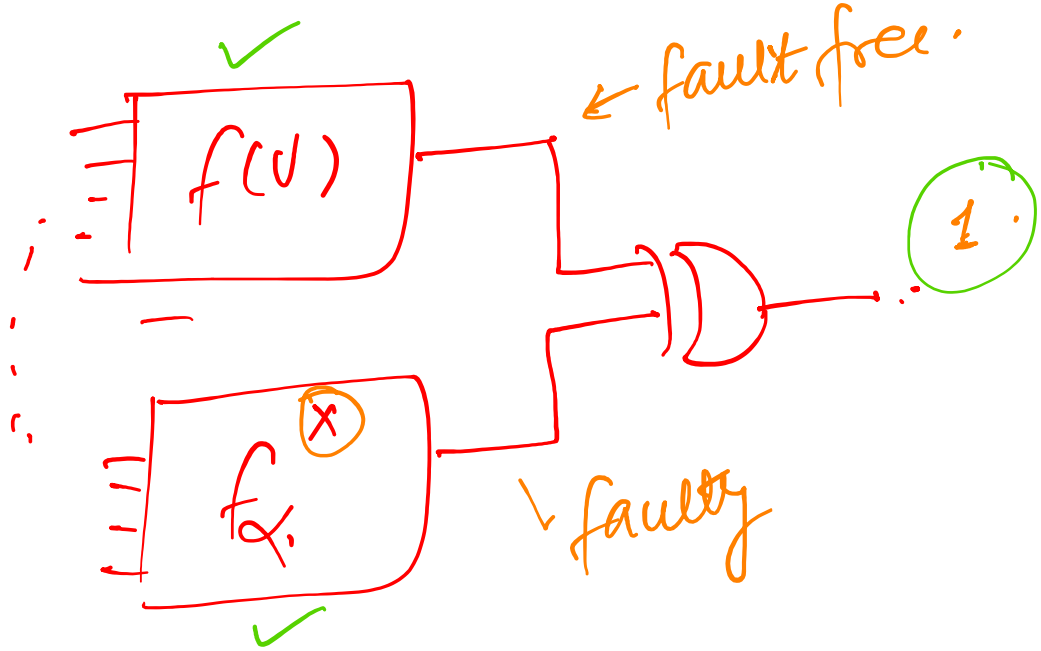
fault excitation

fault propagation

$$\frac{\partial f}{\partial x_i} = f_{x_i} \oplus f_{\bar{x}_i}$$

$f(V) \oplus f_k(V) = 1$

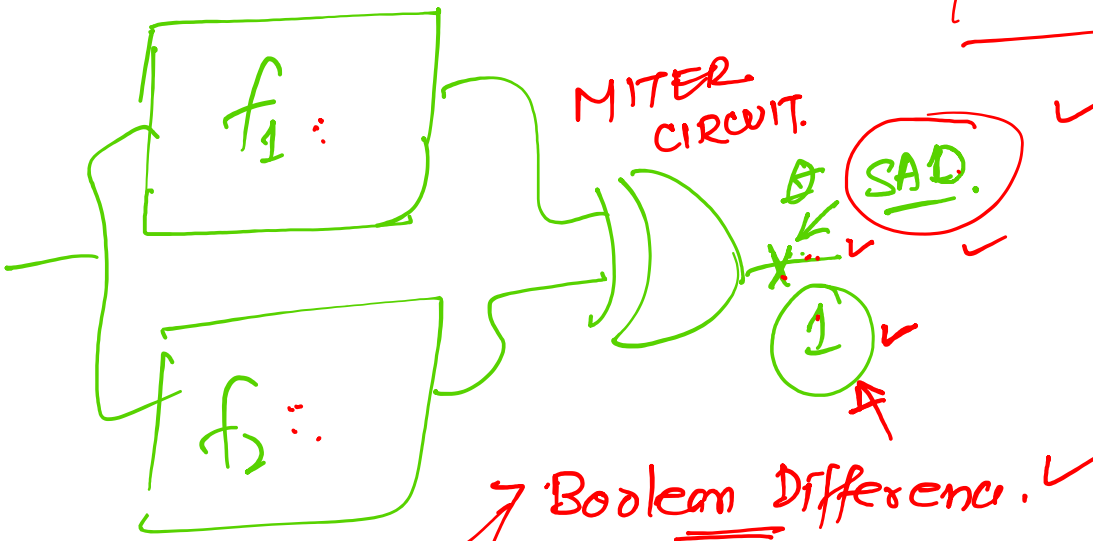
SAT based method



SAT clause & solve.

Equivalence checker

$f_1 \equiv f_2$



ATPG ⇒ EC

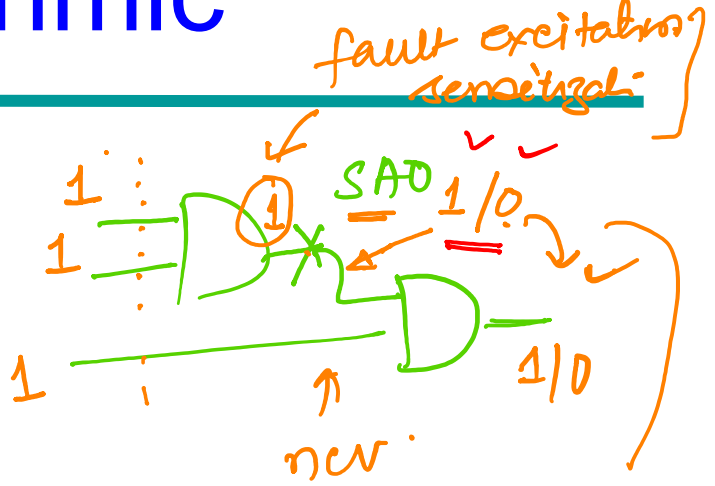
ATPG

⇒ Algebraic Method
- Boolean Difference
- SAT based
- BDD based

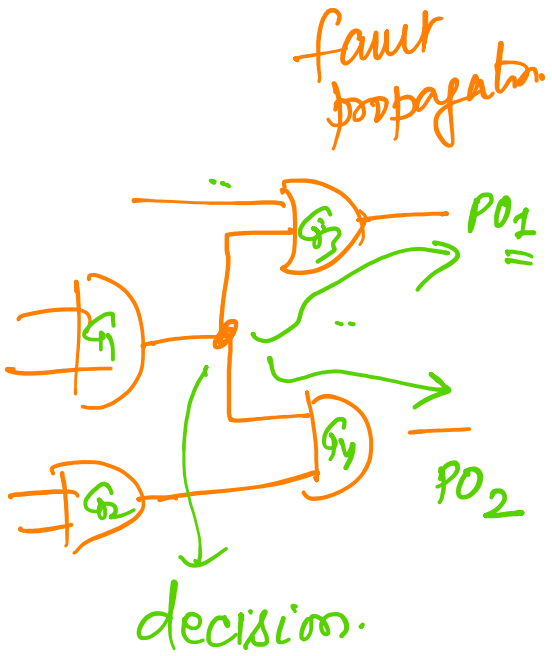
Algebr Algorithmic Method
- D-Algorithm
- PODEM
- FAN
- SPIRIT

ATPG - Algorithmic

- Path Sensitization Method
  - Fault Sensitization
  - Fault Propagation
  - Line Justification

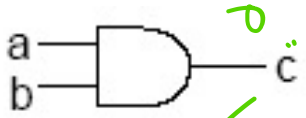


- Path Sensitization Algorithms
  - D- Algorithm (Roth)
  - PODEM (P. Goel)
  - FAN (Fujiwara)
  - SOCRATES (Schultz)
  - SPIRIT (Emil & Fujiwara)



Common Concept

- Fault Activation problem → a LJ Problem
- The Fault Propagation problem →
  1. Select a FP path to PO → Decision
  2. Once the path is selected → a set of LJ problems
- The LJ Problems → Decisions or Implications



To justify c = 1 → a = 1, b = 1 (Implication)

To justify c = 0 → a = 0 or b = 0 (Decision)

- Incorrect decision → Backtrack → Another decision

Automatic Test Pattern Generation: Algorithmic

PODEM

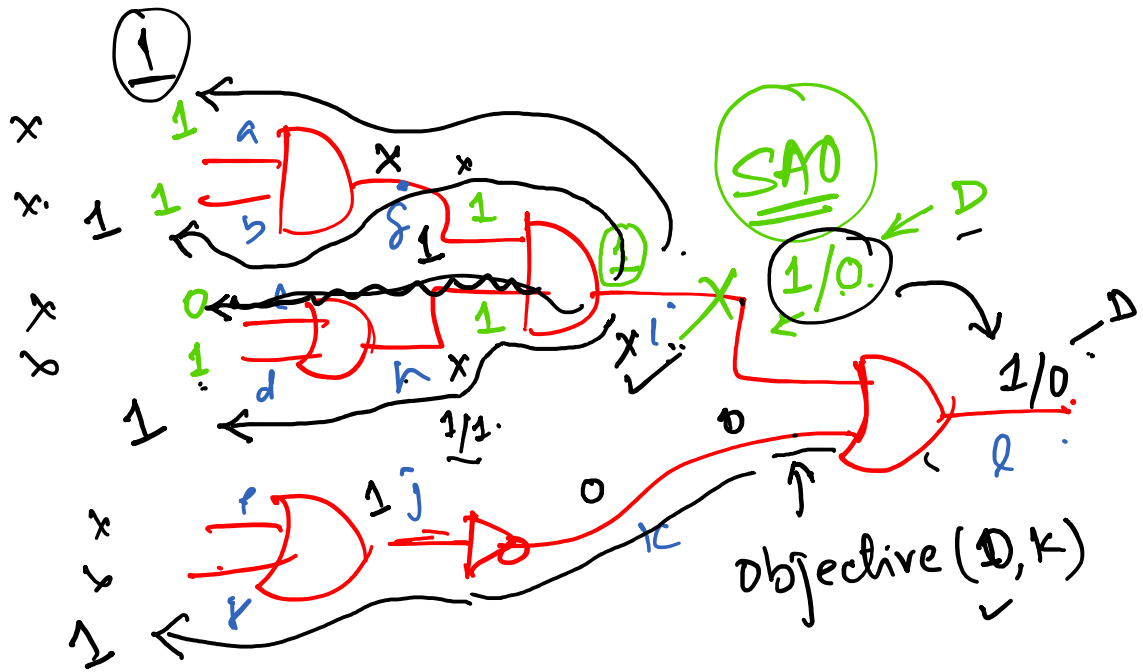
a b c d e f

1 1 X 1 X 1

Path Oriented Decision Making (PODEM)

=

Prabhu. Goel. (IBM) ← Verilog)

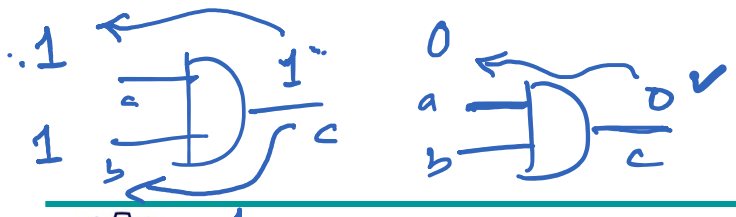


Objective (1, i)

Trace a path to PI

Assign the value to PI

Perform Implication = Logic simulation



fault-ta / fault-y

0	0	0
0	1	D
0	X	X
1	0	D
1	1	1
1	X	X
X	0	X
X	1	X
X	X	X

(0, D, $\bar{D}$, 1, X)

9 valued → (0, 1, X)

0/0, 0/1, 0/X, 1/0, 1/1, 1/X

X/0, X/1, X/X

0/1

0/0

Sequential circuit.

5 valued logic.

Thank You