EE-677: Foundation of CAD for VLSI

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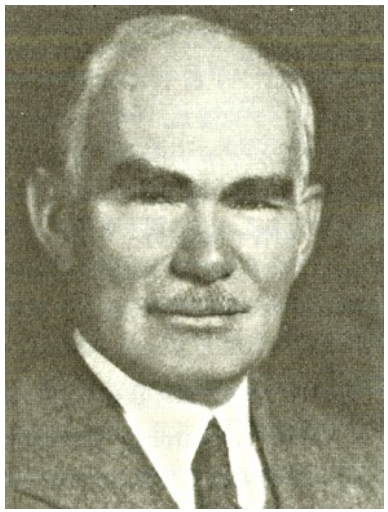
Introduction

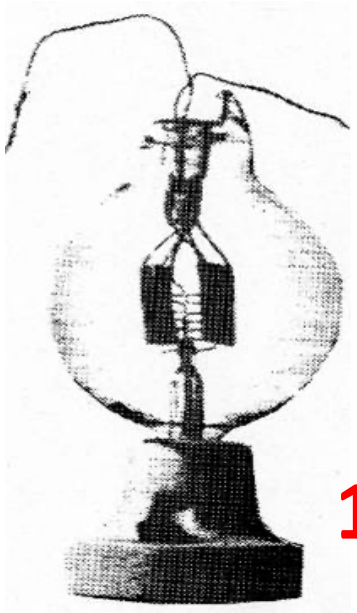
History of Electronics

- Electronics is the most important invention in the 20th cent.
- Electronic Circuits in 100 years

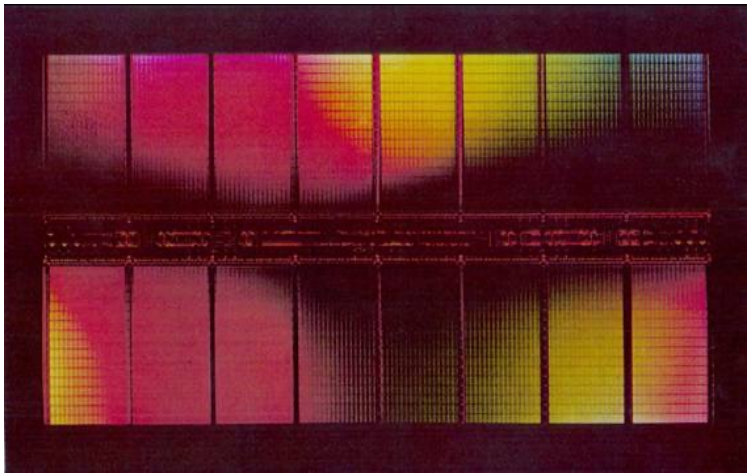
  Vacuum tube → VLSI

15 yeas ago, it was the 100 year anniversary

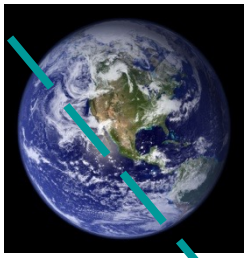




1906



Wanted: CUSTOMERS, who breathe, eat, and live in…..



Global & Regional Political & Macro-Economic Environments

~$ 50,000B

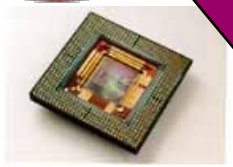
Customer Demand

Electronic End Equipment

~$ 1050B

Semiconductors

~$ 400B



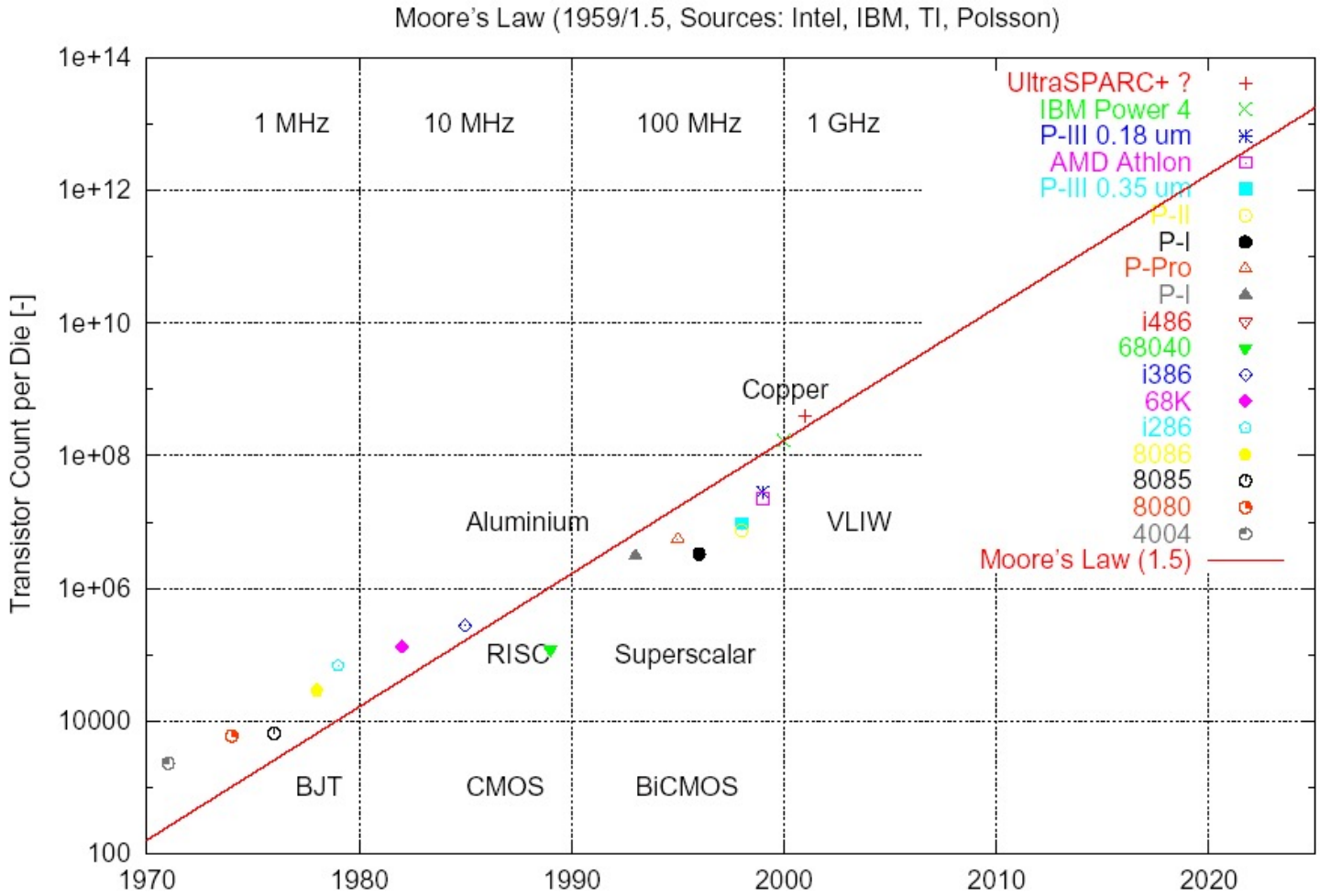
Semiconductor Equipment & Materials

~$ 100B

ITRS International Technology Roadmap for Semiconductors

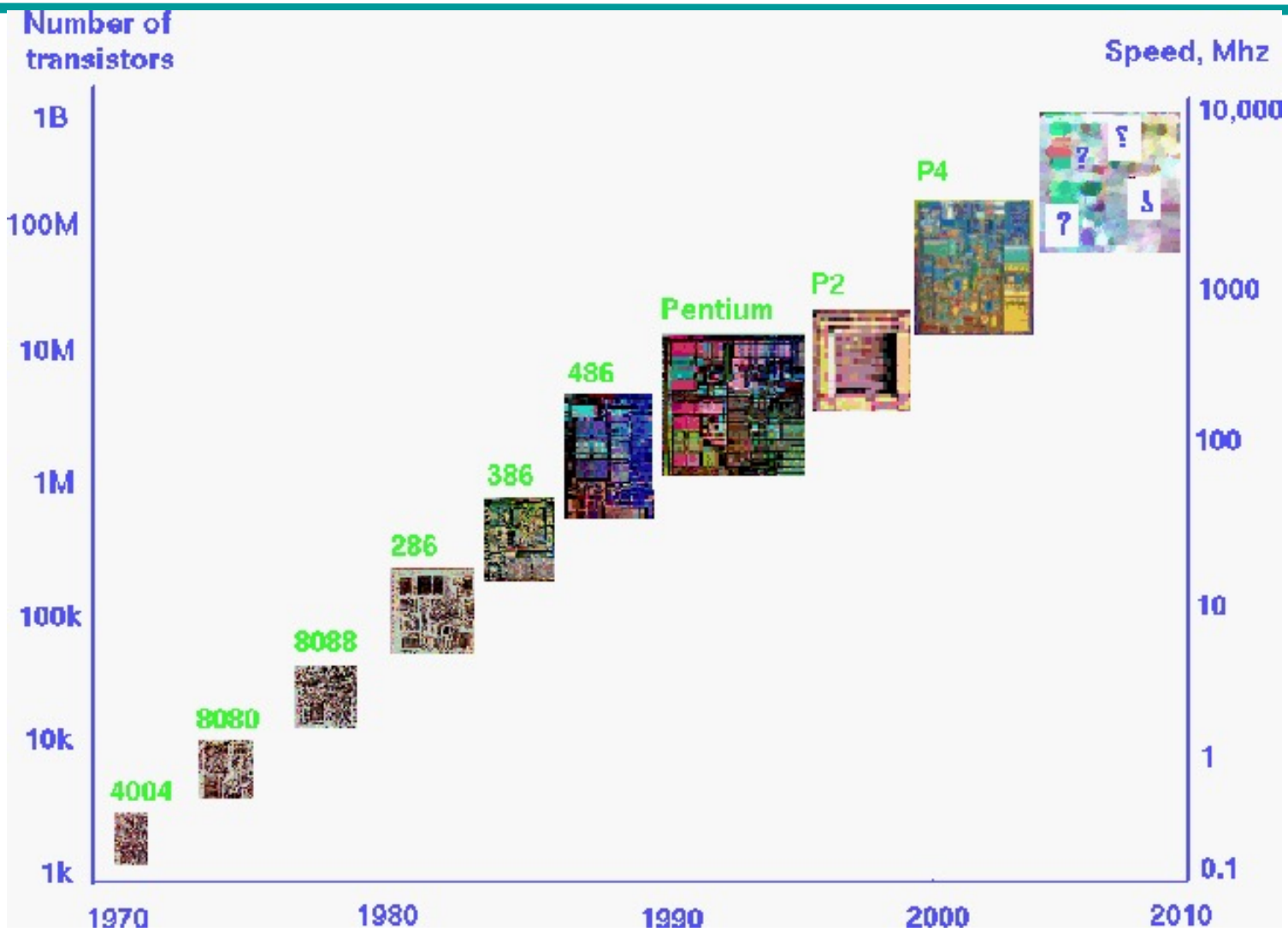
Sources: NASA Gov. ; SEMI

Motivation: Moore's Law
Complexity Growth of VLSI circuits

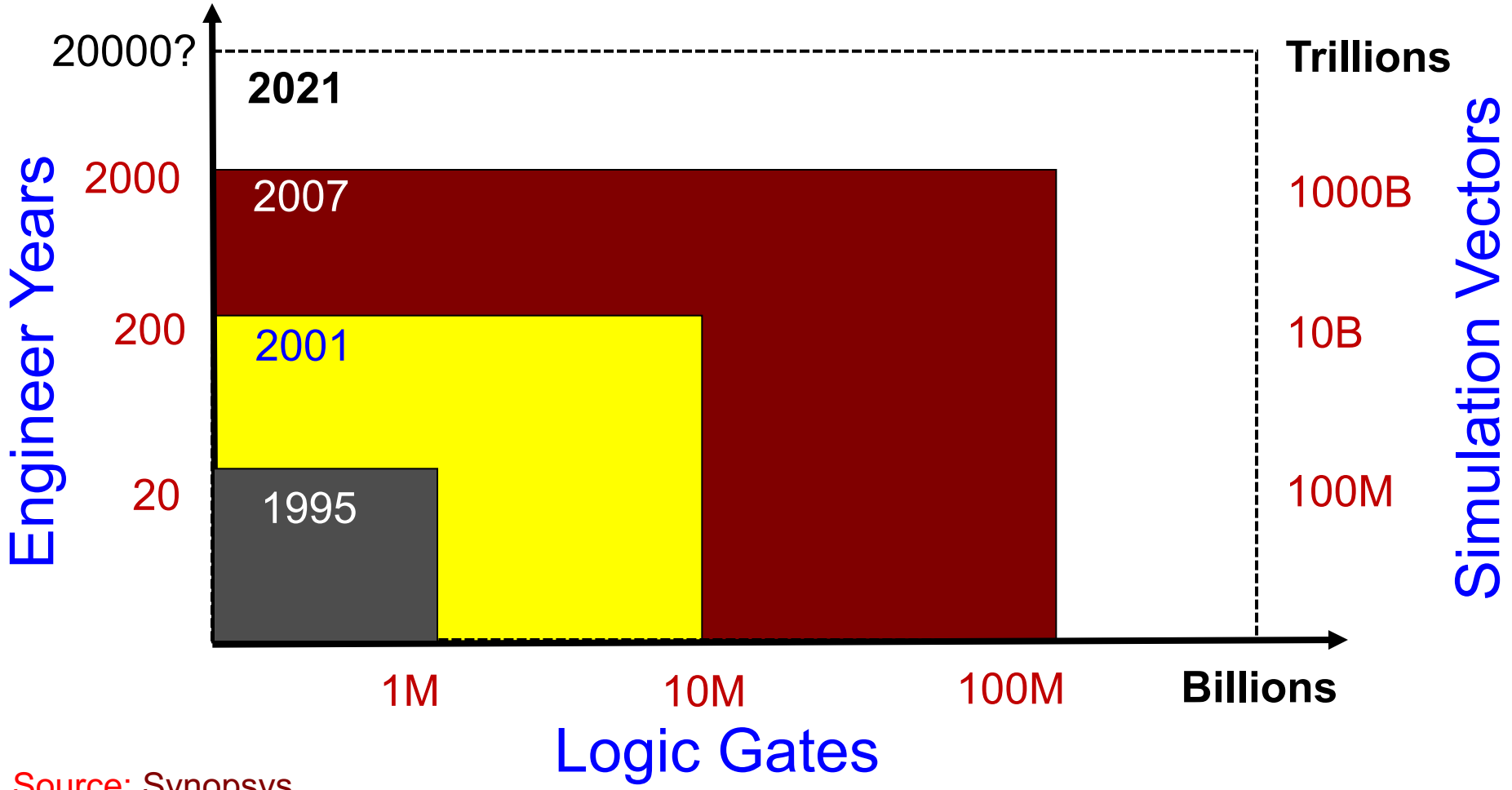


Source (Copp, *Int. AOC EW Conf., 2002*)

Design Complexity

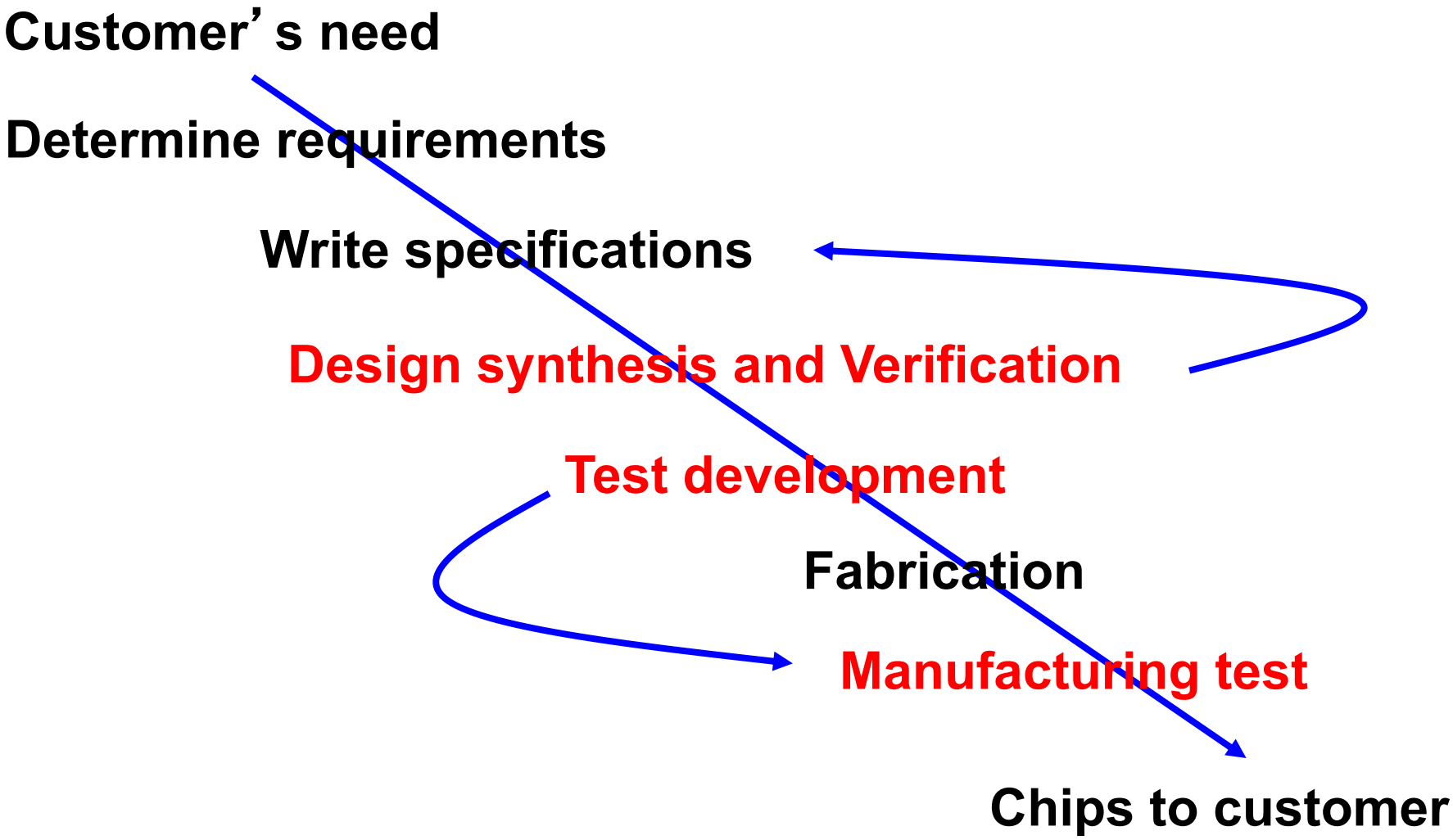


Design Validation Complexity

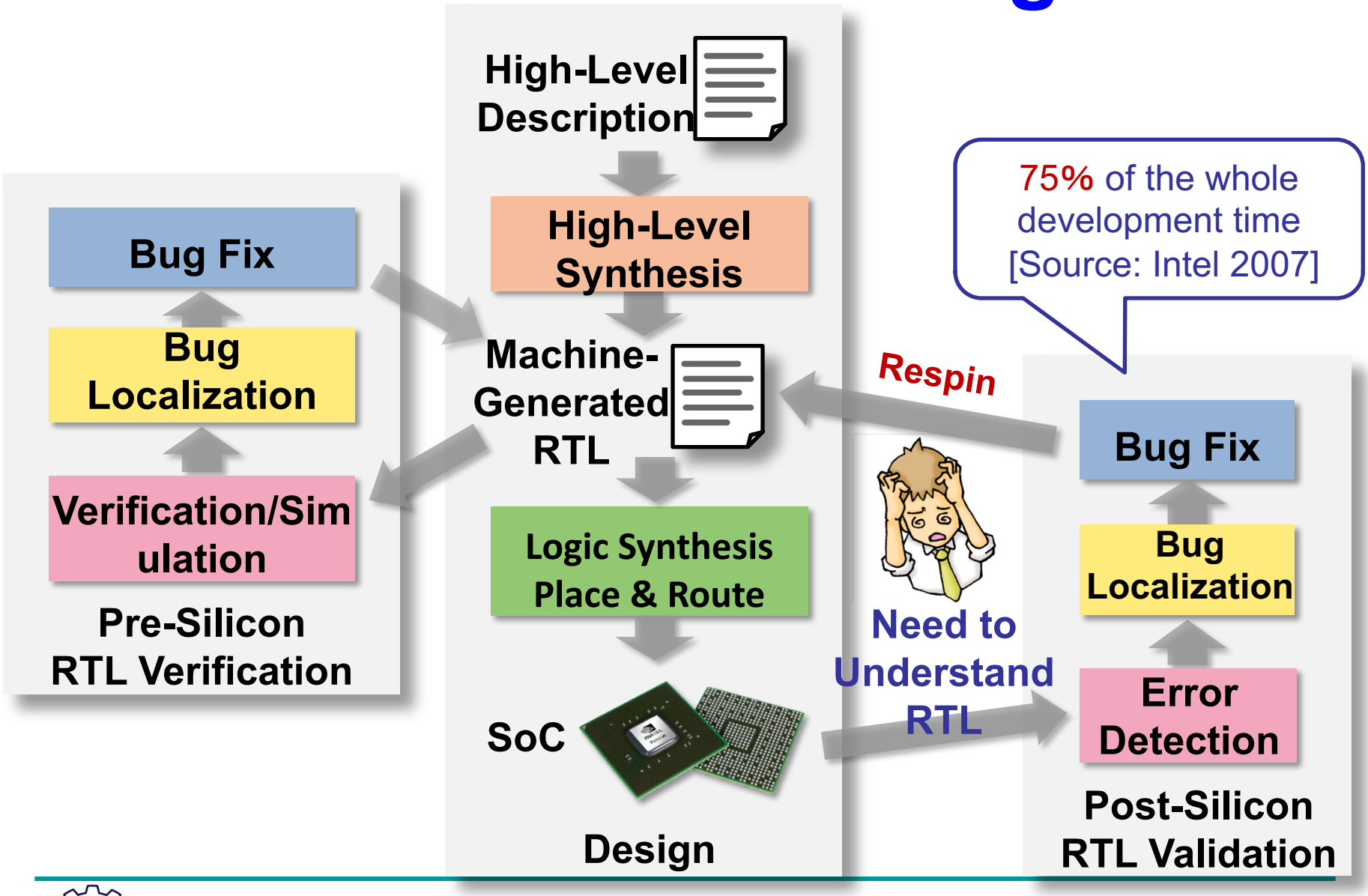


Source: Synopsys

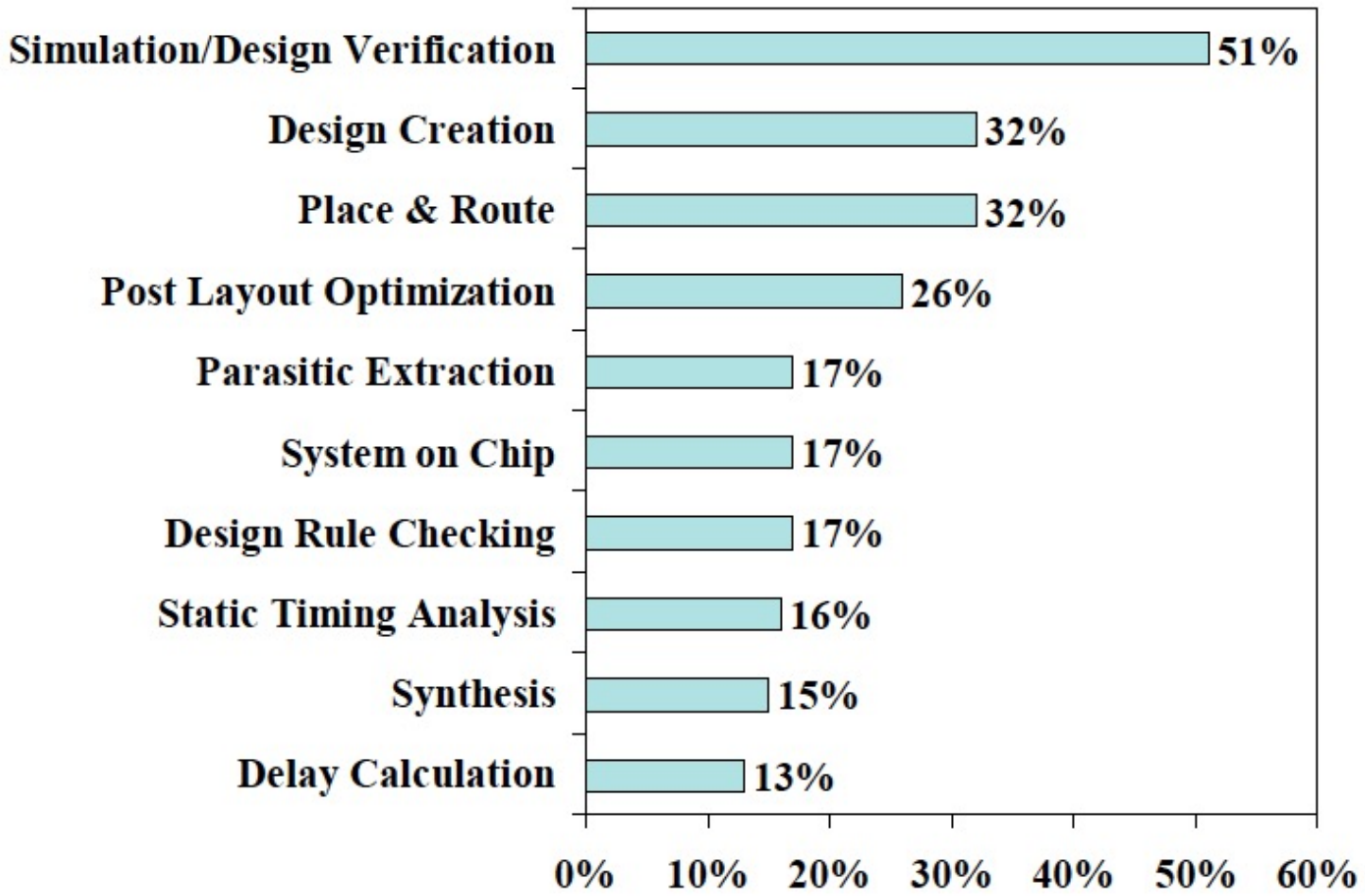
VLSI Realization Process



Conventional SoC Design Flow

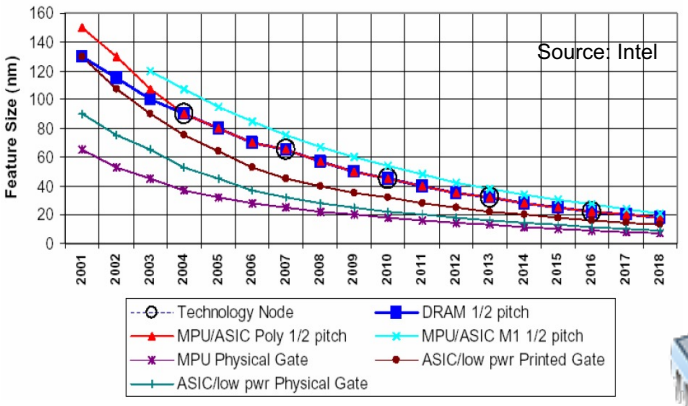


Verification challenge

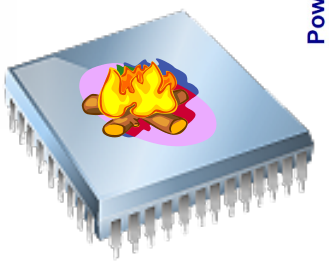


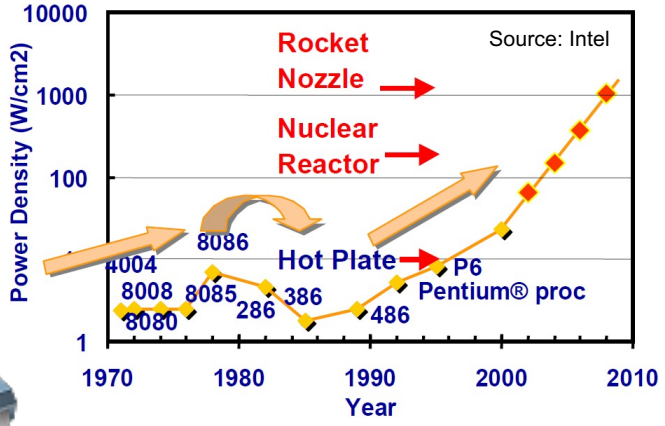
Bottlenecks in Design Cycles:
Survey of 545 engineers by EETIMES 2000

Challenges under Deep Submicron Technologies

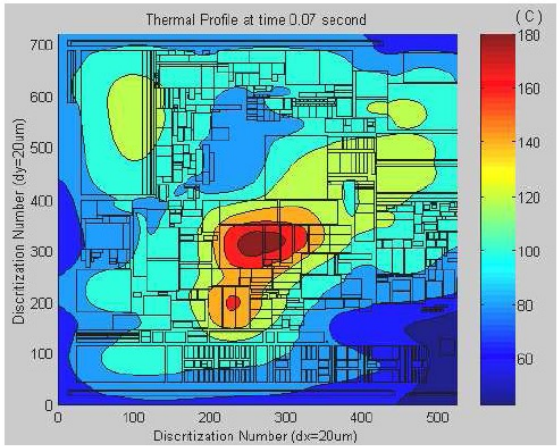


Chip size decreases



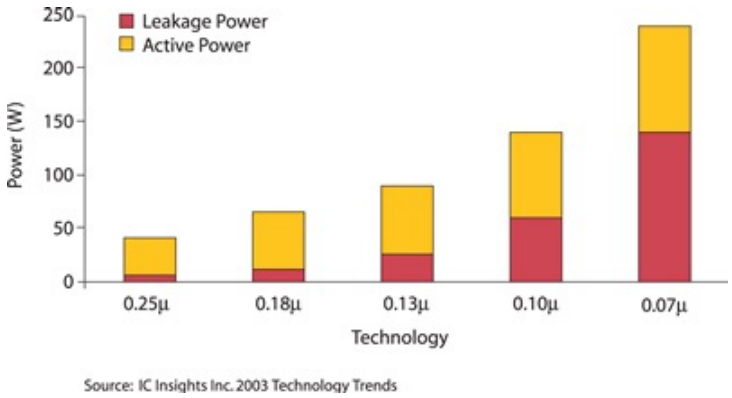


Power density increases



Source: Wang et al. ISPD2003

Chip becomes hotter



Source: IC Insights Inc. 2003 Technology Trends

Leakage power make it worse

Design Optimization Parameters

- Area
- Performance
- Testability
- Power
- Security
- Intelligence

Course Outline

- VLSI Design Flow
- High Level Synthesis
- Logic Synthesis
- Physical Design
- Hardware Software Co-design [if time permits]
- Reversible Circuit Design [if time permits]

Course Schedule

Class Hours: Slot 2

- Monday (9:30 am to 10:25 am)
- Tuesday (10:35 am to 11:30 am)
- Tuesday (11:35 am to 12:30 pm)

Office Hours

- TBD

Course Evaluation

- Mid Term Exam (15%)
- Final Exam (30%)
- Assignments (20%)
  - Set of assignments (mostly programming bases)
- Course Projects (15%)
  - Projects to implement CAD algorithm
- Continuous Evaluations (20%)
  - Weekly (Thursday) tests (90% best will be counted)

- [Bonus] Presentation/Viva (5%) – In cases needed
- [Bonus] Research Project (15%)

Grades

Absolute Grade

- > 90: AA
- 81 – 90: AB
- 71 – 80: BB
- 61 – 70: BC
- 51 – 60: CC
- 45 – 50: CD
- 40 – 44: DD
- < 40 : FR

Books (Design Verification)

- Synthesis and Optimization of Digital Circuits
  - Giovanni De Micheli
- Logic Synthesis and Verification
  - Hatchel & Somanzi
- Algorithm for Physical Design Automation
  - Naveed Shervani
- Current Literature (IEEE TC/TCAD/TVLSI)

Thank You