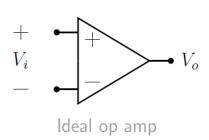
# Expt 9 – Measurement of Opamp DC Parameters

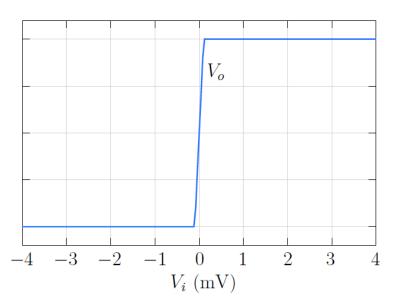
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Oct 8, 2021 (Friday)
EE 230 Analog Circuits Lab
Joseph John
2021-22/I
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#### Summary

- Measurement of the Major Opamp DC Parameters
  - Input Offset Voltage, V<sub>OS</sub>
  - Input Bias currents, I<sub>B</sub><sup>+</sup>, IB
  - Input Offset Current, I<sub>OS</sub>
  - DC Open-loop Voltage gain, A<sub>OL</sub>

#### Input Offset Voltage, Vos

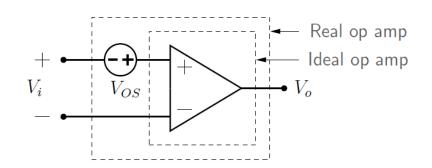


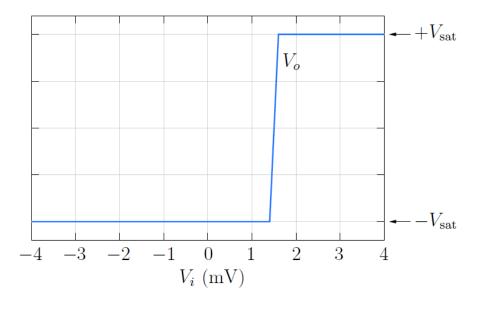


 $V_{OS}$  (typ -5 to +5mV)

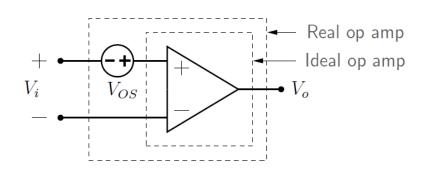
 V<sub>OS</sub> – the amount input voltage to be applied to make V<sub>o</sub> = 0

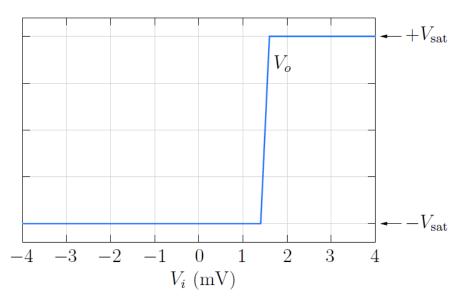
 Due to device parameter mismatches





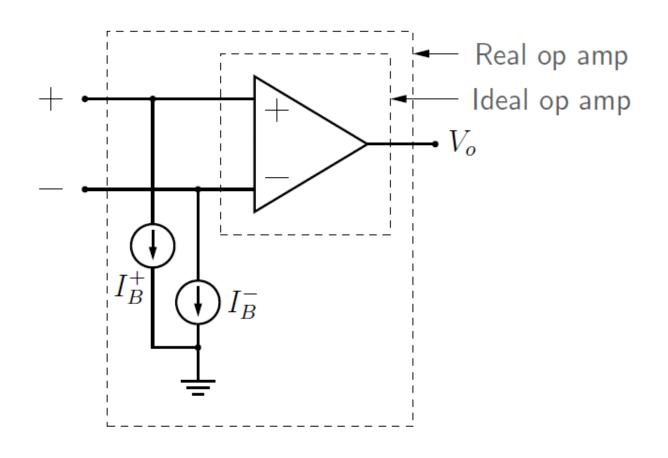
#### Input Offset Voltage, Vos





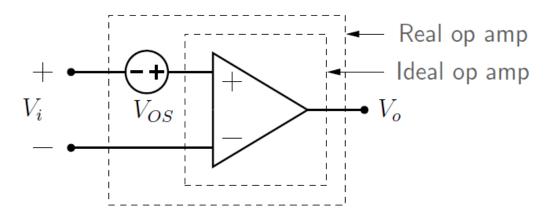
- External input voltage that must be applied to make Vo go to zero
- This external source balances out the input offset voltage of the op amp.
- Input offset voltage ( $V_{OS}$ ) must be of equal magnitude and of opposite polarity to the voltage we applied externally.

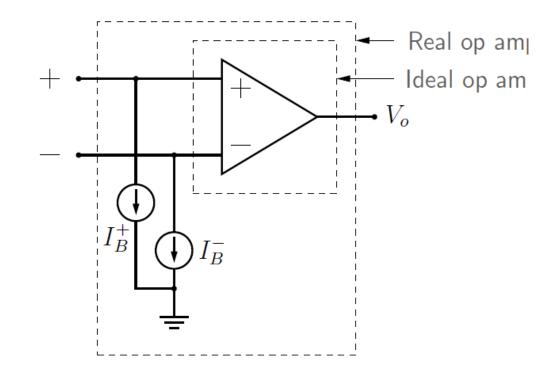
#### Input Bias currents, I<sub>B</sub><sup>+</sup> and I<sub>B</sub><sup>-</sup>

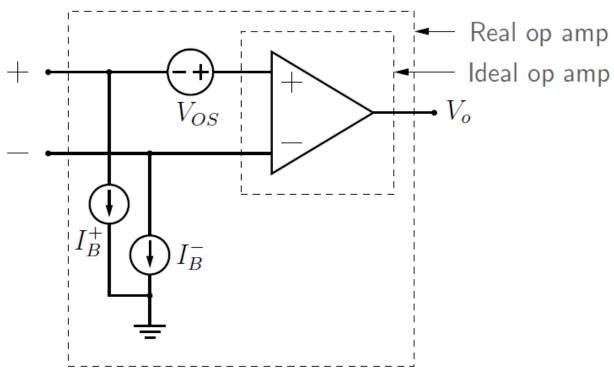


- Due to the non-zero base currents in BJT Opamps (such as UA741 and LM324)
  - nA range

- Due to the non-zero base currents in JFETinput Opamps (such as TL084)
  - pA range

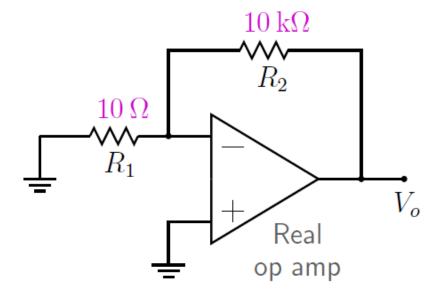






Combined effect of VOS and bias currents

## Measurement of V<sub>OS</sub>



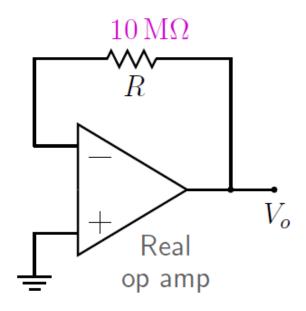
#### 741 Opamp

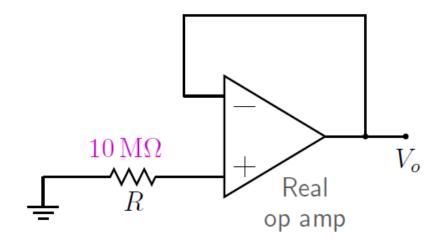
- Vo = 0.39 V
- $V_{OS} = 0.39 \text{ mV}$

- Effect of bias currents negligible
  - Small (R<sub>1</sub> and R<sub>2</sub>)
- Opamp amplifier configuration, with high gain
- Offset voltage gets amplified

• 
$$V_{OS} = Vo/[1+(R_2/R_1)]$$
  
 $\approx Vo/(R_2/R_1)$ 

#### Measurements of Input Bias Currents: I<sub>B+</sub> and I<sub>B-</sub>





 Effect of V<sub>OS</sub> negligible

- Drops due to bias currents much higher than due to V<sub>OS</sub>
- Bias current direction?

741 Opamp

- Vo = 0.28 V
- $I_{B-} = 28 \text{ nA}$

741 Opamp

- Vo = -0.34 V
- $I_{B+} = 34 \text{ nA}$

## Comparison: Measured V<sub>OS</sub>, I<sub>B</sub>, and I<sub>OS</sub>

	TL081	LM324
Vos	0.18 mV	-12.82 mV
I <sub>B+</sub>	20 pA 10.94 n.	
I <sub>B-</sub>	30 pA 10.9 nA	
I <sub>B</sub>	25 pA 10.92 nA	
los	10 pA	0.04 nA

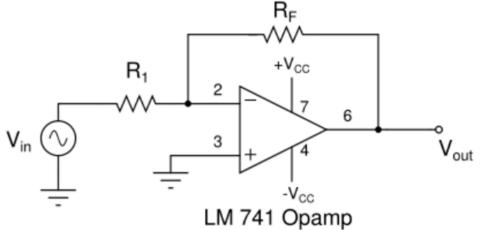
- TL081
  - JFET input Opamp
- LM324
  - BJT input Opamp

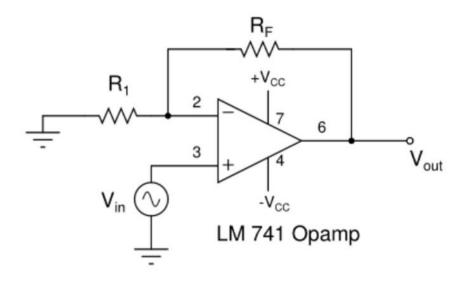
## Input Bias Current ( $I_B$ ) and Input Offset Current, ( $I_{OS}$ )

- $I_B = (I_{B+} \text{ and } I_{B-})/2$
- $I_{OS} = |I_{B+} I_{B-}|$
- How to reduce the effect of I<sub>R</sub>?
- How to reduce the effect of  $I_{OS}$ ?

#### 741 Opamp Measurements

- $I_{B} = (34 + 28)/2 = 31 \text{ nA}$
- $I_{OS} = |34 28| = 6 \text{ nA}$





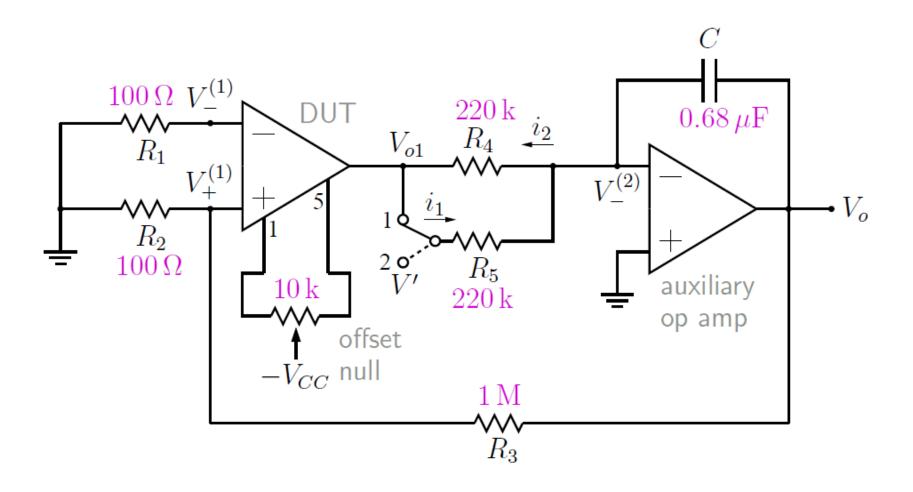
## Implications of V<sub>OS</sub>, I<sub>B</sub> and I<sub>OS</sub>

 Signal inputs should be at least tens of mV (for general purpose Opamps)

Choose resistor values carefully

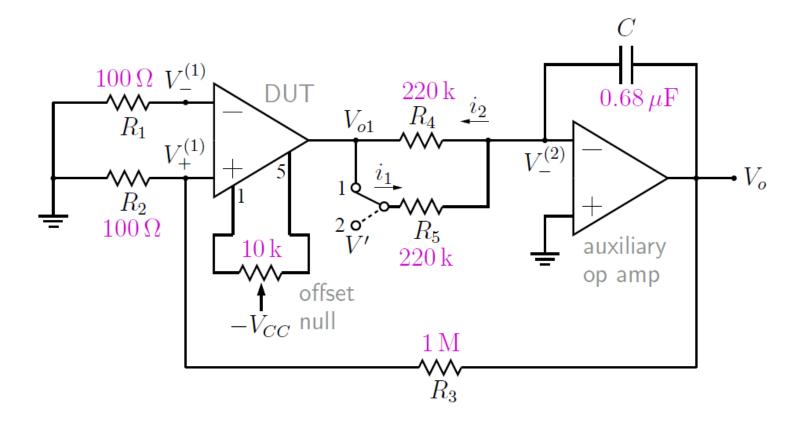
Choose medium range resistor values – neither too high, nor too low

#### DC Open-loop Voltage gain, A<sub>OL</sub>



Servo mode

DUT and Aux
 Opamp
 together
 working in –ve
 feedback



V'	V <sub>o1</sub>	Vo	A <sub>OL</sub>
1.2 V	- 1.2 V	0.12 V	<b>10</b> <sup>5</sup>
3.15 V	-3.15 V	0.175 V	2x10 <sup>5</sup>
2.1 V	- 2.1 V	0.175 V	1.2 x10 <sup>5</sup>

#### Announcements

- Oct 15 (Fri) Holiday
- Oct 22 (Fri) Exp 10 and Quiz 10
- Oct 29 (Fri) Endsem Exam
  - 2 hour (2:00 4:30pm) in two slots of 1 hour each
- Midsem and Quiz 7 and Quiz 8 Corrections
  - By Oct 15, 16 (at least Midsem + Quiz 7)
- Nov 5 (Fri) No Lab!!