High Level Synthesis

Testability

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EE-677: Foundations of VLSI CAD

Lecture 12 on 30 August 2021

CADSL

High Level Synthesis

Objective

- Area
- Performance
- Power
- Reliability

Register binding,

Improve the reliability

Test of circuit

Circuit.

n input 2^n ✓ ✓

100 input

2^{100} @ 10 GHz.

2. input - 4

10 - 1024 ✓

20 - 1M.

$$\frac{2^{100}}{2^{10^{10}}} \text{ sec} = \frac{(2^{10})^{10}}{10^{10}} = \frac{10^{30}}{10^{10}} = 10^{20} \text{ sec}$$

$$\frac{10^{20}}{60 \times 60 \times 24 \times 365 \times 100} \text{ yr} \quad \text{B. Centr} \checkmark$$

≈ 6-7

6 × 60 = ≈360.

test within seconds] to find input stimuli which can be applied within few seconds.

Fault.

⇓

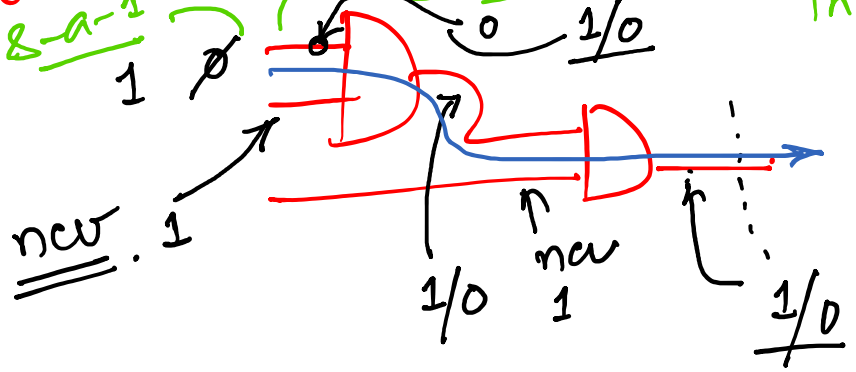
SSAFM:

Defect →

Single Stuck-at Fault Model.

s-a-0] – want to check whether this net is stuck to logic 0 or not.

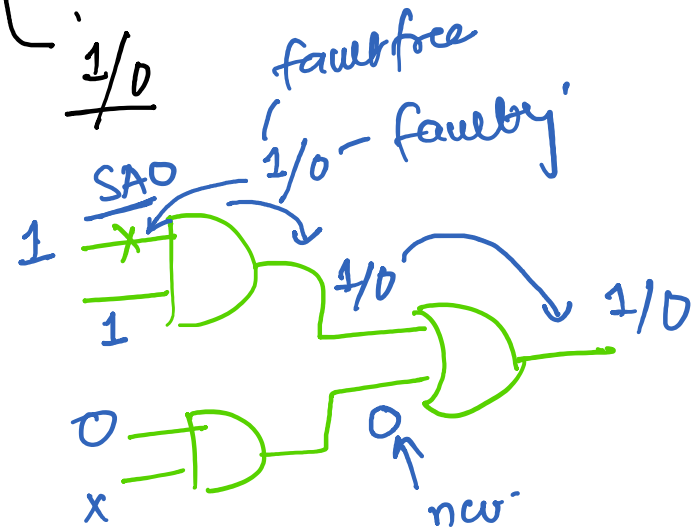
s-a-1



fault excitation

fault propagation

Line justification



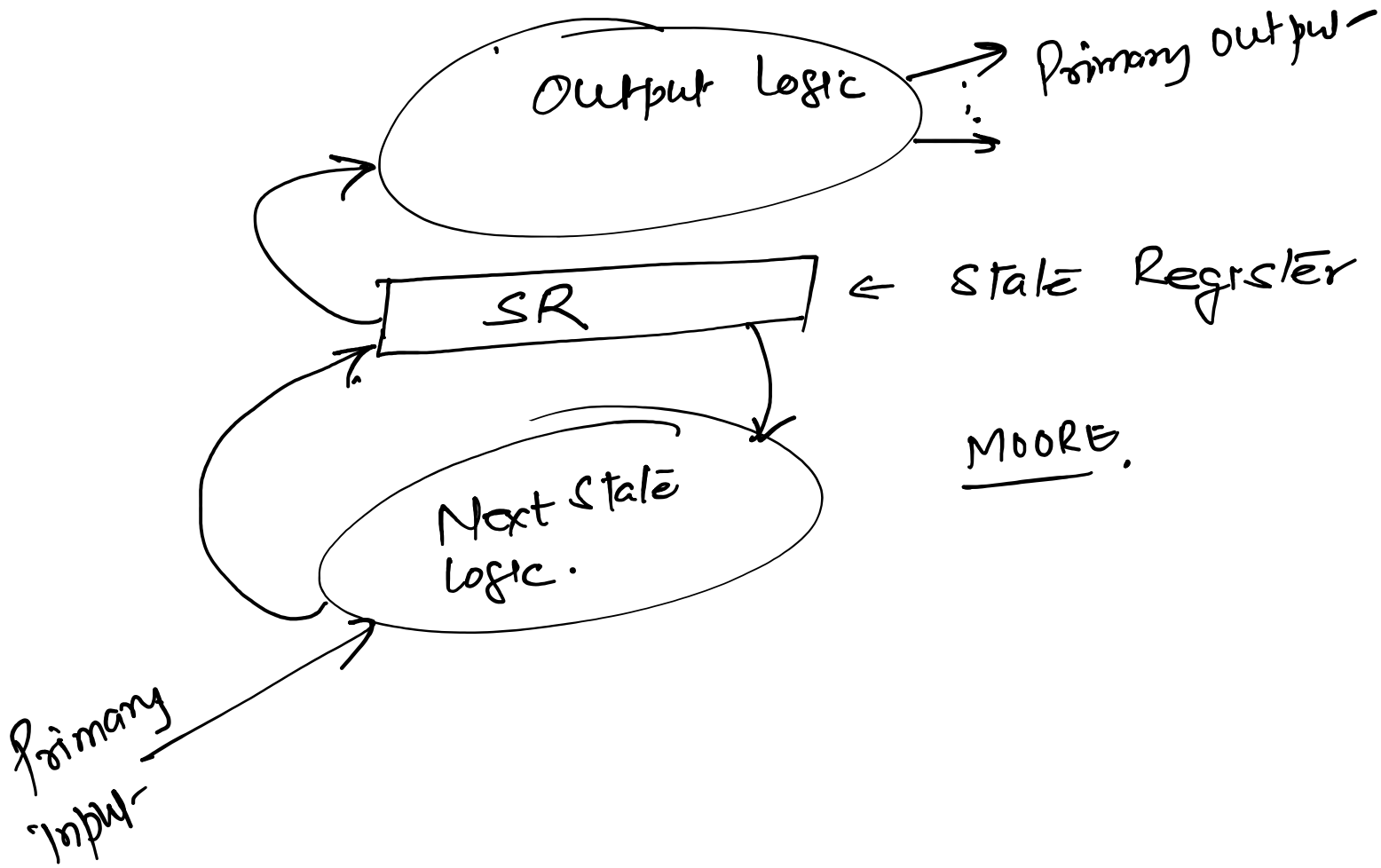
faults = 2 × #nets

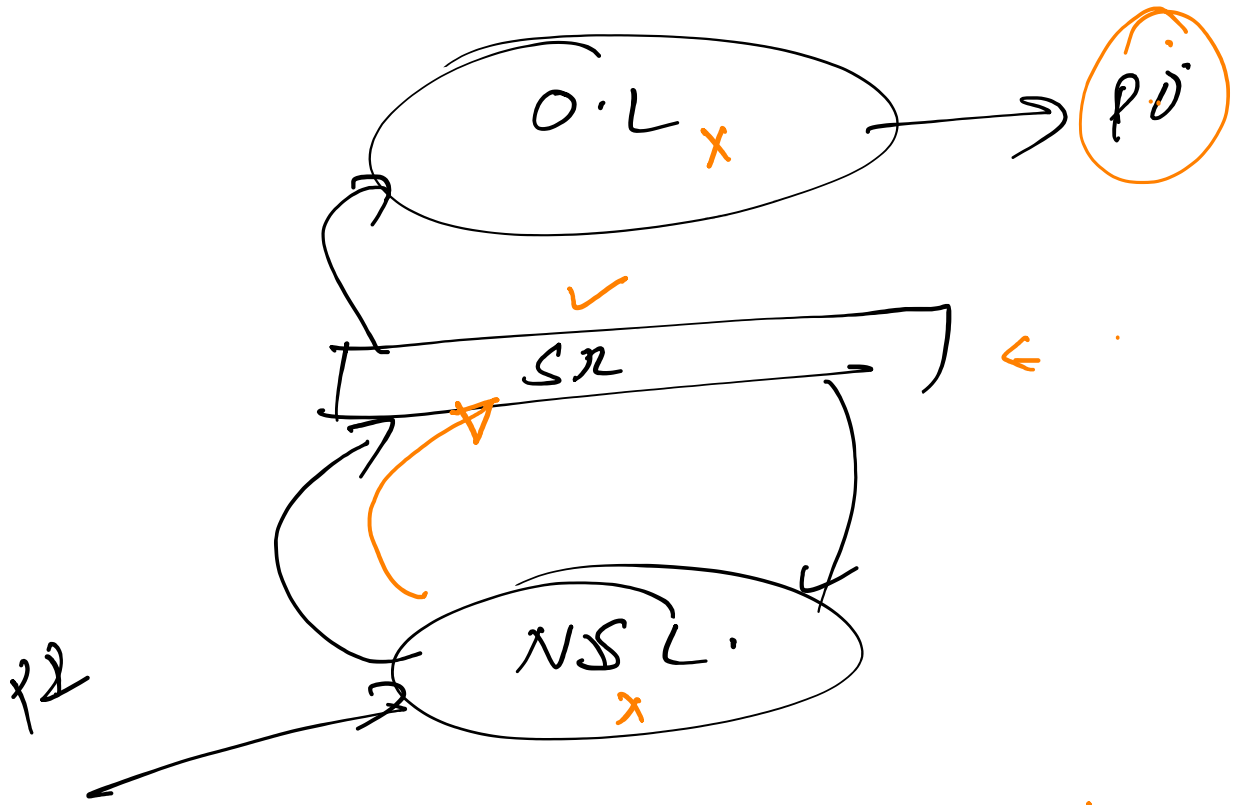
$\propto$ #gates

#faults $\propto$ #gates

Combinational logic.

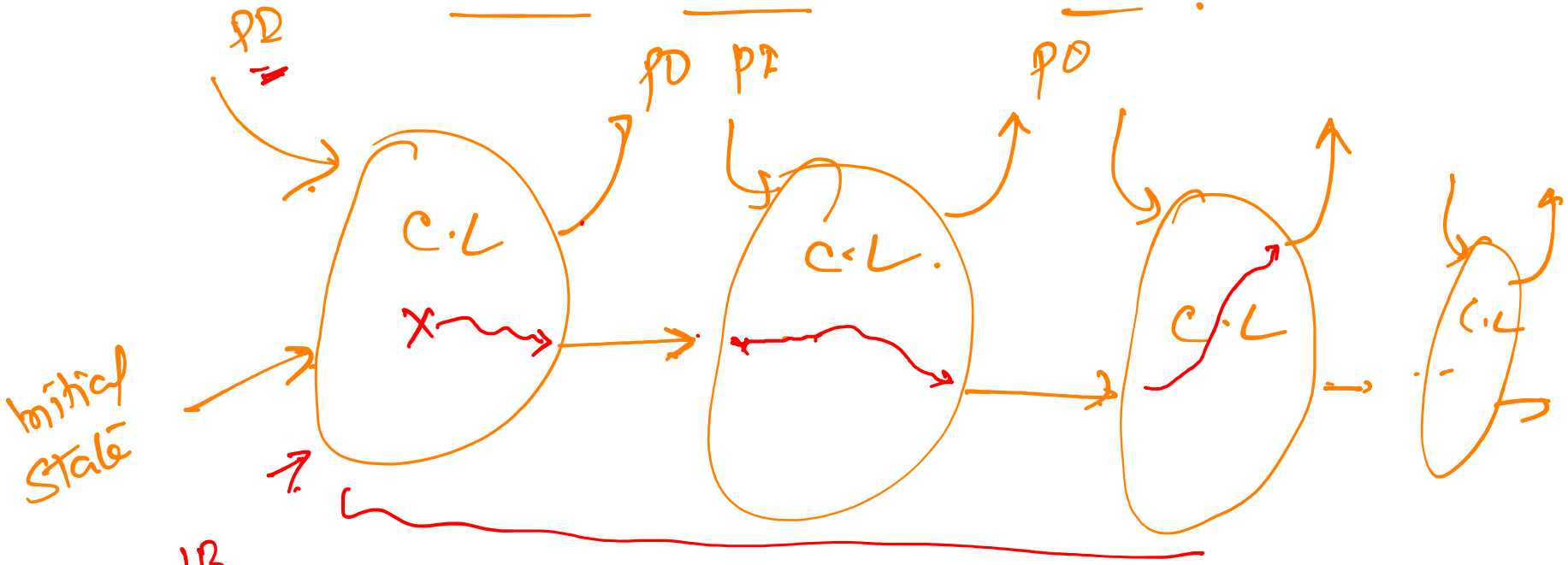
SEQUENTIAL CIRCUITS.


Output Logic
Primary output
SR
← State Register
Next State logic.
MOORE.
Primary input



aim - to propagate fault effect to primary output

TIME FRAME EXPANSION.



How many time frame you need to expand!

Sequential depth → Cyclic ← q^{FF} }

→ Acyclic.

How HLS can help in reducing the sequential depth of the circuit.

⇓

So that it can become better testable.

Thank You