# EE-677: Foundation of CAD for VLSI


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*Introduction*

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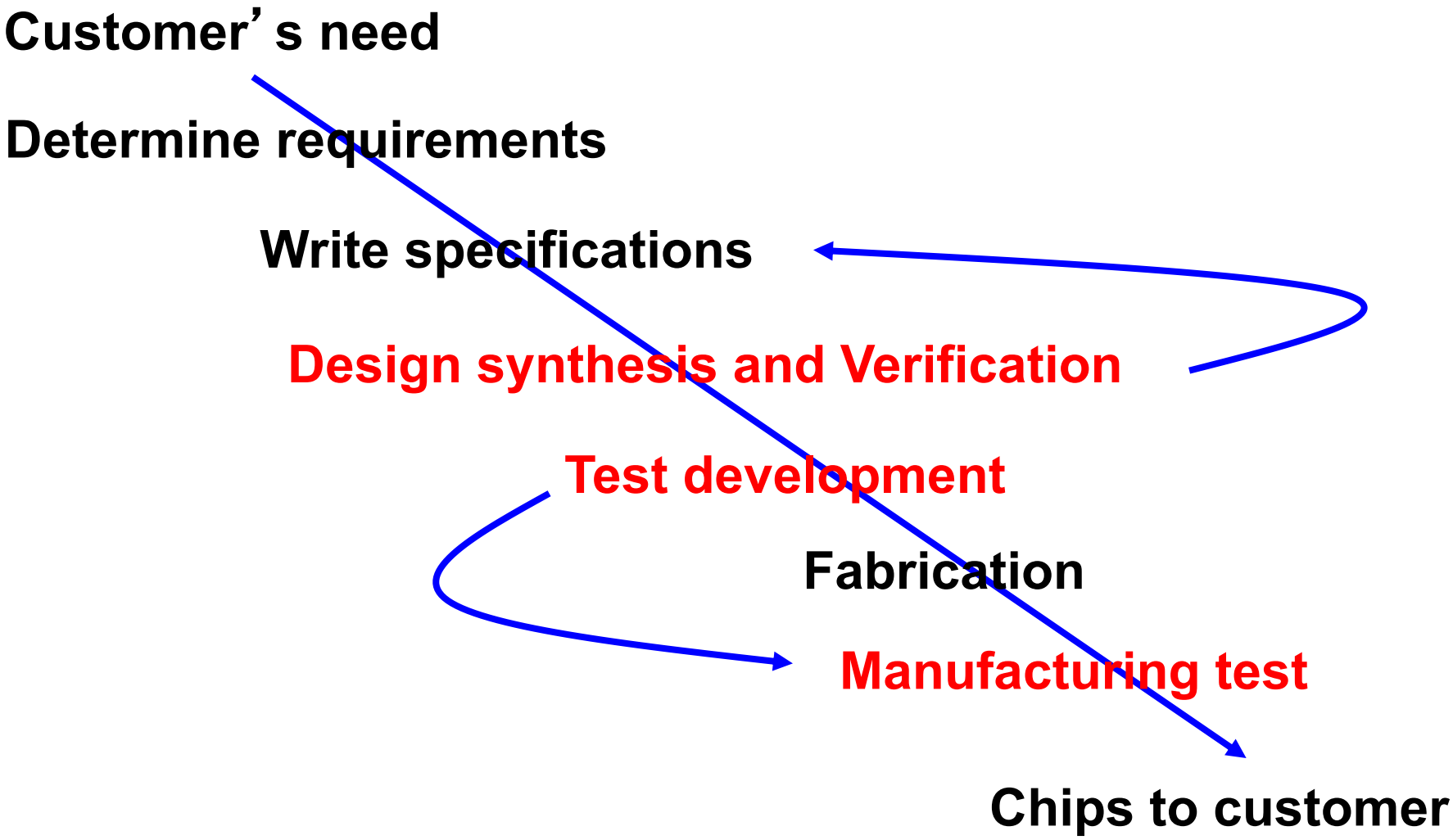
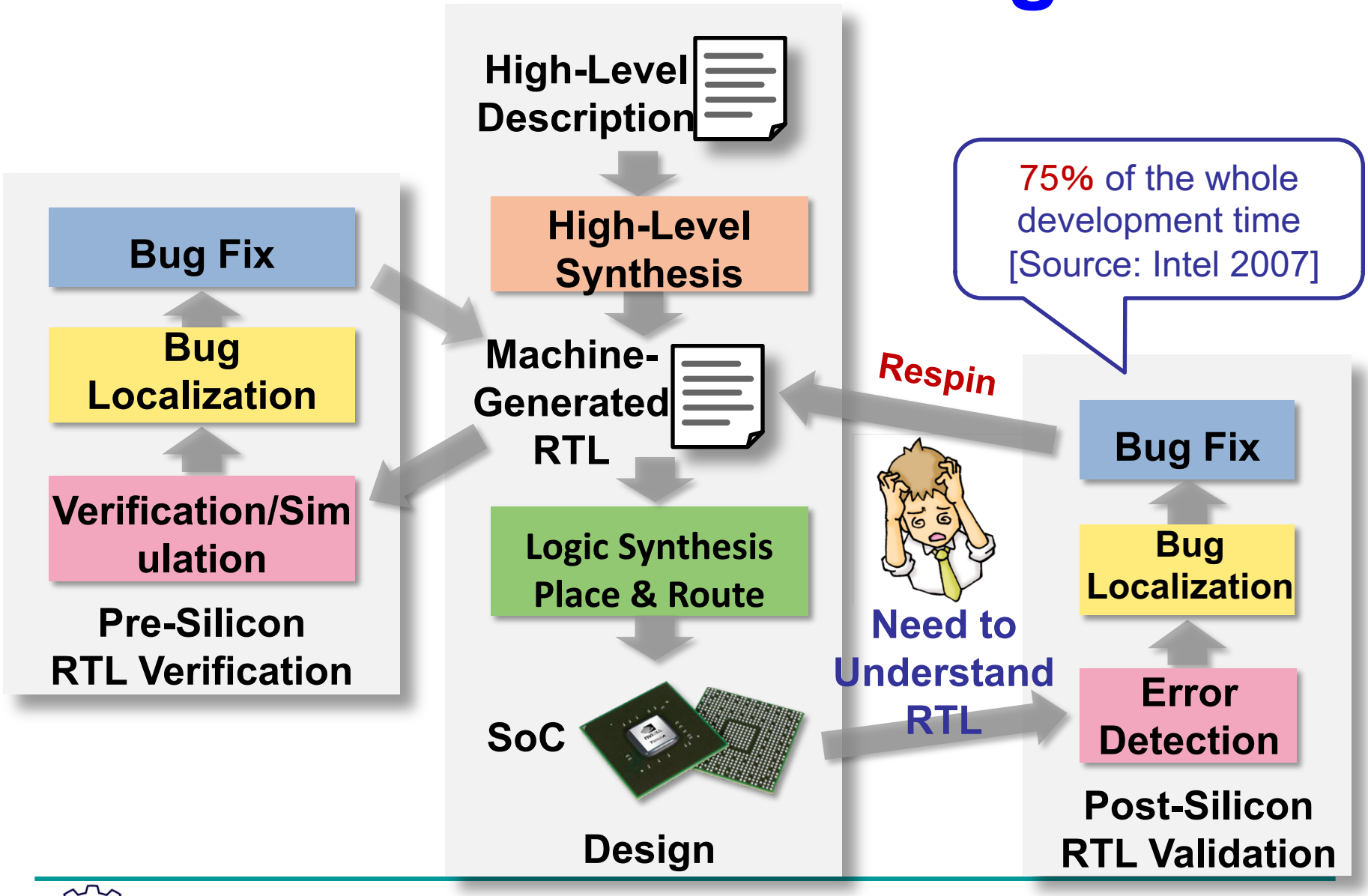
CADSL

# VLSI Realization Process



# Conventional SoC Design Flow



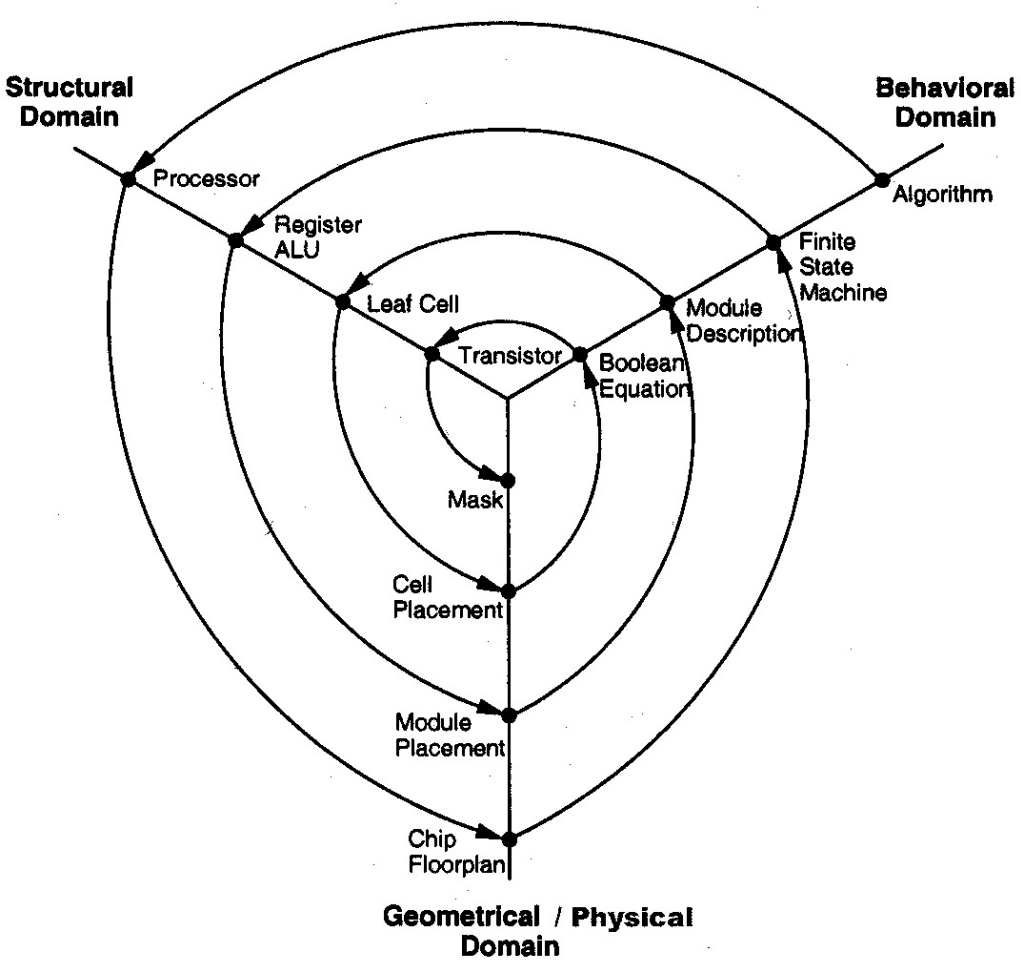
# Design Optimization Parameters

- Area
- Performance
- Testability
- Power
- Security
- Intelligence

# Structured Design

- **Hierarchy**: Divide and Conquer
  - Recursively system into modules
- **Regularity**
  - Reuse modules wherever possible
  - Ex: Standard cell library
- **Modularity**: well-formed interfaces
  - Allows modules to be treated as black boxes
- **Locality**
  - Physical and temporal

# Gajski Y-Chart



# Definitions

- *Design synthesis:* Given an I/O function, develop a procedure to manufacture a device using known materials and processes.

- *Verification:* Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.

- *Test:* A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

# Thank You