

Logic Testing

ATPG ✓

Virendra Singh

Professor

Department of Electrical Engineering &
Dept. of Computer Science & Engineering
Indian Institute of Technology Bombay

<http://www.ee.iitb.ac.in/~viren/>

E-mail: viren@{ee, cse}.iitb.ac.in



EE-677: Foundations of VLSI CAD



Lecture 24 on 05 Oct 2021

CADSL

Q Algebraic $\begin{cases} \rightarrow \text{Boolean Difference} \\ \rightarrow \underline{\text{SAT.}} \end{cases}$

\Rightarrow [Algorithmic $\begin{cases} \rightarrow \underline{\text{PODEM. (1981)}} \\ \text{Prabhu Goel. (Verilog)} \\ \rightarrow \underline{\text{FAN}} \\ \downarrow \\ \underline{\text{learning}} \end{cases}$

$a=0$

$d=0$

ATPG - Algorithmic

❖ Path Sensitization Method

- Fault Sensitization ✓
- Fault Propagation ✓
- Line Justification ✓

❖ Path Sensitization Algorithms

- D- Algorithm (Roth)
- PODEM (P. Goel)
- FAN (Fujiwara)
- SOCRATES (Schultz)
- SPIRIT (Emil & Fujiwara)

Common Concept

- ❖ Fault Activation problem → a LJ Problem
- ❖ The Fault Propagation problem →
 1. Select a FP path to PO → Decision ✓
 2. Once the path is selected → a set of LJ problems
- ❖ The LJ Problems → Decisions or Implications



To justify $c = 1 \rightarrow a = 1, b = 1$ (**Implication**)

To justify $c = 0 \rightarrow a = 0$ or $b = 0$ (**Decision**)

*Redundant
UNTESTABLE*

- ❖ Incorrect decision → **Backtrack** → **Another decision**

Automatic Test Pattern Generation: Algorithmic

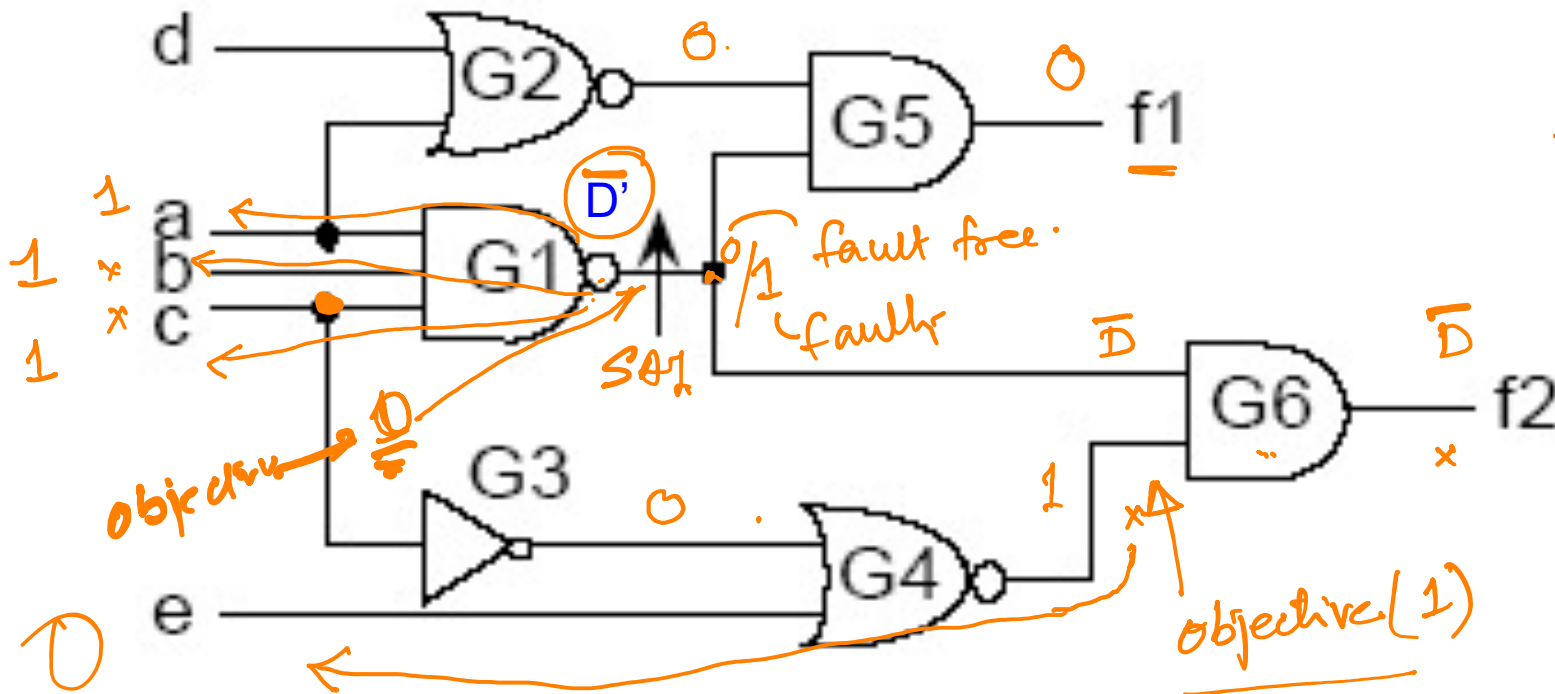


PODEM

$\exists D=0$

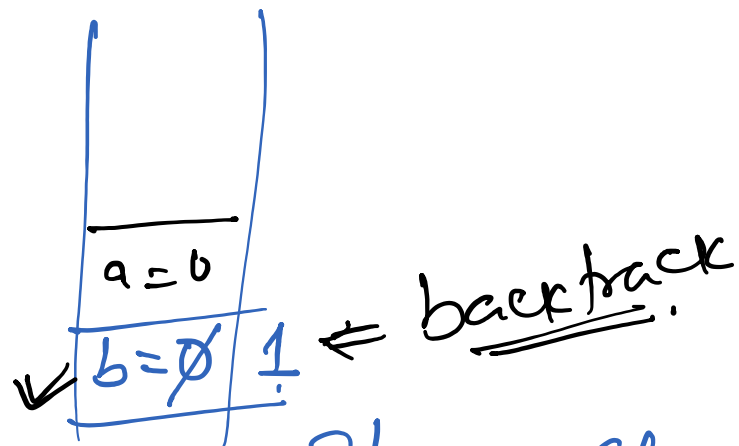
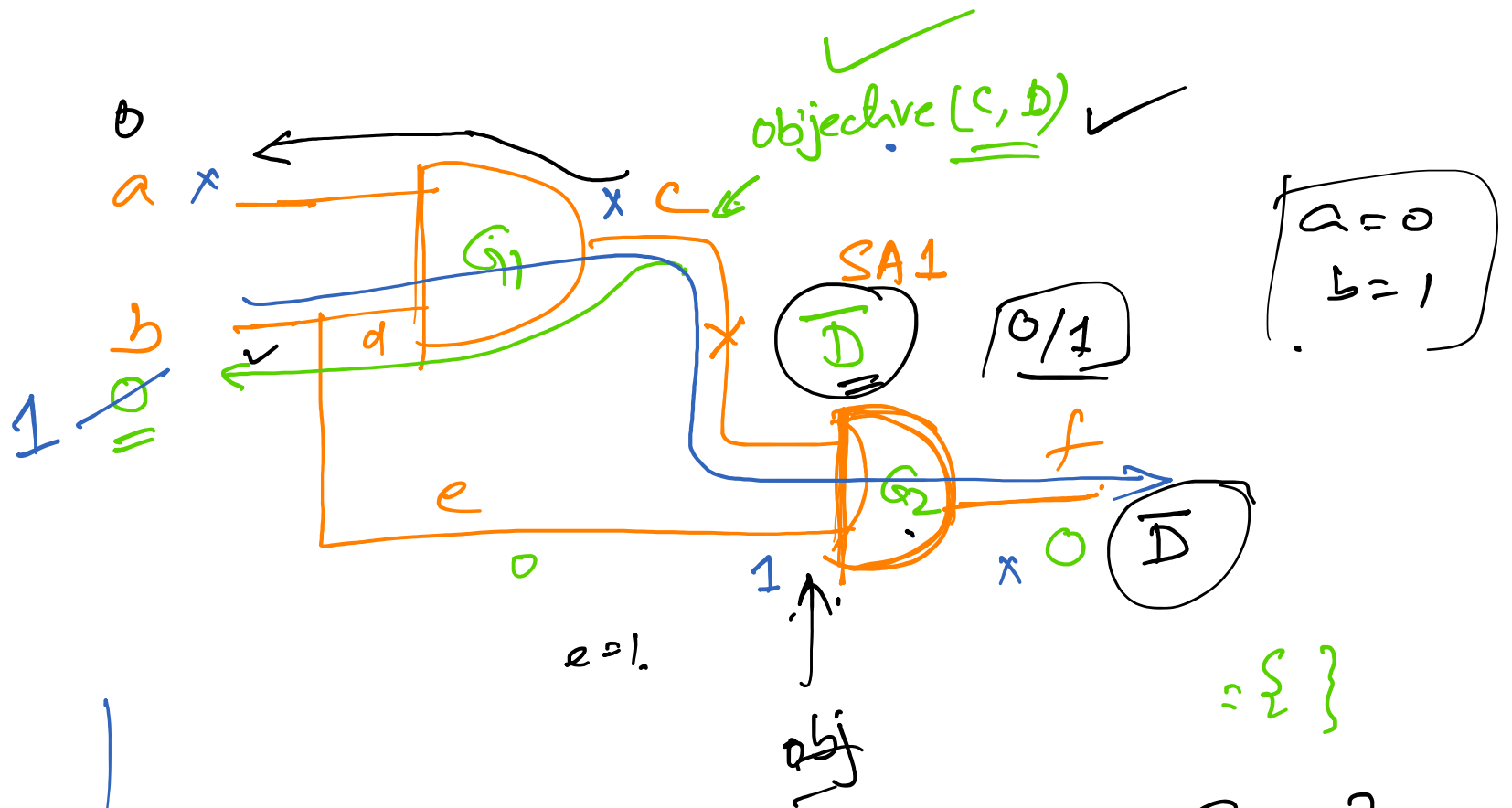
↑ ↓

Implication



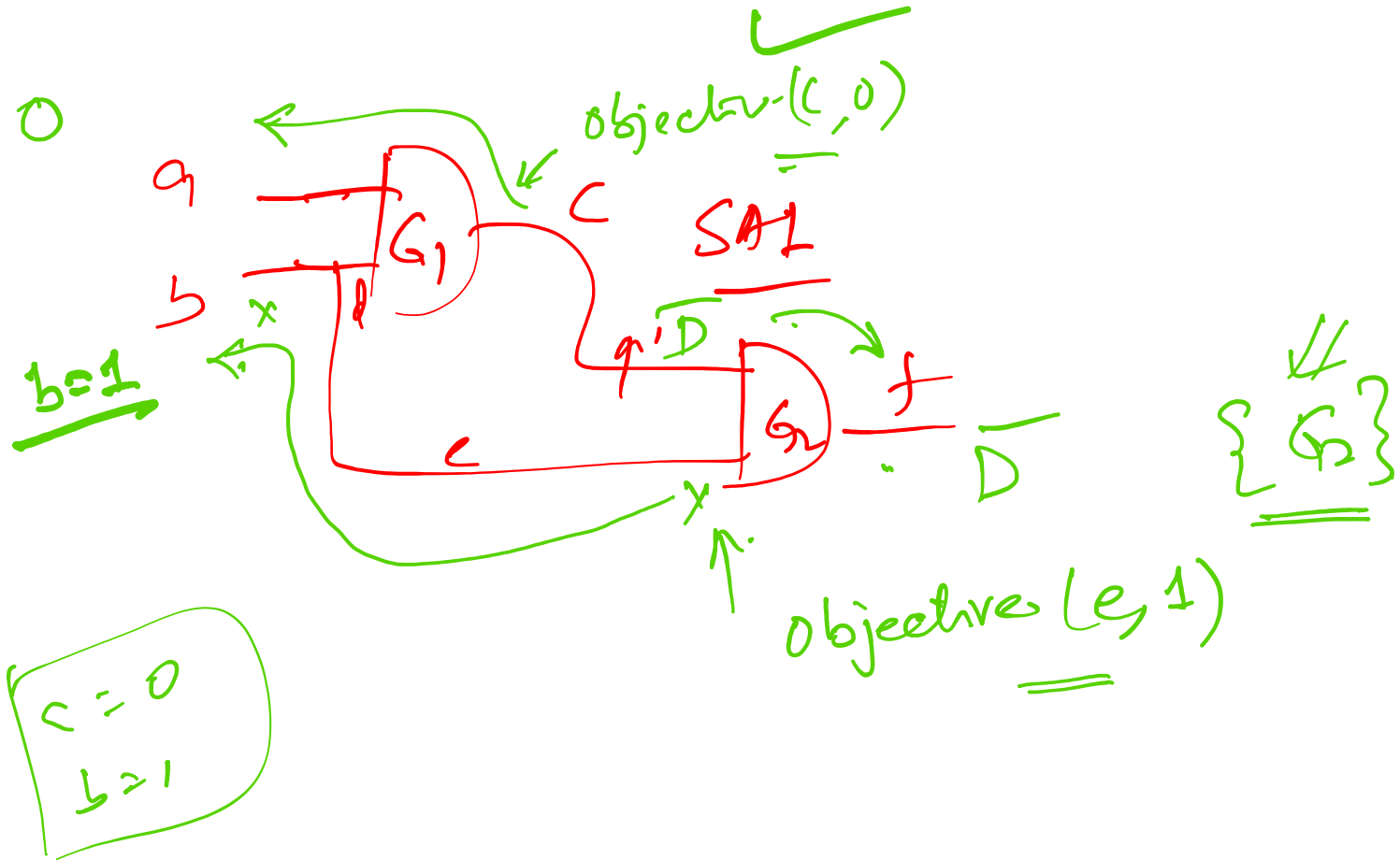
D – frontier: The set of all gates whose output value is currently x but have one or more **fault** signals on their inputs

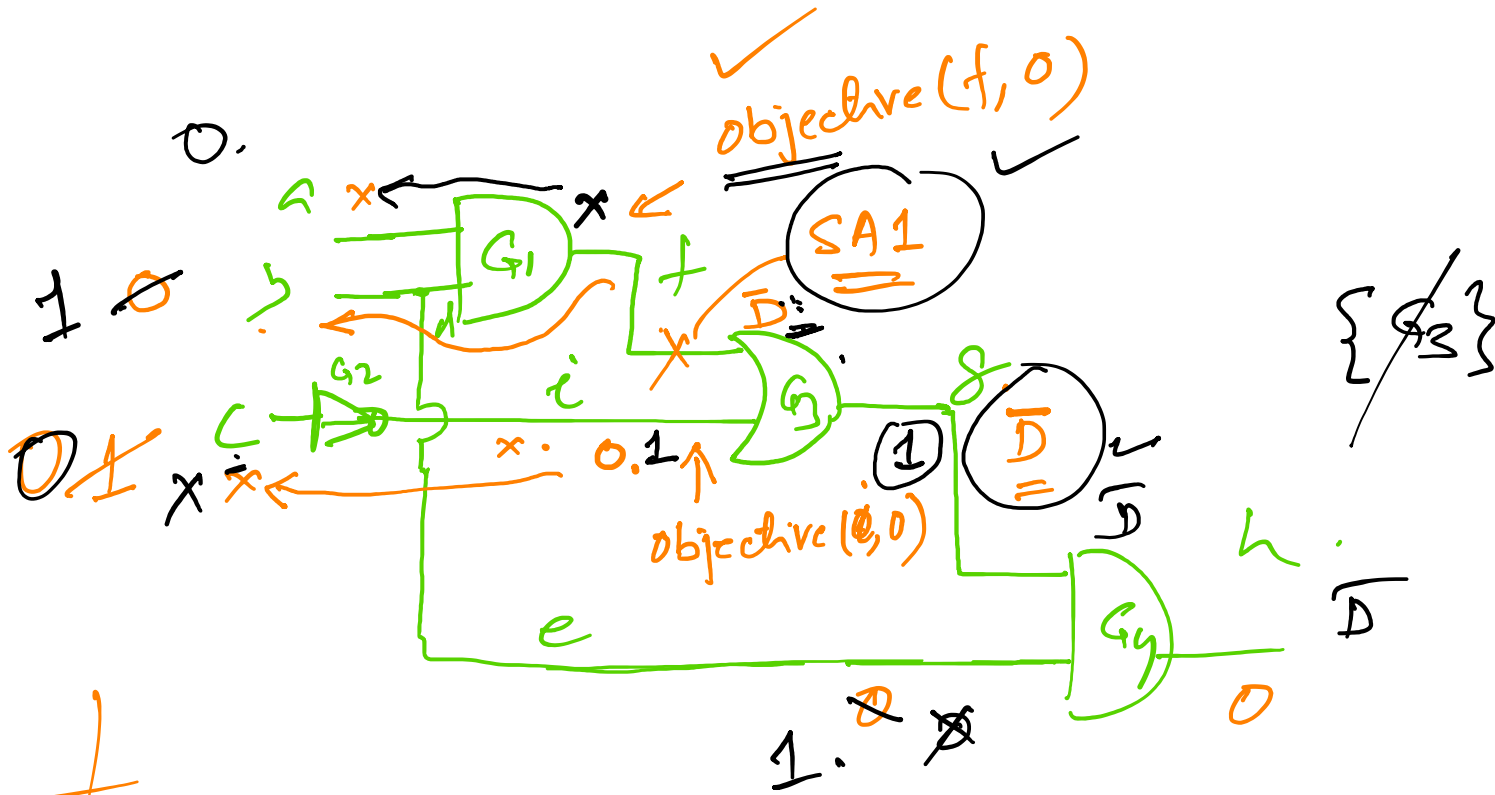
$\{G6\}$



Stack of decisions







Handwritten notes in a grid:

- $c=1$
- ~~$c=x$~~
- ~~$b=0$~~ 1

A red circle highlights a crossed-out x with a red 5 below it.

a var :



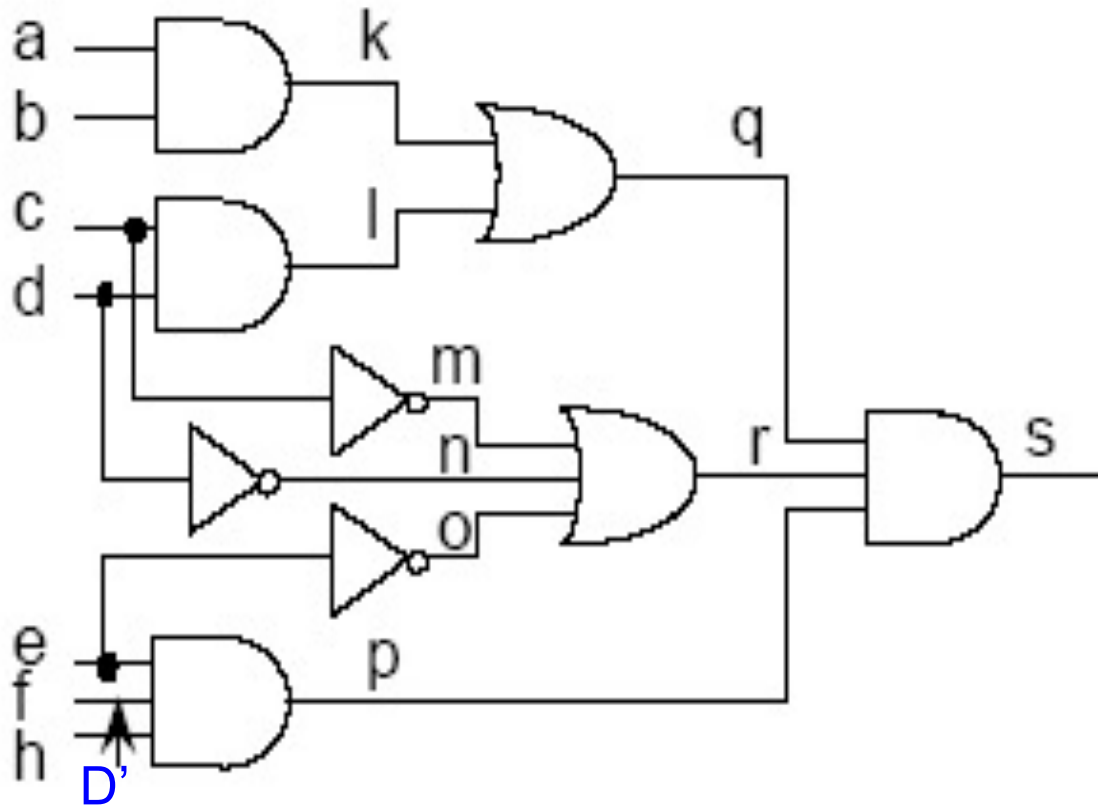
Static
05 Oct 2021

CAD@IITB

10

CADSL

Decisions during LJ



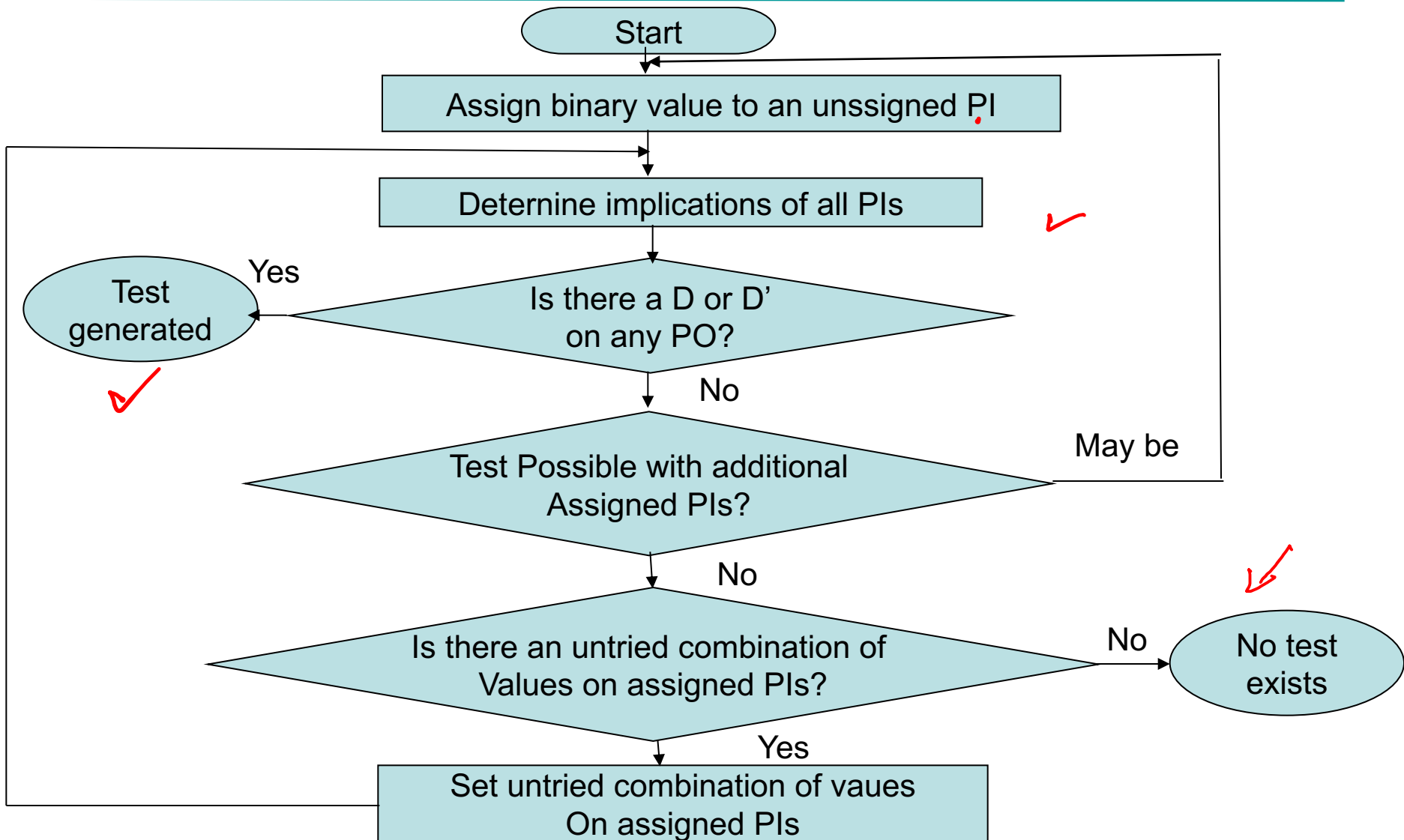
J – Frontier : A set of all gates whose output value is known but not implied by its input value

PODEM High-Level Flow

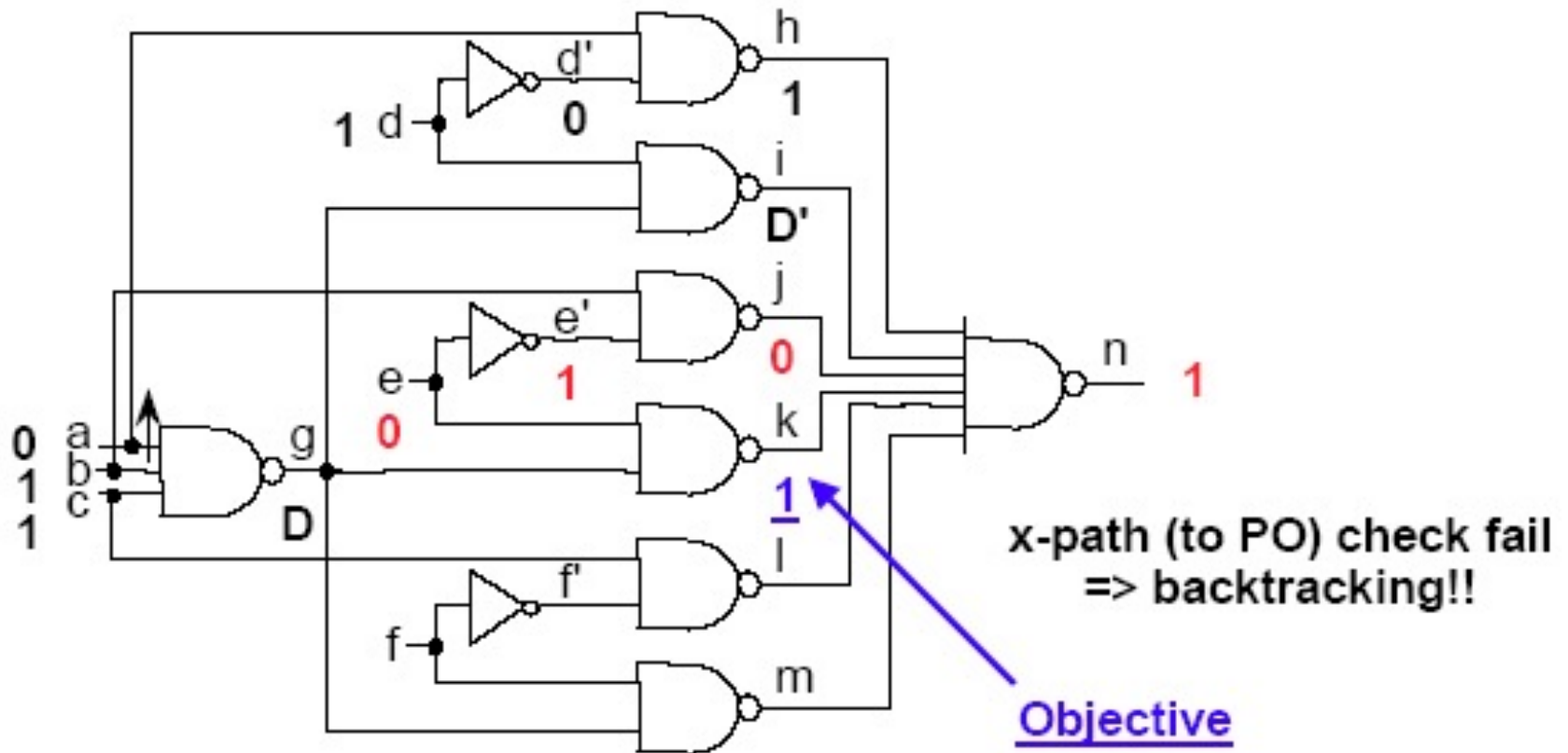
1. Assign binary value to unassigned PI
2. Determine implications of all PIs
3. Test Generated? If so, done.
4. Test possible with more assigned PIs? If maybe, go to Step 1
5. Is there untried combination of values on assigned PIs? If not, exit: untestable fault
6. Set untried combination of values on assigned PIs using objectives and backtrace. Then, go to Step 2



PODEM-Algorithm



PODEM : Example

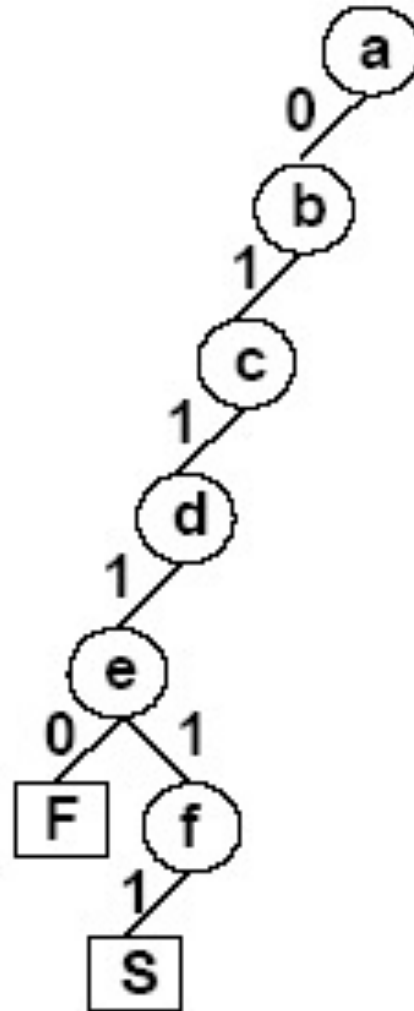


PODEM : Value Comp

Objective	PI assignment	Implications	D-frontier	Comments
a=0	a=0	h=1	g	
b=1	b=1		g	
c=1	c=1	g=D	i,k,m	
d=1	d=1	d?0 i=D	k,m,n	
k=1	e=0	e?1 j=0 k=1 n=1	m	x-path check fail !!
	e=1	e?0 j=1 k=D	m,n	reversal
l=1	f=1	f?0 l=1 m=D n=D		



PODEM : Decision Tree



Thank You

