EE 230 – Analog Lab - 2021-22/I (Autumn)

Experiment 5: NMOS Output Characteristics, Common Source Amplifier, and Current Mirror

(Ver 2, Aug 26,2021)

Part A – NMOS Output Characteristics

Learning Objectives

1. Working knowledge of using NMOS model files to simulate NMOS dc circuits.
2. Understanding the overall output characteristics of an NMOS transistor and the dependence of I_D on V_{GS} and V_{DS}.
3. Understanding the biasing and performance of an NMOS Common-Source amplifier.
4. Understanding the design and implementation of a practical current mirror using a general purpose *NMOS* arrays IC (ALD1106).

1.1 NGSPICE Simulation of MOSFET Circuits

Simulation of MOSFET circuits is very different compared to that of BJT circuits. MOSFET parameters depend directly the process technology used, such as 5 μm, 0.5 μm, 180 nm, etc. Accordingly, one has to use the right model for the MOSFET circuit in question.

Please refer to Chapter 11 of the NGSPICE-34 Manual on "MOSFETs". We will be using MOS Level 1 model, which is the most basic one, and referred to mostly in basic textbooks, such as Microelectronic Circuits: Sedra & Smith.

In particular, go through "Sec 11.2.5 Notes on Level 1-6 models" (pp.156-159) of the NGSPICE-34 Manual.

Model file format

MXXXXXXX nd ng ns nb mname <m=val > <l=val > <w=val >
+ <ad=val > <as=val > <pd=val > <ps=val > <nrd=val >
+ <nrs =val > <off > <ic=vds , vgs , vbs > <temp =t>

(where **nd**, **ng**, **ns**, and **nb** are the drain, gate, source, and bulk (substrate) nodes, respectively. **mname** is the model name and **m** is the multiplicity parameter, which simulates 'm' paralleled devices. All MOS models support the 'm' multiplier parameter. Instance parameters **l** and **w**, channel length and width respectively, are expressed in meters. The drain and source diffusion areas are ad and as, in square meters (m2). If any of l, w, ad, or as are not specified, default values are used.)

The dc characteristics of the level 1 MOSFETs are defined by the device parameters **vto**, **kp**, **lambda**, **phi** and **gamma**. These parameters are computed by ngspice if process parameters (**nsub**, **tox**, ...) are given, but users specified values always override. **vto** is positive (negative) for enhancement mode and negative (positive) for depletion mode N-channel (P-channel) devices.

Charge storage is modeled by three constant capacitors, **cgso**, **cgdo**, and **cgbo**, which represent overlap capacitances, by the nonlinear thin-oxide capacitance that is distributed among the gate, source, drain, and bulk regions, and by the nonlinear depletion-layer capacitances for both substrate junctions divided into

bottom and periphery, which vary as the **mj** and **mjsw** power of junction voltage respectively, and are determined by the parameters **cbd**, **cbs**, **cj**, **cjsw**, **mj**, **mjsw** and **pb**.

Please refer to the Table on "MOS level 1, 2, 3 and 6 parameters" (pp157-159) to understand the various parameters used in the MOSFET model as well as their default and sample values.

Sample model file for MOSFET DC Circuits

```
.model NXYAA5U nmos Level=1 Vto=0.7 KP=80u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.0
```

Note: Most of the discrete MOSFET devices use either the 5 μm or the 0.5 μm technology.

1.1.1 Simulation Exercises

Try worked out exercise problems where all the basic parameters of NMOSFET are given.
For example: Problems on page 253 (Sedra & Smith, 5ed.) – problem sheet included in the folder.

Exercise 1

a) Given: $V_t = 0.7$ V, $V_{GS} = 1.5$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, W=10 μm, L=1 μm. Find I_D for i) $V_D = 0.5$V, ii) $V_D = 0.9$ V, iii) $V_D = 3$ V.
   (Ans: i) 275 μA ; ii) 320 μA ; iii) 320 μA).
b) Given $V_t = 0.7$ V, $I_D = 100\ \mu A$, $V_{GS} = V_{DS} = 1.2$ V. Find I_D for $V_{GS} = 1.5$ V (Ans: 256 μA)

1.2 NMOS Output Characteristics

Circuit schematic used for measuring the NMOS output characteristics is shown in Fig.1.
Circuit values: $V_{DD} = 10$ V, $R_1 = 2.2$ kΩ, $R_2 = 10$ kΩ (Pot), $R_D = 2.2$ kΩ.

ALD 1106 – NMOS Array
Note: The body of each NMOS (pin 4 is the common body terminal) must be connected to the most negative point in the circuit.

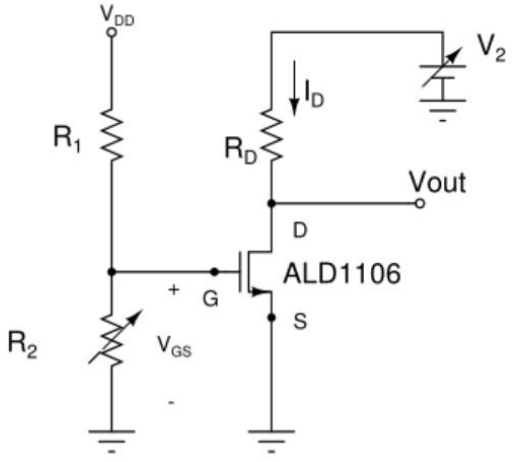

Fig 1 Circuit diagram used for NMOS characteristics

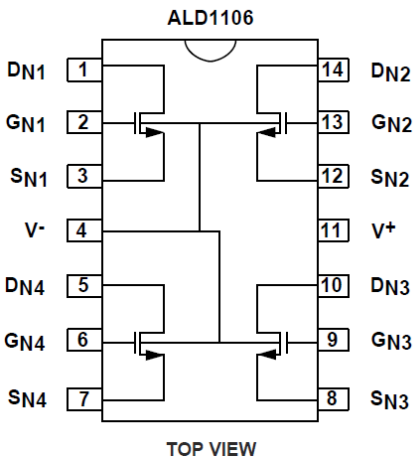

Fig.2 Pinout of ALD1106 NMOS array

Experiment

The output characteristics (i.e. I_D vs V_{DS}) were obtained by setting a few VGS values with the potentiometer R_2. Now for each of these V_{GS} values, the supply voltage V_2 was varied and the corresponding V_{DS} values were measured. I_D was calculated as $I_D = (V_2 – V_{DS})/R_D$.

1.2.1 NGSPICE Simulation

i) Using the following NMOS model given earlier obtain the output characteristics for a few VGS values. You may use dc analysis for plotting. See an example given in the **Ngspice-PPT-2017.pdf** for obtaining the NMOS output characteristics (see Expt 1 handout for details of the above PPT).

Note: Modify the sample model file parameters to obtain I_D of 1 mA (approx.) for VGS = 2 V. Try VGS values of 2 V, 3 V, 4 V and 5 V.

Part B – Common-Source Amplifier

2.1 NMOS Common-Source Amplifier (Bias Circuit)

Circuit schematic of an NMOS Common-Source amplifier bias circuit is shown in Fig.3.

Circuit values used: V_{DD} = 12 V, R_1 = 8.2 kΩ, R_2 = 3.3 kΩ, R_S = 1 kΩ, R_D = 3.3 kΩ.

ALD 1106 – NMOS Array.

Note: The body of each NMOS must be connected to the most negative point in the circuit.

Experimental results: Measured values of node voltages and current I_D will be shared during the Lab lecture.

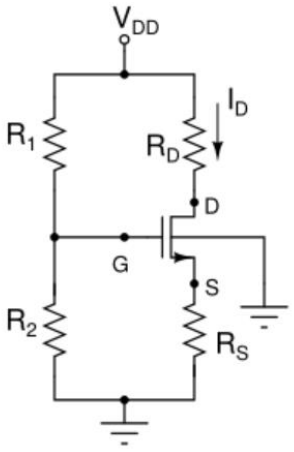

Fig.3 Common-Source Amplifier – bias circuit

Analysis

Assume the following sample values for the NMOS transistor. (W/L) = 10 ; $k_n' = \mu_n C_{ox}$ = 100 μA/V^2 ; V_t = 1 V. Assume I_D = 1 mA (approximately).

2.1.1 NGSPICE Simulation

Modify the NMOS model file with the given device parameters. Keep LAMBDA = 0 (i.e. no channel-length modulation). Obtain current I_D and voltages V_G, V_D and V_S. Compare your results with the analysis.

2.2 NMOS Common-Source Amplifier

Circuit values: V_{DD} = 12 V, R_1 = 8.2 kΩ, R_2 = 3.3 kΩ, R_S = 1 kΩ, R_D = 3.3 kΩ, C_S = 100 μF, C_1 = 10 μF

ALD 1106 – NMOS Array.
Note: The body of each NMOS must be connected to the most negative point in the circuit.

Experimental results: Will be shared during the Lab lecture. V_{in} = 50 sin ωt mV (f = 1 kHz)

Analysis of CS amplifier

i) Small-signal parameters: Calculate the small-signal parameters g_m and r_o assuming I_D = 1 mA (g_m = transconductance and r_o is the output resistance). Take $V_A = 1/\lambda$ = 100 V.

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D} \quad ; r_o = \frac{V_A}{I_D} \ .$$

ii) Calculate the voltage gain of the CS amplifier, $Av = -g_m (R_D || r_o)$ – assuming $R_L = \infty$.

2.2.1 NGSPICE Simulation

Modify the NMOS model file with the given device parameters, and LAMBDA = 0.01. V_{in} = 50 sinωt mV (f = 1 kHz). Perform .**tran** analysis and plot V_{in} and V_{out} waveforms. Find out the midband voltage gain and compare it with your analytical results.

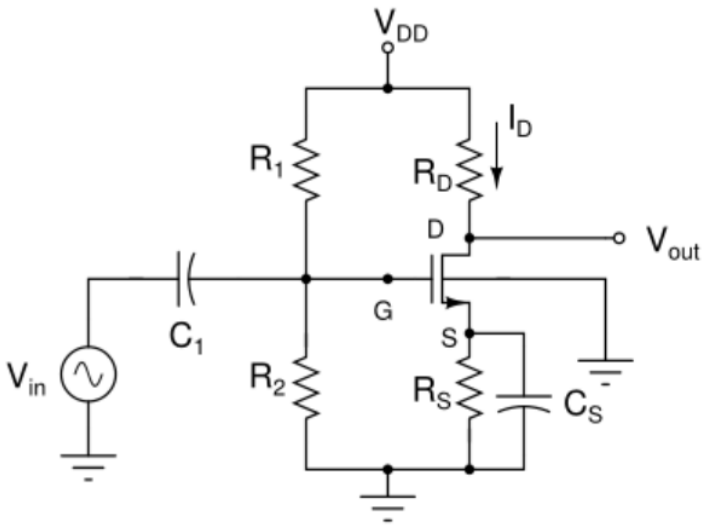

Fig.4 Common-Source Amplifier – full circuit

Part C – NMOS Current Mirror based Current Source

3.1 NMOS Current Mirror based Current Source

Circuit schematic of an NMOS current mirror based current source is shown in Fig.5.

Circuit values: V_{DD} = 12 V, R = 8.2 kΩ.

ALD 1106 – NMOS Array.

You may assume the NMOS transistor parameters: (W/L) = 10 ; $k_n' = \mu_n C_{ox}$ = 100 μA/V^2 ; V_t = 1 V ; V_A = 100 V (= 1/λ)

Note: The body of each NMOS must be connected to the most negative point in the circuit.

Experimental results: Will be shared during the Lab lecture.

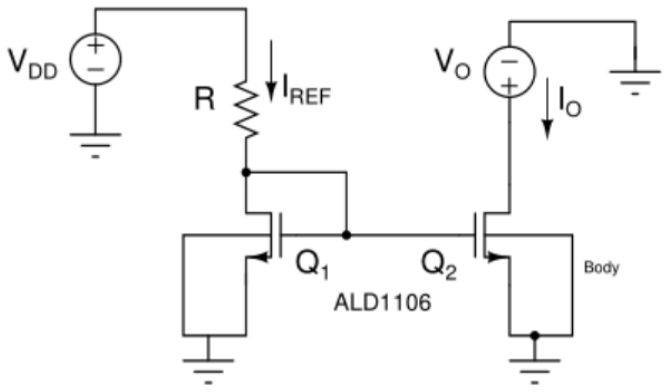

Fig.5 NMOS Current mirror based Current source

Analysis

Using the NMOS parameters given above, estimate current I_{REF} and the output current I_O for a few V_O values (1 to 5 V).

Note: $I_o = I_{REF}\left(1 + \frac{V_o - V_{GS}}{V_A}\right)$

3.1.1 NGSPICE Simulation

Using the NMOS parameters modify the NMOS model file and obtain current I_{REF} and the output current I_O for V_O values (1 to 5 V in steps of 0.2 V). Compare your results with the hand calculations.

Lab Report

1. For Experiment 5, please limit your Lab report to just 4 pages – one page for the NMOS characteristics, two pages for the Common source amplifier (biasing circuit and the amplifier) and one page for the NMOS current mirror based current source.
2. In each page, please include one of your NGSPICE programs, and one or two plots or the printed values, as the case may be. Please also add one line of what you learned.
3. The purpose of asking you to make shorter Lab reports is to make sure that you save some time. However, we assume that you have done all that was asked in the Lab handout (analysis and simulations). These and related topics may be asked in the Quizzes, as well as in the Midsem and Endsem examinations.