High Level Synthesis

⇒ Power Issues

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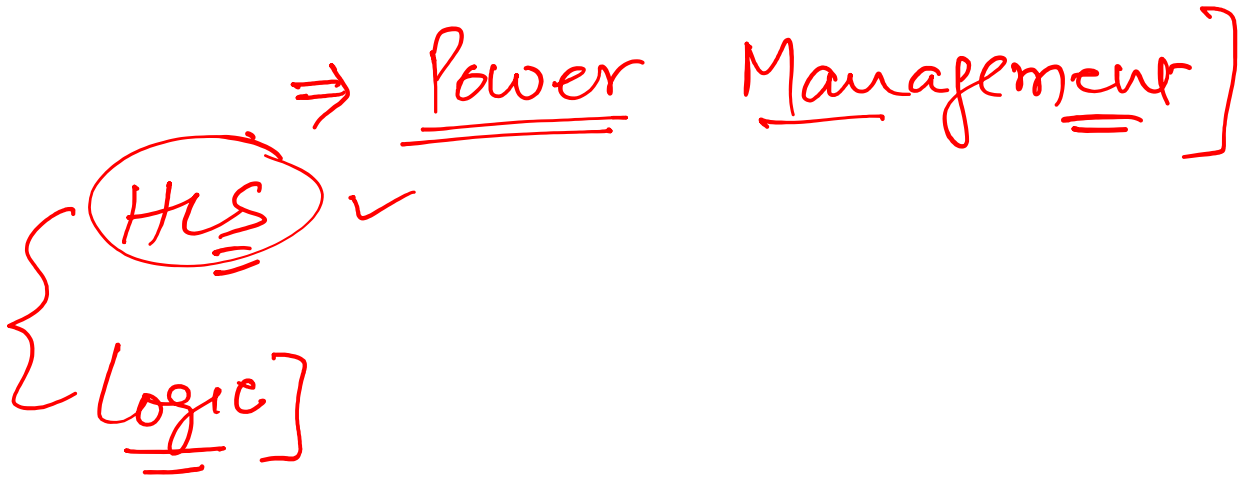
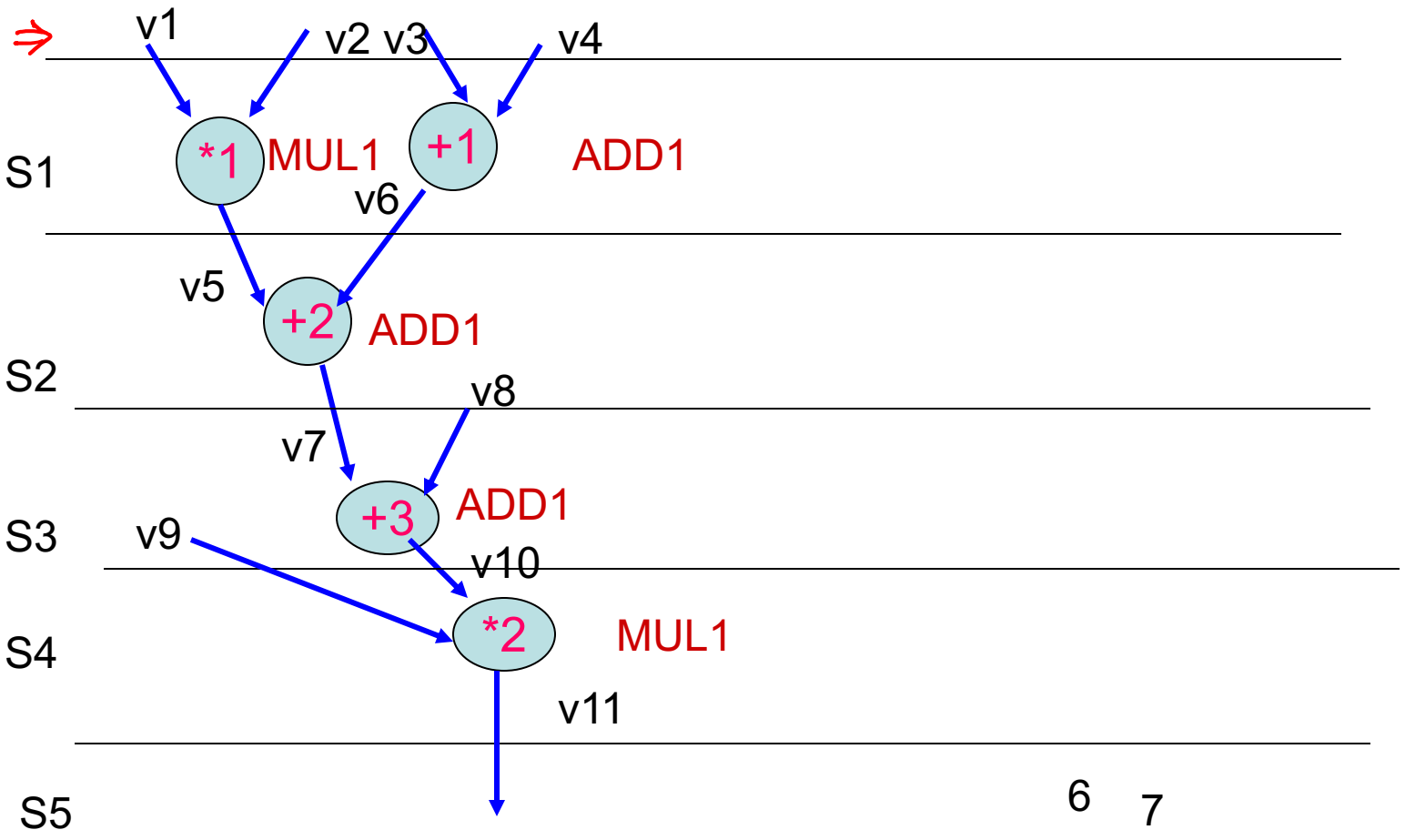
EE-677: Foundations of VLSI CAD

Lecture 15 on 06 Sep 2021

CADSL


⇒ Power Management]
HLS
Logic]

Scheduled DFG



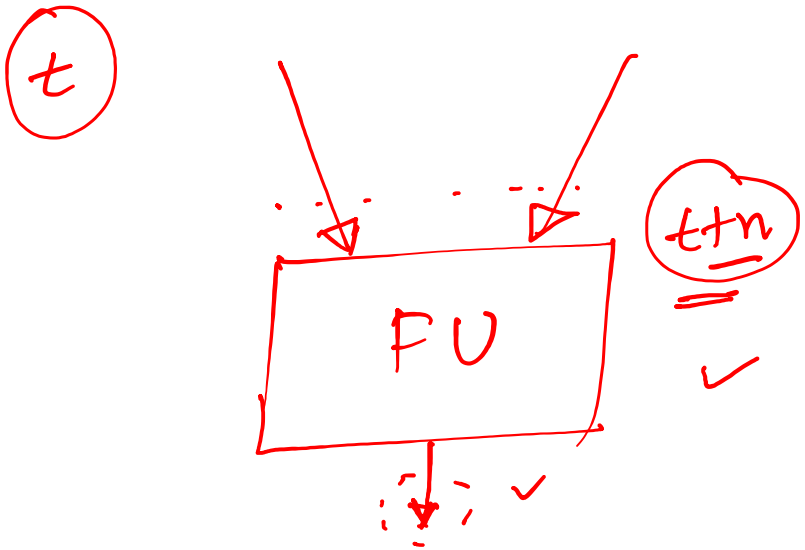
Variable Assignments

left edge algorithm.

Register	Assignment1	Assignment
R1	V1, V5, V7, V9	V1, V9
R2	V2, V6, V8, V10	V2, V10
R3	V3	V3, V5, V7
R4	V4	V4, V6, V8

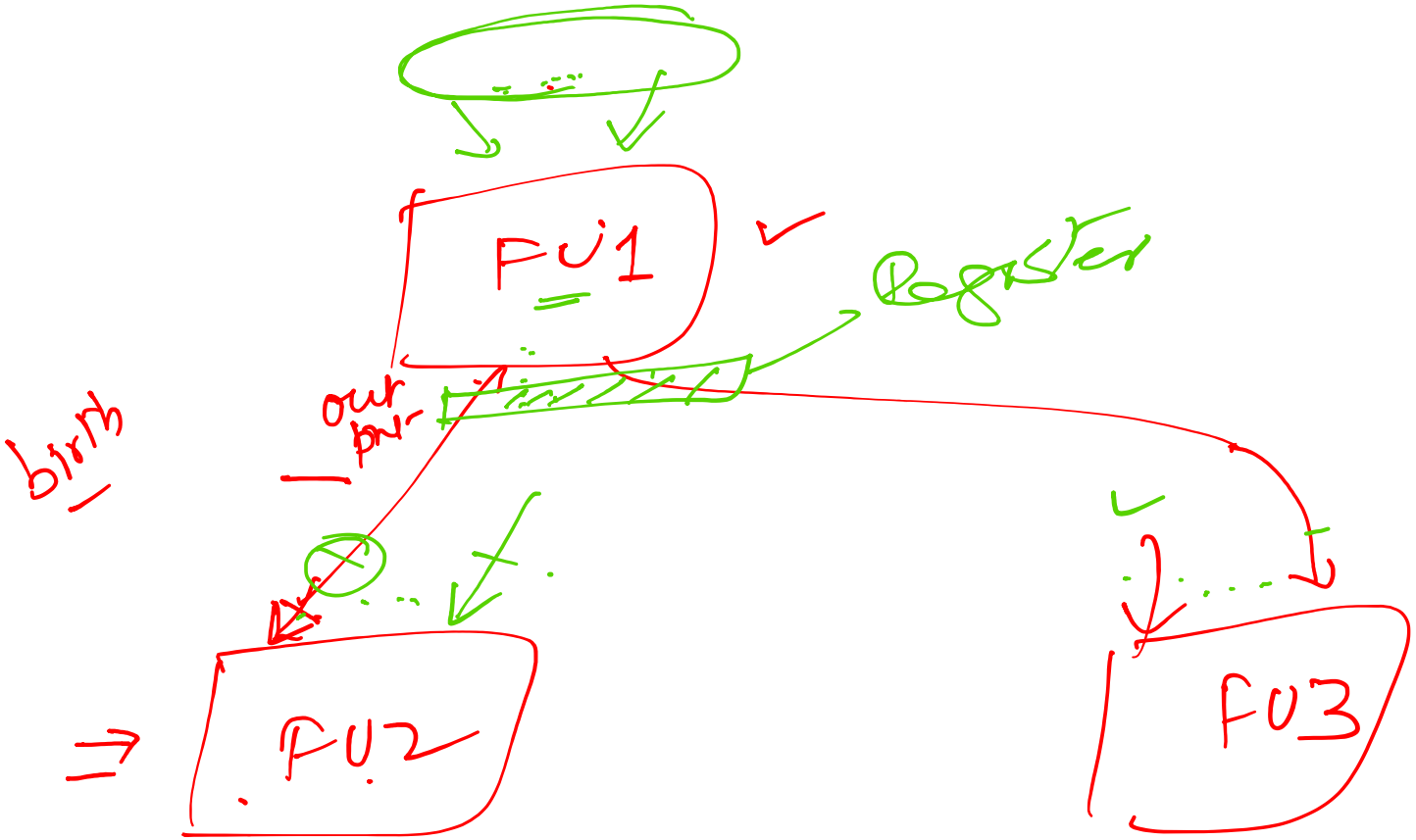
spurious switch.

minimize spurious switching



every FU every operation

Both inputs should change at the same time.


FU1
Register
birth
our par
FU2
FU3

Power Management Technique

Perfect Power Management{

- For each functional unit *fu*{
  - for each operation mapped to *fu* (*op*){
    - if op is the last operation born in fu return TRUE;
    - for each input variable v_{ini} of operation *op*{
      - tbirthLnext <- birth time of left input of the operation succeeding op on fu
      - tbirthRnext <- birth time of right input of the operation succeeding op on fu
      - SET_DEATH_TIME (vin_i, max (tbirthLnext, tbirthRnext);

Power Reduction Techniques

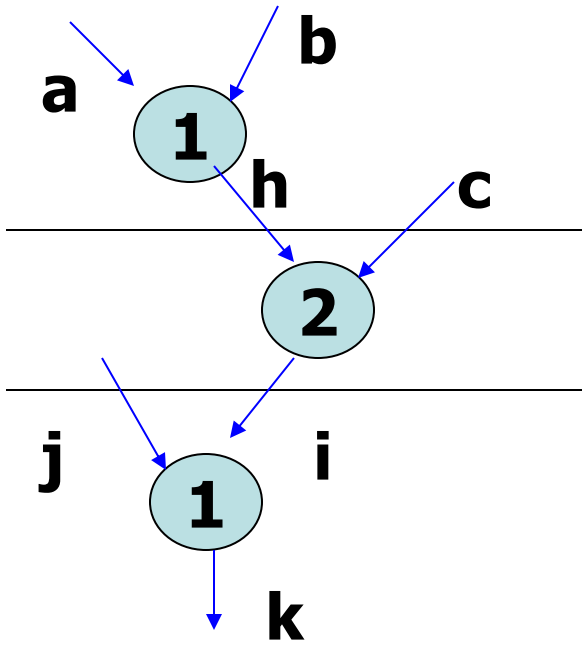
- if (LIFETIME (vin_i) conflicts with lifetime of other variable mapped to the same register) return FALSE;
- Set multiplexers at *fu's* input to select vin_i

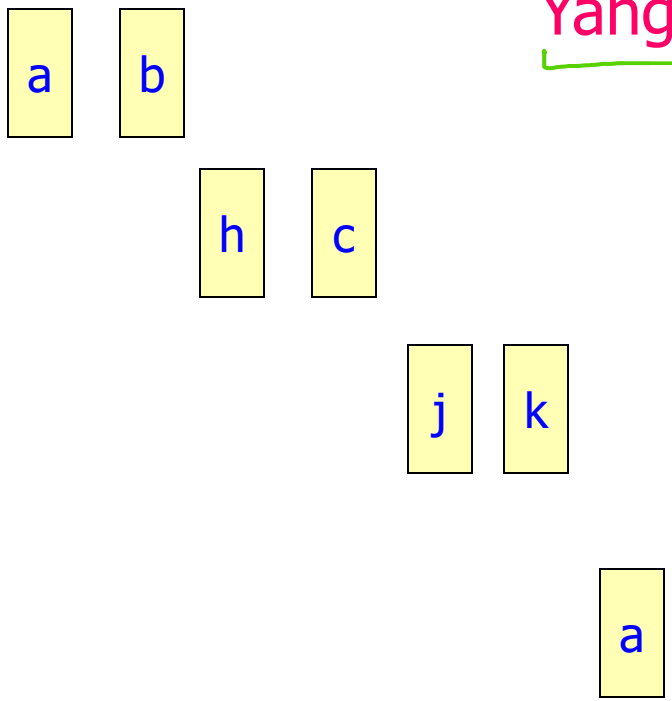
  until max ($tbirthL_{next}$, $tbirthR_{next}$);

}

}}

Power Management using Latches

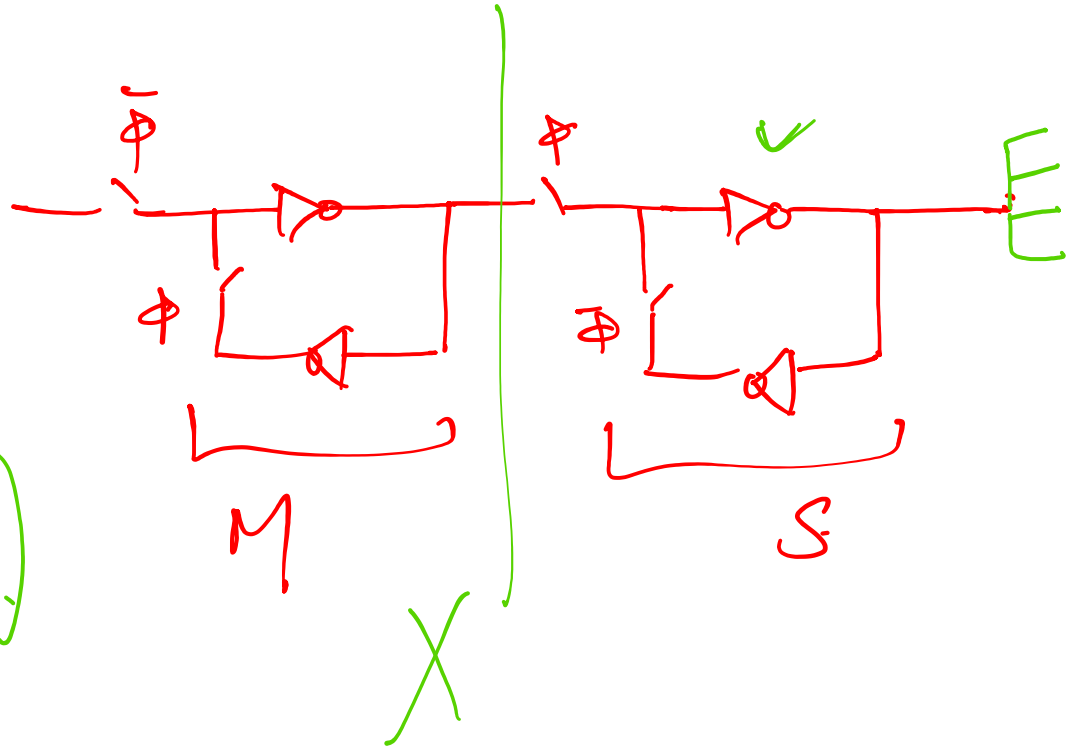




Yang et al

Latch

DFF ✓ Master Slave D Latches ✓

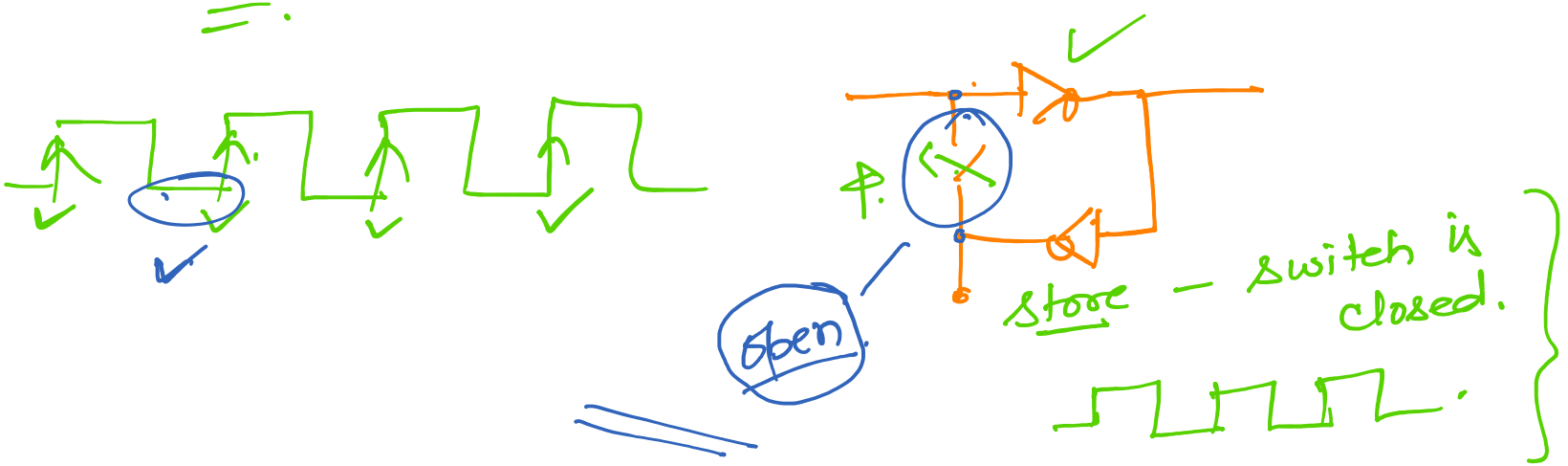


Reduce power if we can use only latch

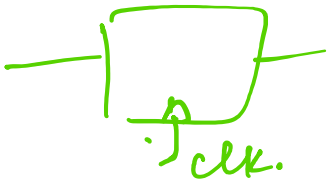
30% reduction

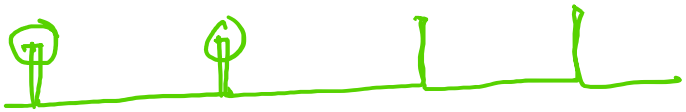
FF ?

Synchronous behaviour.

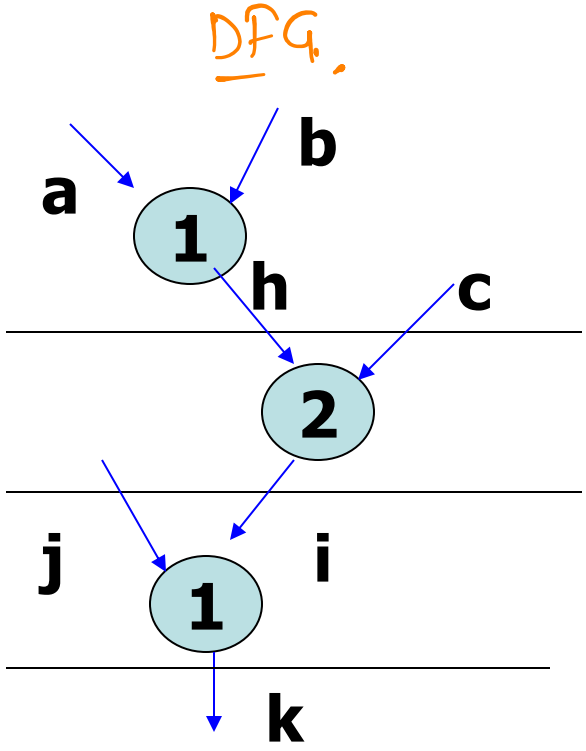


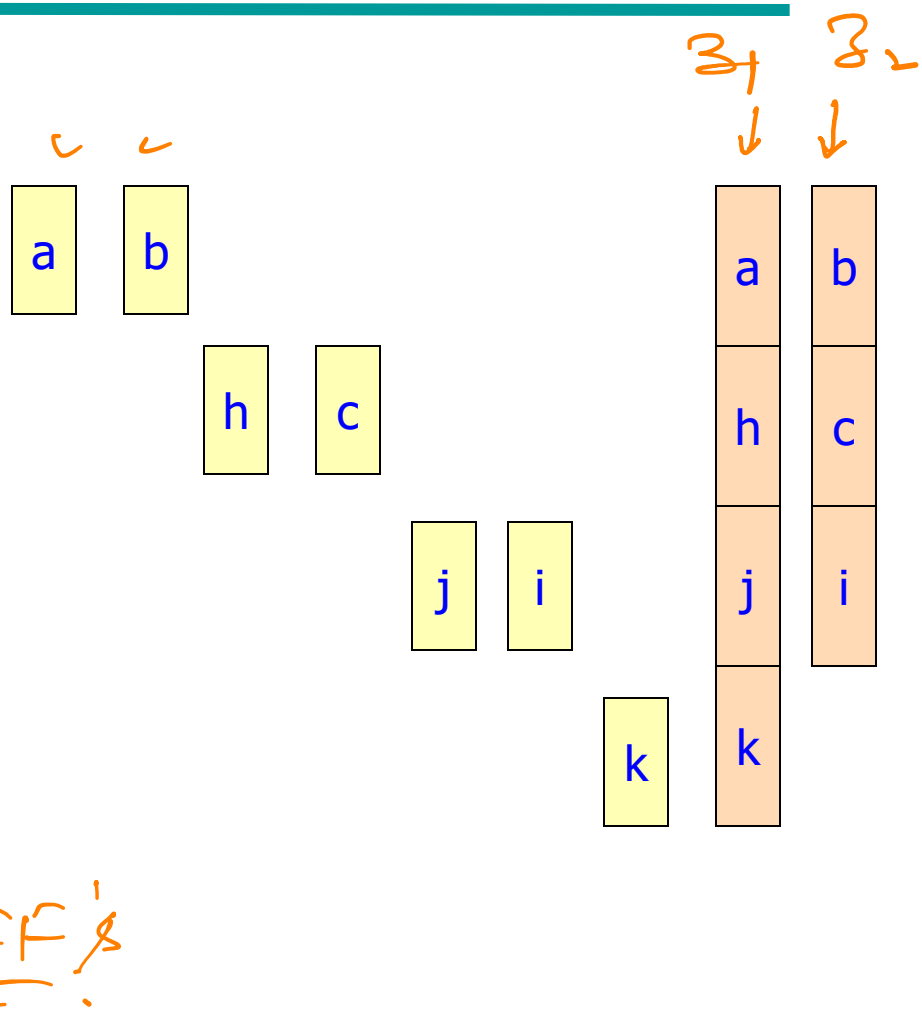
Control input transitions





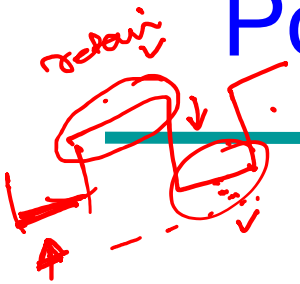
Power Management using Latches

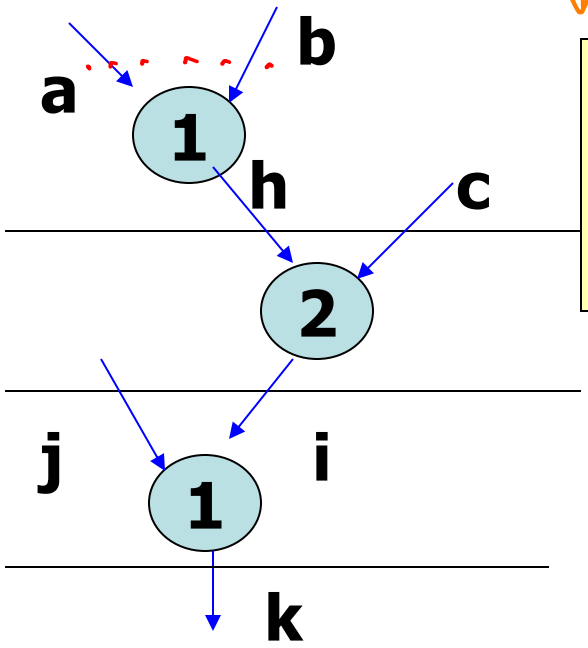




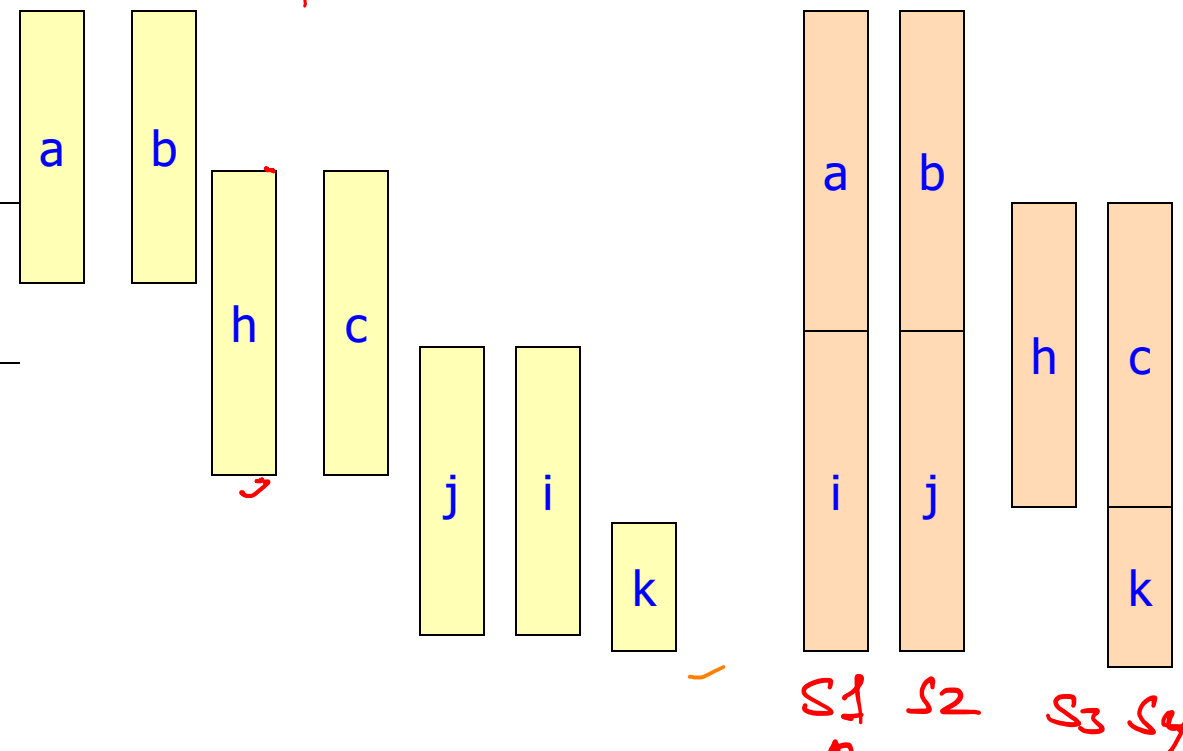
FF's

Power Management using Latches





extend the liveness range of variables to 2 cycles.

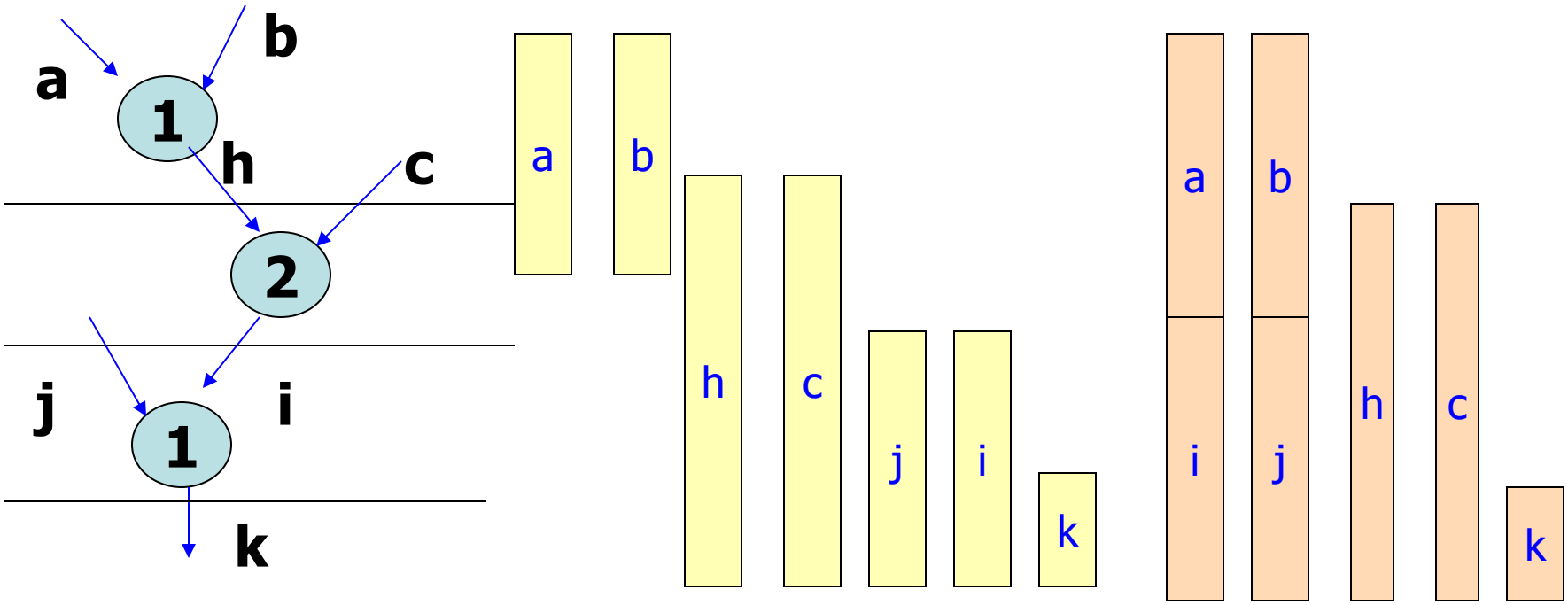


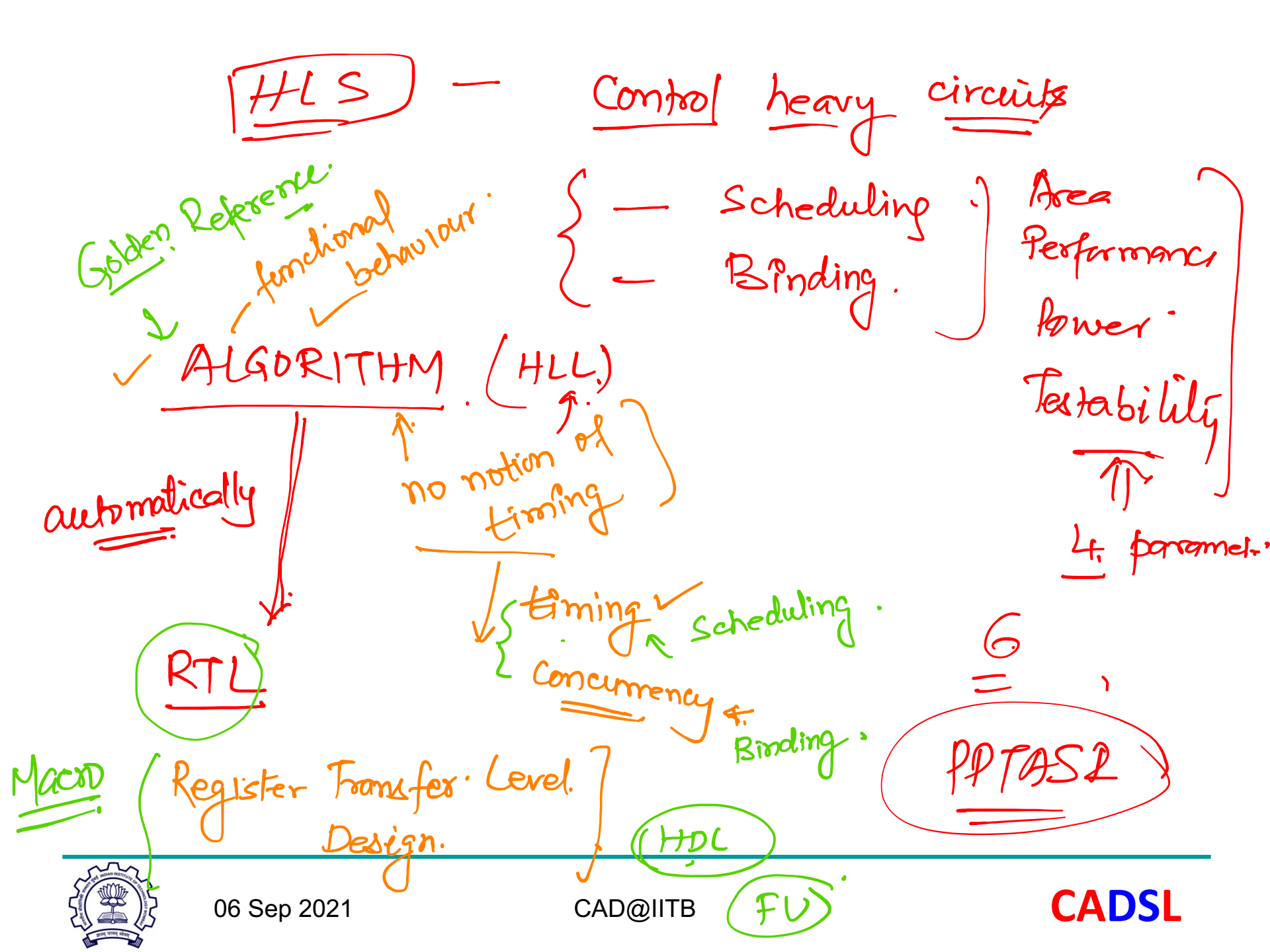
j, k will produce spurious transitions

Storage element

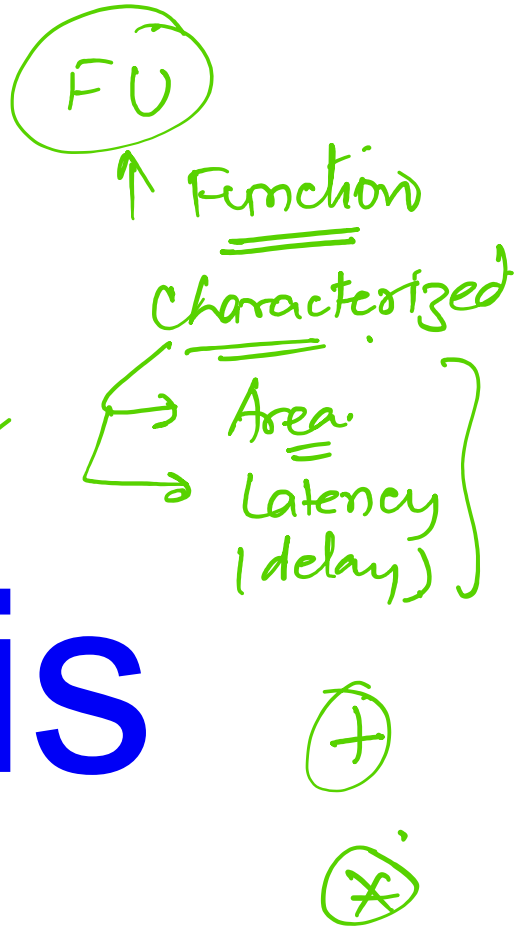
FF / Latch.

Power Management using Latches




HLS — Control heavy circuits
Golden Reference
functional behaviour
ALGORITHM (HLL)
automatically
RTL
no notion of timing
Timing
Scheduling
Concurrency & Binding
Scheduling
Binding
Area
Performance
Power
Testability
4 parameters
6
=
PPTAS2
MACRO
Register Transfer Level Design
HDL
FU

Logic Synthesis



Representation of logical function

~~Optimiz~~ optimization – K Map)

Boolean Algebra)

SOP / POS / AIG ⇐ non-canonical representation

Truth Table / SOM / POM / ROBDD / Reed Muller

Canonical

Thank You