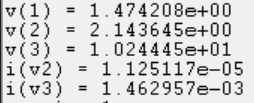
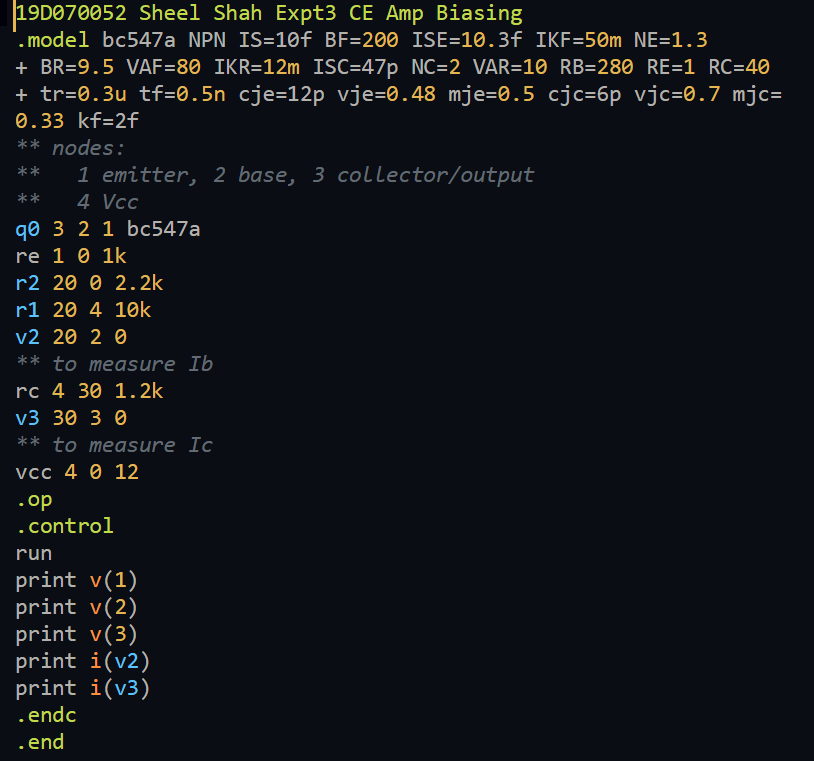
Sheel Shah, 19D070052, Expt3

Q1.

Analysis:  
Req = 2.2 || 10 = 1.8k. Veq = 12\*2.2/12.2 = 2.16V.  
Veq = ib x Req + 0.7 + (beta +1)\*ib\*Re => ib = 7.2 uA.   
Ic = beta\*ib => ic = 1.44 mA  
Vo = 12 – ic\*rc = 10.272V  
Ve = (beta+1)\*ib \*re = 1.45V  
Vb = Ve + 0.7 = 2.15V

Simulation:  
  
(refer to the code below to see what node number is what node)

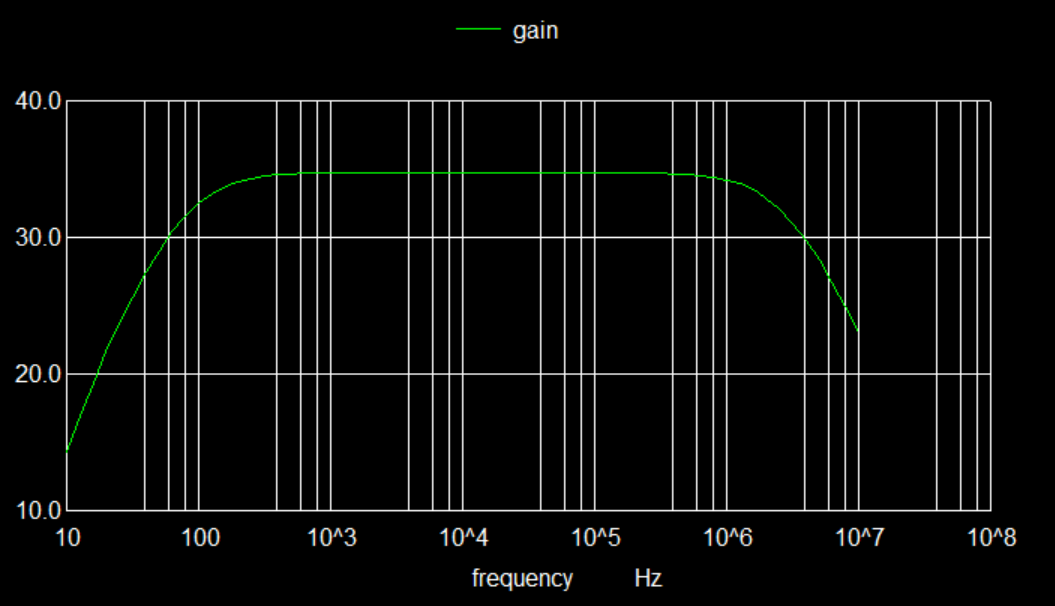
Code:  


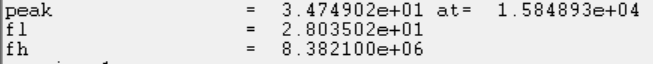
Learnings:

1. Not all the assumptions we make are accurate/correct.
2. Simulations and analysis can be slightly different, but shouldn’t be too off.

Q2.



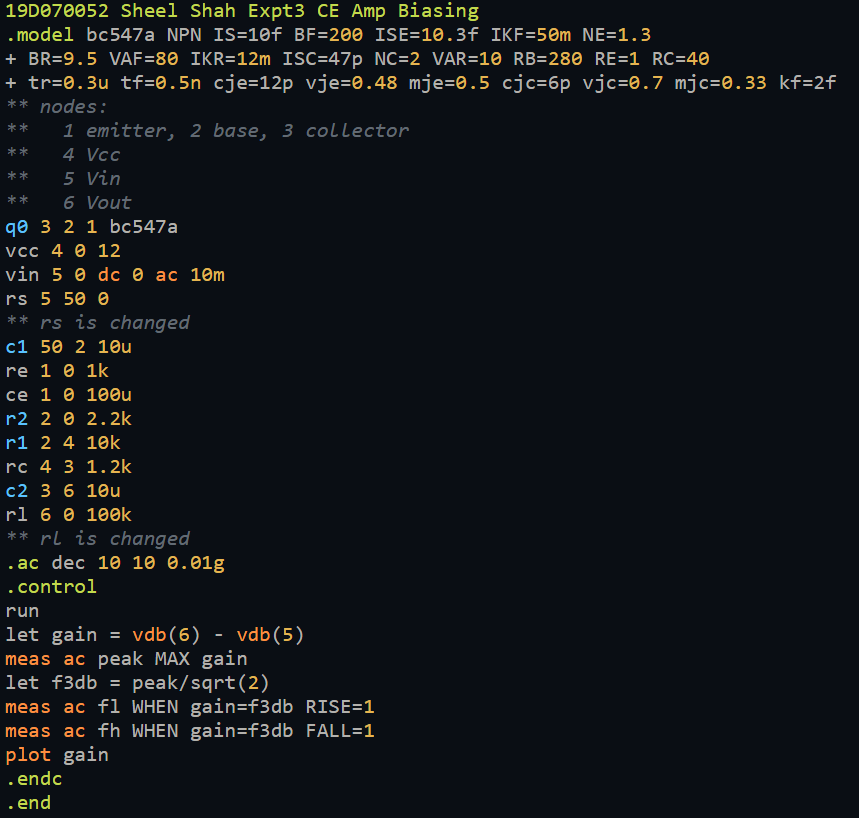




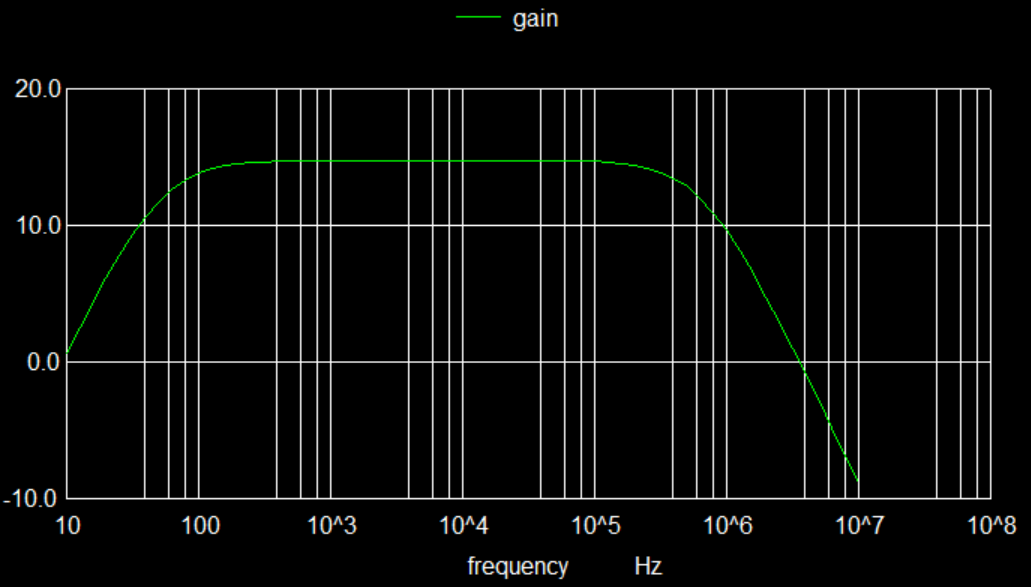
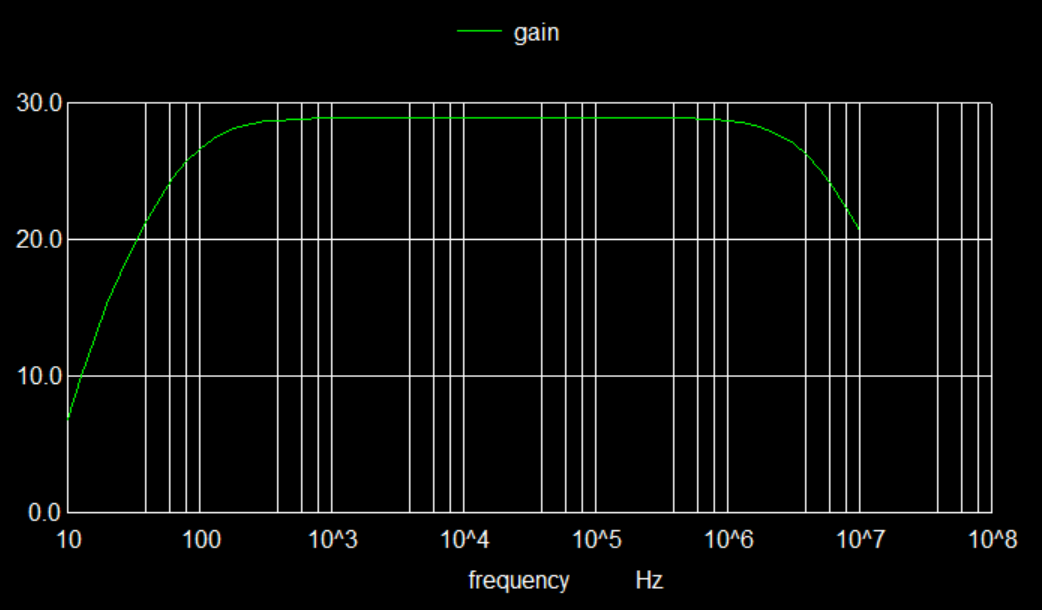
Learnings:

The CE amp has good gain, and a decent bandwidth. However, we know that Rin and Rout values are not appropriate.

Q3.



When Rl is 12k, gain is 34.038 dB. When Rl is 1.2k, gain is 28.917 dB.  
When Rs is 2.2k, gain is 25.283 dB. When Rs is 10k, gain is 14.774 dB.



Learning:

Gain is directly proportional to Rc||Rl and hence decreases with Rl.  
As Rs increases, gain decreases.

Q4.





Learnings:

The CC amp buffer helps increase Rin, as well as decrease Rout, making the overall amplifier much better.