# EE 709 Course Outline

Madhav P. Desai (madhav@ee.iitb.ac.in)

January 4, 2022

This course will cover the verification, testing and validation of VLSI circuits. Only digital VLSI circuits will be considered. The material covered in the course will be

1. Re-introduction to Boolean algebra and first-order logic.
2. Representations of Boolean functions: canonical representations, two-level and multi-level Boolean formulas, binary decision diagrams.
3. Equivalence checking of combinational functions relative to their implementations.
4. The satisfiability problem, and heuristics for its solution.
5. Verification of sequential systems: finite state machine equivalence checking.
6. Higer order logic and temporal logic. Describing and verifying properties.
7. The testing problem.
8. Fault models.
9. Test generation.
10. System architectures for test: scan, memory testing.
11. Simulation: coverage, fault simulation, symbolic simulation, semi-formal verification.

12. Other topics as time permits.

The theoretical content of the course requires a strong background in Boolean algebra. Further, the course itself is motivated by the need to verify complex systems, so there will be a practical aspect (re: programming, use of tools). The overall evaluation scheme will be 30% in semester quizzes/tests, 20% assignments, and 50% final exam.

Useful texts for the theoretical content:

- Z. Kohavi, N. Jha, *Switching and Finite Automata Theory*, Cambridge.
- Irving Copi, *Symbolic Logic*, Pearson.

Additional reading material will be suggested during the course.