EE 350 – Module 5 Technical Paper Writing & Presentation

Shiladri Chakraborty

Where we are now in the course



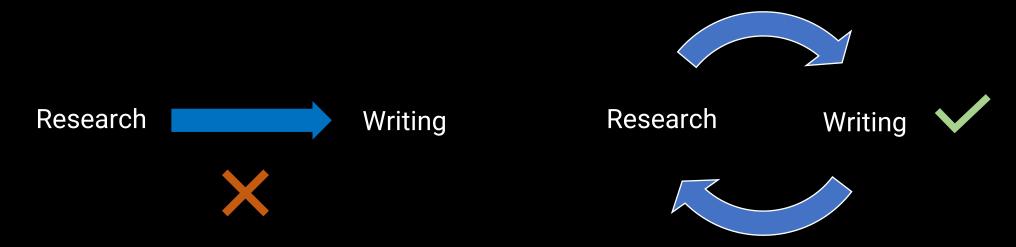
Learning Objectives of This Module

- Understand the different parts of a technical paper
- How to draft a technical paper ?
- How to give a technical presentation?
- Style in academic writing

Why writing/communication is important for research?

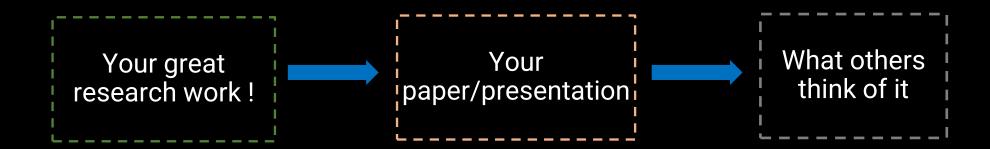
1. Writing/communication is a tool for research, not an outcome

- You understand a research problem better when you write about it, talk about it
- Write while you do the research, not at the "end" of it
 - -> improves both research output and writing



Why writing/communication is important for research?

- 2. Writing/communication is critical for doing "justice" to your research efforts
 - If your great idea or work is not communicated well,
 - -> it does "injustice" to you!
 - -> it does "injustice" to science and society-at-large!



Structure of a technical paper

Broad parts

- Title
- Abstract
- Keywords
- Introduction
- Methods
- Results
- Conclusions
- Appendix
- Acknowledgement
- References

Basic "elements"

- Text divided into sections and subsections
- Equations
- Figures
- Tables

Planar Transformer with Asymmetric Integrated Leakage Inductance Using Horizontal Air Gap -

Michael D'Antonio, Student Member, IEEE, Shiladri Chakraborty, Member, IEEE, and Alireza Khaligh, Senior Member, IEEE

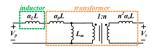
Abstract-This manuscript presents a novel planar-based transformer winding and core structure with controllable leakage inductance generation for integrated magnetics applications. As a result of limitations in integrated magnetics from the literature, a new approach is proposed utilizing semi-interleaved winding and controllable leakage via a leakage flux core leg featuring horizontal air gap. The proposed transformer design is analyzed via detailed reluctance modeling to determine closed-form equations for the magnetizing and asymmetrically distributed leakage inductances. Next, a genetic-algorithm-based multi-objective design optimization problem is developed, seeking to minimize the core and winding losses of the proposed transformer subject to a set of parametric and geometric constraints in a DC-AC dual-active-bridge topology for microinverter applications. The optimization was extended to include other integrated magnetics structures from the literature, where it is determined that the proposed transformer is superior from the perspectives of efficiency, footprint area, and parasitic capacitance. Based on the results of the optimization analysis, two designs with theoretical transformer CEC efficiency drops (i.e. CEC efficiency reduction a discrete series induced, and a near-ideal transformer with specifically due to the transformer loss mechanisms) of 1.19% and low leakage inductance, represented in Fig. 1 0.83% were fabricated and evaluated for electrical and thermal performance in the proposed 40 V, 400 W microinverter.

High-frequency transformers are at the heart of many widely used isolated power converter topologies like flyback, phaseshifted-full-bridge (PSFB), resonant (LLC, CLLC), and dualactive-bridge (DAB), among others [1]. In flyback and PSFBbased topologies, the leakage inductance of the transformer is an undesirable parasitic element, which leads to voltage spikes across switches and is thus intended to be kept as low as possible in a good design. On the contrary, resonant and DABbased topologies include an impedance network between the magnetizing inductance into a single transformer structure primary and secondary side of the transformer, consisting of [2]- [16]. In general, the techniques for leakage integration series and parallel inductances. The series inductor acts as an involve manipulation of the transformer core structure [4]energy storage and delivery element and is hence not intended [6], insertion of additional magnetic materials into the core to be minimal. Rather, its value should be high enough to

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insformer. In non-integrated magnetics applications, the series inductor (with $\alpha_r = 1$) and ideally low leakage transformer (where $\alpha_n \approx \alpha_n \approx 0$) are mplemented with independent core and winding sets. In integrated magnetics applications, the series inductor can be eliminated (with $\alpha_T = 0$) as the desired inductance is integrated into the transformer's leakage inductance where $\alpha_p + \alpha_s \approx 1$ when L_m is sufficiently larger than L.

satisfy power-flow, voltage-gain, and zero-voltage-switching (ZVS) requirements of the circuit

Traditionally the inductance network would be realized by 1 and $\alpha_n \approx \alpha_s \approx 0$. More recently, following the trend to design converters with low cost, low loss, and high power density, integration of the series inductor and transformer has been proposed, where the series inductance is realized by the insformer's leakage inductance [2]. To further improve the performance of the integrated structure, an increase in circuit switching frequency has been coupled with the utilization of planar cores with low profile height [2]. The integrated transformer case is also shown in Fig. 1 where α $\{\alpha_p, \alpha_s\} \neq 0$, and hence the inductance distribution in the transformer could be arbitrarily designed.

Previous literature has investigated different ways to controllably achieve desired values of leakage inductance and structure [7]- [13], or manipulation of the winding structure [14]- [16]. The approach in [4] considers the use of vertically Manuscript received February 19, 2021; revised May 23, 2021; accepted stacked transformer and inductor cores, exhibiting limitations in complex transformer core implementation and multiple winding PCBs. An improved planar-based matrix transformer implementation is considered in [5]- [6], where the magnetics core structure includes designated legs and flux paths for a series inductance and ideal transformer.

> In [7]- [9], the primary- and secondary-side windings are both wound around the transformer core center leg, and controllable leakage inductance is realized by placing an intentional air-gap between the primary- and secondary-side wind

Title

IEEE Trans. double-column format

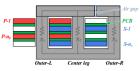
Author names (absent for manuscript under "double-blind" review)

Abstract

"Introduction" section

former, [15] proposes to wind the primary- and secondary side windings asymmetrically (i.e. placing a different number A. Overview of the Proposed Design of primary- and secondary-side turns) around the outer legs A cross-section view of the proposed transformer design of the transformer core as shown in Fig. 2(c). In light of is shown in Fig. 3, including the core, me core's equivalent the winding structure, this transformer is henceforth deemed the asymmetrically-wound controllable leakage transformer (ACL). By asymmetrically distributing the windings, controllable leakage inductance can be generated by tuning the core

reluctance model, and the transformer windings [1]. The core can be realized through the use of an E-core, plus two I-core segments separated by an air gap. In light of the construction, the proposed implementation is henceforth referred to as the



the core is the equivalent reluctance network, realized by a single equivalent reluctance for each core leg. Each winding layer may be comprised of an arbitrary number of turns. White portions in the winding structure indicate the absence of turns on the respective PCB layer

'EII' transformer. As can be observed, the terminal windings are wound around the left leg and the center leg, achieving partial interleaving in the left core window. The mutual flux path is completed between the outer left leg and the center leg, while the leakage flux path is completely between the winding legs and the outer right leg. Due to the fact that the leakage flux path is completed through the outer right leg, there is freedom to place an air gap anywhere along the core leg. As such, the air gap is shown to be placed along the top-section of the core (deemed a horizontal air-gap) to reduce the magnitude of the

(b) equivalent reluctance network modeling. In (a), inner core dimensions perpendicular component of the H-field at the winding, and improve the H-field symmetry along the cross-section of the windings [17]. As a result, the winding DC-to-AC resistance ratio is reduced as compared to placement of the air gap along the vertical section of the core.

B. Reluctance Modeling

The detailed reluctance model of the core is presented in Fig. 4. Due to the fact that the mutual flux path is ungapped in the proposed implementation (where otherwise the air-gap is a dominant reluctance component compared to he core reluctances), consideration of separate reluctances for the corners and straight core segments is critical, originally motivated and modeled in [18]. The considered lengths and areas of each reluctance segment is shown in Table I, and the reluctances can be calculated via

$$R_x = \frac{l_x}{\cdots \cdots A}$$

where l_x is the length of the reluctance segment, A_{τ} is the effective cross-section area of the reluctance segment, and $\mu_{r,x}$ is the relative permeability of the core segment. The air-gap

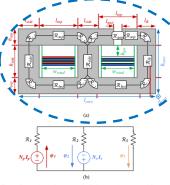


Fig. 4. Proposed transformer (a) detailed core reluctance modeling, and are labeled in red, while the external core dimensions are labeled in blue.

Additional dimensions related to the winding structure are identified in green. The primary-side windings extending outside of the core footprint on the left have not been shown for implicity.

TABLE I. LENGTHS AND AREAS FOR EACH RELUCTANCE IN FIG. 4(a).

Reluctance (x)	Length	Area	
Side (side)	h_{oide}	$l_{side}d_{core}$	
Corner 1 (c1)	$\pi(h_{top} + l_{side})/8$	$d_{core}(h_{top} + l_{side})/2$	
Top / bot (top / bot)	l_{top}	$h_{top}d_{core}$	
Corner 2 (c2)	$\pi(h_{top} + l_{side}/2)/8$	$d_{core}(h_{top} + l_{side}/2)/2$	
Top' (top')	$l_{top} - l_{gap}$	$h_{top}d_{core}$	
Gap (gap)	l_{gap}	$h_{top}d_{core}$	
Leak (lk)	h_{side}	likdcore	
mer 3 (c3)	$\pi(h_{ton} + l_{lk})/8$	$d_{core}(h_{ton} = l_{lk})/2$	

From the equivalent circuit, equations for the flux in each of the three core legs can be derived as

$$\phi_1 = \frac{N_p I_p (R_2 + R_3) - N_s I_s R_3}{R_T}$$

$$\phi_2 = \frac{-N_p I_p R_3 + N_s I_s (R_1 + R_3)}{R_T}$$
(6)

"Methods" section

Figure

Table

Equation

T₅ transformer performance was validated across a wide range of operating points. The transformer core and conduction losses were analytically verified for an array of input voltages, namely 20 V to 60 V, with power levels between 40 W and 400 W, with results shown in the contour plots in Fig. 16. It is clear that the losses are quite uniform between the 20 V and 60 V operation cases across all power levels.

V. EXPERIMENTAL RESULTS

A. Transformer characterization

The selected EII Sec. transformer designs for the ES8 (T_4) and custom design (T_5) from the previous section, each shown in Fig. 17, were fabricated by a Ferrite core manufacturer and evaluated for their electrical characteristics. Due to the fact that the magnetizing flux path is realized with an un-gapped core, it is first important to characterize the permeability of the core, as the material permeability is only guaranteed within ±20% [31], and additional effects at the core interfaces may attribute to additional permeability reduction. A unique experimental were produced in separate batches. The effective permeability of the E58 core was concluded to be $\mu_r = 950$, while the effective permeability for the custom core was $\mu_r = 1250$.

Using the calibrated permeability, the transformer's electrical characteristics were compared to predictions and 3D FEA simulations. The results of the comparison are highlighted in Table VI. Due to the permeability reduction, the achieved magnetizing inductance is less than the value expected con-

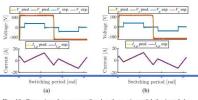
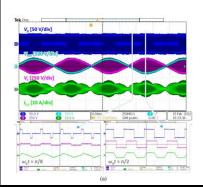


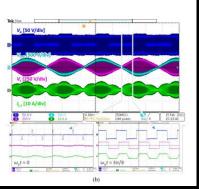
Fig. 18. Comparison between predicted and experimental behavior of the main-circuit at an example DC-DC operating point with, (a) E58-EII Sec. T_4 , and (b) Custom-EII Sec. T_5 . The demonstrated waveforms are indicated

may increase conduction losses due to increased RMS current, however there is no significant penalty to core loss, as the flux density in the ungapped magnetizing flux path is proportional value of permeability was extracted for each core, as they to μ_r (cf. (5)-(7)). Nevertheless, comparison of the transformer experimental parameters to prediction and 3D FEA simulation is accurate with the proper value of permeability, validating the

B. Hardware testing

The EII transformer prototypes were connected to a microinverter circuit with the specifications in Table II to verify sidering the nominal permeability value (cf. Table V). This the effectiveness of the proposed design under nominal power





"Results" section



Fig. 20. Experimental efficiency of the microinverter with the expected loss breakdown between the transformer and devices at each power level.

core loss density in this segment of the core as the cross-section area is the lowest in the magnetizing flux path. In comparison, the T_5 transformer in Fig. 19(d) exhibits significantly reduced core temperatures at 25.2 °C, while the surrounding windings reached ~ 29 °C. The reduced temperatures in both the core and windings exemplify improved loss performance of T.

3) Efficiency analysis: The efficiency of the circuit was analyzed at the 120 W, 200 W, and 300 W average power levels, as they contribute most significantly to the microinverter's CEC efficiency. The results of the efficiency characterization are shown in Fig. 20, where a peak efficiency of 96.5% is achieved at the 200 W power level with the T_5 transformer. Generally, up to 1% efficiency improvement is realized with the T_5 transformer compared to T_4 . In addition to the general efficiency number, the predicted loss contributions from the transformer core, windings, and devices are shown as clustered columns on Fig. 20. It is evident that reduction of core loss is a principal contributor to improved, efficiency with T_5 .

VI. CONCLUSION

This manuscript has presented a novel planar-based integrated transformer concept and optimal design comparison to other similar transformers from literature. The proposed transformer achieves asymmetrically distributed controllable leakage inductance through an independent core leg, where a horizontal air gap is used for reluctance control. Closed-form expressions of the core and winding losses of the proposed design in a DC-AC single-stage microinverter topology are developed and combined with the reluctance modelling in a multi-objective design optimization of the transformer geometry. Extending the design optimization to other integrated transformers from literature revealed benefits in the pro-(specifically regarding controlled AC resistance and low core losses), footprint area, and parasitic capacitance, alongside simple winding layout and manufacturability. The proposed transformer design was then analyzed considering a fixed outer geometry versus a fully custom geometry, where a theoretical 0.4% CEC efficiency improvement (from 1.19% to 0.83%) could be achieved at the cost of increased footprint area. Based

TABLE VII. TRANSFORMER DESIGN PARAMETERS CONSIDERED FOR

Tr	l_{side} [mm]	d_{core} [mm]	w_{wind} [mm]	l_{gap} [mm]	r_{gw} [%]
A	5	38.6	23.1	1.7	7.2
В	10.5	49.9	16.2	2.4	14.4
С	12.5	49.9	8.45	2	22.3

on the design analyses, two optimal transformer prototypes were connected to a DC-AC microinverter circuit, and a peak efficiency of 96.5% was achieved.

APPENDIX

Transformer Designs in P_{cond} Analysis

In developing the analytical framework reacrding the DCto-AC side resistance ratios, three unique transformer designs were considered that realized a wide variation across the design space. These three designs were informed from the custom transformer multi-objective design analysis in Section IV-E. With reference to the Pareto front in Fig. 15, Transformer A is one of the bottom-right corner designs with a PCF of 1%, Transformer B is the finally selected design T₅, and Transformer C is the design in the upper-left corner. Key design specifications related to conduction losses are highlighted in Table VII, where clearly the designs have unique values geometric variables as well as r_m.

ACKNOWLEDGMENT

This material is based upon work supported by the U.S.Department of Energy is Office of Energy Efficiency and Renewable Energy (EERE) under the Solar Energy Technologies Office Award Number DE-EE0008350.

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"Appendix" section

"Acknowledgement" section

"Conclusion" section

"References" section

Title

Quiz 1

What is your take on the following titles?

"A Comparative study of Artificial Neural Networks Using Reinforcement learning and Multidimensional Bayesian Classification Using Parzen Density Estimation for Identification of GC-EIMS Spectra of Partially Methylated Alditol Acetates"

Valafar and Varafar, "A comparative ... Acetates," Jul. 2020.

1 Too vague "Attack vulnerability of complex networks"

Holme et. al, "Attack vulnerability of complex networks," Phys. Rev. E, May 2002.



Title

- Should be specific, concise but descriptive
- Preferably fewer than twelve words
- Avoid qualifying words such as "new", "novel", "faster"
- Avoid using "filler"/redundant words
- Include keywords that will help a reader find your paper

Examples of "bad" and "good" titles

"A better approach of managing environmental and energy sustainability via a study of different methods of electric load forecasting"

- Verbose
- Uses qualifying words like "better"

"A human expert-based approach to electrical peak demand management"

- Concise, informative
- Avoids any qualifying words like "better", "new"
- Avoids redundant words like "study", "different"

Abstract

Quiz 2

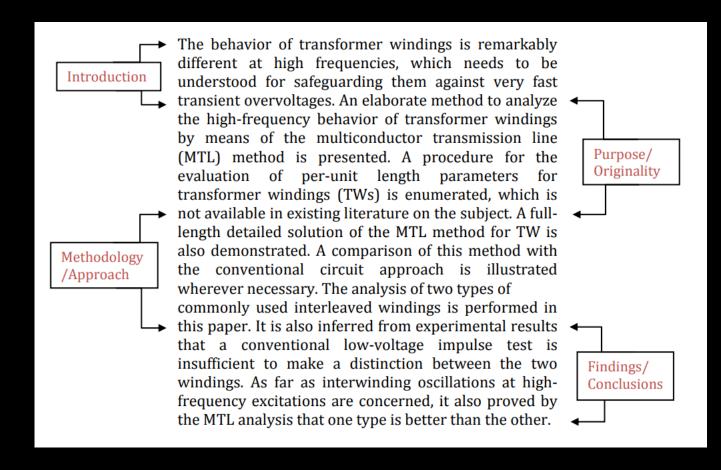
Title, abstract and keywords are considered to be vitally important parts of a technical paper. Why do you think so?

- Title, keywords: used to search a paper online
 - -> decides if your paper will appear in an online search
- Title, abstract: most researchers glance through title and abstract before deciding to read a paper
 -> decides if your paper will be read

Abstract

- Single paragraph up to 250 words
- Follow the structure
 - Background of the problem
 - Specific problem
 - What is your solution
 - Details of the solution
 - Impact of the work
- <u>Should not include</u> acronyms, equations, symbols, references, footnotes
- Use widely-used terms as keywords, not your own made-up acronyms (also don't use too generic terms like "algorithm", "data")

Abstract structure - example



Examples of "bad" and "good" abstracts

"An instrumentation tracker that <u>quickly</u> shows the position of high-speed targets <u>with great precision</u> is described. Range is determined by a FM-CW radar. Azimuth and elevation angles <u>are recorded</u> on magnetic tape or read out to a computer."

- Uses qualifying terms like "quickly", "with great precision"
- Details absent
- Impact of work absent

"This paper describes an instrumentation tracker that provides real-time positional data on high-speed cooperative targets with a precision < 1 m at ranges between 300 m and 10 km. Unambiguous range is determined by a precise digital frequency-modulation-continuous-wave (FM-CW) ranging technique using a target-mounted beacon and a narrow laser ranging beam. This system permits measurement of target position to values much less than target dimension. Azimuth and elevation angles are read out by precision shaft angle encoders and recorded in binary form, along with range and time, on magnetic tape or directly to a real-time computer."

- Shares quantifiable information
- Provides details
- Impact of work highlighted

Introduction

- Typical structure (4-5 paragraphs)
- 1st para product/process, why it is important to analyze + specific research topic
- 2nd and 3rd para review of important literature on the problem + shortcomings
- 4th para methodology adopted in proposed work, contributions (can use bullets or numbered list)
- 5th para outline of the rest of the paper

Introduction - example

DAB Converter for EV On-Board Chargers Using Bare-die SiC MOSFETs and Leakage-Integrated Planar Transformer

Yongwan Park, Student Member, IEEE, Shiladri Chakraborty, Member, IEEE and Alireza Khaligh, Senior Member, IEEE

Abstract-This paper discusses electrical design optimization of a 3.3 kW, 380 V to 250-380 V, 500 kHz, dual-active-bridge dc-dc converter for on-board chargers, operated with constantpower (CP) charging. In order to operate the converter at 500 kHz without concerns on switching performance and efficiency while also improving power-density, a low-parasitics, PCB-based, wire-bondless full-bridge module featuring bare-die SiC MOS-FETs and compact, electro-thermally multi-functional coolers is employed. High switching frequency operation also felicitates realization of the DAB inductor using the transformer's leakage inductance, thereby enhancing power-density by eliminating the need for a discrete inductor. Design strategy for such magnetic integration in a planar transformer is discussed followed by a systematic design optimization of the transformer, including selection of leakage inductance value, core geometry and number of turns for achieving zero-voltage-switching (ZVS) and maximum average efficiency over the entire charging profile. Experimental validation was performed using a proof-of-concept prototype, which is operated up to 3.3 kW and has a final projected power density of 5.44 kW/L. Results demonstrate operation with ZVS over the entire charging profile with satisfactory high-frequency waveforms and a peak efficiency of 98%.

Index Terms-Dual-active-bridge, on-board charger, bare-die SiC MOSFET, planar transformer, power-density.

I. INTRODUCTION

With the continuing global emphasis on transportation elec- peak shaving and reactive power support [2]. trification, the demand for high power-density and high efficiency on-board charger (OBC) systems for electric vehicles dc converters for OBCs, the LLC resonant converter [4] (EV) has been growing significantly [2]. Typical structure of it is a popular choice, which can achieve high power-density a single-phase, two-stage, isolated OBC system is illustrated. I and efficiency due to possible zero-voltage-switching (ZVS) in Fig. 1a. It consists of an ac-dc power factor correction converter stage for drawing high-quality current from the grid, followed by a dc-dc converter stage that regulates the battery voltage as well as provides high-frequency galvanic isolation. The focus of this paper is the dc-dc stage, whose key design requirements are high power-density and high efficiency over CLLC converter [6], which has a symmetric resonant tank, a wide range of battery voltage [3]. An additional desirable one challenge with the CLLC topology is that its efficiency

Manuscript received March 31, 2021; revised July 09, 2021 and September 13, 2021; accepted October 11, 2021. This paper was presented in part at [5] proposed a new bidirectional, series-resonant converter IL, USA, June 2020 [1]. This work was supported by the U.S. Army Research | topology to achieve high efficiency over a wide range of Laboratory as part of the SCAPOPS-II program, under contract number | battery voltage. Another work in [7] proposed a uni-directional W911NF-18-2-0118. (Corresponding author: Shiladri Chakraborty.)

gineering, Maryland Power Electronics Laboratory, Institute for Systems Research, University of Maryland, College Park, MD - 20742, U.S.A (e-mail: vwpark@umd.edu, shiladri007@gmail.com, khaligh@umd.edu.)

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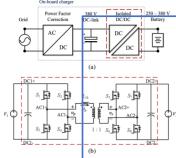


Fig. 1: (a) Block diagram of a two stage, isolated OBC system. (b) Topology of DAB converter, considered for the isolated dc-dc stage in this pape

feature is that the dc-dc converter (as well as the dc-ac stage) should allow bidirectional power flow, since next-generation OBC systems are expected to have vehicle-to-grid (V2G) functionality to enable advanced grid support features like

Among various topologies reported in literature for dcand/or zero-current-switching (ZCS) operation of its switches. However, the resonant tank of the LLC converter is inherently asymmetric, which operates as a series-resonant converter for reverse power flow and as such can only operate in buck mode [5]. While this can be addressed by using the bidirectional can be poor when the switching frequency (f_s) moves far away from the resonant frequency [5]. To overcome this limitation, The authors are with the Department of Electrical and Computer En. | modified hybrid LLC converter, which is operated in different operation modes depending on the load and battery voltage to enhance efficiency. A common shortcoming of all of the aforementioned topologies is that the passive components of the resonant-tank, particularly the resonant capacitors, can add

non-negligible volume, thereby impacting their power-density

[8]. The resonant-transition, phase-shifted full-bridge (PSFB) converter [9] is another possible candidate topology which has the advantages of simple control, low reactive power flow and possible ZVS operation. However, it suffers from problems like duty-cycle loss, limited light-load efficiency and turn-off voltage spikes on the current-fed side devices.

The dual-active-bridge (DAB) converter, shown in Fig. 1b. stage [10] and two-stage [11] OBC systems. This topology has advantages like capacitively-clamped operation of the ation in both directions of power flow. Further, the DAB topology is inherently symmetric and compared to resonanttank topologies, requires lesser passive components, which advantage compared to resonant topologies, which are mostly operated with varying f_s and necessitate wide frequency range, bulkier passive components and EMI filters [12]. The DAB IIID, planar transformer structures with integrated leakage converter also has its own challenges like high circulating power and possible loss of ZVS under light-load and nonunity voltage-gain conditions when operated with square wave modulation, referred to as single-phase-shift (SPS) modulation [13] or adopting auxiliary circuitry such as additional resonant tank [14], inductor and switch pair [15], and the current-fed DAB structure [16]. Notwithstanding the limitations, in view • An electro-thermally integrated, compact, wire-bondless, of the other aforementioned advantages, this work explores the use of the DAB topology for the development of a highperformance dc-dc converter of a two-stage OBC system. The specifications of the converter are listed in Table I and the OBC is assumed to be designed to operate with the constant-power (CP) charging profile. Compared to other charging protocols like constant-current (CC), CP charging results in faster charging and better utilization of the power capacity of the charger [17]. While CP charging also has some concerns with regard to battery capacity fading [18], it is finally considered in this work because of its stated benefits

strategies are pursued, the first of which is operation at a relatively high f_s . Operation at high f_s is a key enabler to enhance power-density by reducing the size of passive components, and for the present design, a value of 500 kHz is chosen. However, an important consideration with operation at high f_s is ensuring ZVS with low conduction losses to ensure good efficiency, which as mentioned earlier, can be challenging for a DAB converter used in charger applications. Unlike the previously-mentioned hardware-based approaches, this is addressed in the present work through combined design and modulation optimization, involving proper selection of values of L_{lk} and the phase-shift parameters. The other two design strategies relate to the key highlights of this work. The rest of the paper is organized as follows. An overall and involve 1) use of a unique full-bridge switch module description of the bare-die SiC-based full-bridge switch modfeaturing bare die SiC MOSFETs and 2) use of a planar ule and planar transformer implementation is presented in transformer with high leakage inductance, which serves as the section II. Section IIIA discusses details of design analysis for

DESIGN SPECIFICATIONS OF THE DC-DC CONVERTER.

Item	Description Item		Description	
Maximum power	3.3 kW	DC-bus voltage (V_1)	380 V	
Switching frequency (f_s)	500 kHz	Battery voltage (V_2)	250 - 380 V	

series inductance of the DAB converter (L_{1k} in Fig. 1b). For has also been investigated as the dc-dc stage of both single- reabling fast and robust switching behavior, several bare-die SiC-based switch module design approaches with integrated gate-drivers and/or decoupling capacitors have been proposed switches, resulting in lower turn-off voltage spikes than PSFB recently [19]-[22], which can be advantageous in terms of the power-density due to their tight composition. However, these approaches either entail fundamental trade-offs between switching and thermal performance [21], [22] or involve wirebonding [19], [20], which prohibits double-sided cooling and may be advantageous in terms of power-density [8]. Moreover, compromises reliability [23]. To mitigate these challenges, the DAB converter is normally operated at fixed f_s , which is an $\mathbf{I}_{\mathbf{I},\mathbf{a}}$ unique bare-die SiC-based full-bridge switch module is used in this work, which results in enhanced switching as well as thermal performance. As discussed later in section inductance reported in literature have limitations like unstable L_{lk} value [24], high values of parasitic capacitances and large footprint area [25], [26]. This work utilizes an integrated planar structure which do not have these limitations and can in this paper. These challenges can be addressed by either be considered a suitable candidate for high-frequency, high using widely-studied phase-shift-based modulation strategies power-density applications. To summarize, the contributions

- bare-die SiC-based switch module featuring extremely low parasitics and double-sided cooling is implemented for high-frequency converter applications, and its performance is validated experimentally under powered condition in a 500 kHz DAB converter, working as the dc-dc stage of a 3.3 kW OBC
- A systematic design procedure for selection of optimal value of L_{lk} and modulation parameters of the DAB converter is presented based on highly accurate analyses of converter operation and ZVS turn-on requirements. As a result, the converter operates with the minimum RMS value of transformer current (I_{rms}) while achieving ZVS during the entire CP charging stage, without requiring any auxiliary circuitry.
- Use of DC-bus voltage modulation in conjunction with converter modulation is proposed to realize ZVS with lowest I, under light-load conditions in the constant-
- A systematic approach towards efficiency-optimal design of a single-layer high-frequency planar transformer with integrated L_{lk} and extremely low parasitic capacitances is proposed by investigating the correlation between the physical design of the transformer and its electrical characteristics.

4th para: Methodology adopted (+ lit. survey continued)

1st para: Background + specific research problem

2nd and 3rd paras: Literature survey + associated shortcomings Writing tip: don't be too critical

> 4th para: Contributions

Introduction - example

non-negligible volume, thereby impacting their power-density [8]. The resonant-transition, phase-shifted full-bridge (PSFB) converter [9] is another possible candidate topology which has the advantages of simple control, low reactive power flow and possible ZVS operation. However, it suffers from problems like duty-cycle loss, limited light-load efficiency and turn-off voltage spikes on the current-fed side devices.

The dual-active-bridge (DAB) converter, shown in Fig. 1b, has also been investigated as the dc-dc stage of both singlestage [10] and two-stage [11] OBC systems. This topology has advantages like capacitively-clamped operation of the switches, resulting in lower turn-off voltage spikes than PSFB topologies and possible zero-voltage-switching (ZVS) operation in both directions of power flow. Further, the DAB topology is inherently symmetric and compared to resonanttank topologies, requires lesser passive components, which may be advantageous in terms of power-density [8]. Moreover, the DAB converter is normally operated at fixed f_s , which is an advantage compared to resonant topologies, which are mostly operated with varying f_s and necessitate wide frequency range, bulkier passive components and EMI filters [12]. The DAB converter also has its own challenges like high circulating power and possible loss of ZVS under light-load and nonunity voltage-gain conditions when operated with square wave modulation, referred to as single-phase-shift (SPS) modulation in this paper. These challenges can be addressed by either using widely-studied phase-shift-based modulation strategies [13] or adopting auxiliary circuitry such as additional resonant tank [14], inductor and switch pair [15], and the current-fed DAB structure [16]. Notwithstanding the limitations, in view of the other aforementioned advantages, this work explores the use of the DAB topology for the development of a highperformance dc-dc converter of a two-stage OBC system. The specifications of the converter are listed in Table I and the OBC is assumed to be designed to operate with the constant-power (CP) charging profile. Compared to other charging protocols like constant-current (CC), CP charging results in faster charging and better utilization of the power capacity of the charger [17]. While CP charging also has some concerns with regard to battery capacity fading [18], it is finally considered in this work because of its stated benefits

In order to meet the above-stated objectives, three design strategies are pursued, the first of which is operation at a relatively high f_s . Operation at high f_s is a key enabler to enhance power-density by reducing the size of passive components, and for the present design, a value of 500 kHz is chosen. However, an important consideration with operation at high f_s is ensuring ZVS with low conduction losses to ensure good efficiency, which as mentioned earlier, can be challenging for a DAB converter used in charger applications. Unlike the previously-mentioned hardware-based approaches. this is addressed in the present work through combined design and modulation optimization, involving proper selection of values of L_{lk} and the phase-shift parameters. The other two design strategies relate to the key highlights of this work | The rest of the paper is organized as follows. An overall and involve 1) use of a unique full-bridge switch module a description of the bare-die SiC-based full-bridge switch modfeaturing bare die SiC MOSFETs and 2) use of a planar transformer with high leakage inductance, which serves as the section II. Section IIIA discusses details of design analysis fo

TABLE I DESIGN SPECIFICATIONS OF THE DC-DC CONVERTER

Item	Description	Item	Description	
Maximum power	3.3 kW	DC-bus voltage (V_1)	380 V	
Switching frequency (f_s)	500 kHz	Battery voltage (V_2)	250 - 380 V	

series inductance of the DAB converter (L_{1k} in Fig. 1b), For enabling fast and robust switching behavior, several bare-die SiC-based switch module design approaches with integrated gate-drivers and/or decoupling capacitors have been proposed recently [19]-[22], which can be advantageous in terms of the power-density due to their tight composition. However, these approaches either entail fundamental trade-offs between switching and thermal performance [21], [22] or involve wirebonding [19], [20], which prohibits double-sided cooling and compromises reliability [23]. To mitigate these challenges, a unique bare-die SiC-based full-bridge switch module is used in this work, which results in enhanced switching as well as thermal performance. As discussed later in section IID, planar transformer structures with integrated leakage inductance reported in literature have limitations like unstable L_{lk} value [24], high values of parasitic capacitances and large footprint area [25], [26]. This work utilizes an integrated planar structure which do not have these limitations and can be considered a suitable candidate for high-frequency, high power-density applications. To summarize, the contributions of this paper are as follows:

- · An electro-thermally integrated, compact, wire-bondless, bare-die SiC-based switch module featuring extremely low parasitics and double-sided cooling is implemented for high-frequency converter applications, and its performance is validated experimentally under powered condition in a 500 kHz DAB converter, working as the dc-dc stage of a 3.3 kW OBC.
- · A systematic design procedure for selection of optimal value of L_{lk} and modulation parameters of the DAB converter is presented based on highly accurate analyses of converter operation and ZVS turn-on requirements. As a result, the converter operates with the minimum RMS value of transformer current (I_{rms}) while achieving ZVS during the entire CP charging stage, without requiring
- Use of DC-bus voltage modulation in conjunction with converter modulation is proposed to realize ZVS with lowest I_{rms} under light-load conditions in the constant-
- · A systematic approach towards efficiency-optimal design of a single-layer high-frequency planar transformer with integrated L_{lk} and extremely low parasitic capacitances is proposed by investigating the correlation between the physical design of the transformer and its electrical

ule and planar transformer implementation is presented in

identifying a range of L_{lk} based on the criterion of minimizing rms, while satisfying the energy-related ZVS criterion of he switches. Final design of the transformer, including an pptimal selection of the value of L_{lk} , choice of core geometry and number of turns for achieving the highest efficiency, is outlined in section IIIB. Transformer design challenges for bperation with CC charging are then highlighted, followed by a discussion on operation under light-load condition. Finally, details of the hardware prototype and experimental results are presented in section IV.

II. OVERALL HARDWARE COMPOSITION

A. Motivation for Use of Bare-die Switches

Selection of bare-die SiC MOSFETs, in contrast to normally used packaged discrete switches, is motivated by two corresponding packaged devices and thus occupy smaller PCB real-estate, which can improve power-density. Secondly,



Fig. 2: (a) Dimensions of the bare-die SiC MOSFET considered in this work. (b) Dimensions of a discrete SiC MOSFET in TO-247 package.

design considerations. Firstly, as illustrated in Fig. 2, bare- decoupling capacitors as well as connections to the transformer die switches occupy significantly smaller footprint area than and gate driver circuitries via PCB traces. For the proof-ofconcept prototype in this work, 200 μ m thick copper sheets are used as the spacers to keep the height of the bus-bars discrete MOSFETs have substantially higher packaging inductance (due to internal bond wires and leads), which limits As an additional design strategy to mitigate possible thermo5th para: Outline of remaining paper

Writing tip: Can combine this para with contributions (State contributions and forward reference them to corresponding sections)

Methods

- A detailed description of the question
- Methods you used to address the question
- Definitions of any relevant terminology
- Any equations that contributed to your work
- Divide contents into suitable sections, sub-sections, sub-sub-sections

- Results (and discussions)
 - Details of simulation/experimental setup (share info to make your work replicable/ your claims verifiable)
 - Results (in form of figs., Tables) of your work and offer interpretation for them
 - Comparison of theoretical/analytical results with simulation/experimental results
 - Benchmarking of your results with previous results in literature
 - Acknowledge any limitations of your work
 - Avoid exaggerating the importance of the results

Results - Benchmarking example

TABLE II

COMPARISON OF THE PROPOSED SWITCH MODULE WITH RECENTLY-PROPOSED BARE-DIE SIC-BASED INTEGRATED MODULES.

Reference	Wire bonds	$L_{loop,power} \ [ext{nH}]$	$L_{loop,gate} \ [ext{nH}]$	Heat removal	Substrate type	Description of Integration	Power loop	Additional C_{oss}
[7]	Yes	2.4 (simulated)	3 (simulated)	Single-sided	AIN DBC	Decoupling cap.	Lateral	Low
[8]	Yes	7.3 (simulated)	N/A	Single-sided	Al ₂ O ₃ DBC	Decoupling cap., gate-driver	Lateral	Low
[10]	Yes	3.38 (simulated)	N/A	Single-sided	FR4 PCB/AIN DBC	Decoupling cap., gate-driver	Lateral	Low
[9]	Yes	3.4 (simulated)	N/A	Single-sided	Al_2O_3 DBC	Decoupling cap., gate-driver	Vertical	Low
[13]	No	4.5 (simulated)*	4.3 (simulated)	Single-sided	AIN DBC	Decoupling cap.	Lateral with planar interconnects	Low
[14]	No	1.6 (experimental)	6 (simulated)	Single-sided	Al ₂ O ₃ DBC	Decoupling cap.	Lateral with planar interconnects	Low
[18]	No	2.09 (simulated)+++	0.012 (simulated)++	⁺ Double-sided	FR4 PCB-embedded	-	Vertical	36%
[19]	No	2 ⁺ (experimental) [*]	N/A	Double-sided	FR4 PCB-embedded	Decoupling cap.	Vertical	20%
[20]	No	0.86*(experimental)*	N/A	Single-sided	FR4 PCB-embedded with Al ₂ O ₃ DBC	Decoupling cap.	Vertical	18%
[27]	No	1.4 ⁺ (experimental) ⁺⁺⁺	20 (simulated)	Single-sided	Flexible board/DBC	-	Vertical	High
[16]	No	4.88*(experimental)	0.25 (simulated) ⁺⁺⁴	Single-sided	FR4 PCB	Decoupling cap.	Vertical	Low
[15]	No	12.33 (simulated)	8.07 (simulated)	Double-sided	FR4 PCB or DBC	Gate-driver	Lateral	Low
[17]	No	1.5 (simulated) ⁺⁺⁺	N/A	Double-sided	Epoxy-resin	Gate-driver	Vertical	Low
[24]	No	5 (experimental)*	N/A	Double-sided	DBC/AMB	-	Vertical	High
[25]	No***	7.5 (simulated) ⁺⁺⁺	N/A	Double-sided	Resin-molded heat-spreader	-	Vertical	High
[26]	No***	1.63*(simulated)+++	N/A	Double-sided	AIN DBC	Decoupling cap.	Vertical	High
[28]	No	8 (simulated) ⁺⁺⁺	4 (simulated)	Double-sided	PCoB	-	Vertical with MFCs	High
[29]	No***	N/A	N/A	Double-sided	PCoB		Vertical with MFCs	Low
This work	No	1.349 (simulated)	5.1 (simulated)	Double-sided	FR4 PCB	Decoupling cap., gate-driver	Vertical with MFCs	5%

^{*} Value including ESL of decoupling capacitors. $^+$ Value for four half-bridge legs. ** Value for two half-bridge legs. ++ Value for eight half-bridge legs. ++ Value not considering placement of corresponding components. (e.g., capacitor for $L_{loop,power}$ and gate-driver IC for $L_{loop,gate}$)

^{***} Wire-bonds still present for connection to gate-drive circuitry.

Some parasitics are estimated from the information presented in each reference.

Conclusions

- Short description of the motivation and scope of the work
- Short description of specific work done
- Summarize your key findings/results (in more detail than in abstract); quote specific information and numbers
- Overall impact of your work
- Shortcomings of work/ suggestions for future areas for research (typically not described in abstract)
- Can also list contributions (if you haven't done so in "introduction")

Example of "Conclusions" section

VI. CONCLUSION

The MTL method is better than the conventional circuit model method for the analysis of TW at very high frequencies. However, no well-formulated and detailed procedures specific to TW are available for the MTL method. This paper has elaborated the method and illustrated calculation of per-unit length parameters. The MTL model of TW can be easily analyzed in SPICE to obtain a time-domain solution. The two solutions—one in the frequency domain and the other in the time domain—can be used to understand the complete behavior of TW to step fronted surges. There can be many applications of this method from design to diagnostics.

This paper further compares the VFTO characteristics of the Nuys and Stearn windings using the MTL method. It has been comprehensively demonstrated through simulations and measurements that the Nuys and Stearn windings respond to standard impulse voltages almost identically. However, the performance of the former is significantly better than that of the latter for VFTOs.

The contribution of the reported work is in three aspects.

1) a detailed algorithm has been presented to analyze TW using the MTL method along with an elaborate explanation of per-unit length parameter calculations; 2) MTL analysis of

the Nuys winding is presented, including the corresponding full-length solution; and 3) the application of the MTL method for comparing responses of different interleaved windings is demonstrated.

Motivation

Summary of specific work done

Impact of work/ future research

Key findings/results

List of contributions

References

- Prefer using conference and journal publications to reports, internet articles, preprints
- Only cite relevant references (follow ethical principles)
- Make sure not to cite work from predatory journals, conference proceedings
- Few important things to keep in mind
 - Reference numbers must match with text
 - References should be listed in the sequence in which they appear in text
 - No reference should be missing from text; similarly remove unused references
 - Strictly follow IEEE reference styles (see "IEEE reference guide" for details)
 - Always cite the main source, not the derivative source



Examples of IEEE reference styles

Conference Proceedings in Print (Paper Presented at a Conference)

The general form for citing conference proceedings is to list the author and title of the paper, followed by the name of the conference *in italics* using standard abbreviations. Write out all the remaining words, but omit most articles and prepositions like "of the" and "on." That is, *Proceedings of the 1996 Robotics and Automation Conference* becomes *Proc. 1996 Robot. Automat. Conf.* If an ordinal number is in the conference name, use the numerical form instead of spelling it out (e.g., "1st" instead of "First"). Include the location if given. For U.S. locations, "USA" must be included after city and state.

Basic Format:

• J. K. Author, "Title of paper," in *Abbreviated Name of Conf.*, (location of conference is optional), (Month and day(s) if provided) year, pp. xxx-xxx.

Examples:

• A. Amador-Perez and R. A. Rodriguez-Solis, "Analysis of a CPW-fed annular slot ring antenna using DOE," in *Proc. IEEE Antennas Propag. Soc. Int. Symp.*, Jul. 2006, pp. 4301–4304.

Periodical With DOI

Basic Format:

• J. K. Author, "Name of paper," *Abbrev. Title of Periodical*, vol. x, no. x, pp. xxx–xxx, Abbrev. month, year, doi: xxx.

Example:

• M. M. Chiampi and L. L. Zilberti, "Induction of electric field in human bodies moving near MRI: An efficient BEM computational procedure," *IEEE Trans. Biomed. Eng.*, vol. 58, no. 10, pp. 2787–2793, Oct. 2011, doi: 10.1109/TBME.2011.2158315.

Source: "IEEE Reference Guide".

Examples of IEEE reference styles

Thesis Online

Examples:

• F. Jensen, "Electromagnetic near-field far-field correlations," Ph.D. dissertation, Dept. Elect. Eng., Tech. Univ. Denmark, Lyngby, Denmark, 1970. [Online]. Available: www.tud.ed/jensen/diss

Report Online

Ensure a year is included and add the URL to the end of the reference.

Basic Format:

• J. K. Author, "Title of report," Company, City, State, Country, Rep. no., (optional: vol./issue), Date. Accessed: Date. [Online]. Available: site/path/file

Examples:

• R. J. Hijmans and J. van Etten, "Raster: Geographic analysis and modeling with raster data," R Package Version 2.0-12, Jan. 12, 2012. [Online]. Available: http://CRAN.R-project.org/package=raster

Book With Chapter Title

Basic Format:

• J. K. Author, "Title of chapter in the book," in *Title of Published Book*, X. Editor, Ed., City of Publisher, State (only U.S.), Country: Abbrev. of Publisher, year, ch. x, sec. x, pp. xxx–xxx.

Examples:

- T. Ogura, "Electronic government and surveillance-oriented society," in *Theorizing Surveillance: The Panopticon and Beyond.* Cullompton, U.K.: Willan, 2006, ch. 13, pp. 270–295.
- L. Li, J. Yang, and C. Li, "Super-resolution restoration and image reconstruction for passive millimeter wave imaging," in *Image Restoration—Recent Advances and Applications*, A. Histace, Ed., Rijeka, Croatia: InTech, 2012, pp. 25–45.

Source: "IEEE Reference Guide".

Appendix

- Material not essential for understanding of the paper, but included for completeness
- Detailed mathematical proofs

Figures/tables

- Should be readable without relying on the accompanying description in the main text
- Symbols used in the figure should be explained in caption/legend
- Give detailed description in caption (should be self-contained; reviewers and readers often glance through the tables/figures at the outset)

Example of descriptive figure caption

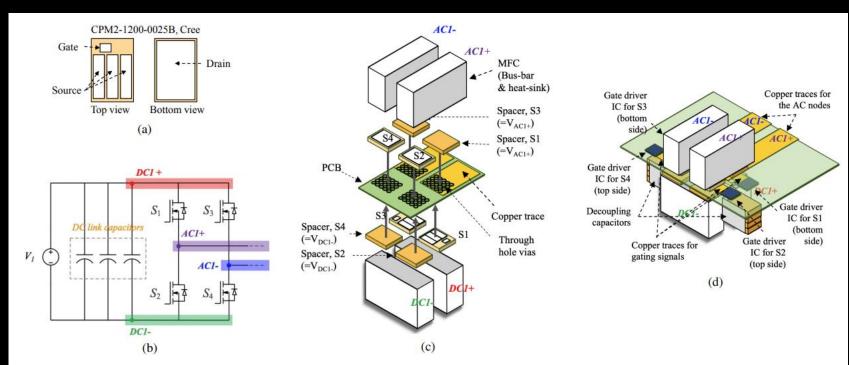


Fig. 3: Illustration of the switch assembly of the converter [30]. (a) Cartoon image of a typical bare-die MOSFET highlighting the gate (G), source (S) and drain (S) pads. (b) Schematic of one full-bridge. (c) Exploded view of the full-bridge assembly. Bare-die switches of each half-bridge are placed in diagonally opposite sides of the PCB with the G and S pads facing the PCB. Connections between the switches of each half-bridge is done using PCB vias, thermo-electrically conducting spacers and multi-functional components (MFCs) which serve as both bus-bars and heat sinks. (d) Assembled view showing location of the dc-link decoupling capacitors and connections via PCB traces to the transformer and gate driver circuitries. The arrangement ensures improved high-frequency electrical performance (due to low loop inductances) and improved thermal improvements (due to quasi double-sided cooling and absence of thermal interface material) in an ultra-compact volume.

- Improves readability
- Compare with a caption like "structure of the module"

How to draft a technical paper/report?

Drafting a technical paper

Before you begin

- Review your notes and update your literature survey
- Check template requirements of the journal/conference
- Initial goal is to get a complete first draft; not a perfect first draft
- Resist the temptation to edit before a first draft is ready

Writing the first draft

- Steps to follows (sequentially)
 - Start from an outline (have bullets and subsections)
 - 2. Take all figures, tables, results and arrange them in a logical order
 - 3. Do not write the "Introduction" section first
 - 4. Write "Methods" first (have placeholders for references, but don't put them yet)
 - 5. Write the "Results and discussion"

Writing the first draft

- Steps to follows (sequentially)
 - 6. Check the draft for proper English, logic flow between sections
 - 7. Write the "conclusions" and contributions (preferably in a numbered format)
 - 8. Write the "introduction"
 - 9. Collect and complete references
 - 10. Write the abstract

Things to do after first draft

- 1. Re-read the draft to identify and delete "filler" or redundant words
 - "it should be pointed out that"
 - "basically", "essentially", "quite", "very"
- 2. Remove jargons
- 3. Give a copy to your peers, ask for specific suggestions (not just typos)
 - was the key idea clear?
 - which section was confusing?

Checklist before final submission

- Perform a spell and grammar check (Latex editors, Word, Grammarly)
- 2. Re-read the draft for consistency of all details, quoted numbers across sections
- 3. Check all references
- 4. Check all figures and table caption numbers with their occurrence in text
- 5. Check for publication-specific document requirement (e.g., IEEE conferences require submitted PDF files to have "embedded fonts")

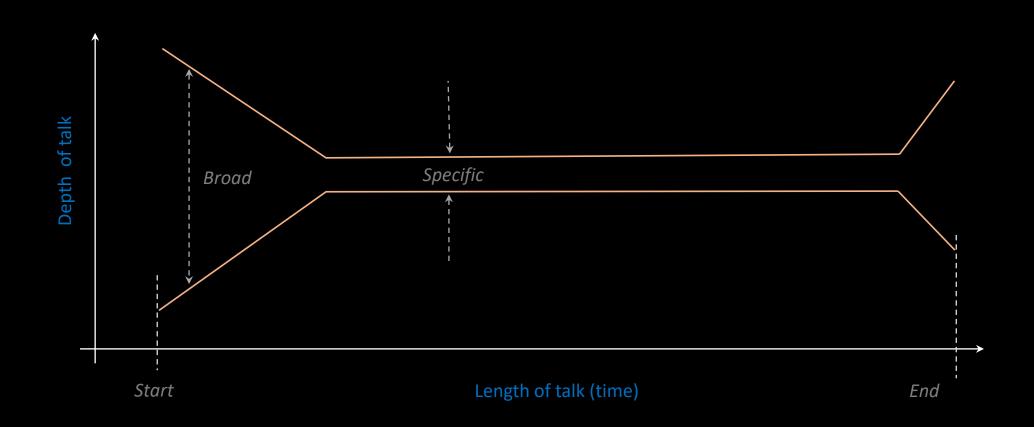
Final thoughts ...

Writing a research document requires you to perform three roles

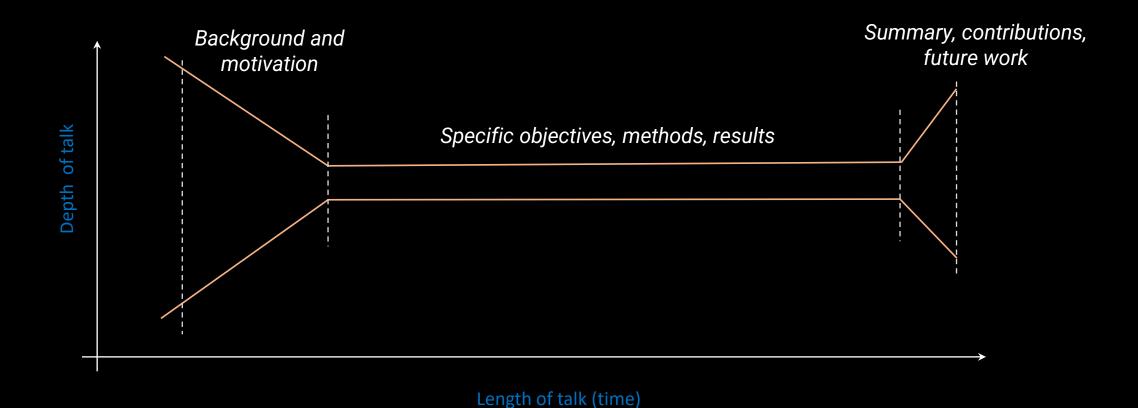
- 1. Write it as a technical person
- 2. Read it as a layman/amateur in the field
- 3. Proof-read it for correct English, formatting

How to give a technical presentation?

How to structure the talk

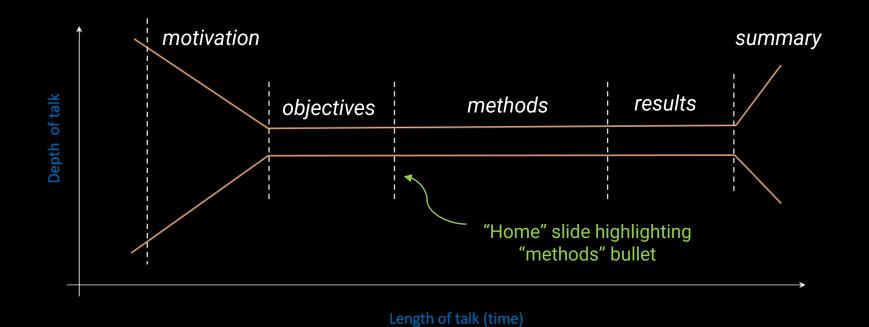


How to structure the talk



How to structure the talk - the "home" slide

- Have an "outline"/"home" slide at the start with bullets listing the main points
- Use this slide at different transition points, highlighting the corresponding bullet
- Gives the audience a clear perspective of how the talk is evolving



Source: "Susan McConnell (Stanford): Designing effective scientific presentation".

- APD-integrated single-stage half-bridge microinverter
- Bare-die SiC-based high power-density, 100 kW traction inverter design
 - Circulating power test of high-power inverters
 - Interleaved leg operation for dc-link capacitor reduction
 - Temperature derating and passive cooling of dc-link capacitors
- Key things to remember

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 - Temperature derating and passive cooling of dc-link capacitors
- Key things to remember

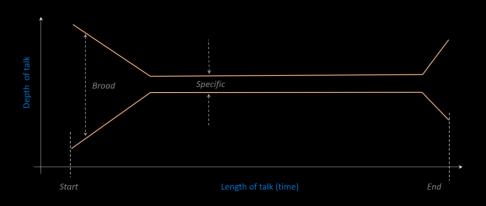
Before you start preparing the slides ...

Identify your audience

- Who are you talking to ? ... pitch the talk at the right level
- Experts in the field (e.g., a conference in the research area)?
- People from different technical backgrounds (e.g., a popular-science or technology topic to people from different departments)?
- The audience decides the "depth" of your talk

Identify the allotted duration

- The duration decides the "length" of your talk
- Never go beyond time!
- Rule of thumb: One slide per minute



General slide preparation tips ...

- Don't make the slide deck a bulleted form of your paper/report/thesis
 - Its goal is to encourage the audience to read your work
 - Don't try to cover all details; focus on the key concepts, results
 - Avoid too much math
 - One/two key message per slide; spell this message out in the title
- Make things visual
 - Try to include some illustration (block-diagram, graphs, tables) in each slide

General slide preparation tips ...

Avoid "busy" slides

- Each slide should have lot of empty space!
- Avoid bullets as much as possible; if you must include bullets max. 3-4 per slide
- Don't include too many images on a slide
- Everything on the slide should be explained! (delete content that you can not cover)

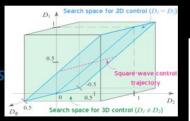
Remember to cite

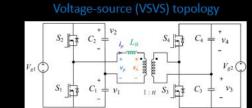
- All rules of plagiarism apply; cite whenever necessary
- Cite at the bottom of each slide; text can be shortened (include a comprehensive reference list at the end of the presentation, following IEEE style)

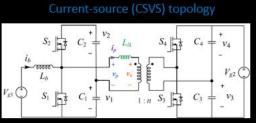
Example of a "busy" slide

Overview of work

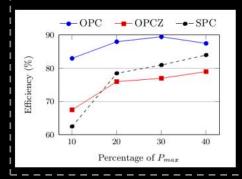
- Title Efficiency Optimization and Topological Innovations of Dual-Active-Bridge-Based Converters (two related parts – part I and II)
- Goal of work- Duty-ratio-based efficiency optimization of both voltagesource & current-source Dual-Active-Half-Bridge (DAHB) converters
- Highlights of work
 - Goal minimize RMS currents and increase ZVS range compared to square-wave operation (SPC)
 - Two control strategies investigated 2D (D₁ =D₂) with and without ZVS & 3D (D₁ ≠ D₂); 3D leads to natural ZVS
 - Look-up table-less, closed-loop implementation strategies proposed for each scheme

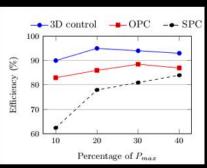


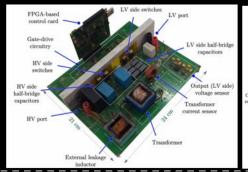


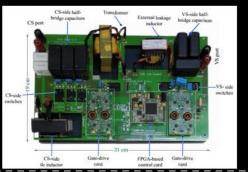












Avoid this

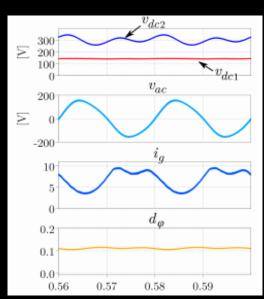
Example of communicating slide's message

Power decoupling control

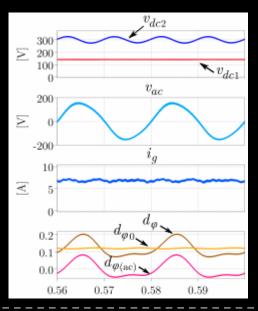
- Fixed phase-shift leads to power fluctuation on dc-side as ac-side voltage is continuously modulated
- To compensate for the ac-side fluctuations, phase-shift is varied over a line cycle
- Implemented using closed-loop control

DC bus average voltage controller (PI) $V_{dcp(ref)} \xrightarrow{+} V_{dcp}$ $i_g \xrightarrow{+} V_{dcp}$ $i_g \xrightarrow{+} V_{dcp}$ Power decoupling controller (PR)

Without power decoupling



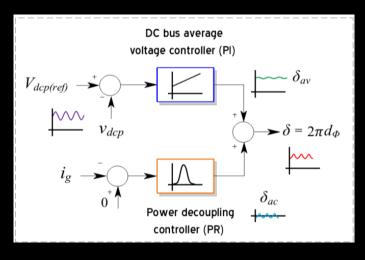
With power decoupling



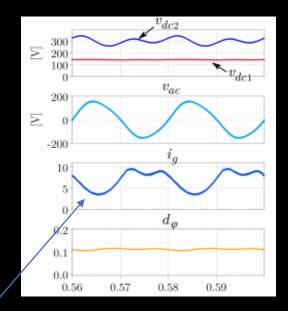
Example – a better way

Power decoupling control eliminates fluctuations in grid current (i_g)

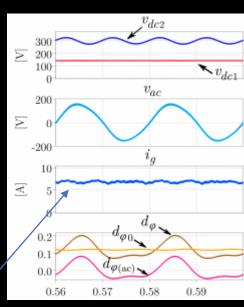
Closed-loop architecture of power decoupling



Without power decoupling



With power decoupling



Grid current fluctuates

Grid current constant

Style and formatting

Fonts

- Type Select a Sans Serif font, not a Serif one e.g., Calibri and not Times New Roman
- Consistency Don't mix up font types, style
 e.g., Slide titles Using "Style and formatting" in one slide and "Structure of

e.g., Slide titles – Using "Style <u>a</u>nd <u>f</u>ormatting" in one slide and "Structure of <u>T</u>he Talk" in another is not good practice

- Size Should not be less than 18
 - References should be in smaller font (14 or less)
- Bullets and sub-bullets Use varying font size, colors, indentations, spacing e.g.,
 - Main bullet point
 - sub-bullet 1
 - sub-sub bullet 1

Style and formatting

- Animations
 - Avoid "flashy" animations
 - Use animations for



Style and formatting

Animations

- Avoid "flashy" animations
- Use animations for
 - Gradual introduction of bullet list items
 - Annotations, highlights to emphasize part of figures, tables
 - Consider using powerful animations like "Morph"

Time management in technical presentations

Tips

- Rehearse your talk to get the timing right
- Have mental checkpoints (slide numbers) of where you should be at a given time
- Some audience interruptions may require long responses; evade them
 - "I will address this in Q&A"
 - "I will explain this more clearly in a latter slide" (if you have one)
 - "Let us discuss this in detail offline"

Time management in technical presentations

- What to do when running short of time?
 - Have a few "primary" slides which can serve to quickly summarize the work
 - Main objectives and methodology in a single-slide (consider using block diagrams)
 - Key results in 2-3 slides, a summary slide (with contributions, take-home messages)
 - Skip to "Results" and "Summary" and complete the talk highlighting the main points

Paper writing - Key things to remember

- 1. Writing is not merely the output of research, but part of the machinery of research!
- 2. Choose a title which is concise but descriptive
- 3. Use suitable keywords in title/abstract so that your paper appears frequently in searches
- 4. Abstract is vitally important because it may decide if your paper is read or not!
- 5. A good abstract i) shares quantifiable information, ii) provides details and iii) highlights impact of the work
- 6. Have detailed captions for figures and tables to improve their readability
- 7. Drafting a good technical manuscript takes multiple iterations
- 8. Suggested writing sequence Outline -> Figures/Tables -> "Methods" -> "Results" -> "Conclusions" -> "Introduction" -> "Abstract"

Presentations – Key things to remember

- 1. Know your audience
- 2. Know the allotted duration
- 3. Use an "outline"/"home" slide to anchor the talk and transition to different talking points
- 4. Avoid "busy" slides
- 5. Try to include an illustration on each slide
- Rehearse the talk to ensure you time it well
- 7. Have a few "primary" slides (focusing on the key take-home messages), which you can use to quickly complete the talk if running short of time

Acknowledgements

Prof. S. H. Kulkarni for various valuable input and suggestions

References/ Suggested supplementary content

YouTube Videos

- "How to Publish a Technical Paper with IEEE", IEEE Explore.
 Available Online. https://www.youtube.com/watch?v=HpkvVuetPA8
- "How to Write a Paper in a Weekend", Prof. Pete Carr. Available Online. https://www.youtube.com/watch?v=UY7sVKJPTMA
- "How to Write a Great Research Paper," Microsoft Research. Available Online. https://www.youtube.com/watch?v=VK51E3gHENc&t=5s
- "How to write a peer reviewed research paper | Full road map".
 Available Online. https://www.youtube.com/watch?v=Xk4CzX2UjS0
- "Workshop on Improving Scientific Writing," Kristin Sainani.
 Available Online. https://www.youtube.com/watch?v=Ah_lv2LW7g&t=5354s
- "How to Give a Great Research Talk," Microsoft Research. Available Online. https://www.youtube.com/watch?v=sT_-owjKlbA
- "How to make Technical presentation," NPTEL, IIT Madras. Available Online. https://www.youtube.com/watch?v=lQrj_7xkeNl&t=886s
- "Designing effective scientific presentations," Susan McConnell (Stanford).
 Available Online. https://www.youtube.com/watch?v=Hp7ld3Yb9XQ&t=1s

Other References

- "Structure Your Paper," IEEE Author Center.
 Available Online. https://conferences.ieeeauthorcenter.ieee.org/write-your-paper/structure-your-paper
- "Skillful writing of an awful research paper," Royce Murray, Analytical Chemistry, 2011 83 (3), 633-633.
- V. O. K. Li, "Hints on writing technical papers and making presentations," in IEEE Trans. on Education, vol. 42, no. 2, pp. 134-137, May 1999.
- D. R. Morgan, "Dos and don'ts of technical writing," in IEEE Potentials, vol. 24, no. 3, pp. 22-25, Aug.-Sept. 2005.

Highly recommended reading ...

"Skillful writing of an awful research paper," Royce Murray, Analytical Chemistry, 2011 83 (3), 633-633.

(Sarcastically) lists "seven rules" to ensure you manuscript is poorly written

Rule 1: "Never explain the objectives of the paper in a single sentence or paragraph and in particular never at the beginning of the paper."

Rule 2: "Similarly, never describe the experiment(s) in a single sentence or paragraph and never at the beginning. Instead, to enhance the reader's pleasure of discovery, treat your experiment as a mystery, in which you divulge one essential detail on this page and a hint of one on the next and complete the last details only after a few results have been presented. It's also fun to divulge the reason that the experiment should successfully provide the information sought only at the very end of the paper, as any good mystery writer would do."

Rule 3: "Diagrams are worth a thousand words, so in the interest of writing a concise paper, omit all words that explain the diagram, including labels. Let the reader use his/her fertile imagination.."

Highly recommended reading ...

"Skillful writing of an awful research paper," Royce Murray, Analytical Chemistry, 2011 83 (3), 633-633.

(Sarcastically) lists "seven rules" to ensure you manuscript is poorly written

Rule 4: "Great writers invent abbreviations for complex topics, which also saves a lot of words. Really short abbreviations should be used for very complex topics, and more complicated ones for simple ideas.

Rule 5: "In referring to the previous literature, be careful to cite only the papers that make claims that would support your own, especially those that contain little evidence for the claim, so that your paper shines in comparison."

Rule 6: "It should be anothema to use any original phrasing or humor in your language, so as to adhere to the principle that scientific writing must be stiff and formal and without personality."

Rule 7: "Your readers are intelligent folks, so don't bother to explain your reasoning in the interpretation of the results. Especially don't bother to point out their impact on or consistency with other authors' results and interpretation, so that your paper can be an island of original thinking."