

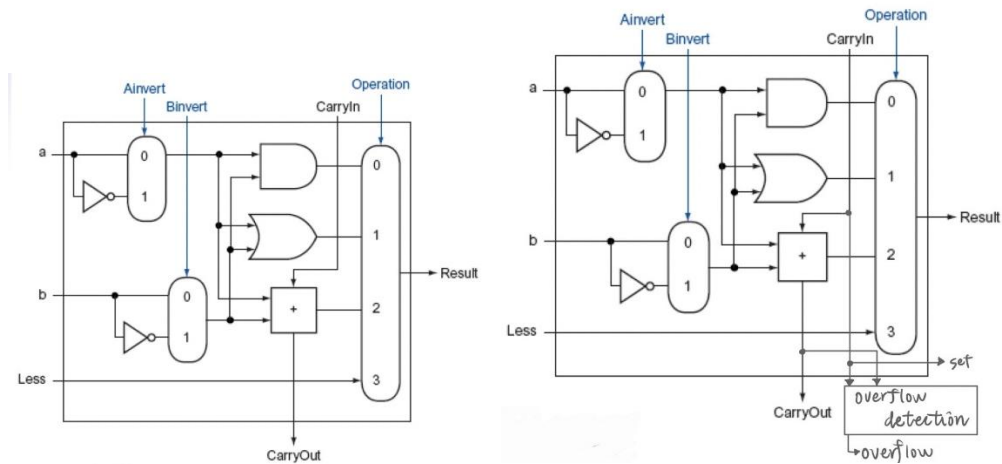
# Computer Organization

109550134 梁詠晴

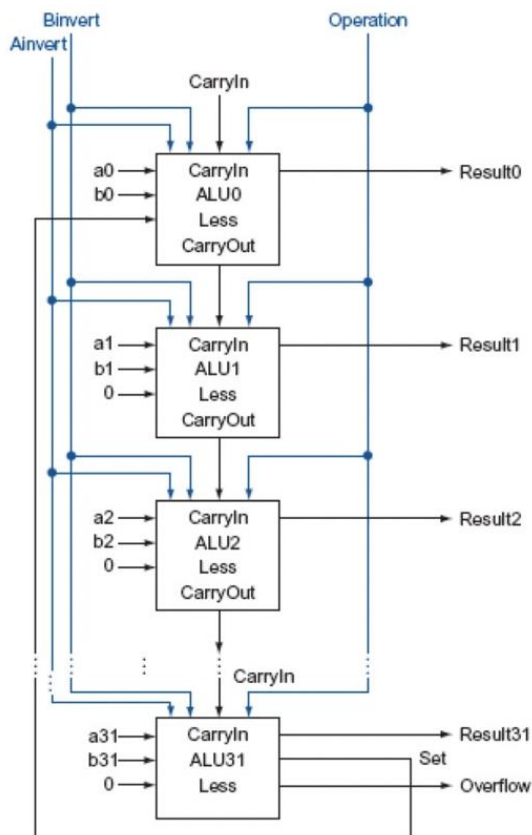
Architecture diagrams:

ALU\_top

ALU\_btm



32 bit ALU



## Hardware module analysis:

### ALU\_top :

1. A、B invert : 分別判斷 src1 和 src2 的值需不需要 inverse ->得 a,b
2. 用 src 判斷完 inverse 的 a,b 根據 operation 判斷 result :
  - ✧ 00 : result <= (a==1 && b==1)
  - ✧ 01 : result <= (a==1 || b==1)
  - ✧ 10 : result <= FullAdder 以(a,b,cin)輸入計算的結果
  - ✧ 11 : result <= less
3. Carry out : 使用 full adder 時的 carry out

### ALU\_btm :

在 ALU\_top 上外加 overflow detector、set :

1. Overflow <= (carry in != carry out)
2. Set <= full adder 運算結果

### ALU

結合 31 個 ALU\_top, 1 個 ALU\_btm

ALU Action	Name	ALU Control Input
And	And	0000
OR	Or	0001
Add	Addition	0010
Sub	Subtraction	0110
Nor	Nor	1100
Slt	Set less than	0111

ALU control input :

[3] = A\_invert

[2] = B\_invert

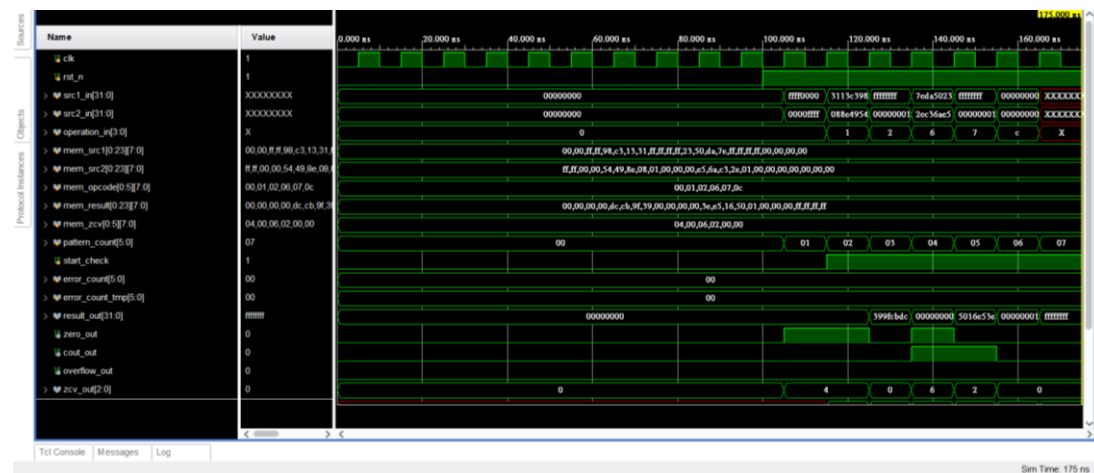
[1:0] = operation

Zero <= (result == 32'b0)? 1: 0;

Cout <= add 或 sub 時 alu\_btm 的 cout

Overflow <= add 或 sub 時 alu\_btm 的 overflow

## Experiment result:



```
Tcl Console x Messages Log

# }
# run 1000ns
*****
Congratulation! All data are correct!
*****
$stop called at time : 175 ns : File "D:/colab_2022/CO_LAB1/lab_1/lab_1.srsc/sources_1/imports/CO_LAB1/testbench.v" Line 104
INFO: [USF-XSim-96] XSim completed. Design snapshot 'testbench_behav' loaded.
```

## Problems you met and solutions:

Vivado 無法加入並開啟檔案·後來搜尋到可以透過將設定 text editor 中的 syntax

checking 設定為 vivado 就可以順利處理檔案

## Summary:

覺得對 module 連接的應用更理解了