

Sareena Manzil, S-Valavu, Pezhakkappilly P. O., Muyattupuzha, Kerala - 686673

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"Truth for us is simply a collective name for verification processes." - William James

Education

Indian Institute of Technology, Madras (NIRF-Rank 1)

Chennai, Tamilnadu

PHD IN COMPUTER SCIENCE AND ENGINEERING

August. 2020 - Present

- We have developed a proof oriented approach to generate a verified and efficient Garbage Collector (GC) for OCaml from scratch which is designed to evolve over time with additional GC feature enhancements. Our approach neatly separates abstract GC correctness from OCaml-specific GC correctness, offering greater flexibility in integrating further GC optimizations while preserving core abstract correctness properties of the GC. As an initial step to demonstrate the viability of our approach, we have developed a verified stop-the-world mark-and-sweep GC tailored for OCaml programs, which is then integrated with OCaml's bytecode interpreter. Our GC is evaluated against the standard OCaml GC and Boehm's GC, and the experimental results are promising. Fully mechanized, our GC is implemented in F* and its low-level subset Low*. The KaRaMel compiler that is associated with Low*, facilitates the extraction of GC coded in Low* to C, which is then integrated with the OCaml runtime
- · Developed a verified graph interface and a verified depth first search (strong reachability property) in F*, that can be used as a library to verify graph search based programs written in F*. Once verified for functional correctness in F*, such programs can be implemented in Low* to verify their concrete memory properties and hence to ensure that no memory bugs are introduced by the implementation. The memory safe and functionally verified Low* code can then be extracted to C code with the help of KaRaMel compiler.
- Work submitted at ICFP. 2024
- · Work submitted at CPP, 2024
- Work submitted at OOPSLA, 2023
- · Course work completed in Automated Program Verification, Analysis of Parallel Programs, Linear Algebra and Advanced Algorithms and Data Structures
- CGPA: **8.5/10.0**

National Institute of Technology, Calicut, Kerala

Kerala

M.Tech in Computer Science and Engineering

July. 2009 - July 2011

- CGPA: 9.02/10.0
- 10.0/10.0 for Final year Project conducted as part of Internship at Intel Technology India Pvt Ltd, Bangalore
- Published a paper titled "Parellelized Disparity Map Generation for Rendering Intermediate Views", which has applications in 3D TV image rendering, at Design and Test Technology Conference (DTTC, 2011) at Intel Corporation, Oregon, USA.

LBS College of Engineering, Kasaragod, Kerala

Kerala

B.Tech in Computer Science and Engineering

Dec. 2000 - June 2004

• Secured 62.5%

Nirmala College, Muvattupuzha, Kerala

Kerala

PRE-DEGREE IN MATHS GROUP

June. 1997 - June 1999

- Secured 83.3%
- Secured 100/100 marks in mathematics

Skills

Formal Verification F*/Low*, Coq, Dafny, Z3

Programming OCaml, Haskell, C/C++, JAVA, Python

Tool Expertise JavaCC/JTB, Latex

Languages Known English, Hindi, Malayalam, Tamil

SHEERA SHAMSU · RÉSUMÉ MAY 25, 2024

Experience

Indian Institute of Technology, Madras

Chennai, Tamilnadu

TEACHING ASSISTANT

January. 2021 - May 2023

- CS5030: Automated Program Verification (2023), responsible for test case development and evaluation of tool assignments (Z3 and Dafny)
- CS3300: Compiler Design (2022), responsible for test case development and evaluation of tool assignments (JavaCC/JTB), evaluation of answer scripts. Sessions taken on JavaCC/JTB tool usage and the requirements for designing a typechecker.
- CS5030: Automated Program Verification (2022), responsible for test case development and evaluation of tool assignments (Z3 and Dafny)
- CS3300: Compiler Design (2021), responsible for test case development and evaluation of tool assignments (JavaCC/JTB). Sessions taken on JavaC/JTB tool usage and the requirements for designing a typechecker.
- CS6225: Programs and Proofs (2020), evaluation of tool assignments (Coq, F*).

TKM College of Engineering, Government Aided Engineering College

Kollam, Kerala

ASSISTANT PROFESSOR

Aug. 2016 - Present (currently enrolled in

PhD program at IIT, Madras)

- Faculty Advisor for Master of Computer Applications batch 2018, 2019, 2020
- Department Time-Table co-ordinator
- · Taught subjects like Functional Programming, C programming, Cryptography and Computer Networks
- Actively participated in guiding and arranging placements and internships.
- Syllabus preparation of various subjects in Kerala Technological University.
- Question paper scheme preparation and valuation lead for functional programming course
- Participated in several committee to help the institution in achieving NAAC and NBA accreditations.

Intel Technologies India Pvt Ltd

Bangalore, Karnataka

SOFTWARE ENGINEER

July. 2011 - June. 2016

- Owned and mentored Post-Silicon functional validation team of Power Conservation Component of Intel's Graphics Driver, developed automated and manual test cases, debugging and bug fixes. Root caused hardware bugs through fine-tuned tests.
- Owned and feature enhanced GUI based Power Spy tool (External and Internal) for the functional validation of the Power Conservation component of Intel's Broadwell Graphics Driver. The tool is used across multiple verticals to gather details and working of the Power conservation component.
- · Developed and planned Pre-Silicon validation test suites which helped to find graphics driver bugs at an early stage.
- Owned Post-Silicon functional validation of Video Post Processing (VPP) Component of Intel's Graphics Driver for the first low power platform of Intel. Bug fixes and development of test cases, both manual as well as automated.
- Owned Post-Silicon functional validation of 3D Component of Intel's Graphics Driver for the first low power platform of Intel, developed test cases for 3D Validation.

Intel Technologies India Pvt Ltd

Bangalore, Karnataka

RESEARCH INTERN

- July. 2010 May. 2011
- Worked closely with GPU micro architecture group responsible for power and performance modeling, architecture analysis, architecture lab, on die interconnect studies, workload characterization, video compression algorithms and firmware development.
- Research on developing computationally less expensive disparity maps for intermediate view generation, from stereoscopic image pairs. Based on the research, a paper titled "Parellelized Disparity Map Generation for Rendering Intermediate Views" is published at Design and Test Technology Conference (DTTC, 2011) at Intel Corporation, Oregon, USA
- Implemented several image processing algorithms in OPENCL and OPENCV for the characterization of GPU workloads.

Ilahia College of Engineering

Muvattupuzha, Kerala

ASSISTANT PROFESSOR

March. 2006 - April. 2009

- Taught subjects like Data Base Management Systems, Theory of Computation, Computer Networks Operating Systems, Artificial Intelligence, Data Structures & Algorithms. (Theory + Lab), C/C++/Java.
- Produced a 100% student pass percentage in the Course Artificial Intelligence.
- Organized and Participated in various student and faculty development activities.

Achievements

DOMESTIC

2016	Cleared common admission test in Computer Science, Chennai Mathematical Institute	India
2015	UGC NET Eligibility, Assistant Professor	India
2009	GATE with 98.67 percentile and an all India rank of 550, Computer Science and Engineering	India
1995	Scholarships, High School level. Kerala Government	India

May 25, 2024 Sheera Shamsu · Résumé 2

Workshops and Posters

Research Highlights in Programming Languages (RHPL) workshop

PRESENTER

• Presented part of my PhD work titled "Towards a Verified Garbage Collector for OCaml"

SAT + SMT Workshop

ATTENDEE

• Attended workshops conducted by eminent faculty and industry persons in formal verification

Department Poster Presentation, Computer Science and Engineering

PRESENTE

• Presented a poster titled, "A verified Depth First Search in F*", which is part of my PhD research work.

IIIT, Hyderabad, India

December. 2023

IIT Madras, India

Dec. 2022

IIT Madras, India

September. 2022