Sheera **Shamsu**

PhD Student, IIT Madras · Expertise in Mechanized Formal Verification

Sareena Manzil, S-Valavu, Pezhakkappilly P. O., Muvattupuzha, Kerala - 686673

8147521107 | sheera.shms@gmail.com | https://in.linkedin.com/in/sheera-shamsu-70377522

"Truth for us is simply a collective name for verification processes." - William James

Education

Indian Institute of Technology, Madras (NIRF- Rank 1)

Chennai, Tamilnadu

PhD in Computer Science and Engineering — *August. 2020 - Present*

- Developed and verified **(safety property that is essential for memory safety)** a **mark and sweep Garbage Collector** in **C** that is compatible with **OCaml objects** and **OCaml heap layout** using **F*/Low***, a proof-oriented programming language that discharges verification conditions using **Z3**, an SMT solver.
- Developed a verified graph interface and a **verified depth first search (strong reachability property)** in F*.
- Work submitted at OOPSLA, 2023
- Work submitted at CPP, 2024
- Course work completed in Automated Program Verification, Analysis of Parallel Programs, Linear Algebra and Advanced Algorithms and Data Structures
- CGPA: **8.5/10.0**

National Institute of Technology, Calicut, Kerala

Kerala

M.Tech in Computer Science and Engineering — *July. 2009 - July 2011*

- CGPA: **9.02/10.0**
- **10.0/10.0** for Final year Project conducted as part of Internship at Intel Technology India Pvt Ltd, Bangalore
- Published a paper titled "Parellelized Disparity Map Generation for Rendering Intermediate Views", which has applications in 3D TV image rendering, at Design and Test Technology Conference (DTTC, 2011) at Intel Corporation, Oregon, USA.

LBS College of Engineering, Kasaragod, Kerala

Kerala

B.Tech in Computer Science and Engineering — *Dec. 2000 - June 2004*

- Secured 62.5%

Nirmala College, Muvattupuzha, Kerala

Kerala

Pre-Degree in Maths group — *June. 1997 - June 1999*

- Secured 83.3%
- Secured **100/100** marks in mathematics

Skills

Formal Verification	F*/Low*, Coq, Dafny, Z3
Programming	OCaml, Haskell, C/C++, JAVA, Python
Tool Expertise	JavaCC/JTB, Latex
Languages Known	English, Hindi, Malayalam, Tamil

Experience

Indian Institute of Technology, Madras

Chennai, Tamilnadu

Teaching Assistant — *January. 2021 - May 2023*

- CS5030: Automated Program Verification (2023), responsible for test case development and evaluation of tool assignments (Z3 and Dafny)
- CS3300: Compiler Design (2022), responsible for test case development and evaluation of tool assignments (JavaCC/JTB), evaluation of answer scripts. Sessions taken on JavaCC/JTB tool usage and the requirements for designing a typechecker.
- CS5030: Automated Program Verification (2022), responsible for test case development and evaluation of tool assignments (Z3 and Dafny)
- CS3300: Compiler Design (2021), responsible for test case development and evaluation of tool assignments (JavaCC/JTB). Sessions taken on JavaC/JTB tool usage and the requirements for designing a typechecker.
- CS6225: Programs and Proofs (2020), evaluation of tool assignments (Coq, F*).

TKM College of Engineering, Government Aided Engineering College

Kollam, Kerala

Assistant Professor

Aug. 2016 - Present (currently enrolled in PhD program at IIT, Madras)

- Faculty Advisor for Master of Computer Applications batch 2018, 2019, 2020
- Department Time-Table co-ordinator
- Taught subjects like Functional Programming, C programming, Cryptography and Computer Networks
- Actively participated in guiding and arranging placements and internships.
- Syllabus preparation of various subjects in Kerala Technological University.
- Question paper scheme preparation and valuation lead for functional programming course
- Participated in several committee to help the institution in achieving NAAC and NBA accreditations.

Intel Technologies India Pvt Ltd

Bangalore, Karnataka

Software Engineer

July. 2011 - June. 2016

- Owned and mentored Post-Silicon functional validation team of Power Conservation Component of Intel's Graphics Driver, developed automated and manual test cases, debugging and bug fixes. Root caused hardware bugs through fine-tuned tests.
- Owned and feature enhanced GUI based Power Spy tool (External and Internal) for the functional validation of the Power Conservation component of Intel's Broadwell Graphics Driver. The tool is used across multiple verticals to gather details and working of the Power conservation component.
- Developed and planned Pre-Silicon validation test suites which helped to find graphics driver bugs at an early stage.
- Owned Post-Silicon functional validation of Video Post Processing (VPP) Component of Intel's Graphics Driver for the first low power platform of Intel. Bug fixes and development of test cases, both manual as well as automated.
- Owned Post-Silicon functional validation of 3D Component of Intel's Graphics Driver for the first low power platform of Intel, developed test cases for 3D Validation.

Intel Technologies India Pvt Ltd

Bangalore, Karnataka

Research Intern

July. 2010 - May. 2011

- Worked closely with GPU micro architecture group responsible for power and performance modeling, architecture analysis, architecture lab, on die interconnect studies, workload characterization, video compression algorithms and firmware development.
- Research on developing computationally less expensive disparity maps for intermediate view generation, from stereoscopic image pairs. Based on the research, a paper titled "Parellelized Disparity Map Generation for Rendering Intermediate Views" is published at Design and Test Technology Conference (DTTC, 2011) at Intel Corporation, Oregon, USA
- Implemented several image processing algorithms in OPENCL and OPENCV for the characterization of GPU workloads.

Ilahia College of Engineering

Muvattupuzha, Kerala

Assistant Professor

March. 2006 - April. 2009

- Taught subjects like Data Base Management Systems, Theory of Computation, Computer Networks Operating Systems, Artificial Intelligence, Data Structures & Algorithms. (Theory + Lab), C/C++/Java.
- Produced a 100% student pass percentage in the Course Artificial Intelligence.
- Organized and Participated in various student and faculty development activities.

Achievements

Domestic

2016	**Cleared common admission test in Computer Science**, Chennai Mathematical Institute	*India*
2015	**UGC NET Eligibility**, Assistant Professor	*India*
2009	**GATE with 98.67 percentile and an all India rank of 550**, Computer Science and Engineering	*India*
1995	**Scholarships, High School level**, Kerala Government	*India*

Workshops and Posters

Research Highlights in Programming Languages (RHPL) workshop

IIIT, Hyderabad, India

Presenter

December. 2023

- Presented part of my PhD work titled "Towards a Verified Garbage Collector for OCaml"

SAT + SMT Workshop

IIT Madras, India

Attendee

Dec. 2022

- Attended workshops conducted by eminent faculty and industry persons in formal verification

Department Poster Presentation, Computer Science and Engineering

IIT Madras, India

Presenter

September. 2022

- Presented a poster titled, "A verified Depth First Search in F*", which is part of my PhD research work.