

# **Digital Calculator**

BY

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under the guidance of

**Prof. Varun Saxena, School of Engineering JNU, Delhi**

in the partial fulfillment of the requirements  
for the award of the degree of

**Bachelor of Technology**  
(a part of Five-Year Dual Degree Course)



**School of Engineering**

**Jawaharlal Nehru University, Delhi**

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# JAWAHARLAL NEHRU UNIVERSITY

## SCHOOL OF ENGINEERING

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### CERTIFICATE

This is to certify that the synopsis entitled “**Digital Calculator**” being submitted by **Mr. Sheersho Banerjee** (Enrolment No.- 20/11/EE/026), **Mr. Sagar Tripathi** (Enrolment No. 20/11/EE/023), **Mr. Estari Saikiran** (Enrolment No. 20/11/EE/016), and **Mr. Raj Sonkar** (Enrolment No. 20/11/EE/048) in fulfillment of the requirements for the award of the **Bachelor of Technology** (part of Five-Year Dual Degree Course) in **Electronics & Communication Engineering**, will be carried out by him under my supervision.

In my opinion, this work fulfills all the requirements of an Engineering Degree in the respective stream as per the regulations of the School of Engineering, Jawaharlal Nehru University, Delhi. This thesis does not contain any work, which has been previously submitted for the award of any other degree.

**Dr. Varun Saxena**

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# Synopsis

## Title: Digital Calculator

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**Problem Statement:** Binary calculation is the fundamental operation of digital computers. It is used in a wide variety of applications, such as arithmetic processors, communication systems, and cryptography. However, binary addition can be complex and time-consuming to implement, especially for large numbers.

**Objective of Project:** To design and implement a digital calculator using the concept of finite state machines. We will perform addition, subtraction, and multiplication with the calculator

**Background:** Binary addition is the addition of two binary numbers. It is performed by adding the corresponding bits of each number, starting from the least significant bit (LSB) and working towards the most significant bit (MSB). If the sum of two bits is greater than or equal to 2, a carry is generated and added to the next bit.

In subtraction using 1's complement, it is done by taking the 1's complement of the subtrahend and adding it to the minuend. If there is a carry out from the most significant bit, then it is added to the least significant bit.

In multiplication, Multiply each digit of the multiplier by each digit of the multiplicand, starting from the LSB. Write the product of each multiplication below the multiplicand, aligned with the corresponding digit of the multiplier. Shift each product down by one place, depending on the position of the digit in the multiplier. Add the products together, ignoring any leading zeros. This is called 'Shift and Add Multiplier'.

**Outcome:** The outcome of this project will be a binary addition/subtraction/multiplication device implemented using a finite state machine. The device will be able to operate on two binary numbers of a fixed length and produce the correct result.

**Proposed Methodology:** Design the finite state machine: The first step is to design the finite state machine for the binary calculation device. This involves identifying the different states of the device and the rules for transitioning between states.

Implement the finite state machine: Once the finite state machine has been designed, it can be implemented using a variety of hardware and software platforms.

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