Implementation of a 10-Bit Delta Sigma Analog to Digital Converter

A Project Report

submitted by

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under the guidance of

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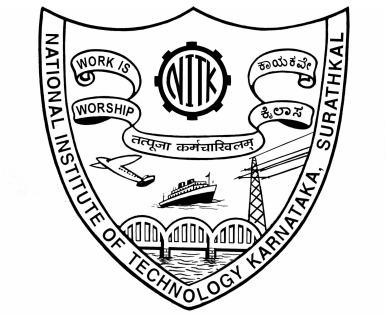
in partial fulfilment of the requirements

for the award of the degree of

BACHELOR OF TECHNOLOGY



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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SURATHKAL, MANGALORE - 575025

April 17th, 2018

DECLARATION

by the B.Tech students

We hereby ***declare*** that the Project entitled **Implementation of a 10-Bit Delta Sigma Analog to Digital Converter** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirements for the award of the Degree of ***Bachelor of Technology*** is a ***bonafide report of the research work carried out by us***. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.

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Date: April 17th, 2018

CERTIFICATE

This is to *certify* that the Under Graduation Project work report titled **Implementation of a 10-bit Delta Sigma Analog to Digital Converter** submitted by

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as a record of the work carried out by them is accepted as a *U. G Project Work Report* submitted in partial fulfillment for the award of the degree **Bachelor of Technology in Electronics and Communication Engineering** in the department of Electronics and Communication Engineering at National Institute of Technology Karnataka, Surathkal during the academic year 2017-18.

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ACKNOWLEDGEMENTS

We take this opportunity to thank our project mentor, Dr.M .S. Bhat, for his guidance and encouragement throughout this project. Despite the myriad mistakes we made throughout, his kindness and patience helped us persevere and prioritise learning at every phase of the project.

We express our deep gratitude to Mr. Sreenivasulu Polineni, Research Scholar, whose constant guidance and support helped us in strengthening our understanding in Analog Electronics and Data Converters. His impeccable patience, in helping us clear our myriad doubts, resolve issues that cropped up time and again as we did the project, greatly helped us push through all the dead ends and conceptual shortcomings. It was wonderful to work on a completely new concept, with such a strong support and guidance at every phase of the project.

We extend our warm thanks to Mr. Guruthilak Shriyan, for helping us in the VLSI Lab. A warm thanks to Dr. Ratnamala Rao, Dr. A.V. Narasimhadhan and Dr. Prashantha H. Kumar who comprised the evaluation team at NITK.

We express our gratitude to Dr. T. Laxminidhi, Head, Department of Electronics and Communication Engineering, NITK, for giving us this wonderful opportunity.

We would like to take this opportunity to express our thanks towards the teaching and non-teaching staff in the Department of Electronics and Communication Engineering, NITK for their invaluable help and support in these four years of our study.

ABSTRACT

Signal processing tasks are chiefly done using digital methods, owing to the ease of implementation and robustness of digital circuits. These digital structures can be combined to obtain accurate, fast and power efficient systems.Since physical signals are analog in nature, data converters are needed to interface with the Digital Signal Processing core. The increasing speed and capability of the digital cores has given rise to the need to improve the speed and accuracy of the converters associated with them. Among various available architectures, Delta-Sigma ADC is suitable for high resolution and low to moderate frequencies of operation.

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CHAPTER 1
Introduction

In the ever increasing portable device market, medical electronic devices, mobile phones and personal digital media are imposing strict requirements on speed and accuracy. This ever increasing demand for processing efficiency has pushed for the need to improve the data conversion process (Analog to Digital conversion). ADC design is highly dependent on input operating frequency and amplitude. Most of the applications demand an ADC that can vary the resolution depending on the input signal frequency requirements that change widely for different applications. Conventional high resolution AD (Analog to Digital) converters like flash type operate at Nyquist rate and are unable to make use of the high speeds achieved with scaled VLSI technology. These Nyquist rate converters require a complex anti-aliasing filter to limit the input frequencies to the sample and hold and AD circuitry. Delta Sigma (DS) ADCs are a cost effective alternative for high resolution (greater than 10 bits) converters, that can be integrated with the signal processing blocks. It uses oversampling and noise shaping to achieve this improvement in resolution and noise filtering, despite using a low resolution AD converter and a single bit quantiser. The AD conversion is followed by decimation to bring down the sampling rate to Nyquist rate followed by low pass filtering to eliminate the shaped noise.

1.1 Problem definition

The task is to implement a Delta Sigma ADC with a resolution greater than 10 bits. The first task was to understand and implement an amplifier with a high gain to be used as an integrator in the switched capacitor circuit. The second requirement was to implement a comparator required for the analog to digital conversion stage of the ADC.

1.2 Overview

For the integrator stage of the switched capacitor circuit, a two stage and three stage Operational Transconductance Amplifier (OTA) architecture were implemented, since OTAs known to offer a high gain (greater than 70 dB). Parameters like power supply, slew rate and DC gain were fixed, following which the circuit was designed using the basic MOSFET Saturation equations [1].

A clocked regenerative comparator and a dynamic two stage comparator were implemented and used in our design [2,3]

In this report, chapter 2 gives a brief description of the Delta Sigma Modulator, OTA and comparator concepts, gradually building up to the design procedure. The results of the simulations and analysis are presented in chapter 3.

CHAPTER 2
Description

2.1 Fundamentals of ADCs

Delta Sigma Modulators rely heavily on oversampling and noise shaping. The basic building blocks and operation of an ADC is illustrated in the below Figure 2.1. The basic ADC consists of an anti-aliasing filter (AAF), a sample and hold circuit (S/H), a quantiser and a coder. The AAF prevents the high frequency components of the input signal from aliasing into the signal bandwidth and corrupting the signal. The filtered signal is then passed though the sample and hold circuit to convert the continuous time signal to a discrete signal, sampled at a rate f_s. The quantiser maps the continuous signal to discrete levels. The coder provides the digitised output, by assigning a unique binary number to each discretised level [4]

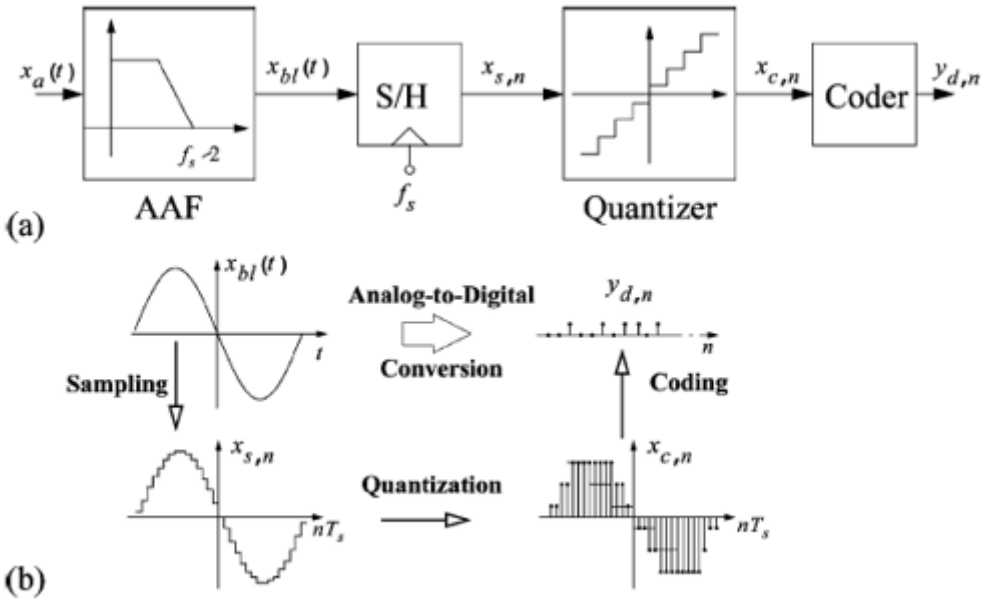

Figure 2.1: a)Block diagram b) Signal characteristics [4]

2.2 Over Sampling

The minimum rate at which a signal has to be sampled to avoid aliasing is called the Nyquist rate. It is twice the maximum input frequency f_{max} ($f_N = 2f_{max}$). Oversampling

is sampling the signal at a frequency f_s, that is Over Sampling Ratio (OSR) times the Nyquist rate f_N (OSR $= f_s/f_N$) Oversampling improves the Signal-to-Quantisation-Noise Ratio (SQNR) and resolution of the ADC. In a DSM based ADC the inband noise power reduces by a factor of OSR, but the total noise power remains the same. The noise spread of Nyquist frequency, is filtered out using a digital low pass filter [4].

2.3 Modelling quantization error as white noise

In quantisation, continuous levels are mapped to discrete levels and it is an irreversible process. Hence, there is a loss in resolution of the quantised signal and degradation in input signal quality. The error generated by this continuous to discrete transformation is known as quantisation error. For a system the input x, is usually bound to full scale input range $[\frac{-X_{FS}}{2}, \frac{X_{FS}}{2}]$ and the quantisation error is confined to [-Δ/2, Δ/2] where Δ is the quantisation step given by

$$\Delta = \frac{Y_{FS}}{(2^B - 1)} \tag{2.1}$$

where Y_{FS} is full scale output range for a B-bit quantiser. Since the PSD of the quantisation noise is uniformly distributed in [-Δ/2, Δ/2] it can be modelled as an additive white noise source e as shown in Figure 2.2 d). The in-band noise power calculated is

$$PE = \frac{\Delta^2}{12.OSR} \tag{2.2}$$

From the above equation, the in-band noise power decreases with OSR at 3dB/octave. The quantisation noise is pushed to the higher frequencies, attenuating the in-band noise power compared to the Nyquist rate frequencies.

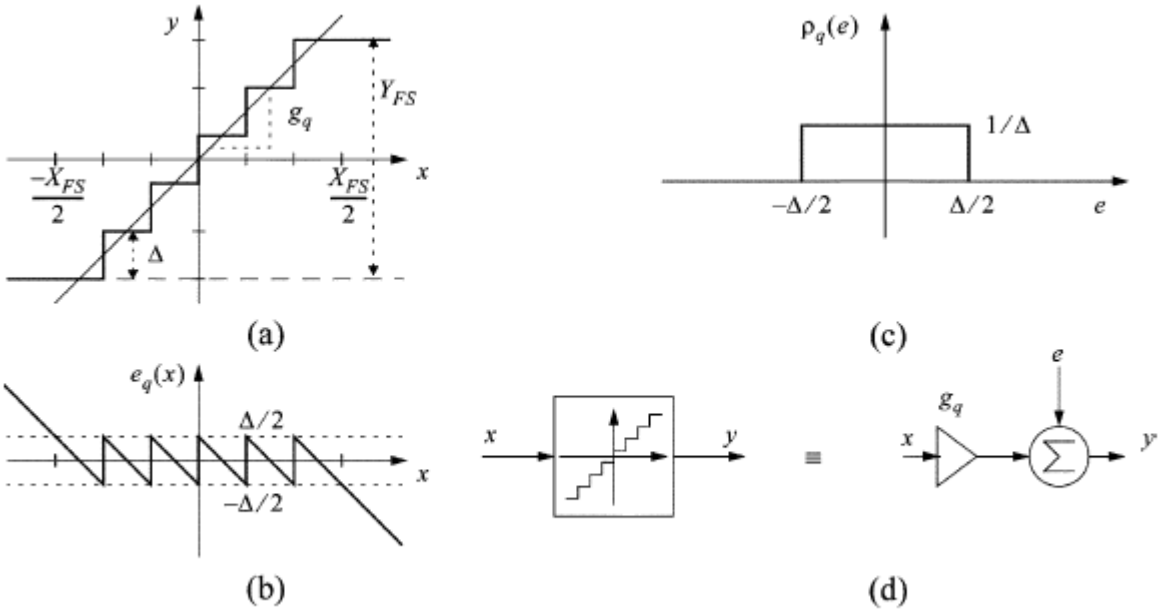

Figure 2.2: a) Ideal quantiser b) Quantisation error c) PSD of white quantisation noise d) Linear model [4]

2.4 Noise Shaping

The DSM can be made more efficient by filtering the noise such that most of its power lies outside the signal band. Consider the feedback loop in Figure 2.3 with a forward gain A, u the input , e the quantisation error (additive model) and v the output. A delay has been included in the feedback path to model the delay in the quantisation process [5].

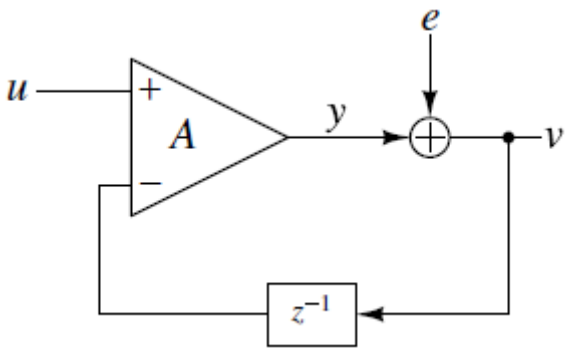

Figure 2.3: Physically realizable discrete time feedback loop [5]

$$V(z) = \frac{A}{1 + A.z^{-1}}.U(z) + \frac{1}{1 + Az^{-1}}.E(z) \tag{2.3}$$

therefore,

$$V(z) = STF.U(z) + NTF.E(z)$$

Where,

$$Signal\ Transfer\ Function\ (STF) = \frac{A}{1 + A.z^{-1}}$$

$$Noise\ Transfer\ Function\ (NTF) = \frac{1}{1 + A.z^{-1}}$$

It is observed that for large A, NTF = 0 and STF = 1. This implies that for large values of A, the noise can be conveniently eliminated. The pole of the system is at z = -A. For a discrete time system to be stable, the poles have to be within the unit circle. However since A should ideally be large, the system becomes unstable as it is outside the unit circle in the z-domain. Therefore, making A large for all frequencies is not feasible. Hence keeping in mind that the input signals are in the low frequency range due to over-sampling, the focus can be on keeping A high for lower frequencies. This can be achieved by replacing the block with frequency independent gain A, by a block with frequency dependent gain. This gain should be infinite at lower frequencies, so that the NTF has low value in the low frequency range, i.e in the signal bandwidth $[0, \frac{\pi}{OSR}]$. An integrator is the lowest order system with these characteristics [5].

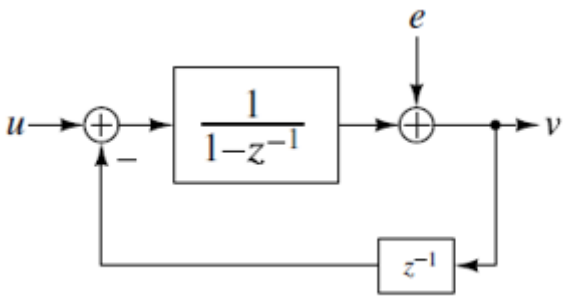

Figure 2.4: Feedback system with attenuated quantisation noise at low frequencies

For the system given in Figure 2.4 with $A = \frac{1}{1-z^{-1}}$, the STF = 1 and NTF = $(1-z^{-1})$. Thus the NTF is a high pass filter with response as shown in Figure 2.5.

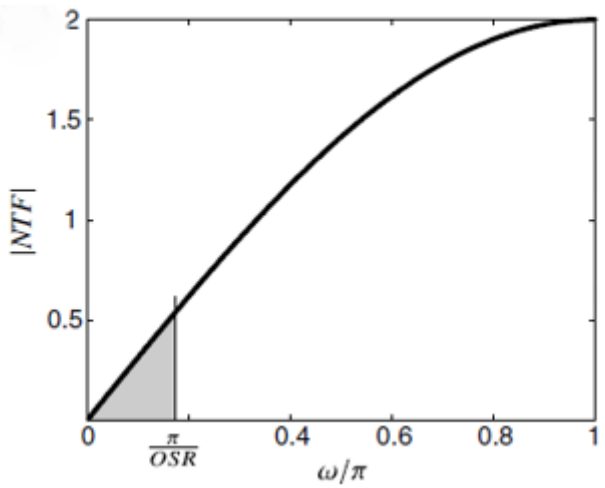

Figure 2.5: Noise transfer function

2.5 Role of OTA in Delta Sigma ADC Design

OTAs are an integral part of many analog and mixed signal systems. The main advantage of using delta sigma modulators in AD conversion is the improvement in the in-band Signal to Quantisation Noise Ratio (SQNR) owing to the noise shaping properties of the DSM.

The resolution of the ADC depends on how effectively the input can be amplified by the op-amp in the switched capacitor circuit. Hence it is important for the OTA to have as high a gain as possible along with a good Gain Bandwidth product (GBW).

The Effective Number Of Bits (ENOB) of the ADC increases with the OSR as the in-band noise power reduces with increasing OSR [4]. When the OTA is used as an integrator in the switched capacitor circuit of a DSM, the maximum sampling rate depends on the closed loop linear settling time, which is inversely related to the GBW. Thus in order to have a smaller settling time, an OTA with a higher GBW is required.

The relative error between the final output value at $t = \infty$ and the OTA output at infinite DC gain, called static error E_s, is also inversely related to the DC gain . Thus to reduce the settling time and static error, the OTA is to be designed so as to have a high GBW and high DC gain to improve the switched capacitor performance.

2.6 Single Stage OTA

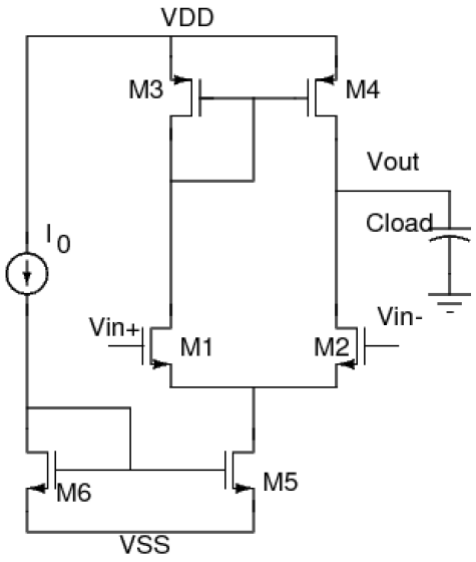

Figure 2.6: Single Stage OTA

The architecture for a single stage OTA is as shown. Typically single stage OTAs provide a gain of 40 dB The following specifications are considered while designing the aspect ratios of the MOSFETS and the DC currents-

1. Small signal gain A_v
2. Input common mode range (ICMR) i.e the maximum and minimum input common mode voltage
3. Slew rate for a given load capacitance, SR
4. Power Dissipation

The following design equations are obtained for the single stage OTA

1. Obtain the min bias current required for the slew rate specified for the given load capacitance
$$I_5 = SR.C_L \tag{2.4}$$
2. The max input common mode voltage is used to obtain the aspect ratio of M3 as follows
$$S_3 = \frac{I_5}{K_3'.[V_{DD} - ICMR(+) - V_{T3} + V_{T1}]^2} \tag{2.5}$$
Aspect ratio of M4 is the same as that of M3
3. Using the relation for the GBW of the OTA to calculate g_{m1}.
$$GBW = \frac{g_{m1}}{C_L} \tag{2.6}$$

4. Thus the aspect ratio of M1 is found using

$$S_1 = \frac{g_{m1}^2}{K_1'.I_5} \tag{2.7}$$

5. Aspect ratio of M5 is found using

$$S_5 = \frac{2.I_5}{K_5'.V_{DS5(SAT)}^2} \tag{2.8}$$

Where

$$V_{DS5(SAT)} = ICMR(-) - V_{SS} - \sqrt{\frac{I_5}{K_1'.S_1}} - V_{T1} \tag{2.9}$$

2.7 Two Stage OTA

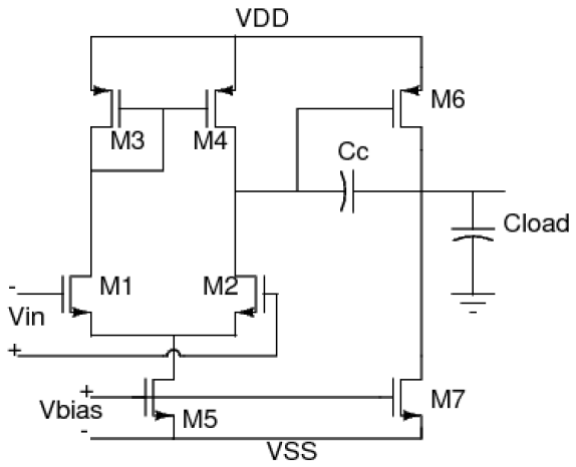

Figure 2.7: Two Stage OTA

Two stage OTAs are preferred over Single stage OTAs as they offer higher gain, usually greater than 70 dB. The following relationships are based on the circuit

- *Slew rate* $SR = I_5/C_c$
- Gain Bandwidth GBW = g_{m1}/C_c
- Output pole $p_2 = -g_{m6}/C_l$
- RHP zero $z_1 = g_{m6}/C_c$
- $ICMR(+) = V_{DD} - \sqrt{I_5/K_3'.S_3} - |V_{T3}| + V_{T1}$
- $ICMR(-) = V_{SS} - \sqrt{I_5/K_1'.S_1} + V_{T1} + V_{DS5(SAT)}$
- Saturation voltage $V_{DS5(SAT)} = \sqrt{2I_{DS}/K'.S_K}$

It is important to maintain high Phase margins (PM) in a system to prevent ringing of the output signal. A PM of 60 degrees is preferable. The PM for the OTA is less than 45 degrees, hence a compensation capacitor Cc is needed to pull up the PM. Placing the output pole p_2 at 2.2 times higher than the GBW provides a PM of 60 degrees, given the RHP zero z_1 is beyond ten times GBW [1] . Thus the requirement placed on Cc is

$$Cc > 0.22 \cdot C_L \tag{2.10}$$

- The min value of the tail current is determined using slew rate

$$I_5 = SR \cdot C_c \tag{2.11}$$

- The aspect ratio of M3 is

$$S_3 = \frac{I_5}{K_3' \cdot [V_{DD} - ICMR(+) - V_{T3} + V_{T1}]^2} \tag{2.12}$$

- C_c and GBW are used to determine the input transconductance of the transistors

$$g_{m1} = GBW \cdot C_c$$

.

- Aspect ratio of M1 is obtained using

$$S_1 = \frac{g_{m1}^2}{K_1' \cdot I_5} \tag{2.13}$$

- Using negative ICMR to obtain $V_{DS5(SAT)}$.

$$V_{DS5(SAT)} = ICMR(-) - V_{SS} - \sqrt{\frac{I_5}{K_1' \cdot S_1}} - V_{T1} \tag{2.14}$$

- And this can be used to extract S_5.

$$S_5 = \frac{2.I_5}{K_5'.V_{DS5(SAT)}^2} \tag{2.15}$$

- M6 can be found by mirroring of loads M3 and M4. Thus $V_{SG4} = V_{SG6}$. Also g_{m6} is ten times g_{m1} for a reasonable phase margin.

$$S_6 = S_4 \cdot \frac{g_{m6}}{g_{m4}} \tag{2.16}$$

- DC current I_6 can be thus found

$$I_6 = \frac{g_{m6}^2}{2.K_6'.S_6} \tag{2.17}$$

- Thus, the aspect ratio of M7 can be found using

$$S_7 = S_5 \cdot \frac{I_6}{I_5} \tag{2.18}$$

2.8 Folded Cascode OTA

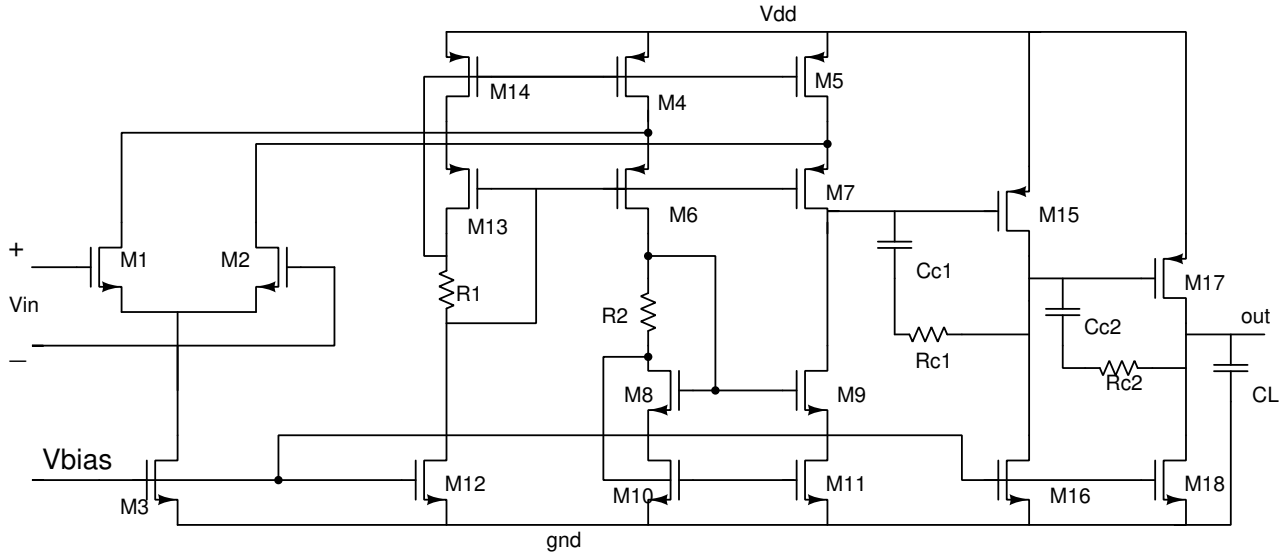

Figure 2.8: FC OTA with cascaded CS stages

The Folded Cascode (FC) OTA (Figre 2.8) uses cascoding in the output stage combined with a differential amplifier. It offers good input common mode range, self compensation and a high gain.

The following design equations are obtained for the FC OTA

1. Obtain the min bias current required for the slew rate specified for the given load capacitance

$$I_3 = SR.C_L \tag{2.19}$$

2. The bias currents I_3, I_4, I_5 of the FC op-amp should be designed such that current in the cascode mirror never goes to zero. Hence $1.2I_3 < I_4 = I_5 < 1.5I_3$

3. The max output voltage can be used to find S_5 and S_7 -

$$S_5 = S_{14} = S_4 = \frac{2 \cdot I_5}{K'_p \cdot V^2_{SD5}} \tag{2.20}$$

$$S_7 = S_{13} = S_6 = \frac{2 \cdot I_5}{K'_p \cdot V^2_{SD5}} \tag{2.21}$$

where

$$V_{DS5}(sat) = V_{DS7}(sat) = \frac{V_{dd} - V_{out}(max)}{2} \tag{2.22}$$

4. The minimum output voltage can be used to find S_5 and S_7-

$$S_{10} = S_{11} = \frac{2 \cdot I_{11}}{K'_n \cdot V^2_{SD11}} \tag{2.23}$$

$$S_9 = S_8 = \frac{2 \cdot I_9}{K'_n \cdot V^2_{SD9}} \tag{2.24}$$

where

$$V_{DS9}(sat) = V_{DS11}(sat) = \frac{V_{dd} - V_{out}(min)}{2} \tag{2.25}$$

5. For the self bias cascode

$$R_1 = \frac{V_{SD14}(sat)}{I_{14}} \tag{2.26}$$

$$R_2 = \frac{V_{DS8}(sat)}{I_6} \tag{2.27}$$

6. Using the relation for the GBW of the OTA to calculate g_{m1} -

$$GBW = \frac{g_{m1}}{C_L} \tag{2.28}$$

7. Thus the aspect ratio of M1 is found using

$$S_1 = \frac{g^2_{m1}}{K'_n.I_3} \tag{2.29}$$

8. The min input common mode voltage is used to obtain the aspect ratio of M3 as follows

$$S_3 = \frac{I_3}{K'_n.[V_{in}(min) - \sqrt{\frac{I_3}{K'_n \cdot S_1}} - V_{T1}]^2} \tag{2.30}$$

The cascaded common source amplifier stages and the compensation network are designed as in two stage OTA

2.9 Comparator-1

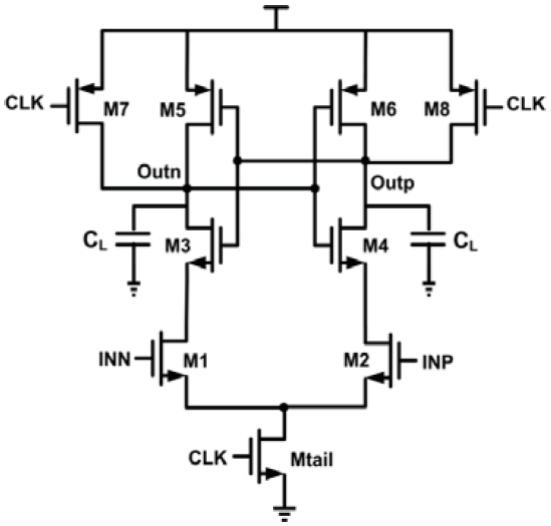

Figure 2.9: Conventional Dynamic Comparator [2]

Comparators are a very important part of many AD converters. Low power, high speed comparators are an important part of high speed ADCs. An attempt was made to implement a very basic comparator that would be a part of the 10 bit ADC. Hence we have considered clocked regenerative dynamic comparator [2] as shown in the Figure 2.4. Clocked regenerative comparators can make fast decisions due to strong positive feedback in the regenerative latch.

The total delay of the comparator in Figure 2.9 is given by

$$t_{delay} = t_0 + t_{latch}$$

The delay t_0, is the capacitive discharge of the load capacitance C_L until the transistors M5 or M6 turn on and is given by

$$t_0 = 2 \cdot C_L \cdot \frac{V_{thp}}{I_{tail}} \tag{2.31}$$

t_{latch} is the latching delay of the two cross coupled inverters, given by

$$t_{latch} = \frac{C_L}{gm_{eff}} \cdot \log_e \frac{V_{DD}/2}{\Delta V_o} \tag{2.32}$$

While designing the comparator it is best to strive to achieve as small a delay as

possible.

2.10 Comparator-2

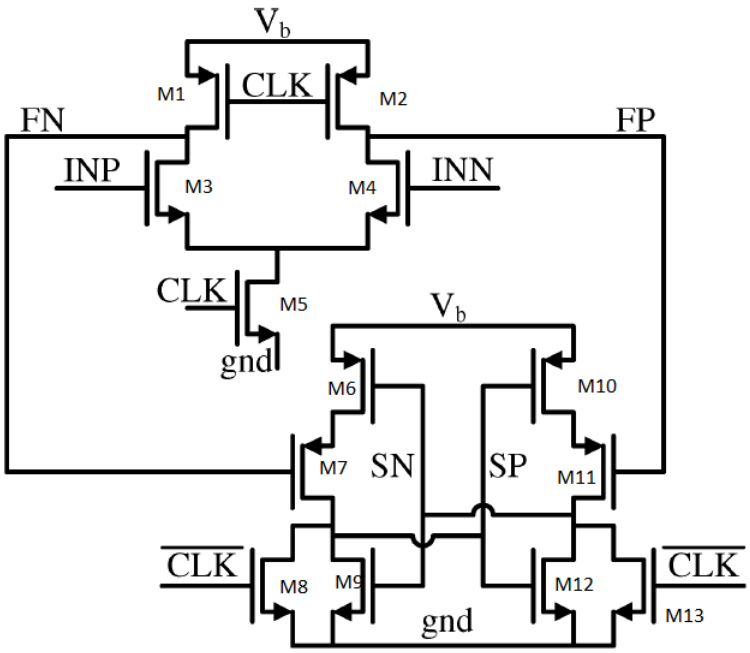

Figure 2.10: Dynamic two stage comparator

The double tailed dynamic comparator implemented for the first set of simulation did not generate the right output in the DSM circuit implemented. Hence a dynamic two stage comparator as shown in Figure 2.10 was considered for implementation. First stage is a voltage amplification stage with INP and INN as the differential input and FP and FN as the differential output.The second stage contains a simple voltage amplifier and positive feedback amplifier [3].
When clk is low (precharge),

- M1, M2 turn on. FP, FN, SP and SN are pulled up to V_b.

When clk is high (evaluate),
If $INP > INN$,

- FN discharges faster than FP
- Therefore, M7 turns on faster than M11.
- M7 on implies SP is pulled up to V_b, M11 off implies SN is pulled down

If $INN > INP$,

- FP discharges faster than FN
- Therefore, M11 turns on faster than M7
- M7 off implies SP is pulled down to zero, M11 on implies SN is pulled up to V_b

2.11 First Order Delta Sigma Modulator

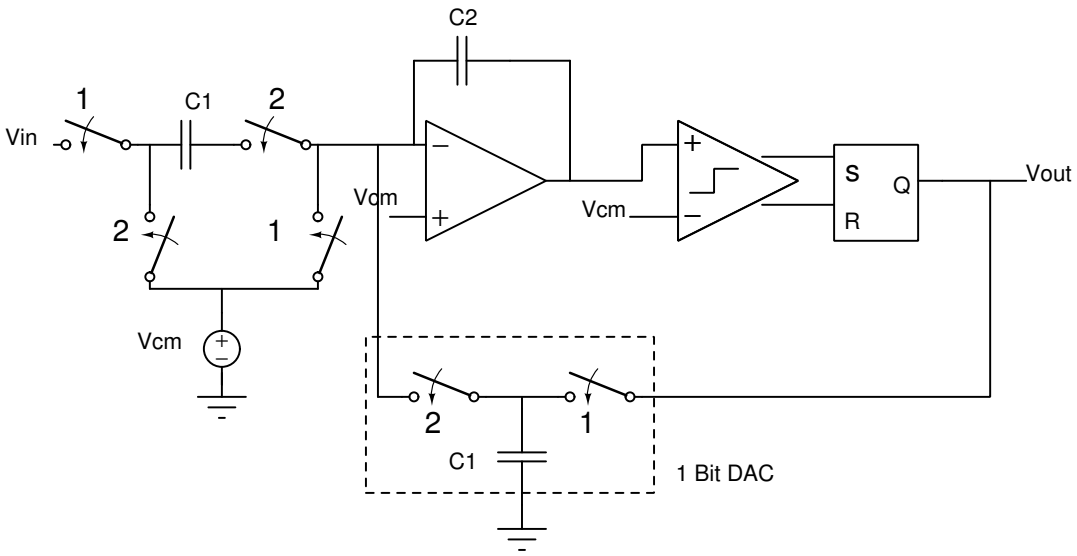

Figure 2.11: Circuit diagram of the implemented first order DSM

DSMs are of two types continuous time (CT) and discrete time (DT). DT DSMs use switched capacitor integrators whereas CT circuits employ active RC filters. It is possible to achieve accurate time constants in switched capacitor implementation as it is a ratio of two capacitance. CT implementation might lead to impractical on-chip realizations of capacitance. This is because, in order to reduce thermal noise, resistors have to be made small and capacitor sizes have to be increased. However, a DT DSM requires an anti-aliasing filter, thus increasing power consumption

2.11.1 Switched Capacitor Integrator

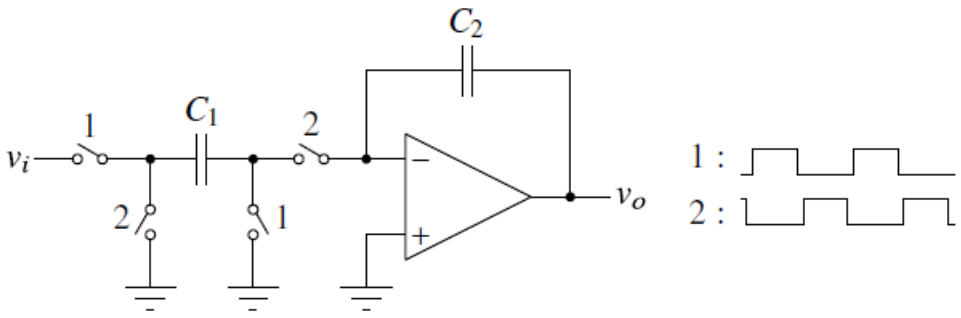

Figure 2.12: Switched capacitor integrator

A switched capacitor (SC) integrator (Figure 2.12) is the first building block of the DSM circuit. The circuit runs on two phases of clocks Phase 1 and Phase 2. The switches

labelled 1 are ON during Phase 1, and those labelled 2 during Phase 2. During Phase 1, C_1 is charged to input voltage $V_i[n]$, C_2 holds the charge it had in the previous phase. In Phase 2, The charge on C_1 accumulates on C_2, thus,

$$q_2[n+1] = q_2[n] + q_1[n] \tag{2.33}$$

Taking Z transform,

$$\frac{Q_2(z)}{Q_1(z)} = \frac{z^{-1}}{1 - z^{-1}} \tag{2.34}$$

Since $Q_1(z) = C_1 \cdot V_i(z)$ and $Q_2(z) = C_2 \cdot V_o(z)$,

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{2.35}$$

From equation (2.35) the above circuit implements a delaying integrator [5].

CHAPTER 3

Analysis and Simulations

3.1 Implementation in Cadence Virtuoso

All the simulations were done in VIRTUOSO CADENCE 180nm Technology, for the constraints given in Table 3.1. The MOSFETS were sized, as per the equations mentioned in chapter 2. However the aspect ratios were tuned to ensure that all MOSFETS were in saturation and also met the design requirements (Table: 3.1)

Design Requirements	Single Stage OTA	Two Stage OTA
Power Supply	1.8V	1.8V
Load Capacitance	0.5pF	0.5pF
ICMR(high)	1.6V	1.6V
ICMR(low)	0.8V	0.8V
Slew Rate,SR	5V/us	5V/us
Gain bandwidth,GBW	25MHz	25MHz
DC gain	40dB	70dB

Table 3.1: Design Parameter Specifications

3.1.1 Single Stage OTA

The gain and phase plots and the CADENCE schematic of the single stage OTA are as shown. The gain obtained was 25 dB. Since a high gain was not obtained using this architecture, the two stage OTA was considered for implementation of the 10-bit DSM

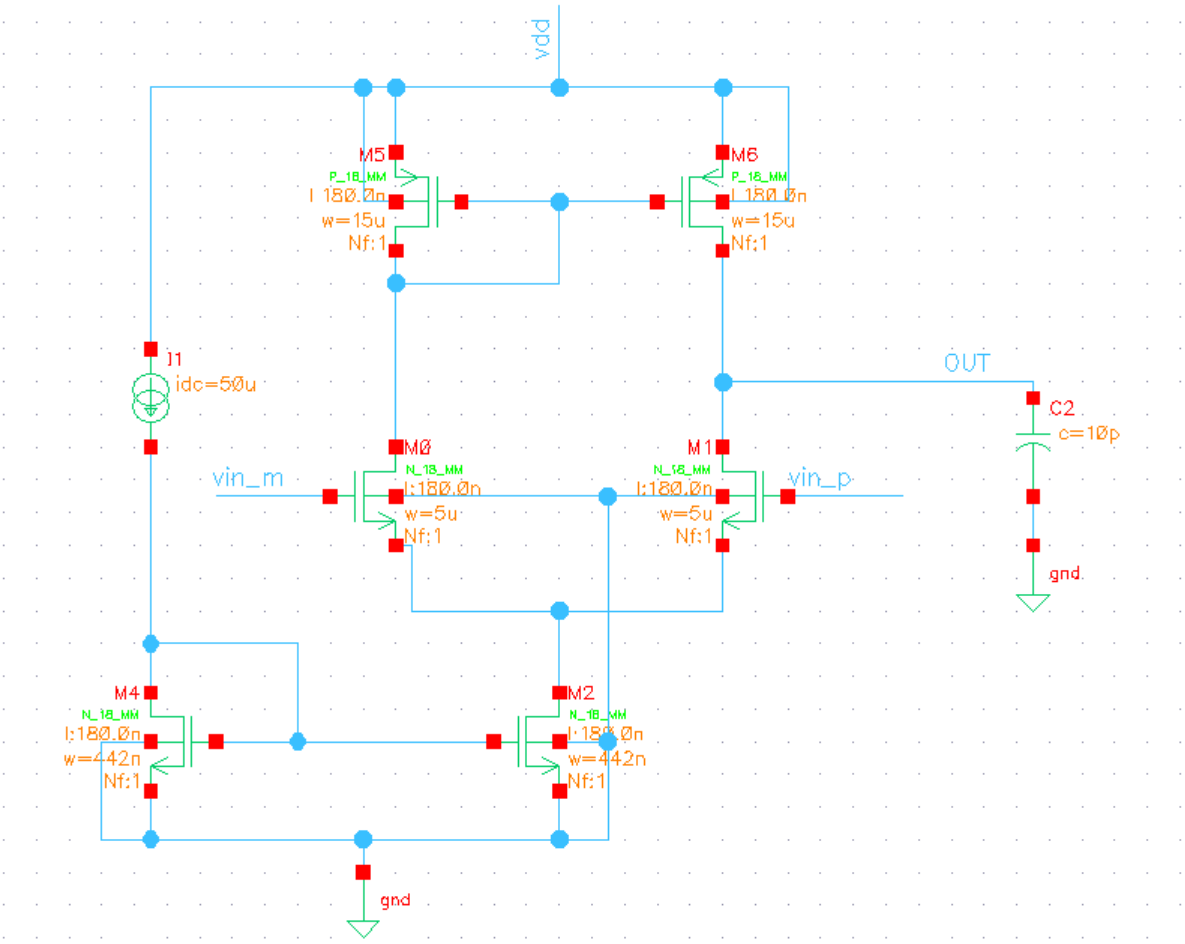

Figure 3.1: CADENCE schematic of the simulated single stage OTA

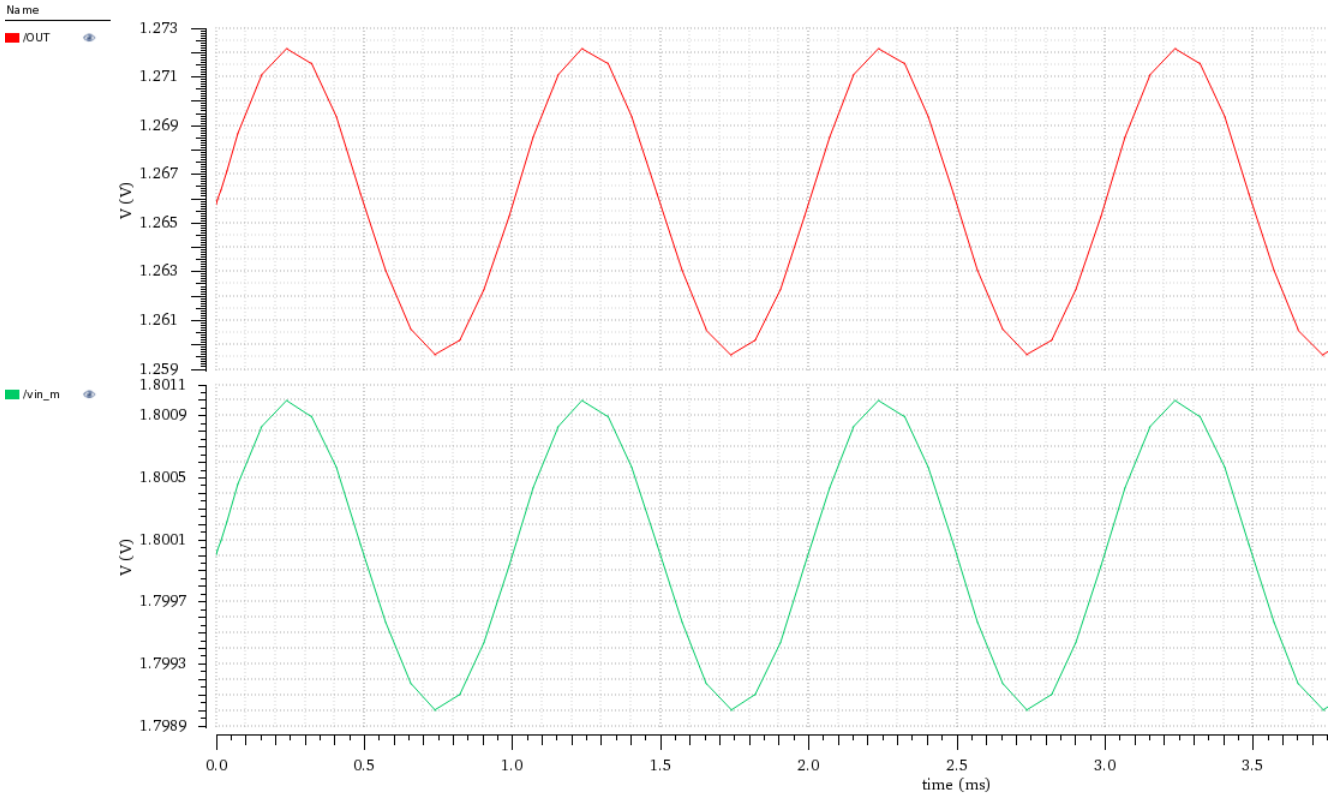

Figure 3.2: Transient response of simulated single stage OTA

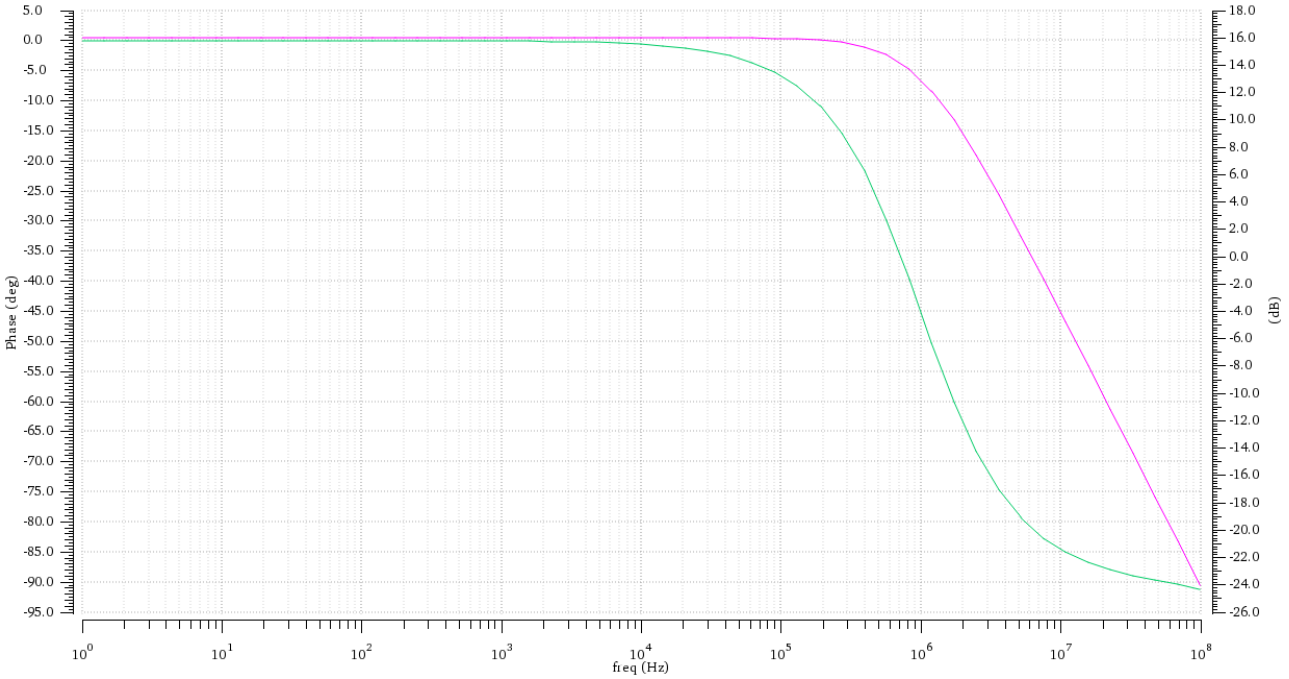

Figure 3.3: Gain and Phase plot of the simulated single stage OTA

3.1.2 Two Stage OTA

The schematics, gain and phase plot, transient response and the slew rate plots for the simulated two stage OTA are as shown below. The power dissipation, CMRR and other

operating parameters of the OTA have been recorded in Table 3.2 We obtained a DC gain of 70 dB which is sufficient to implement at least an ADC with a 10 bit resolution.

Simulated OTA Parameters	Two Stage OTA
Power Supply	1.8V
Load Capacitance	0.5pF
CMRR	70dB
Power Consumption	0.3 mW
Slew Rate,SR	34V/us
Gain bandwidth,GBW	30MHz
DC gain	67dB

Table 3.2: Simulation Results

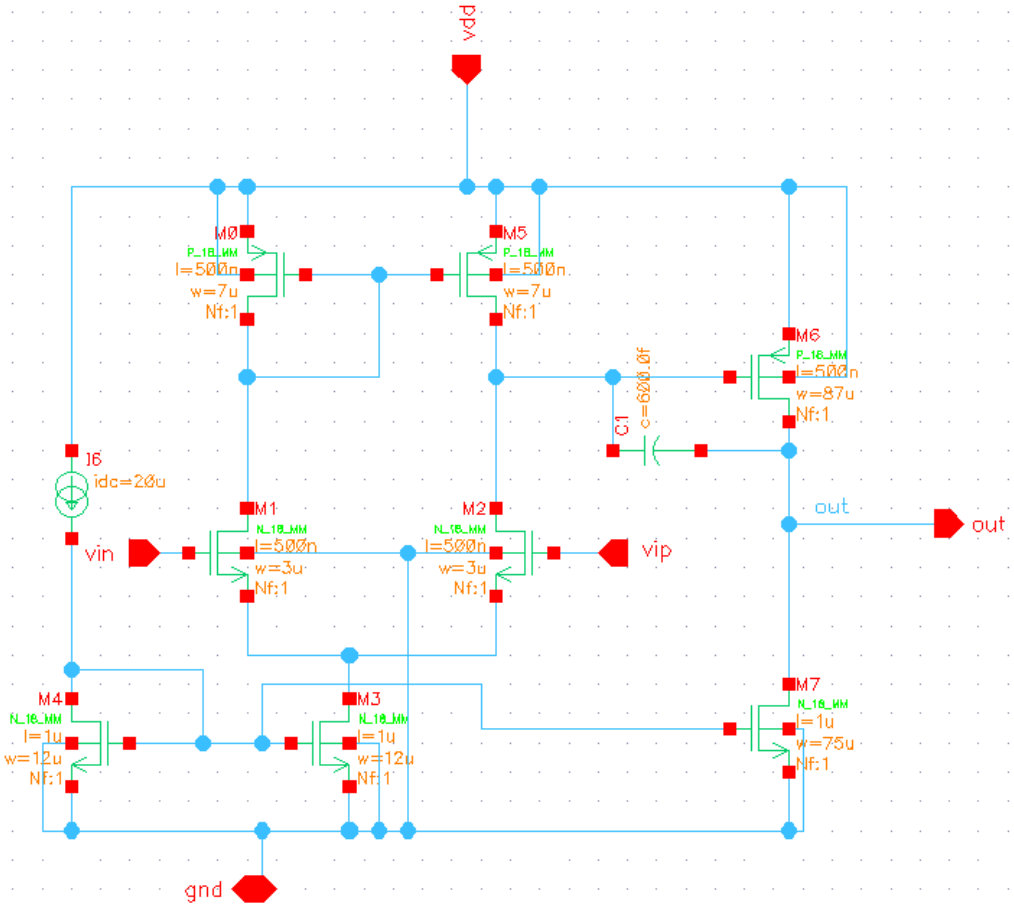

Figure 3.4: CADENCE schematic of the two stage OTA

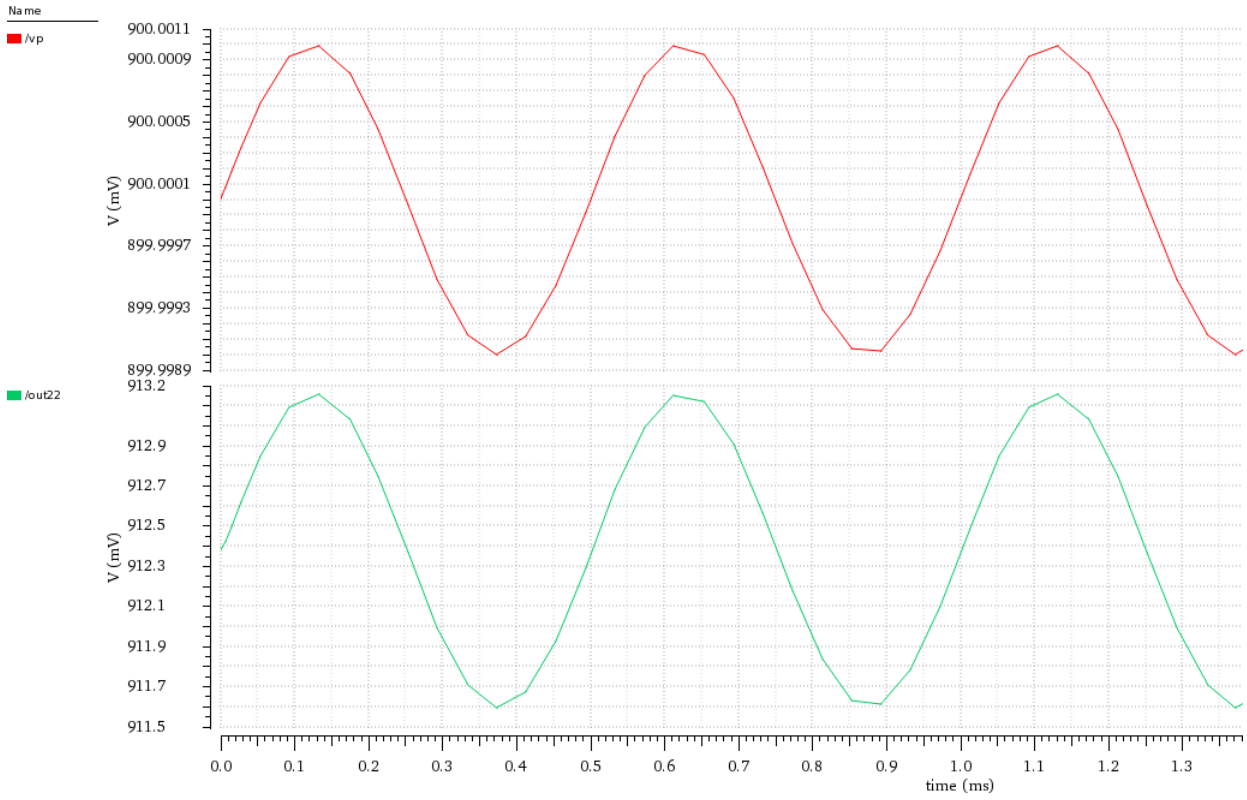

Figure 3.5: Transient response of the simulated two stage OTA

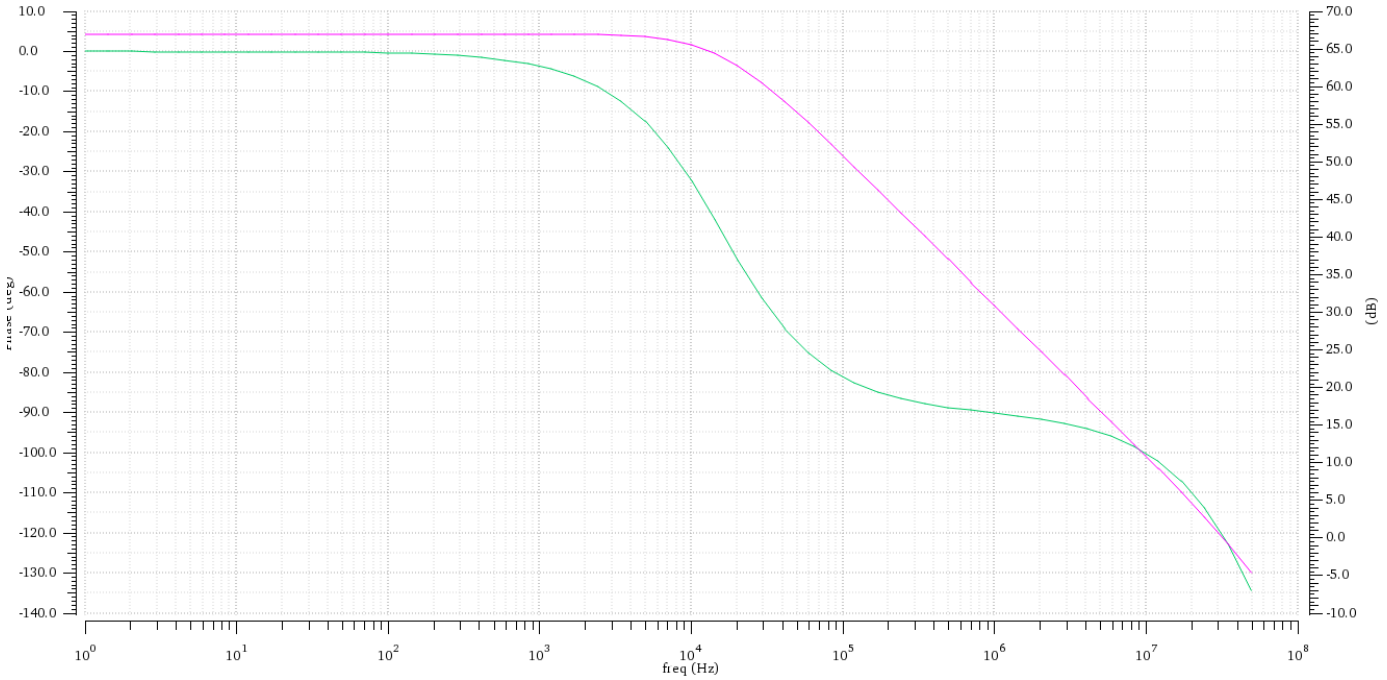

Figure 3.6: Gain and phase plot of the simulated two stage OTA

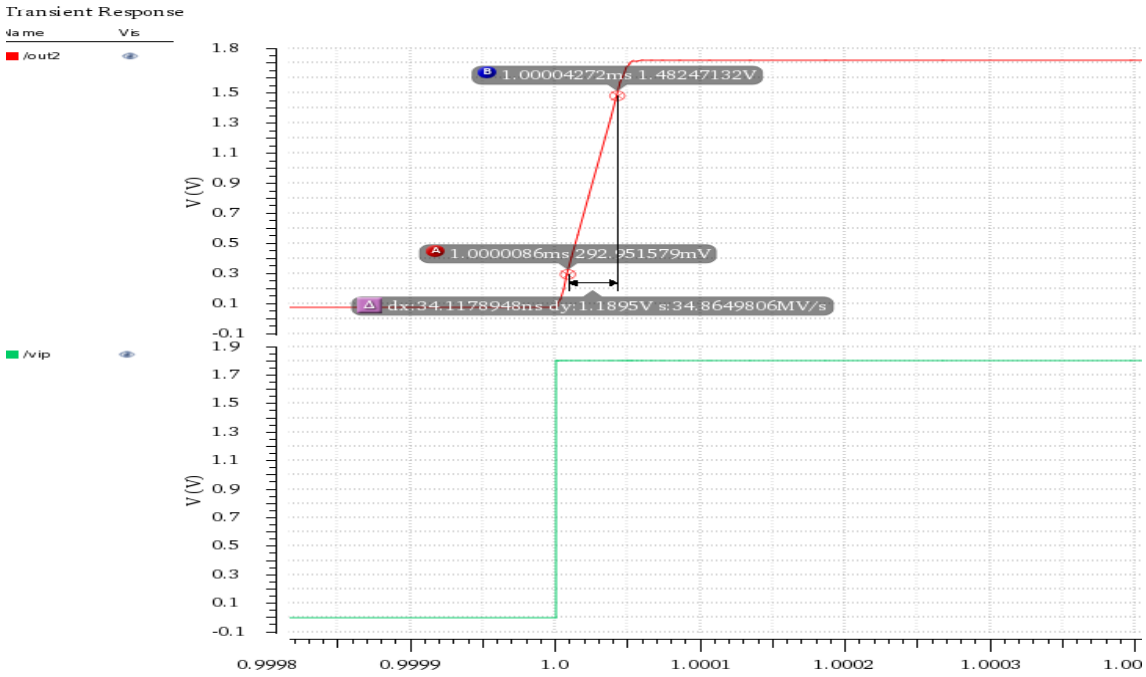

Figure 3.7: Slew rate plot of the simulated two stage OTA

3.1.3 Folded Cascode OTA - Three stage

The Folded Cascode OTA was implemented to improve the gain, which would help improve the SNR and the ENOB of the DSM. All the simulations were done in VIRTUOSO CADENCE 180nm Technology, for the constraints given in table. The MOSFETS were sized, as per the equations mentioned in section 1. However the aspect ratios were tuned to ensure that all MOSFETS were in saturation and to also meet the design requirements (Table:3.3)

Design Requirements	FC OTA
Power Supply	1.8V
Load Capacitance	20pF
ICMR(high)	1.6V
ICMR(low)	0.3V
Slew Rate,SR	10V/us
Gain bandwidth,GBW	10MHz

Table 3.3: Design Parameter Specifications

The schematic, gain and phase plot, and the slew rate plot for the simulated Folded Cascode OTA are as shown below. The power dissipation, CMRR and other operating parameters of the OTA have been recorded in Table 3.4. A DC gain of 87 dB was obtained.

Simulated OTA Parameters	Folded Cascode OTA
Power Supply	1.8V
Load Capacitance	20 pF
CMRR	93dB
Power Consumption	2.604 mW
Slew Rate,SR	54 V/us
Gain bandwidth,GBW	20MHz
DC gain	87dB

Table 3.4: Simulation Results

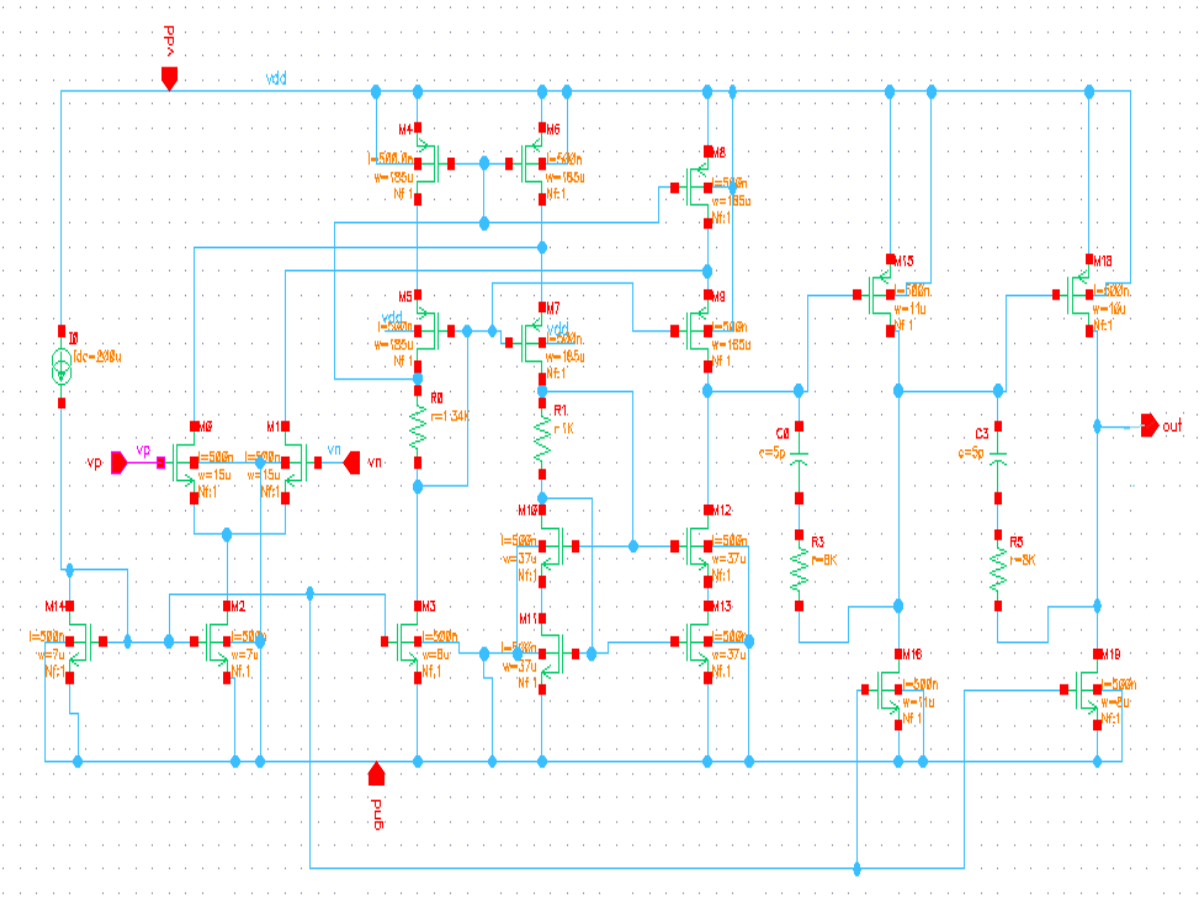

Figure 3.8: CADENCE schematic of the FC OTA

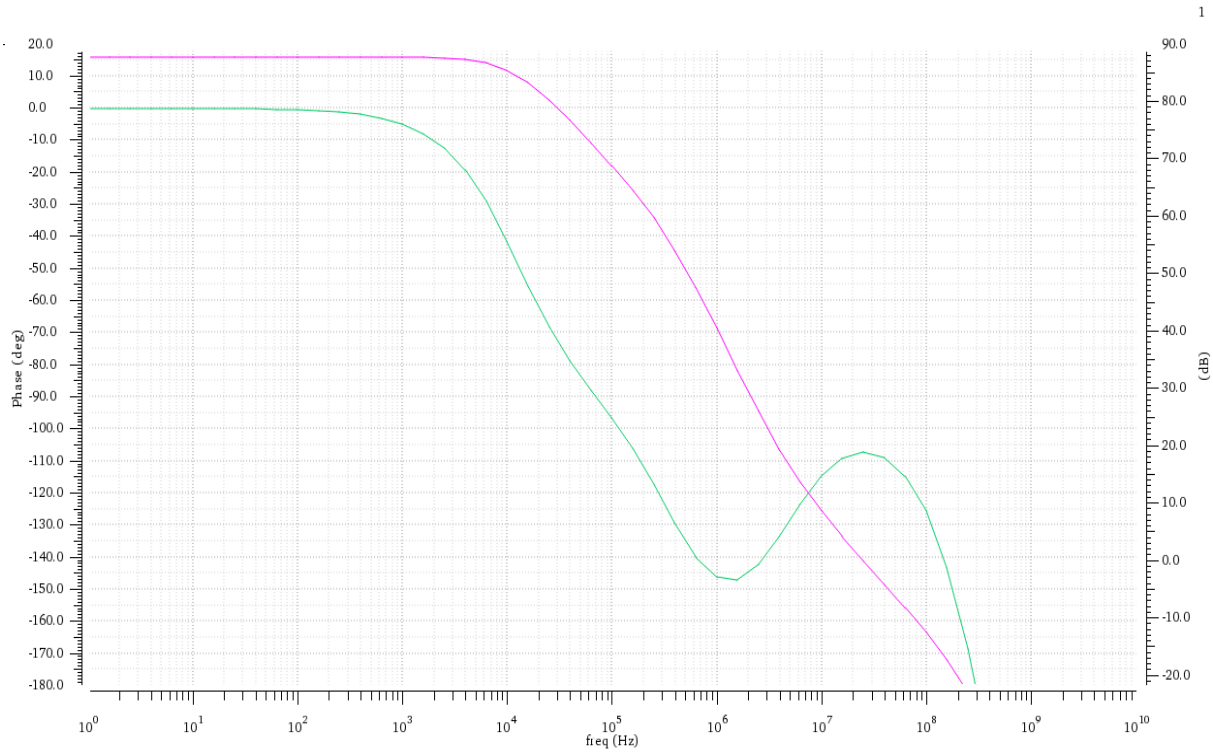

Figure 3.9: Gain and phase plot of the simulated FC OTA-red:gain plot;green:phase plot

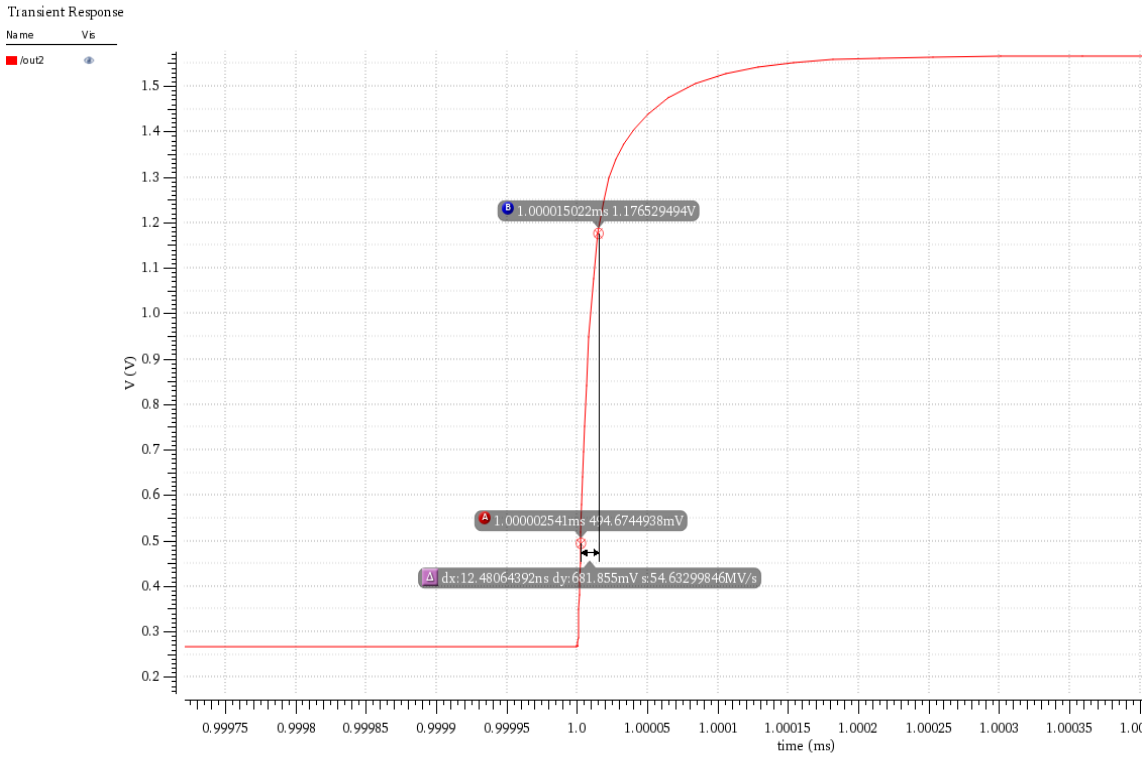

Figure 3.10: Slew rate plot of the simulated FC OTA

3.1.4 Comparator-I

The Clocked Regenerative Comparator was designed for a clock of 200MHz, for a supply voltage 1.8 V. The comparator response is as shown in Figure 3.11. The power dissipation of the circuit is 139 nW. The resolution (input offset voltage) of the comparator is around 1 mV. However, the rise and fall delay of the comparator response is around 750 psec. [Clock ON time = 2.5 ns]. This delay is quite high and there is also high frequency static noise as can be seen from the response. Hence further work needs to be done to improve the response of the comparator.

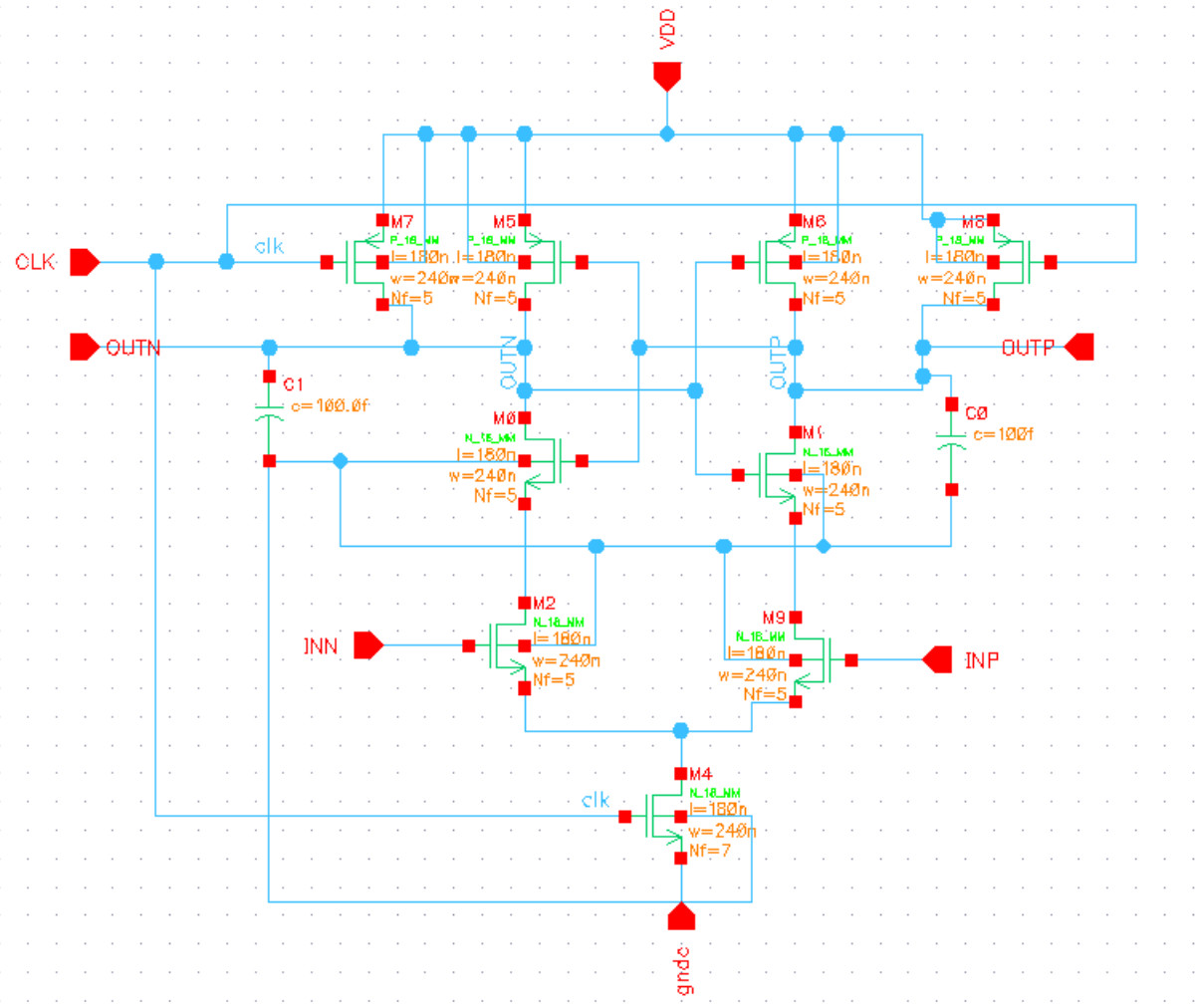

Figure 3.11: CADENCE Schematic of the dynamic comparator

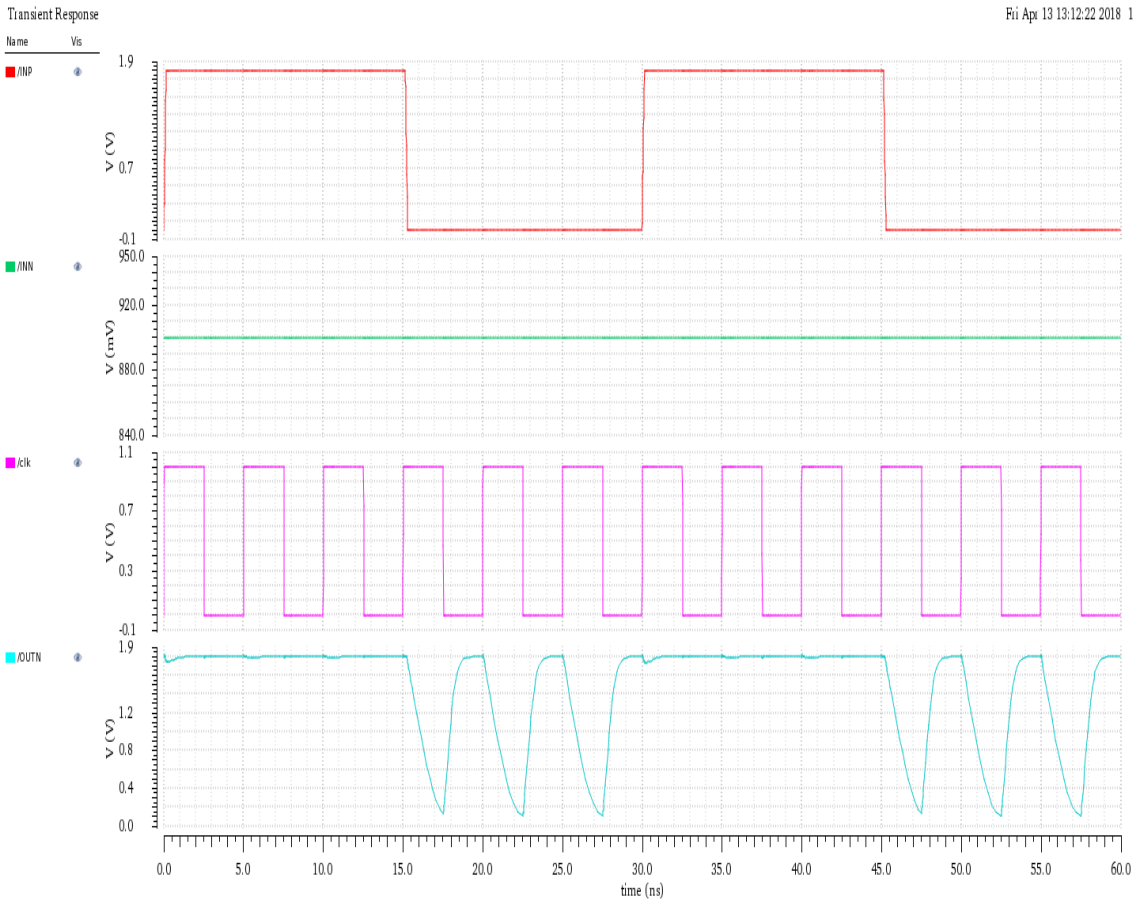

Figure 3.12: Comparator Response i) clk - clock ii) INP, INN - Inputs iii) OUTN - output

3.1.5 Comparator - II

The Dynamic Two Stage comparator was designed for a clock of 1MHz. This comparator works well in the implemented Delta Sigma Modulator.

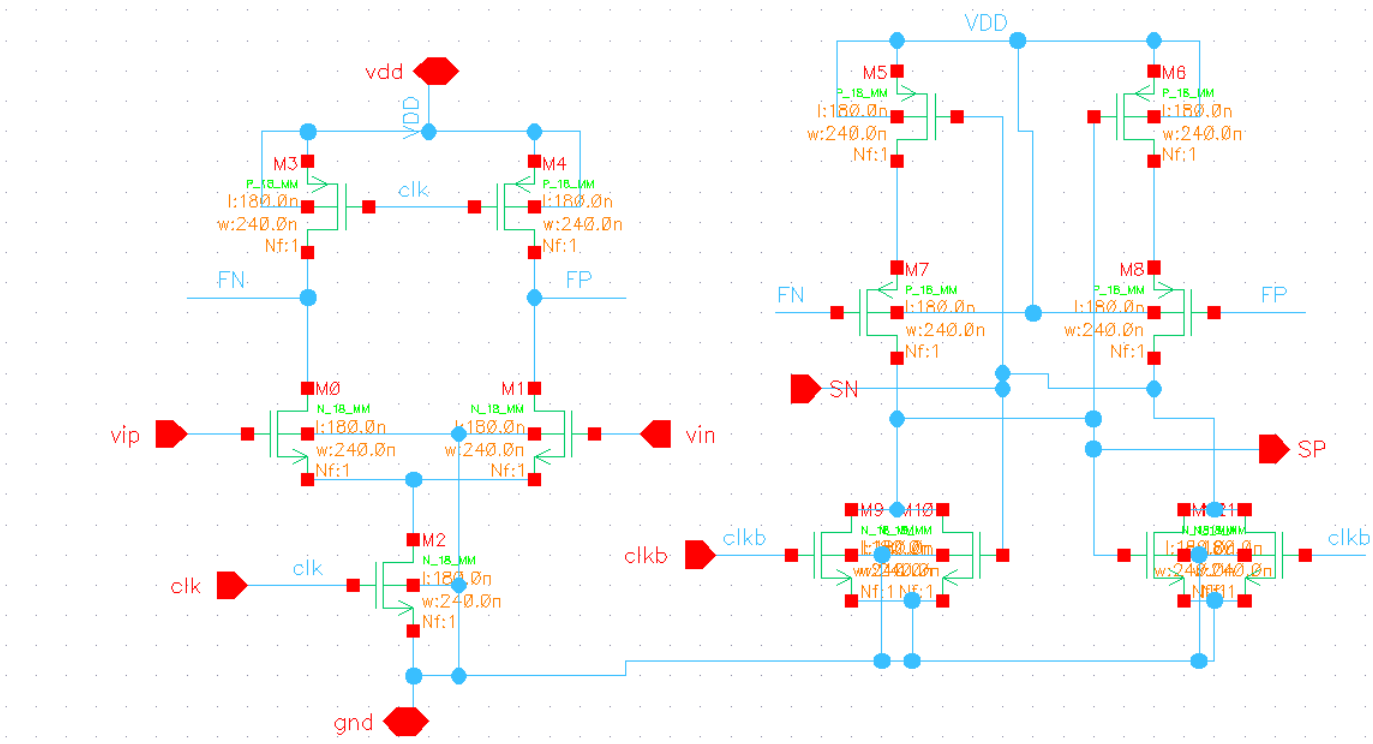

Figure 3.13: CADENCE Schematic of the dynamic two stage comparator

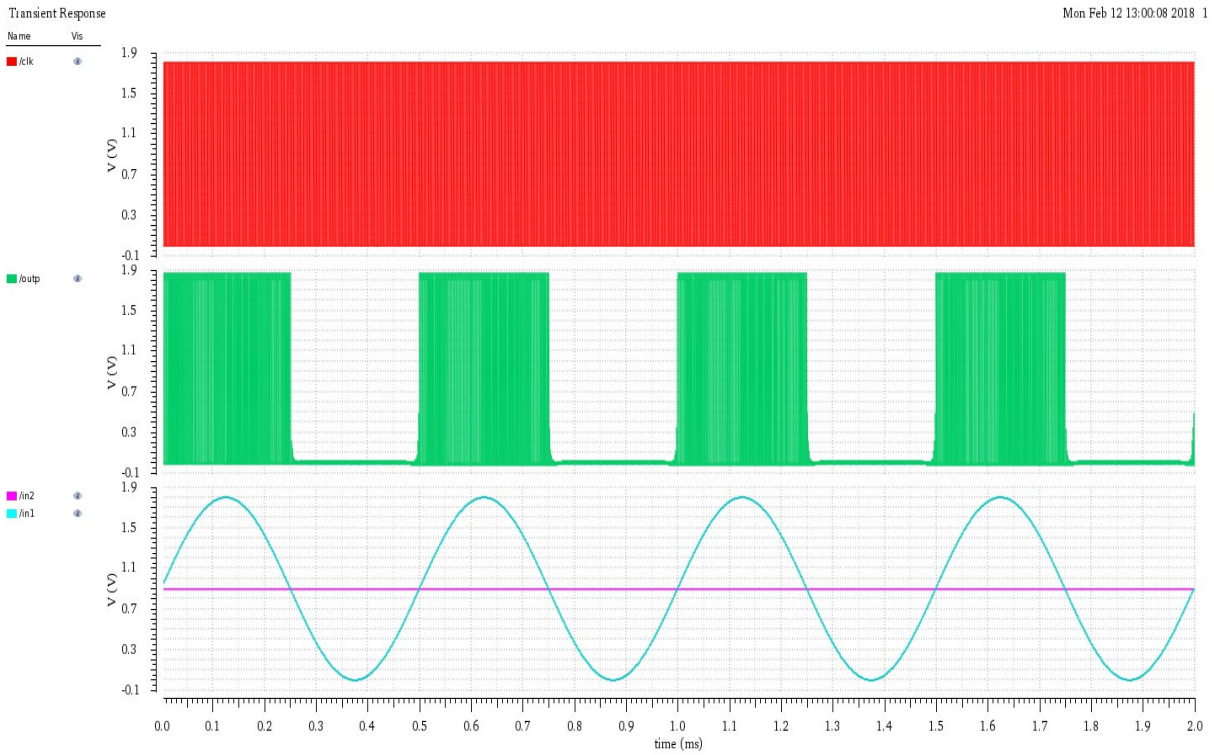

Figure 3.14: Comparator Response i) clk - clock ii) in1, in2 - inputs iii) outp - comparator output

3.1.6 First order DSM with ideal switches

The first order DSM was implemented for a sinusoidal input signal, with a frequency of 2 KHz. The clock frequency is 1 MHz (OSR = 250) The first circuit is implemented using the ideal switches available in the Cadence Virtuoso Library.

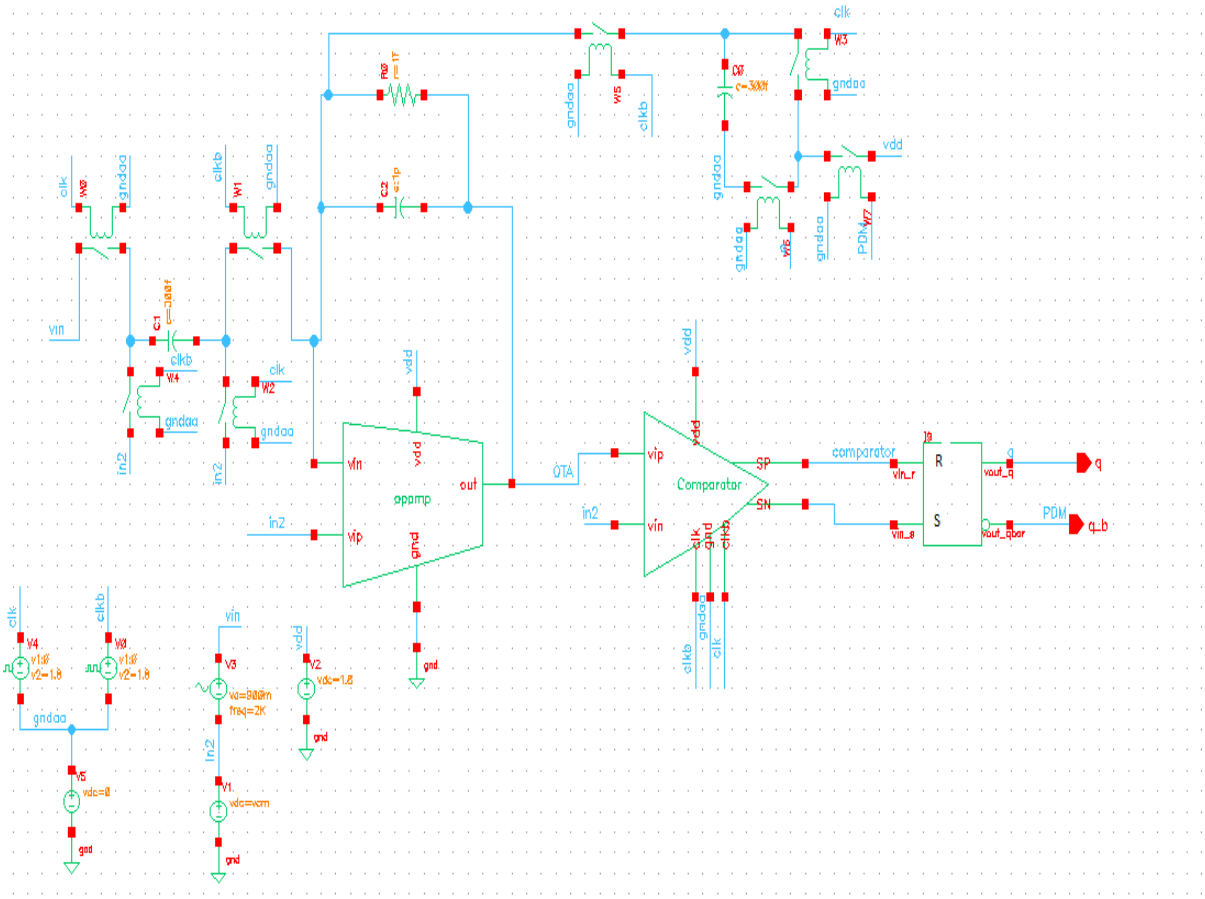

Figure 3.15: Schematic of the 1st order DSM (with ideal switches)

Fig 3.16 shows the Pulse Density Modulation output obtained for the given input.

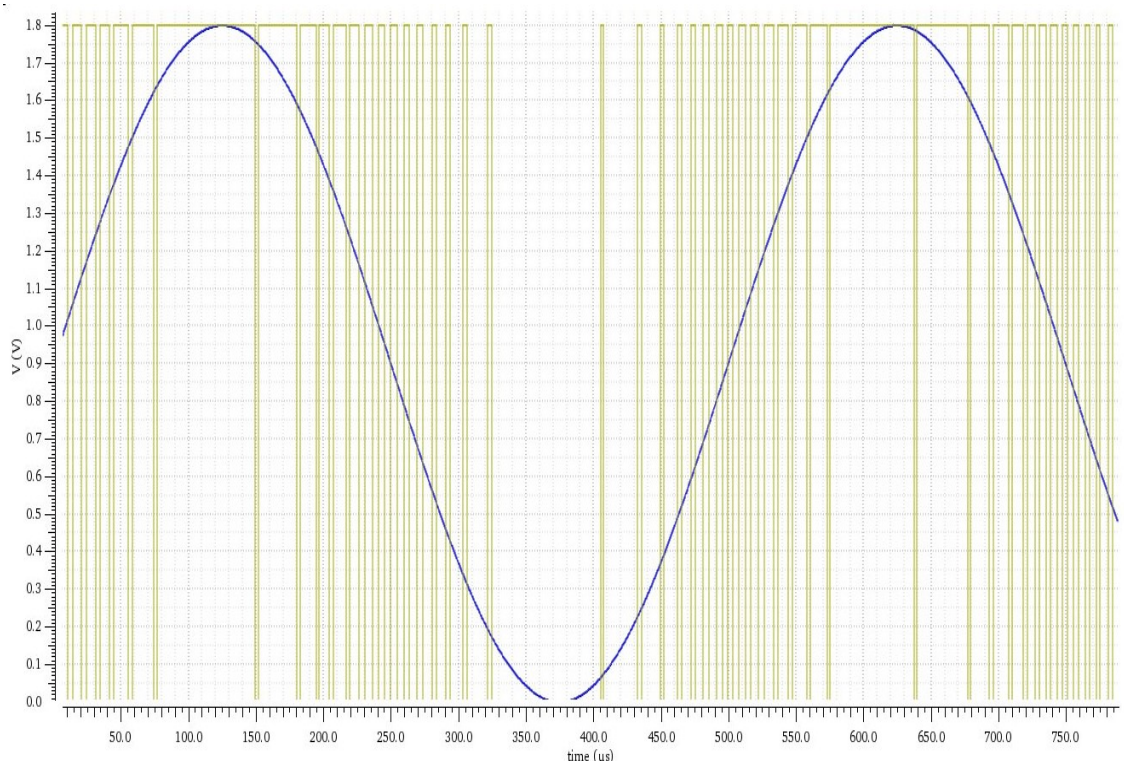

Figure 3.16: Pulse Density Modulated output of the implemented DSM

The FFT of the PDM output was plotted using MATLAB, to observe the noise shaping.(Figure 3.17)

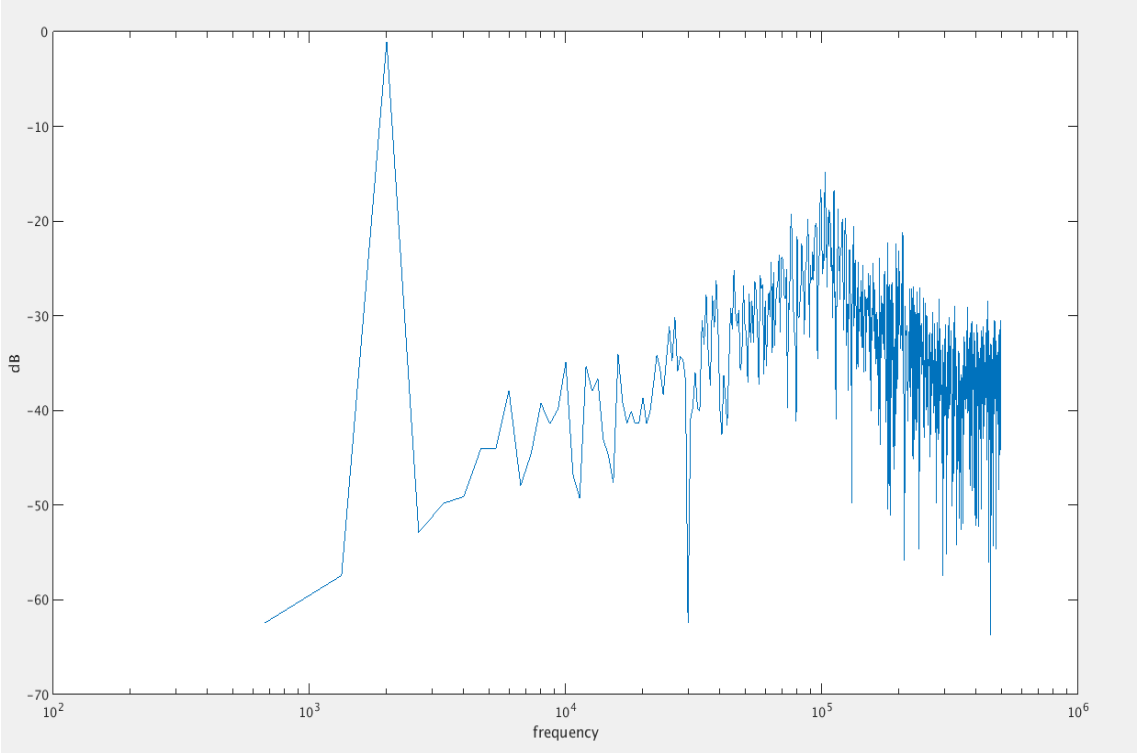

Figure 3.17: Noise-shaped output spectrum of the DSM output

The Signal to Noise Ratio (SNR) was found to be 44 dB (using MATLAB)by setting the filter bandwidth at 4kHz. Hence the Effective Number Of Bits [4] of the implemented DSM is,

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} = 7\ bits$$

Therefore $ENOB = 7\ bits$

The SNR was found to be 55.2dB (using MATLAB) by setting the filter bandwidth at 2kHz. Hence the Effective Number Of Bits of the implemented DSM is,

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} = 8.8\ bits$$

Therefore $ENOB = 8.8\ bits$

3.1.7 First order DSM with non ideal switches

The first order DSM was implemented for a sinusoidal input signal, with a frequency of 2KHz. The clock frequency is 1 MHz (OSR = 250). In this circuit, the ideal switches were replaced by transmission gates and nmos switches. Also the basic two stage OTA was replaced by the three stage folded cascode OTA to improve the SNR of the DSM

Figure 3.20 shows the Pulse Density Modulation output obtained for the given input.

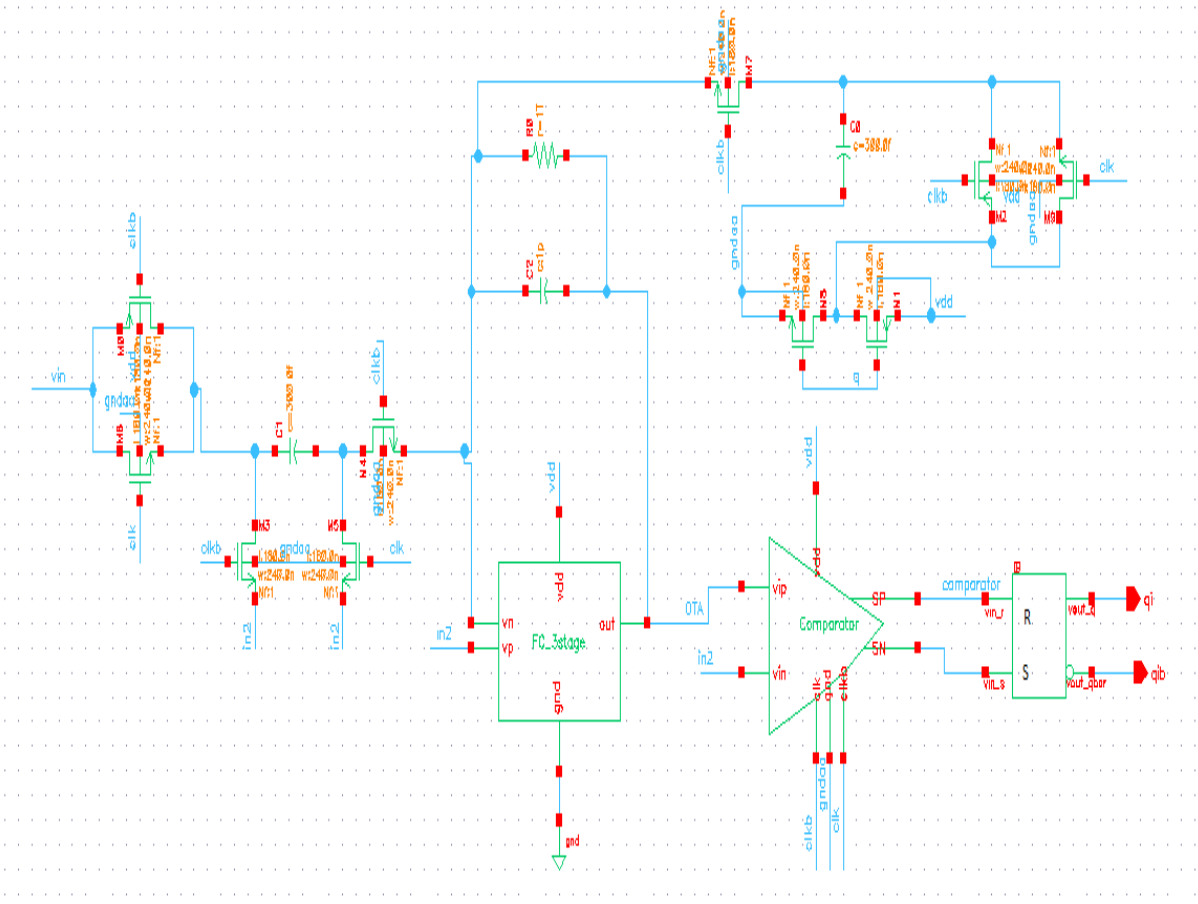

Figure 3.18: Schematic of the 1st order DSM (non ideal switches)

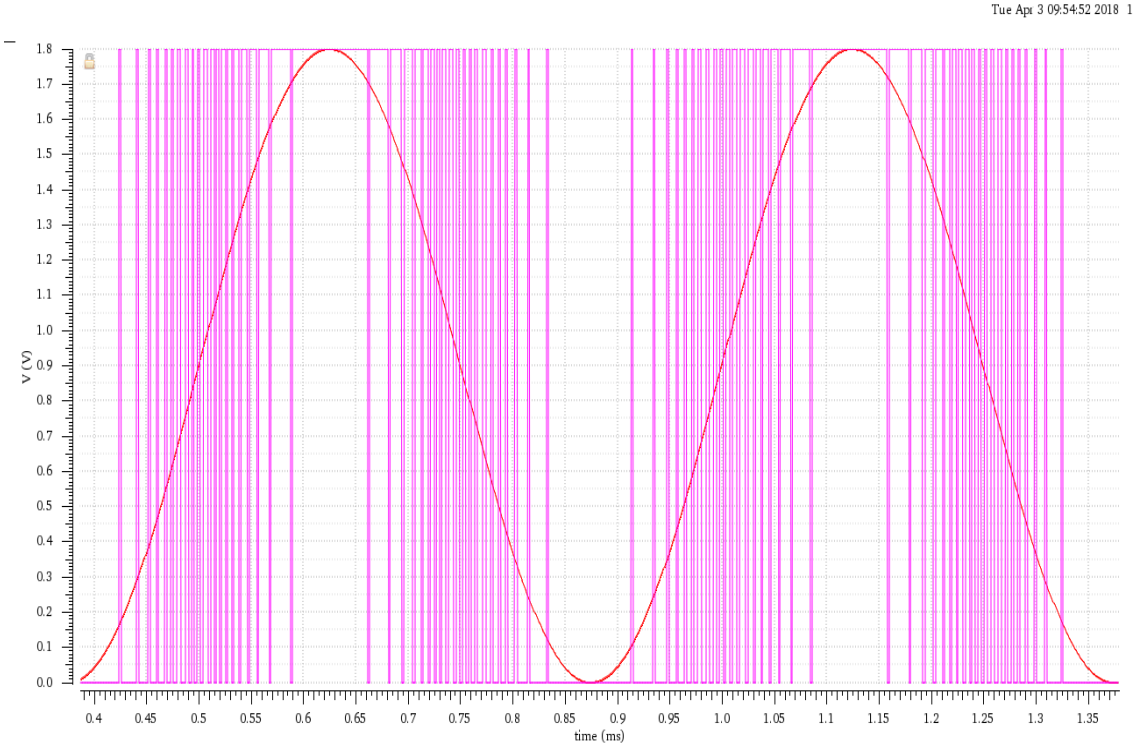

Figure 3.20: Pulse Density Modulated output of the implemented DSM

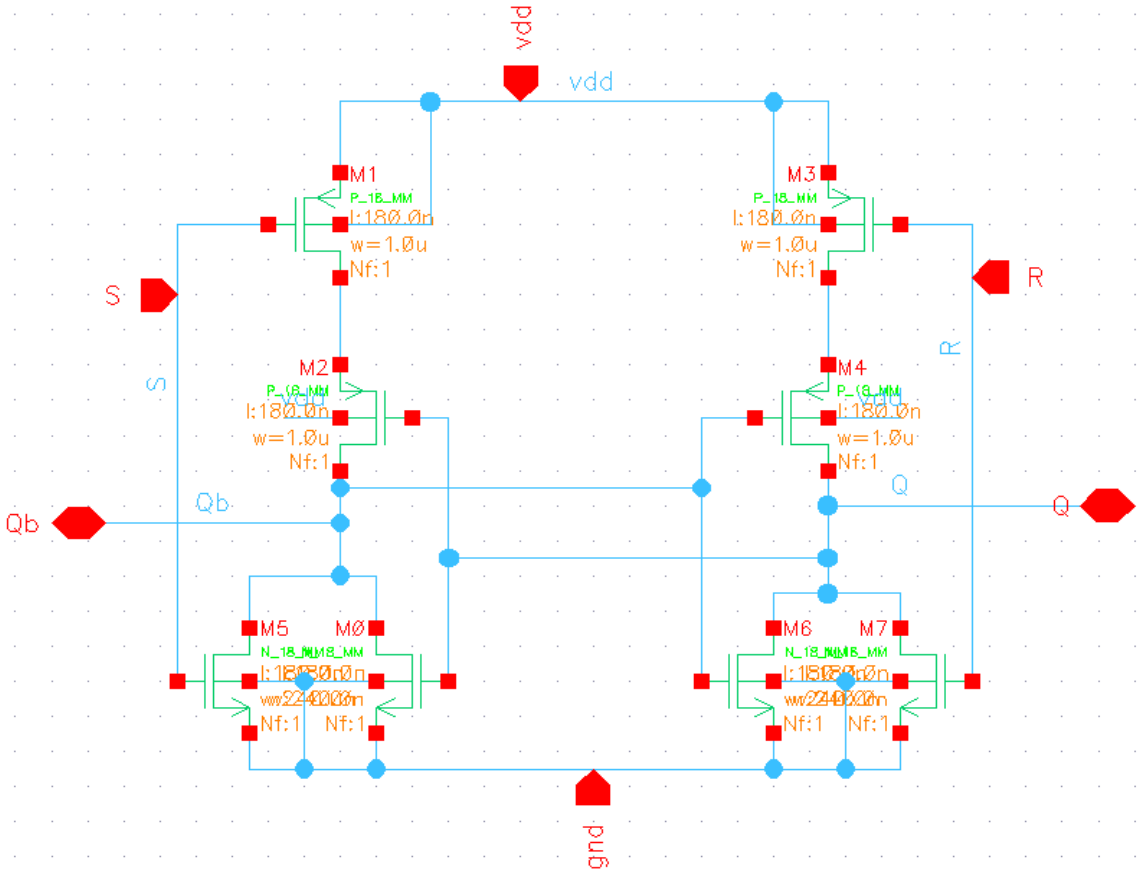

Figure 3.19: Schematic of the SR latch implemented

The FFT of the PDM output was plotted using MATLAB, to observe the noise shaping. (Figure 3.21)

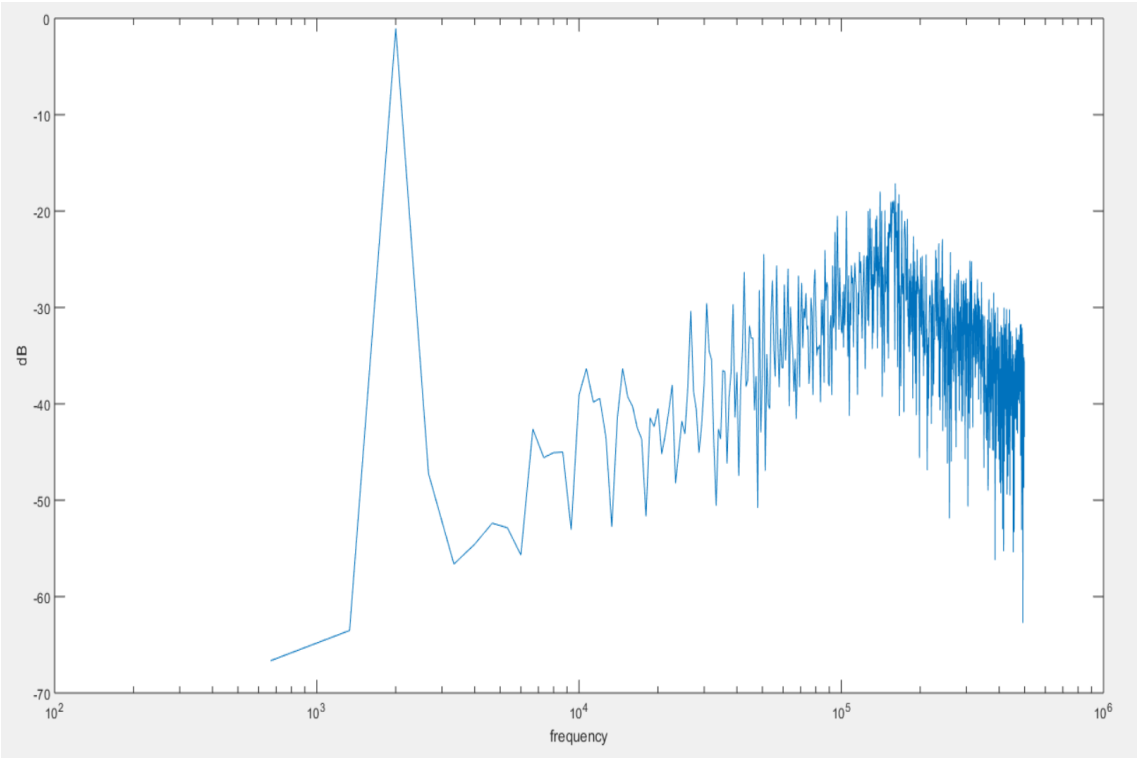

Figure 3.21: Noise-shaped spectrum of the DSM output

By setting the input bandwidth as 2kHz, in the code, the SNR was found to be 60.7dB for the DSM circuit with MOSFET switches and FC OTA. Hence the Effective Number Of Bits of the implemented DSM is,

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} = 9.7\ bits$$

By setting the input bandwidth as 4kHz, in the code, the SNR was found to be 45dB for the DSM circuit with MOSFET switches and FC OTA. Hence the Effective Number Of Bits of the implemented DSM is,

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} = 7.1\ bits$$

Similarly, the SNR and ENOB values were calculated, by replacing the ideal SR latch in the circuit, by a nor gate based latch (Figure 3.19) and are tabulated in Table 3.5. Also, SNR was calculated by varying the filter bandwidth at the output to 2 kHz (input signal frequency) and 4 kHz.

OTA Type	Filter BW	SR latch	Switches	SNR (dB)	ENOB (bits)
2 stage	4kHz	ideal	non-ideal	45.82	7.3
2 stage	2kHz	ideal	non-ideal	57.66	9.2
2 stage	4kHz	non-ideal	non-ideal	40.4	6.4
2 stage	2kHz	non-ideal	non-ideal	45.4	7.2
3 stage	4kHz	ideal	non-ideal	44.92	7.2
3 stage	2kHz	ideal	non-ideal	60.74	9.7
3 stage	4kHz	non-ideal	non-ideal	37.23	6
3 stage	2kHz	non-ideal	non-ideal	45.05	7.2

Table 3.5: SNR and ENOB values

CHAPTER 4

Conclusion

The first order Delta Sigma Modulator was first implemented using ideal circuit elements and later replaced with MOSFET based switches and latches. It was observed that the SNR values dropped considerably for circuits with higher order OTA stages, which might have possibly occurred because of loading from the next stages. Further work has to be done in eliminating all the possible errors that can be caused due to parasitics and loading of the circuit. The highest bit count achieved was 9.7 bits for a 10-bit-ADC, but with a sharp brick-wall type filter bandwidth at the output, which was equal to the input frequency. Further work has to be done to make the circuit achieve such a high ENOB with all ideal circuit elements replaced by real MOSFET switches.
This project helped in understanding the basics of how delta sigma converters work and the role of each stage in the conversion process.

4.1 Future Scope

- Perform PVT corner analysis for the first order DSM.
- Build a reconstruction circuit that performs decimation and filtering of the output signal of the DSM.
- Validate the design with post layout simulations.
- Work on building higher order circuits to improve noise shaping and the Signal to Noise Ratio.

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[3] Michiel van Elzakker, Ed van Tuijl, Paul Geraedts, Danil Schinkel, Eric A. M. Klumperink and Bram Nauta, "A 10-bit Charge-Redistribution ADC Consuming,1.9 uW at 1 MS/s", IEEE Journal of Solid State Circuits, Vol 45, No.5, May 2010

[4] Jos M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 58, No. 1, January 2011

[5] Shanthi Pavan, Richard Schreier, Gabor C. Temes, "Understanding Delta Sigma Converters", IEEE Press Series on Microelectronic Systems, Second Edition, March 2017