**ECE 3544: Digital Design I**
**Project 3 (Part A) – Design and Synthesis of a Parity-Checking System**

Student Name: Sefunmi Ashiru

Honor Code Pledge: I have neither given nor received unauthorized assistance on this assignment.

Sefunmi Ashiru

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**Grading: The design project will be graded on a 100 point basis, as shown below:**

*Manner of Presentation (30 points)*

_____ Completed cover sheet included with report (5 points)

_____ Organization: Clear, concise presentation of content; Use of appropriate, well-organized sections (15 points)

_____ Mechanics: Spelling and grammar (10 points)

*Technical Merit (70 points)*

_____ General discussion: *Did you describe the objectives in your own words? Did you discuss your conclusions and the lessons you learned from the assignment?* (5 points)

_____ Design discussion: *Did you discuss the approach you took to designing any original modules? Did you discuss the approach you took to assembling the top-level module?* (10 points)

_____ Testing discussion: *What was your approach to formulating your test benches? How did you verify the correctness of the modules you designed?* (5 points)

_____ Supporting figures: *Waveforms showing correct operation of the top-level module.* (10 points)

_____ Supporting files: *Do the modules pass any tests applied by the grading staff? Modules whose declarations do not conform to the requirements of the project specification cannot be tested, and will receive no credit.* (15 points)

_____ Validation of the final design on the DE1-SOC board (25 points): ***Modules that exhibit the correct behavior but do not represent the correct implementation will receive no credit***.

_____ **Project Grade**

# Purpose

In this project, I will use Verilog and Quartus to design, test, simulate, and synthesize an error correction system. I will be using a model of 74HC/HCT 280 9-bit odd/even parity generator/checker to identify single bit errors. I must also prepare the board in advised from the required I/O pin assignments Boeing used. If not done the board could be damaged.

# Technical Approach

For my design process I utilized the structural assignment and pre-built functions to implement the block diagram of the error correction system provided. To simplify the process and reduce chance of errors I utilized only continuous and structural assignment methods for design and implementing the modules in my top-level design. As I must develop a module for 74HC/HCT 280 9-bit odd/even parity generator/checker in project 2, I initiated multiple versions of the modules to represent my transmitted and received parity check values. For my bit corrupter I used combinational logic with continuous assignment to act as a transformer from the input_word to a corrupted output word.

# Results

## Testbench

The waveforms from testbench can be found in the Appendix 1

When designing the test for my top-level module I followed a similar test from project 1 4to16 decoder. I set my input word to a constant bit stream and used a for loop to update the index given for my bit corrupter. This allowed me to check whether an error can be created and identified from all 7 bits in the data stream.

I have also provided the test results from testing individual modules such as the 74HC/HCT 280 9-bit odd/even parity generator/checker

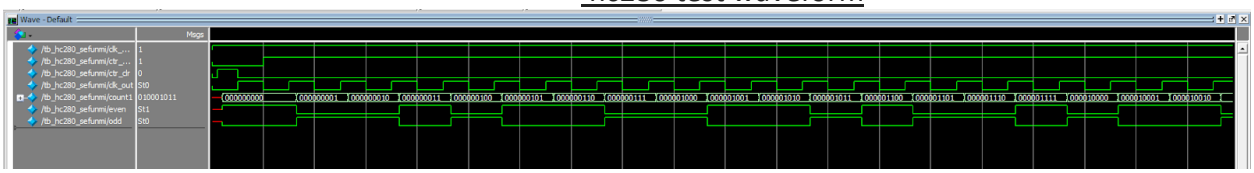
# Conclusions

In Conclusion I feel that I have learned a lot about Verilog structural & continuous design. I have also gained a lot of understanding for synchronous behaving and spotting when errors could occur due to delay values. If I were to proceed again, I would attend office hours earlier to solve issues I am unable to do on my own.

# Appendices

Appendix 1.1 - hc280 parity checker/generator

hc280 test waveform



Appendix 1.2 - Top level design testing

# Top level design testing