

Verification of a 16x16 Bit Unsigned Multiplier

Introduction

This report presents the design and implementation of a hardware-based exhaustive testbench for a 16x16 integer multiplier. The testbench has been implemented on the DE1-SoC board using System Verilog and Quartus. The goal of this project was to develop a system that would test the multiplier thoroughly and quickly, allowing for the detection of any latent errors that may have remained after the previous tests.

Design

The system consists of several modules including the multiplier under test (test_mult), the golden multiplier (gold_mult), the comparator (compare), the 16-bit up counter (count16), the progress display (progress), the status display (status), the buttons (buttons), and the state machine control (control). Each module has been defined with specific interfaces that consist of the clock, reset, control, and data ports. The schematic of the system has been created to show the connections between the modules and to make it easy to comprehend.

The progress display and the status display were implemented using seven-segment displays to indicate the system state and to display the most significant 8 bits of each multiplier operand in hex. The buttons module was implemented to provide debounced reset_n, begin_test, and inject_error signals. The state machine control module was designed to examine the status signals from all other modules and drive the control inputs to all other modules.

While the design and implementation of the system have been completed, the testbench has not been tested yet. The next step will be to test the system to verify its functionality and to ensure that it meets the requirements specified in the project description. If the test results are successful, the system will be demonstrated in class.

Conclusion

In conclusion, this project has provided a valuable opportunity to learn about the design and implementation of a hardware-based testbench and to gain experience with System Verilog and Quartus. The design is expected to provide significant speedup relative to simulation, allowing for exhaustive testing of the 16x16 multiplier.