CSCI 350
Chapter 4
Register Transfer Examples

These examples will show what happens at various steps in the instruction cycle. Note, the expectation is that for all operations except FETCH, after the last step of that operation completes, one will go to step 0 of FETCH.

FETCH:
0. PC = [PC]+1; fetch

POP:
1. MAR, SP = [SP]-1; read
2. wait for read to complete
3. TOS = [MDR]

IADD:
1. MAR,SP = [SP]-1; read
2. H = [TOS]; MDR = M[MAR] at end of cycle
3. MDR, TOS = [H] + [MDR]; write

DUP:
1. MAR,SP = [SP]+1
2. MDR = [TOS]; write

ILOAD
1. H = [LV]
2. MAR = [H] + $[MBR]_U$; read
3. MAR,SP = [SP]+1;
4. PC = [PC]+1; fetch; write
5. TOS = [MDR]

GOTO:
1. OPC = [PC]-1
2. PC = [PC]+1; fetch
3. H = $[MBR]_S$ << 8
4. H = [H] OR $[MBR]_U$
5. PC = [H] + [OPC]; fetch
6. wait for fetch to complete

IFLT:
1. MAR,SP = [SP]-1; read
2. OPC = [TOS]
3. TOS = [MDR] TOS being used as temporary storage here
4. shifter = [OPC]; if (N is 1) go to T below, else go to F

T: 1. OPC = [PC]-1; go to step 2 of F below

F: 1. PC = [PC]+1
2. PC = [PC] + 1;fetch
3. wait for fetch to complete

INVOKEVIRTUAL:

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1.   PC = [PC] + 1; fetch
2.   H = [MBR]U << 8
3.   H = [H] OR [MBR]
4.   MAR = [H] + [CPP]; read
5.   OPC = [PC] + 1;
6.   PC = [MDR]; fetch
7.   PC = [PC] + 1; fetch
8.   H = [MBR]U << 8
9.   H = [H] OR [MBR]U
10.  PC = [PC] + 1; fetch
11.  TOS = [SP] - [H]
12.  MAR, TOS = [TOS] + 1
13.  PC = [PC] + 1; fetch
14.  H = [MBR]U << 8
15.  H = [H] OR [MBR]U
16.  MDR = [SP] + [H] + 1; write
17.  MAR, SP = [MDR]
18.  MDR = [OPC]; write
19.  MAR, SP = [SP] + 1
20.  MDR = [LV]; write
21.  PC = [PC] + 1; fetch
22.  LV = [TOS]
```