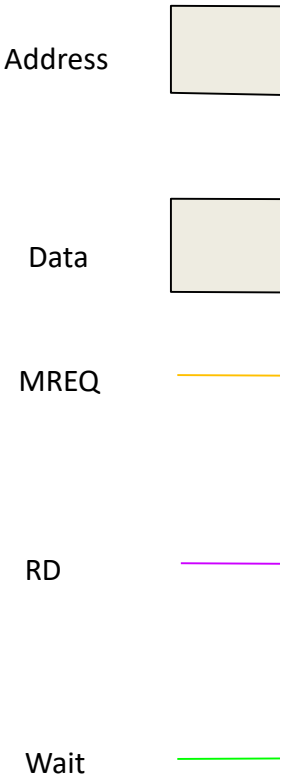
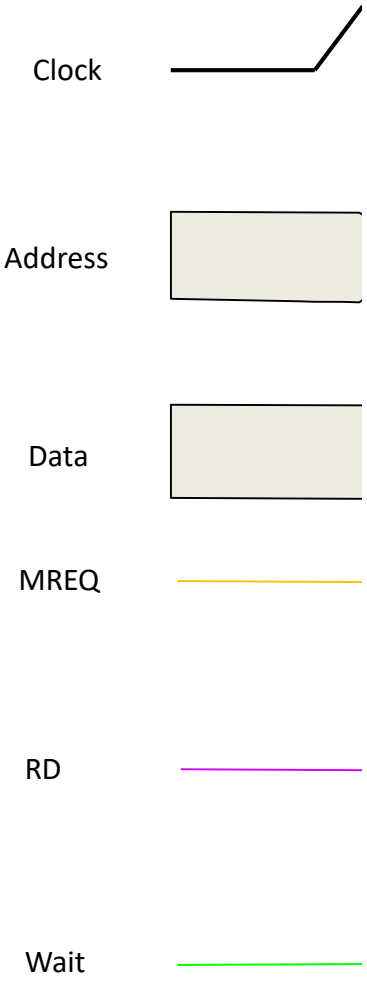
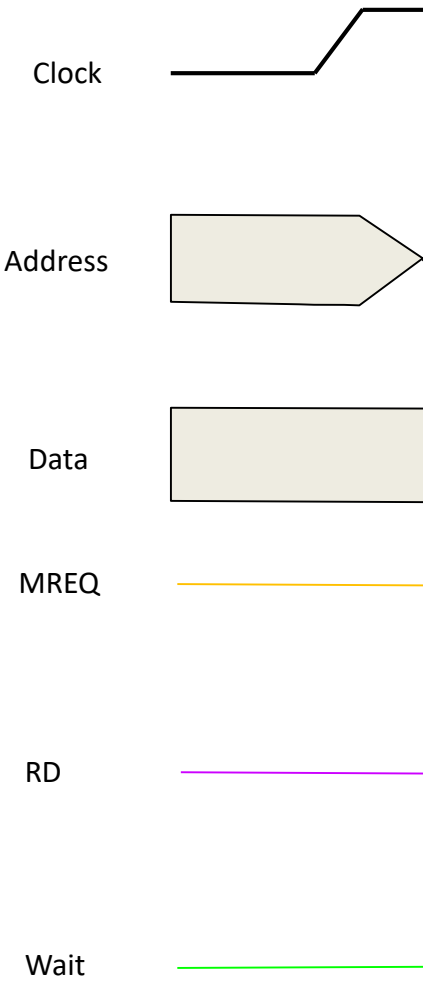
Synchronous Bus
Read Operation
Uses Wait Signal



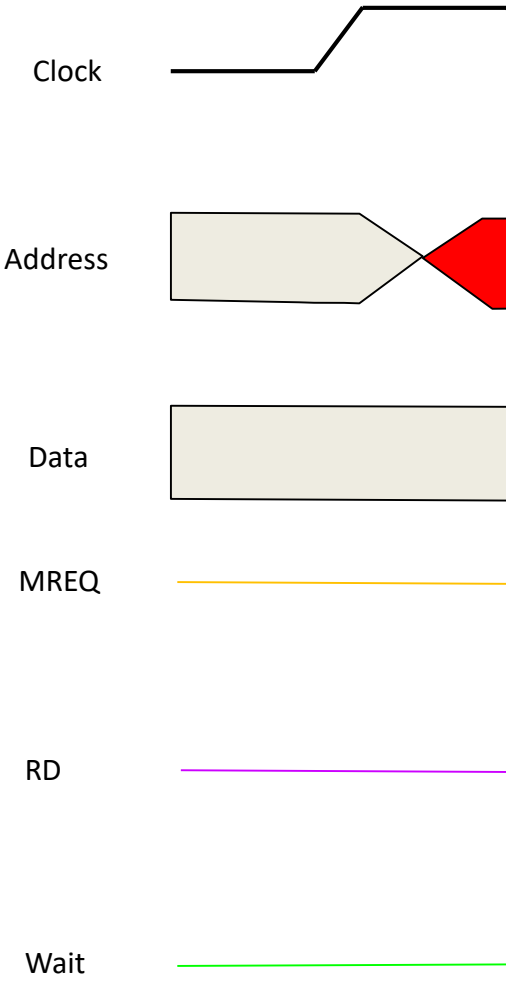
Signals in “rest” (i.e. bus inactive) state



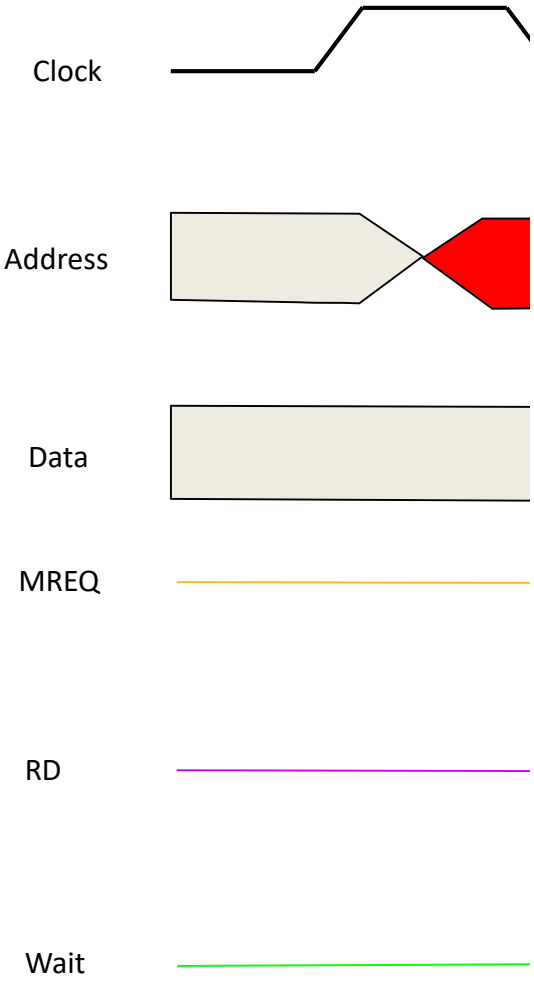
Leading edge of the next clock pulse begins



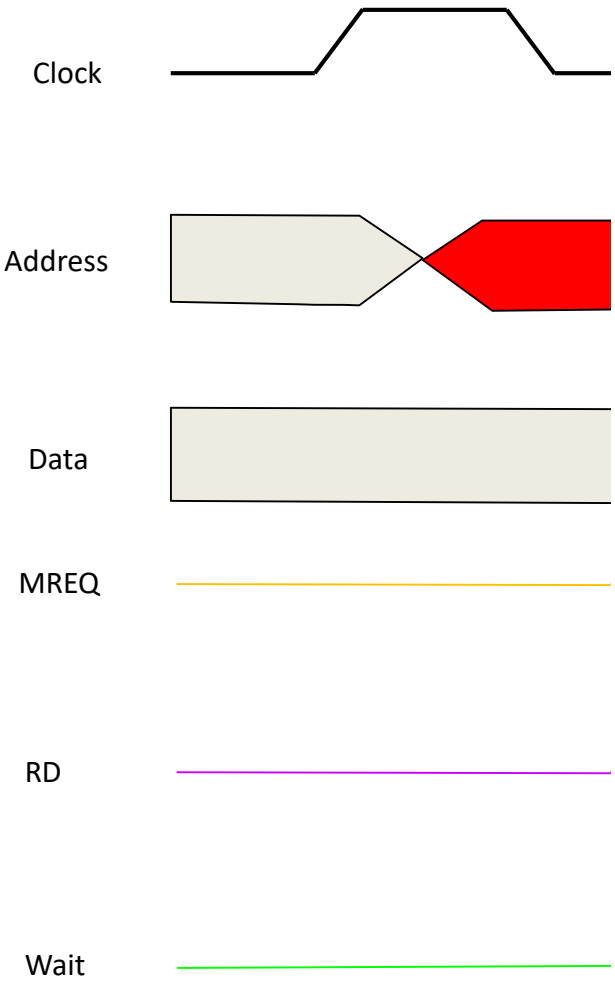
Rising edge detected, address of desired memory address being placed on the address lines



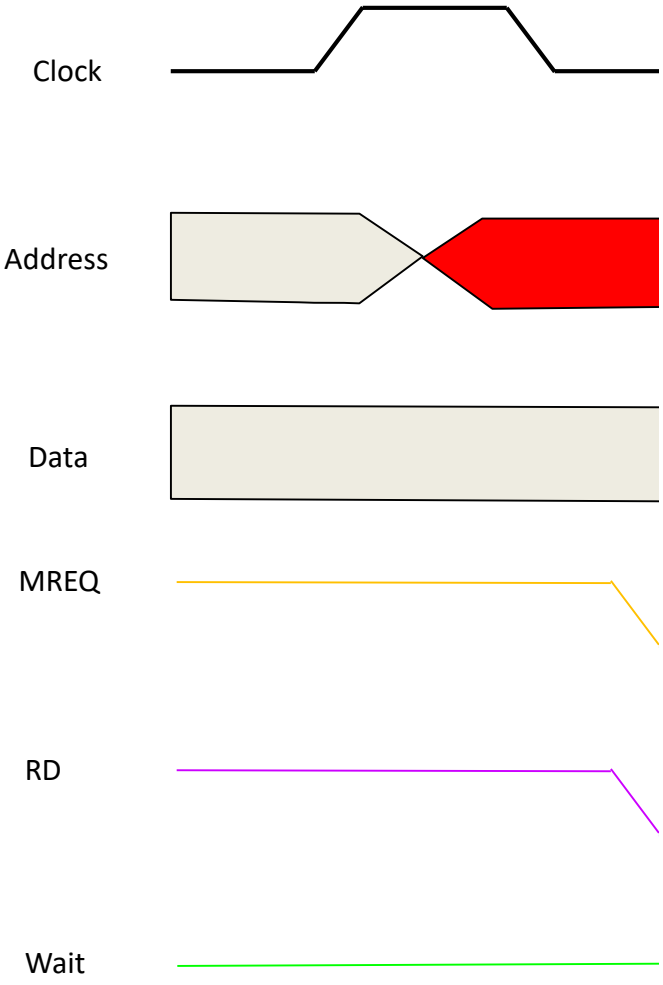
Address value more advanced in being placed on address line; falling edge of clock pulse has not yet commenced. Address must be stable within time T_{AD} of rising edge



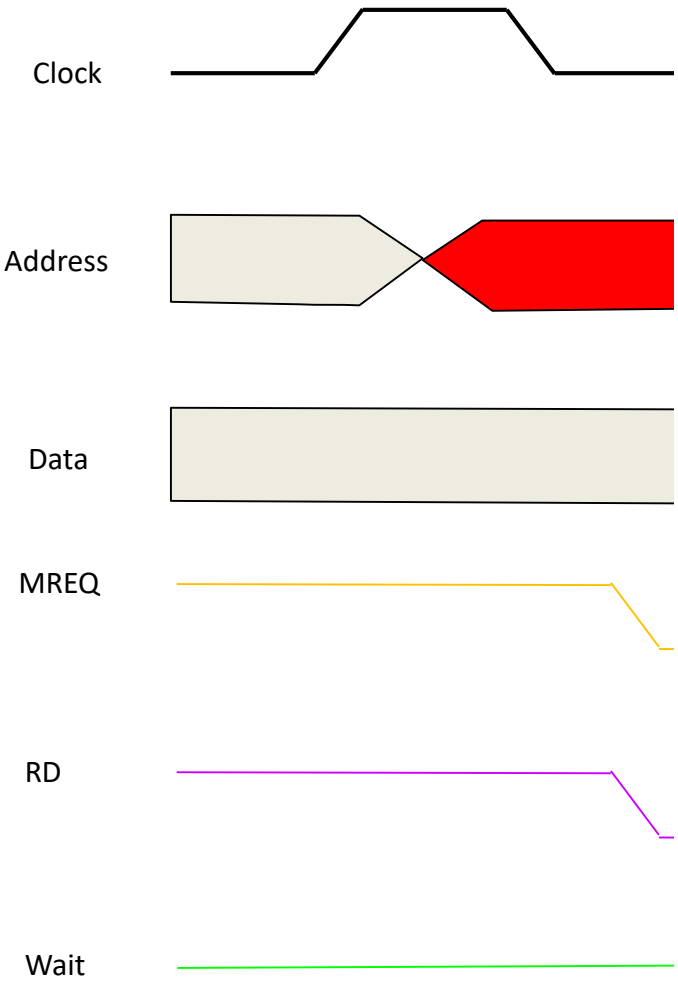
Address reached stability and now falling edge of clock pulse arrives



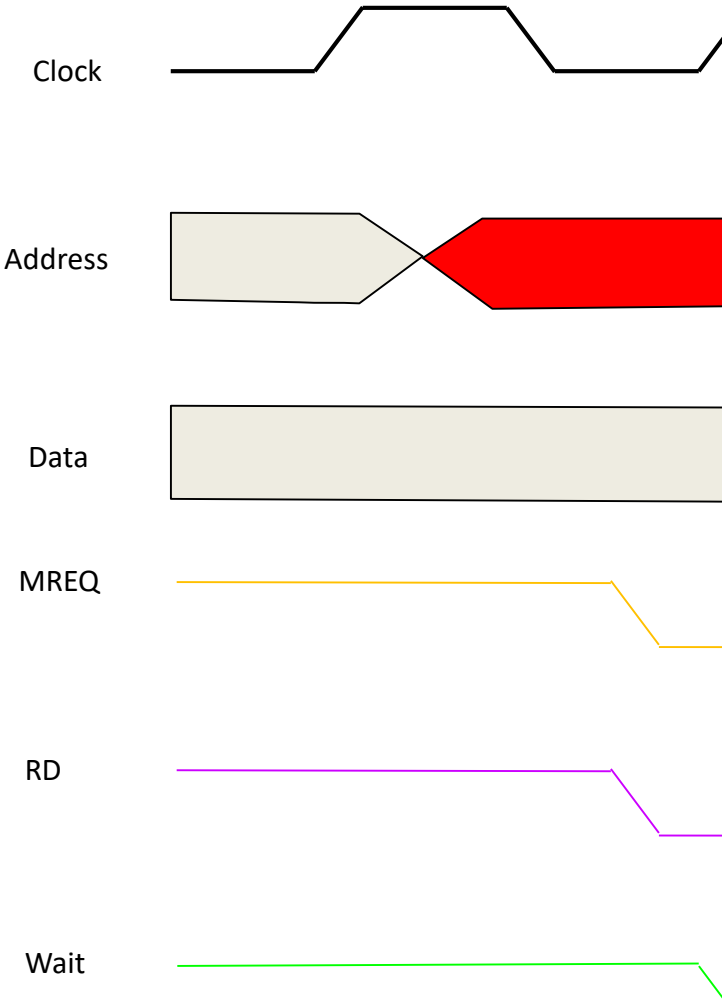
Clock pulse is completed; must wait at least times T_M and T_{RL} of falling edge before asserting the MREQ and RD signals



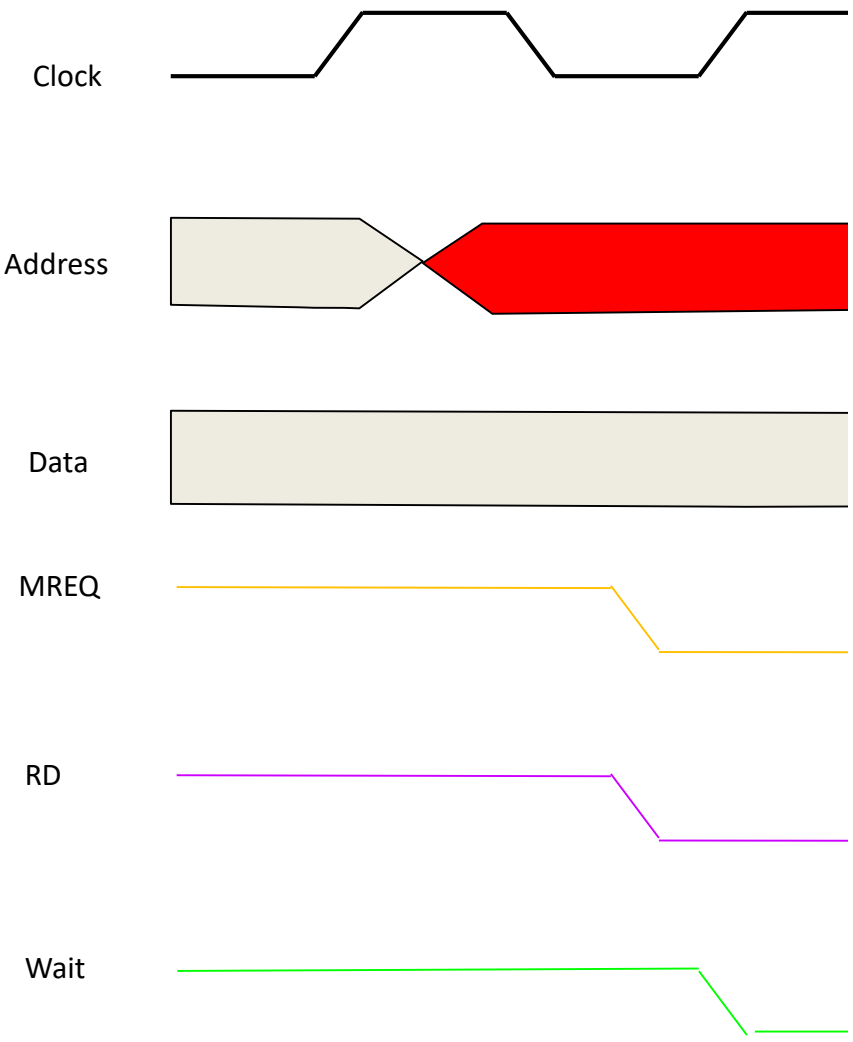
Commence asserting MREQ and RD signals to identify desired slave device and desired operation



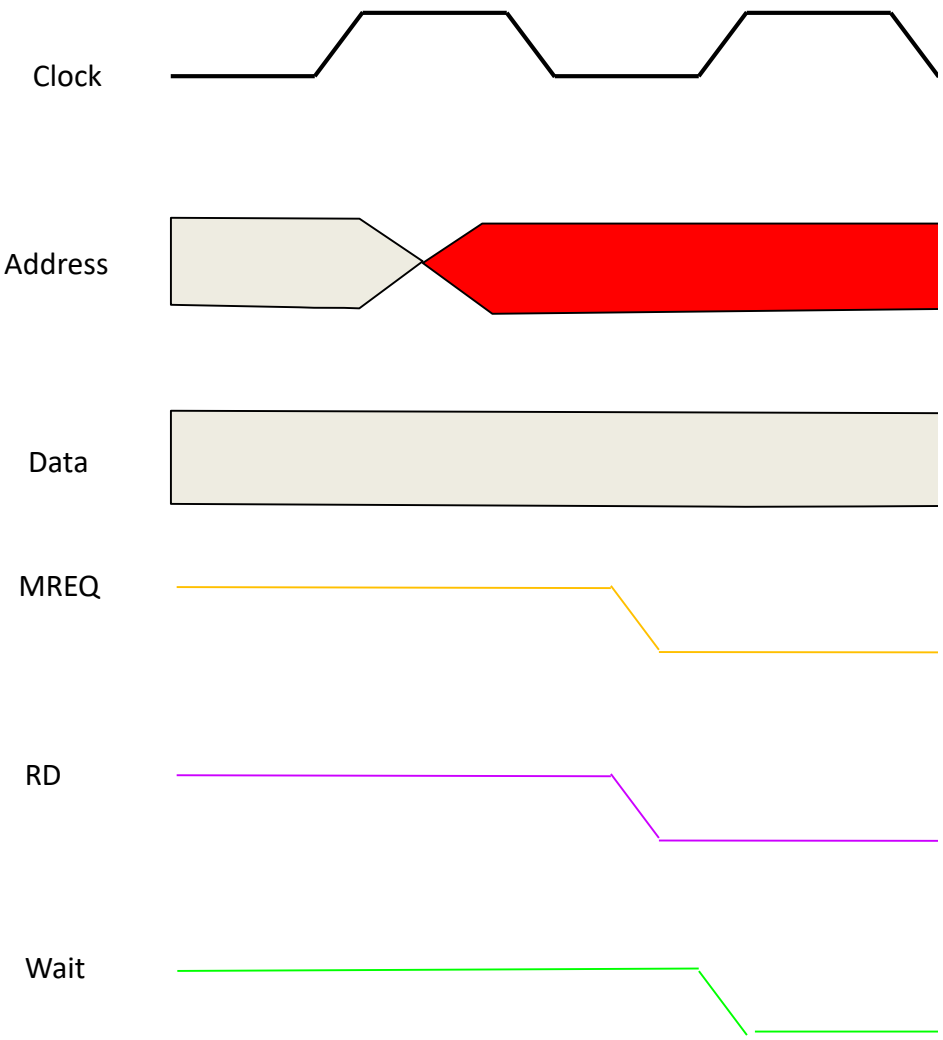
MREQ and RD signals reach desired assertion value.



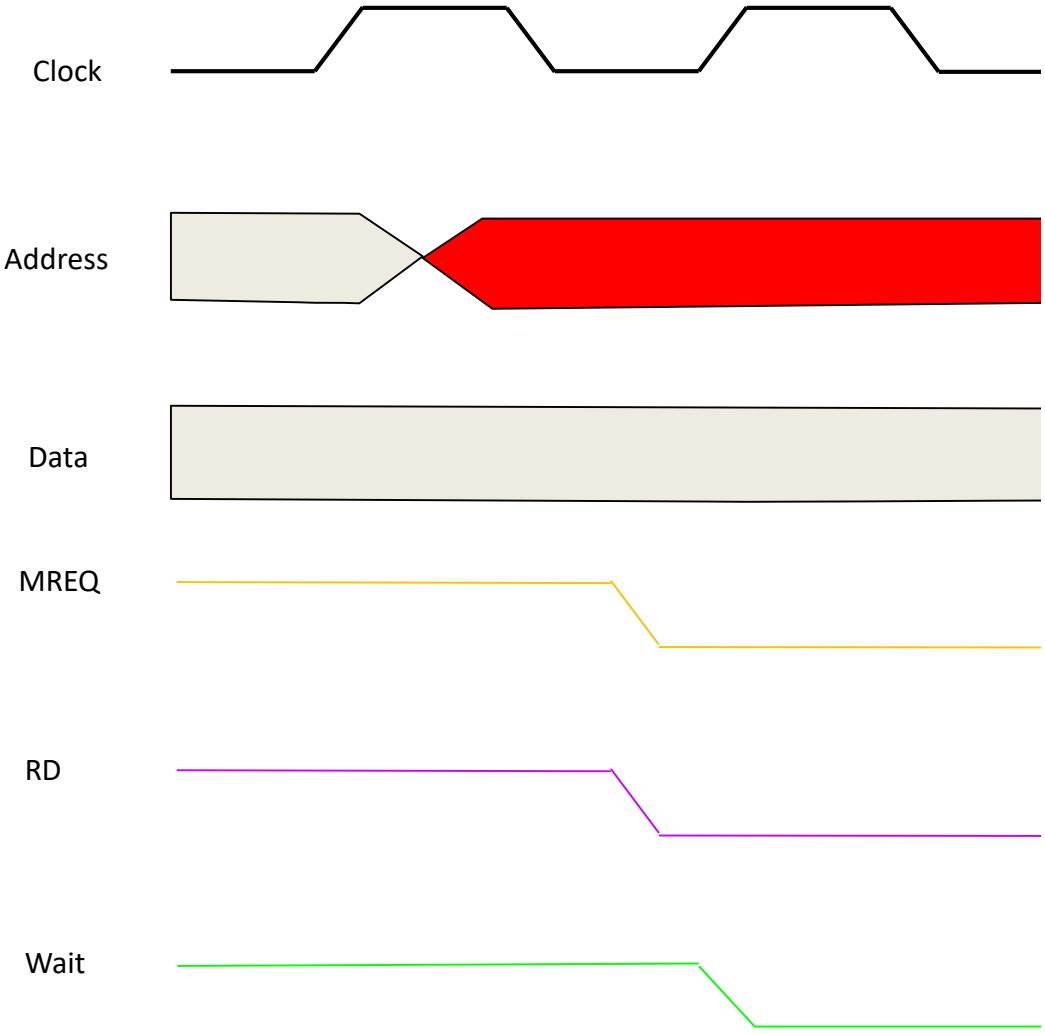
Since it is known ahead of time that the desired operation cannot be completed before the third clock pulse, at the start of the next pulse the wait line will be asserted.



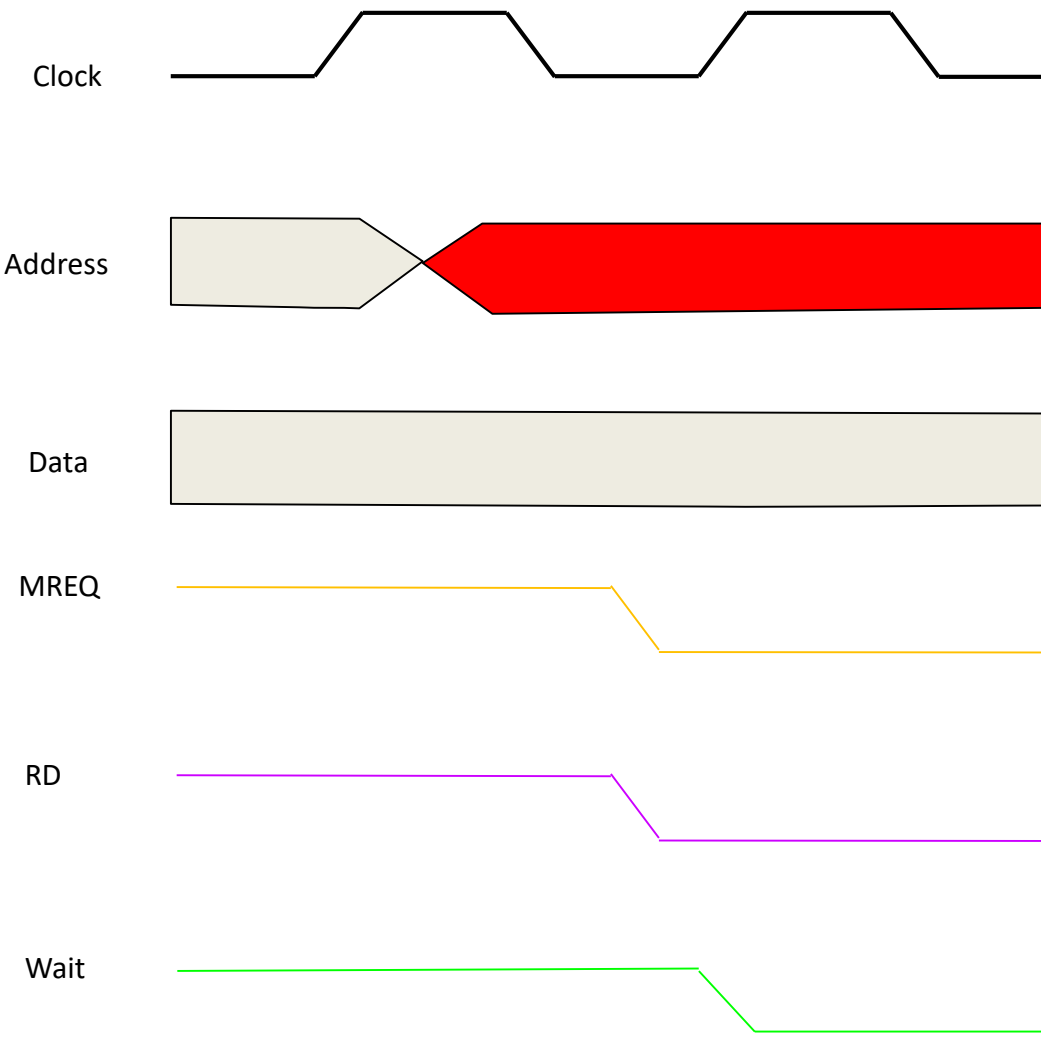
Status of the bus lines before the arrival of the falling edge of the second clock pulse



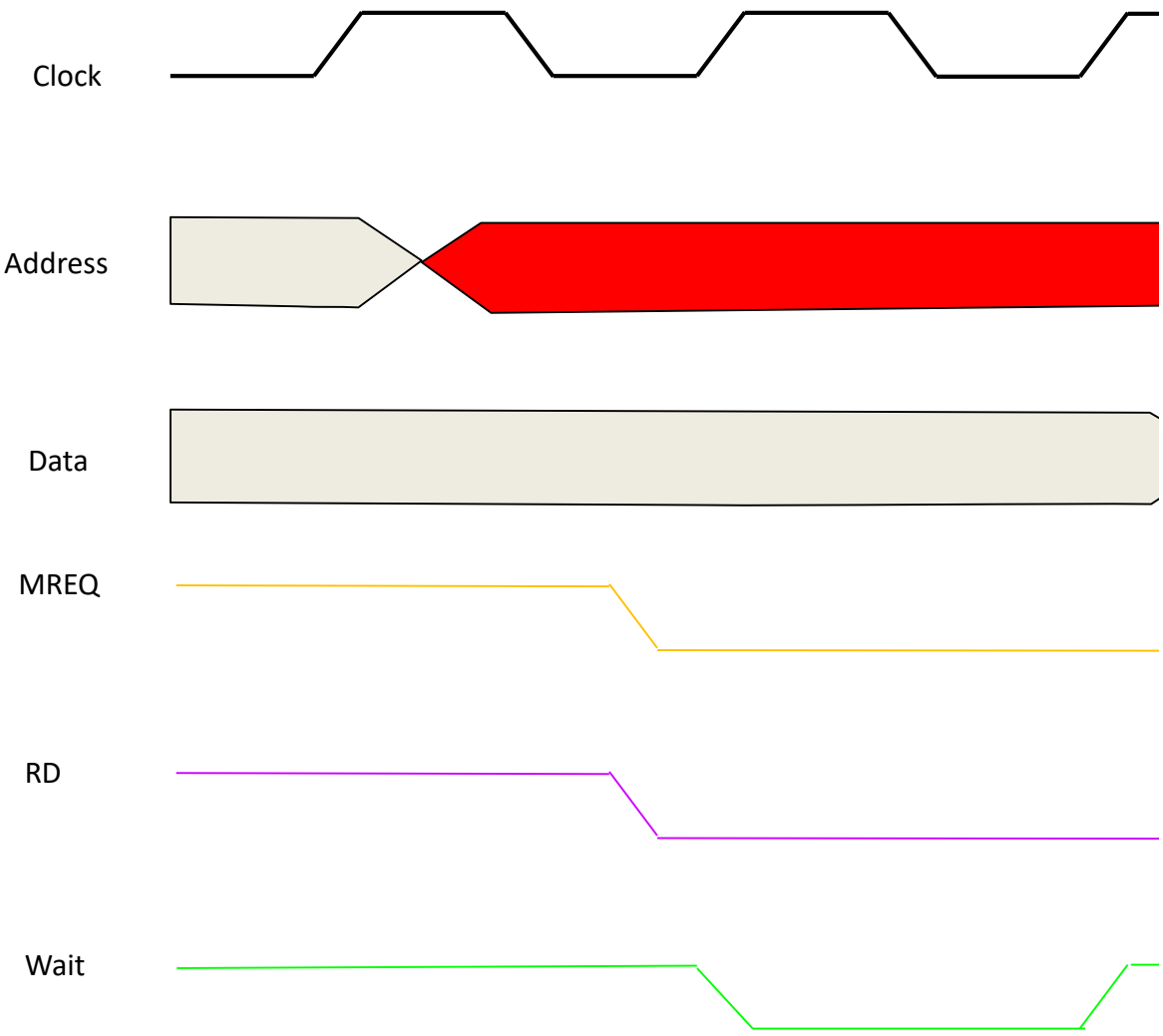
The active WAIT signal means nothing needs to be completed before the next clock pulse.

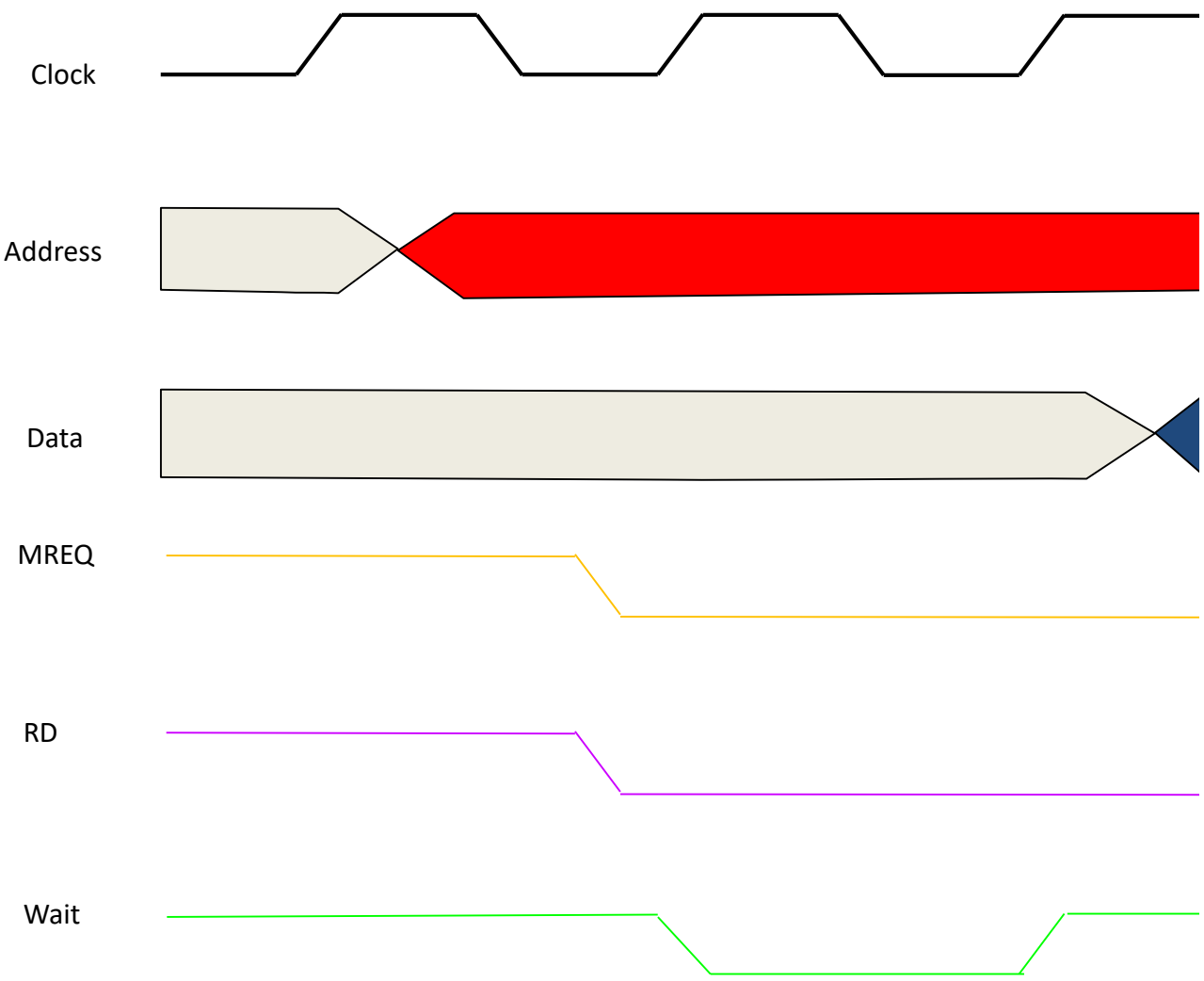


The second clock pulse ends and the system is between pulses, there is no action on the data lines.

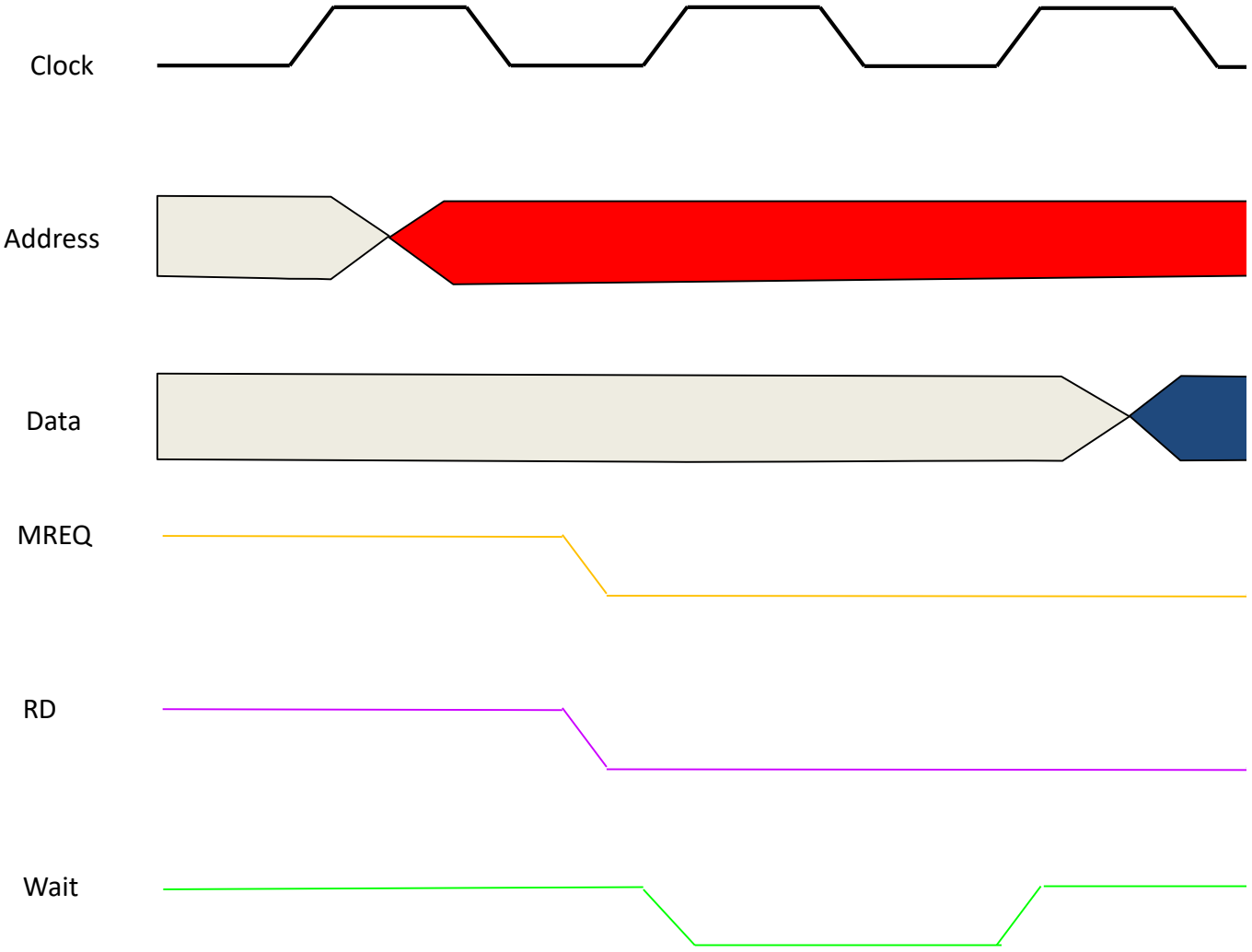


It was determined beforehand that the specifications available for the master device (cpu), slave device (memory) and the clock being used would only necessitate a wait of one additional clock pulse, so with the arrival of the next clock pulse, the WAIT signal can be returned to its unasserted value.

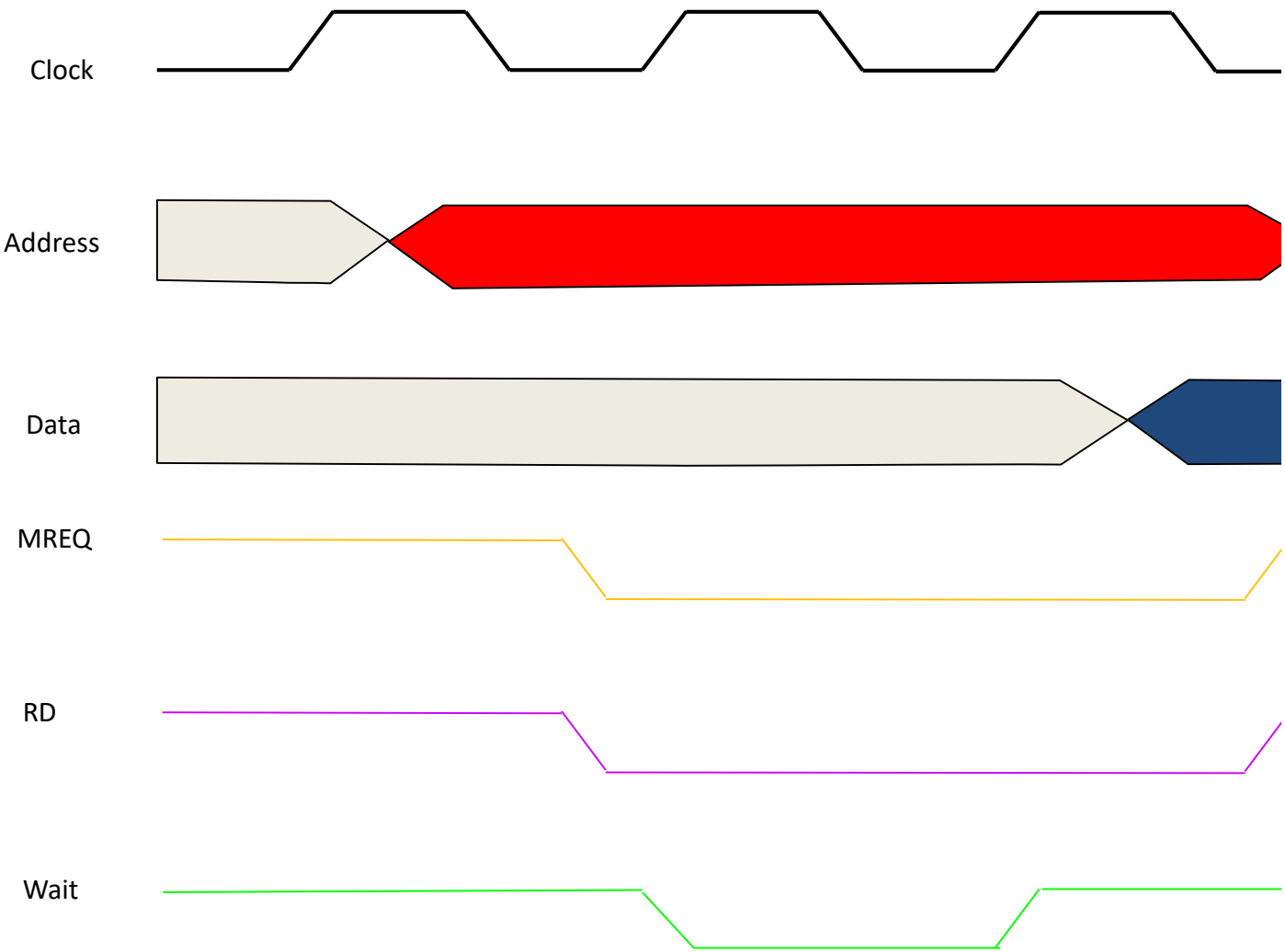

Clock
Address
Data
MREQ
RD
Wait

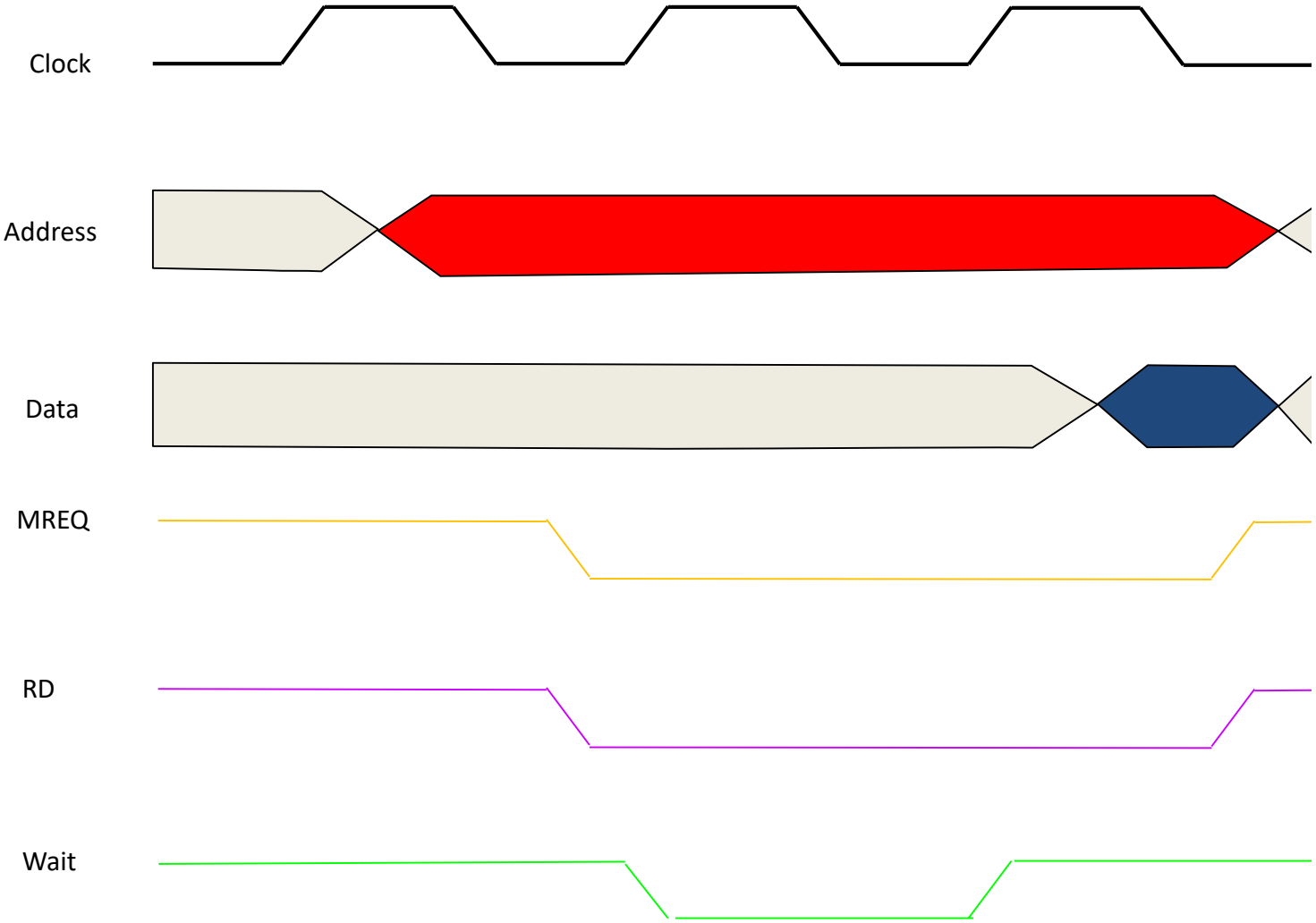


The data read from memory is appearing on the data lines of the bus. It must be completed at least by time T_{DS} before the falling edge of the current pulse, however.

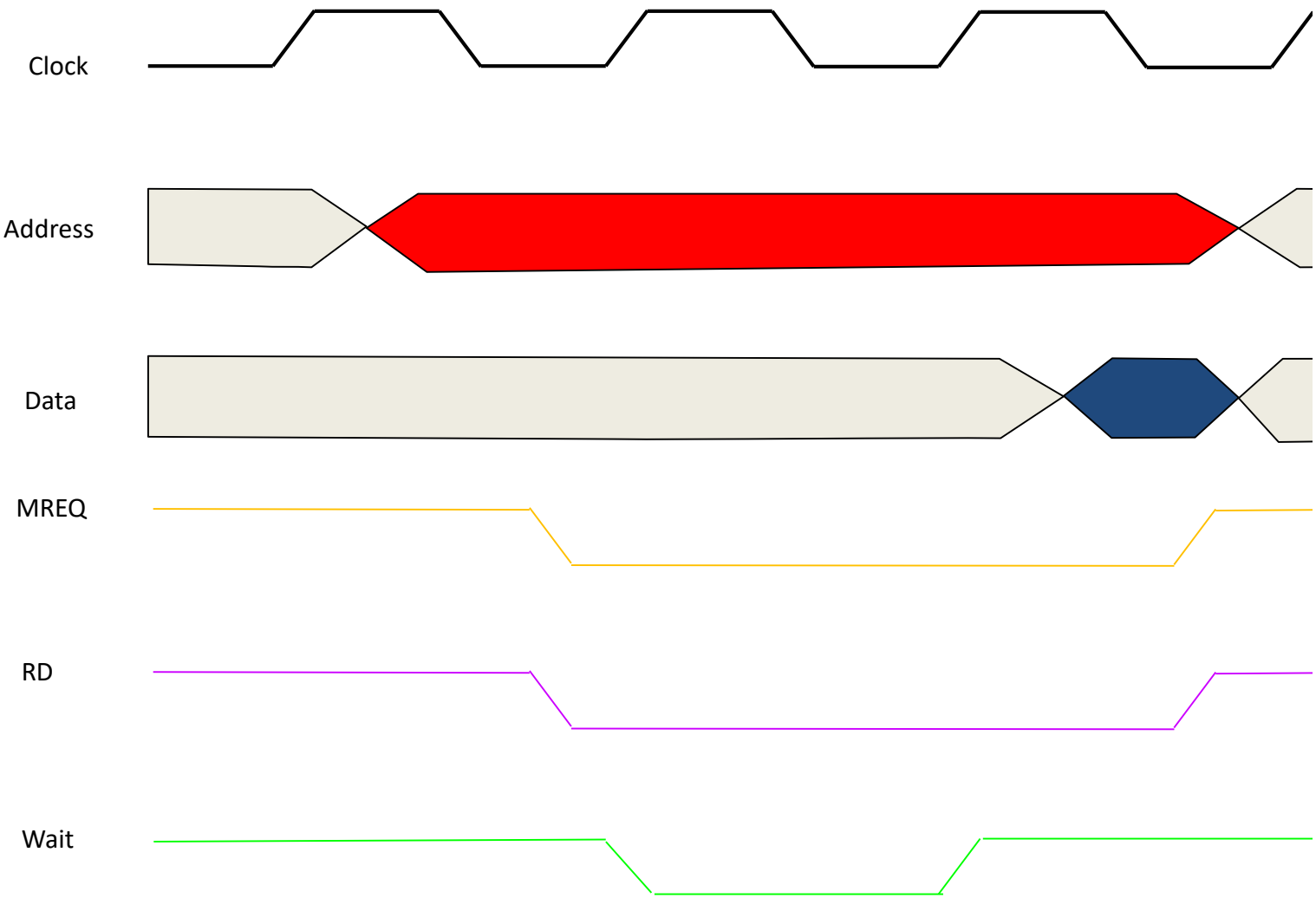


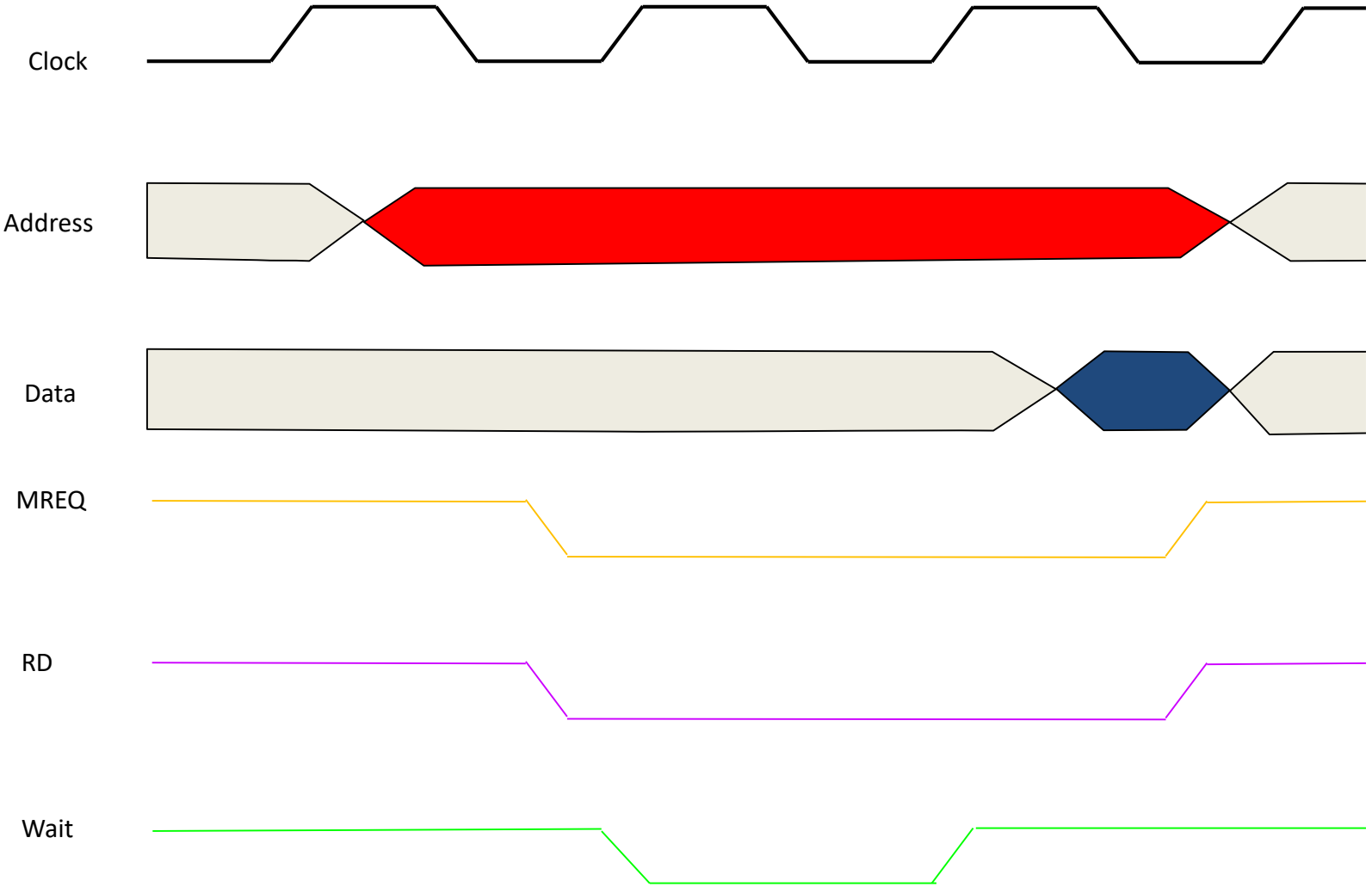
Data has reached stability and is being input by the cpu, the falling edge has arrived and we must wait for times T_{MH} and T_{RH} before we can unassert the MREQ and RD signals, respectively.


Clock
Address
Data
MREQ
RD
Wait



The memory read via the bus is complete and a new bus operation can commence with the arrival of the next clock pulse if need be. The address can data values from the just concluded operation become “old values” as far as the next bus activity is concerned.


Clock
Address
Data
MREQ
RD
Wait


Clock
Address
Data
MREQ
RD
Wait