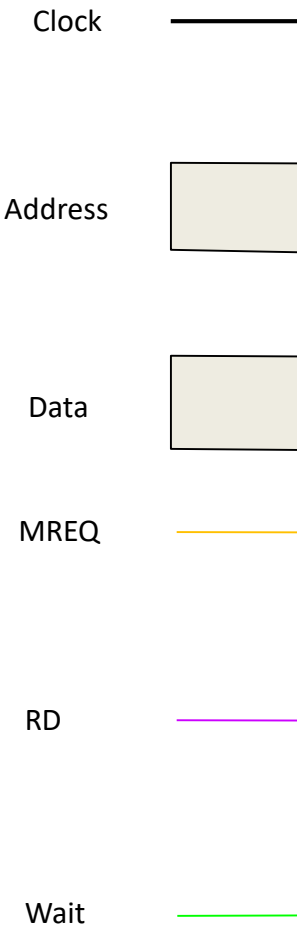
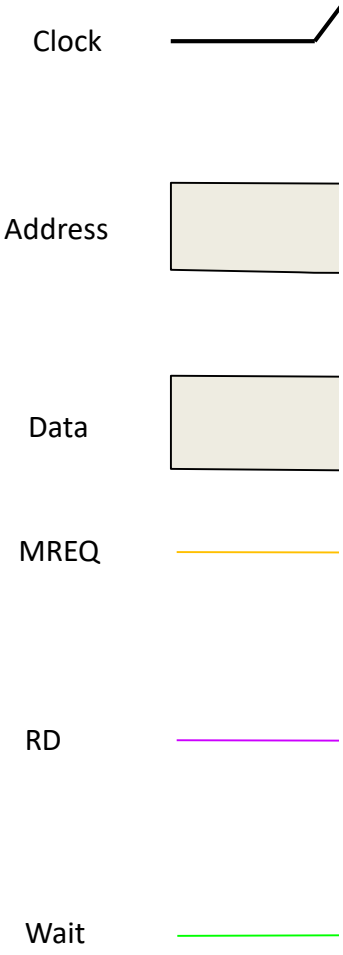
Synchronous Bus

Read Operation

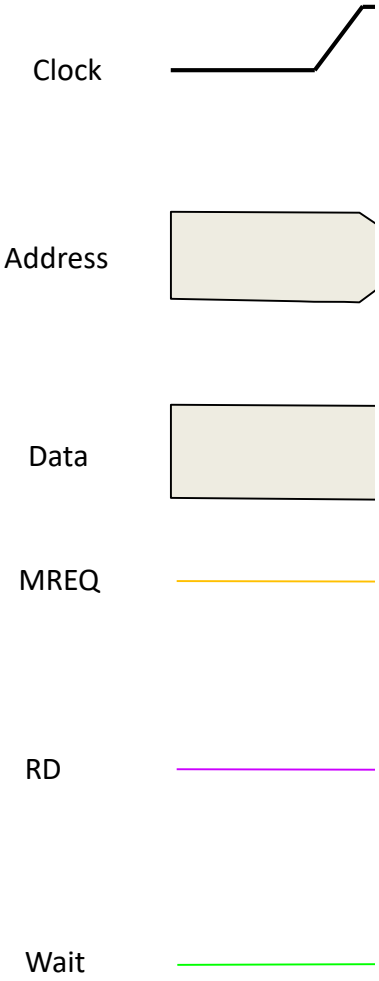
No Waiting



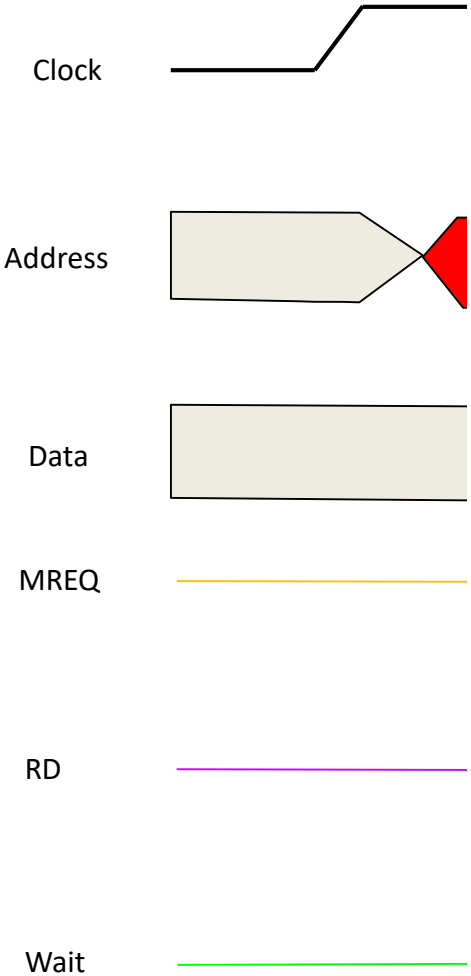

Signals in “rest” (i.e. bus inactive) state

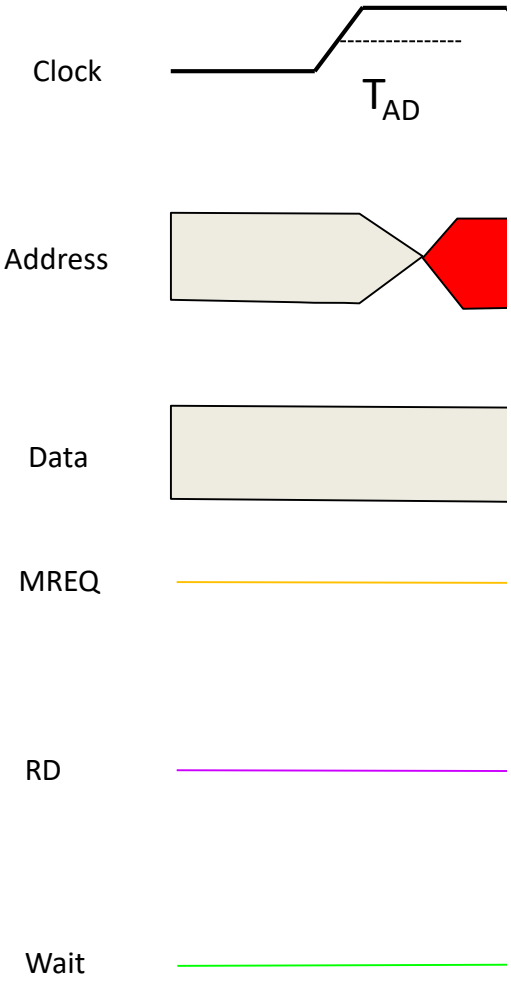



Leading edge of the next clock pulse begins the first clock cycle, T1

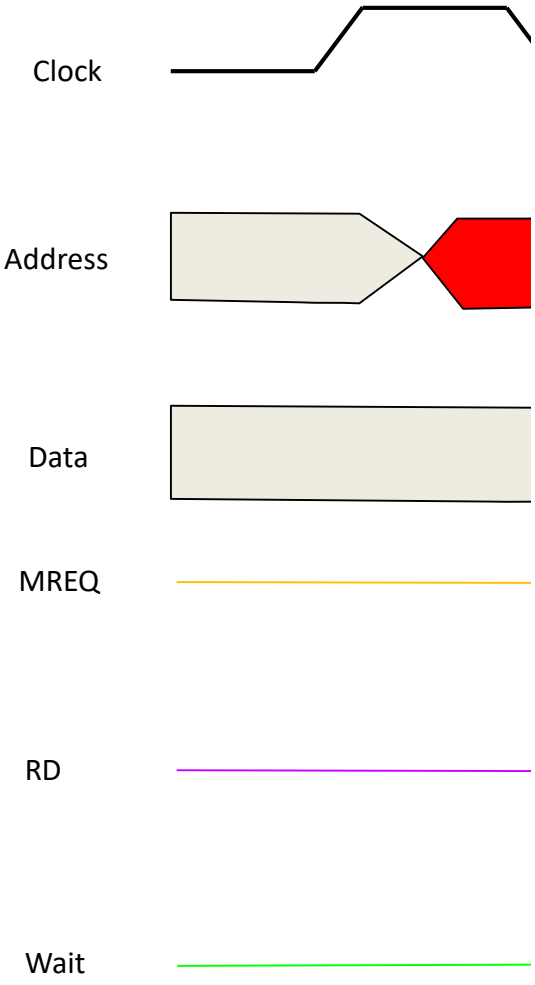



Once the rising edge is recognized, the cpu starts placing the desired memory address on the address lines.

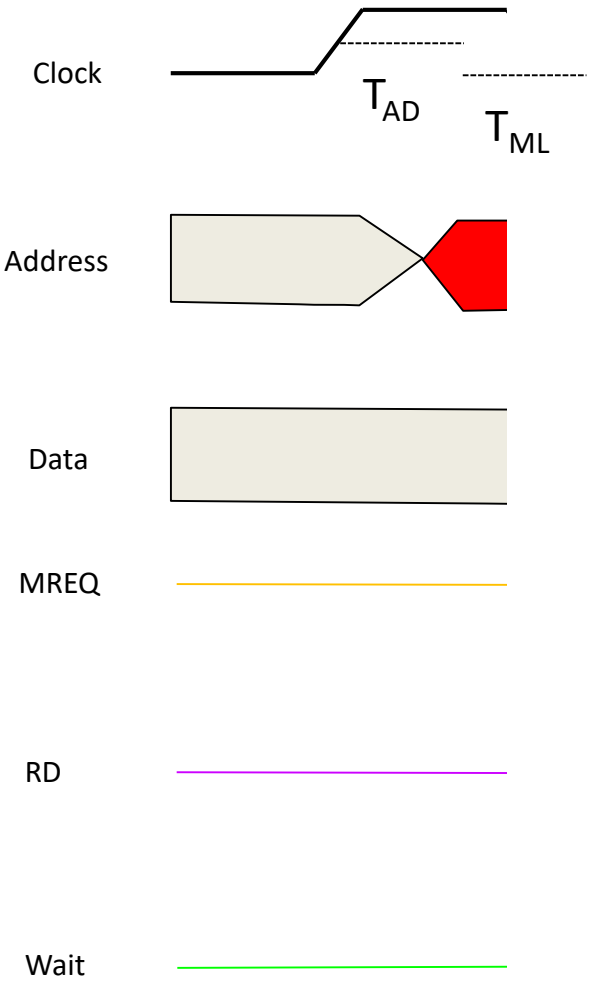

Clock
Address
Data
MREQ
RD
Wait



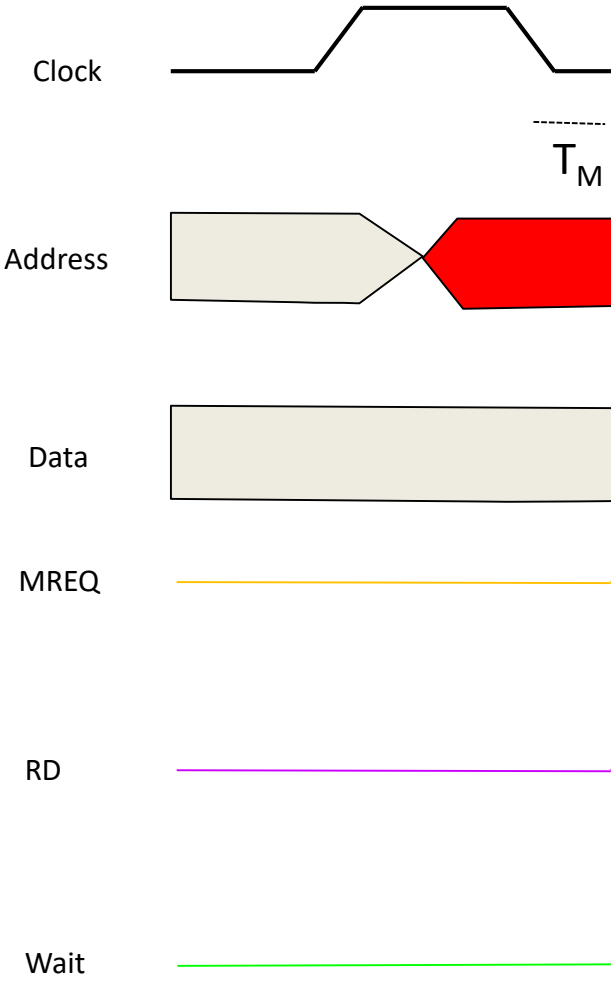

The new address must stable on the address lines within a time $T_{AD}$ from when it started being placed on these lines



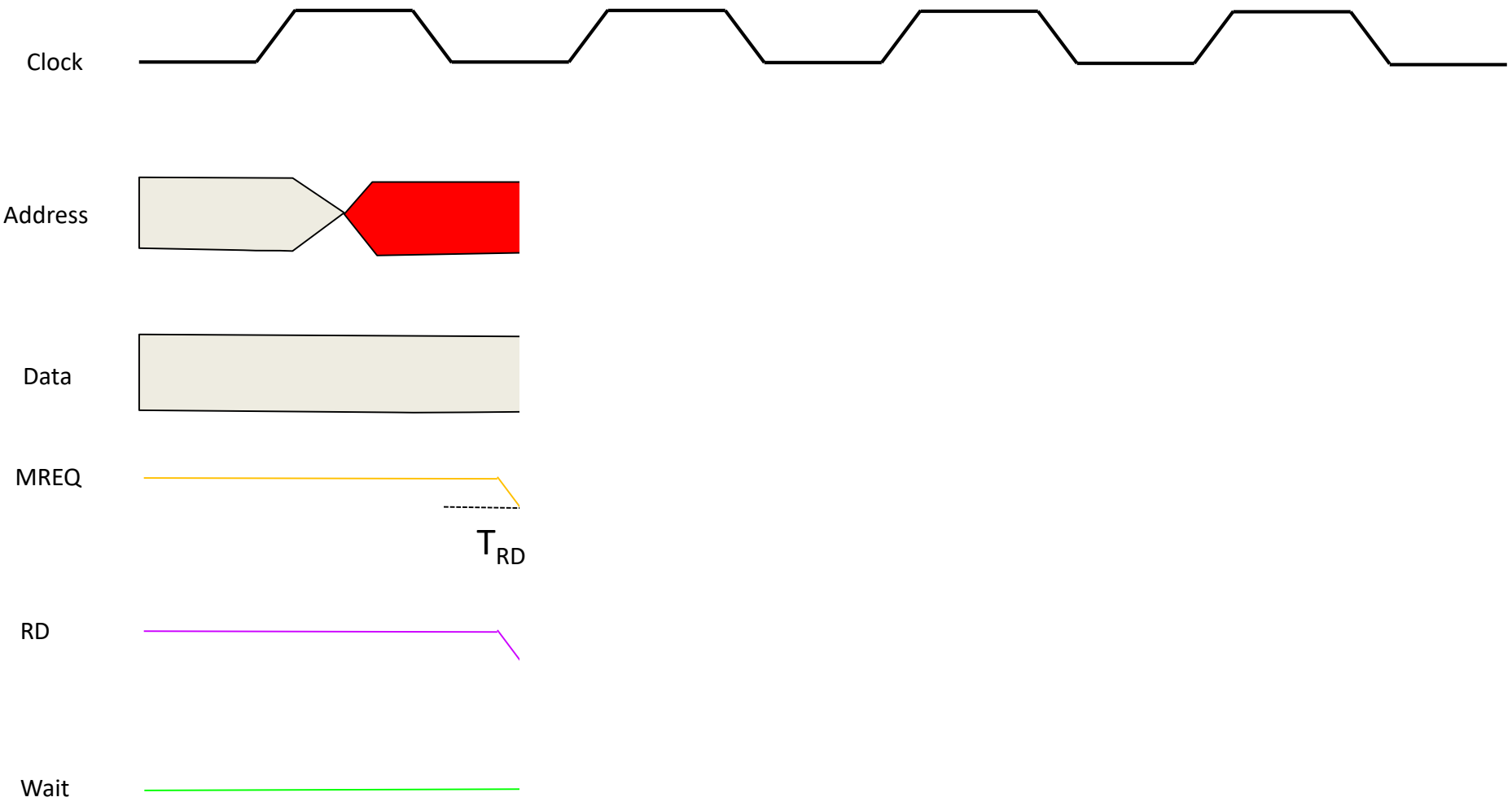

Falling edge of clock pulse begins



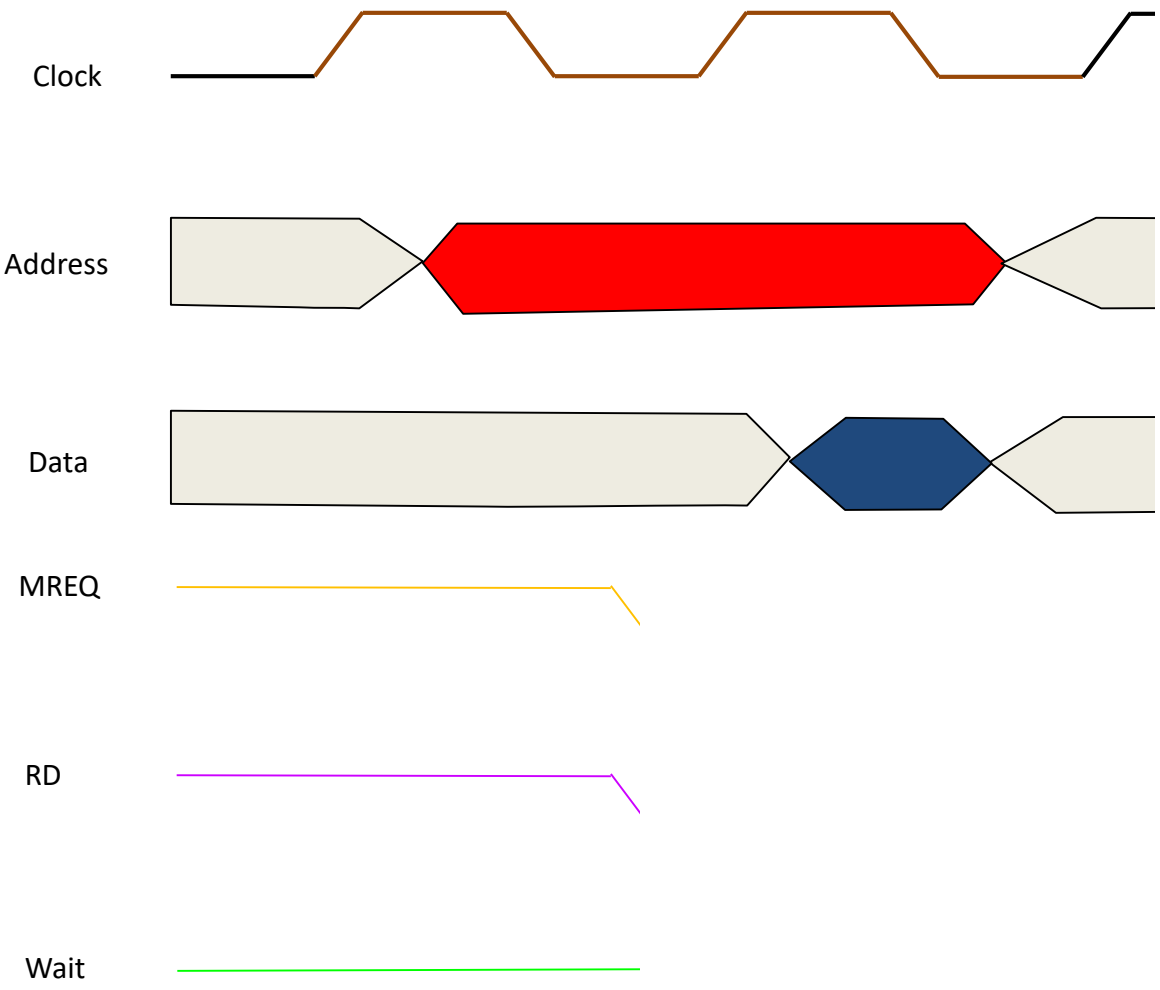

Other constraints specify that the address must be stable for at least time $T_{ML}$ before asserting the MREQ signal (here, making it low)



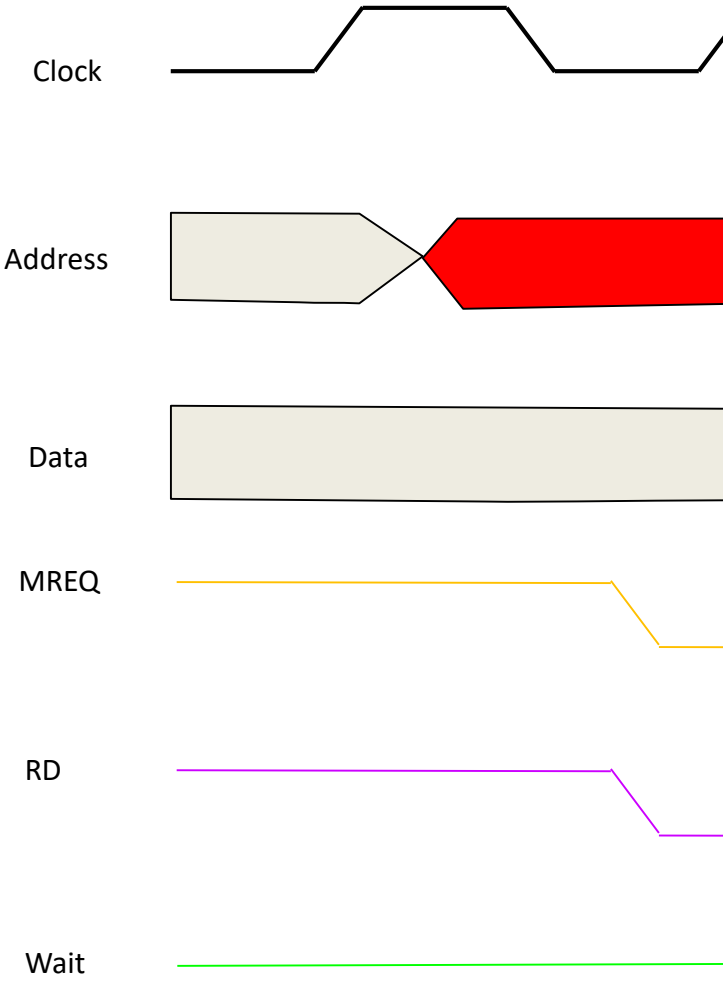

While yet another constraint says the assertion of MREQ must take place within time $T_M$ of the midpoint of the falling edge.



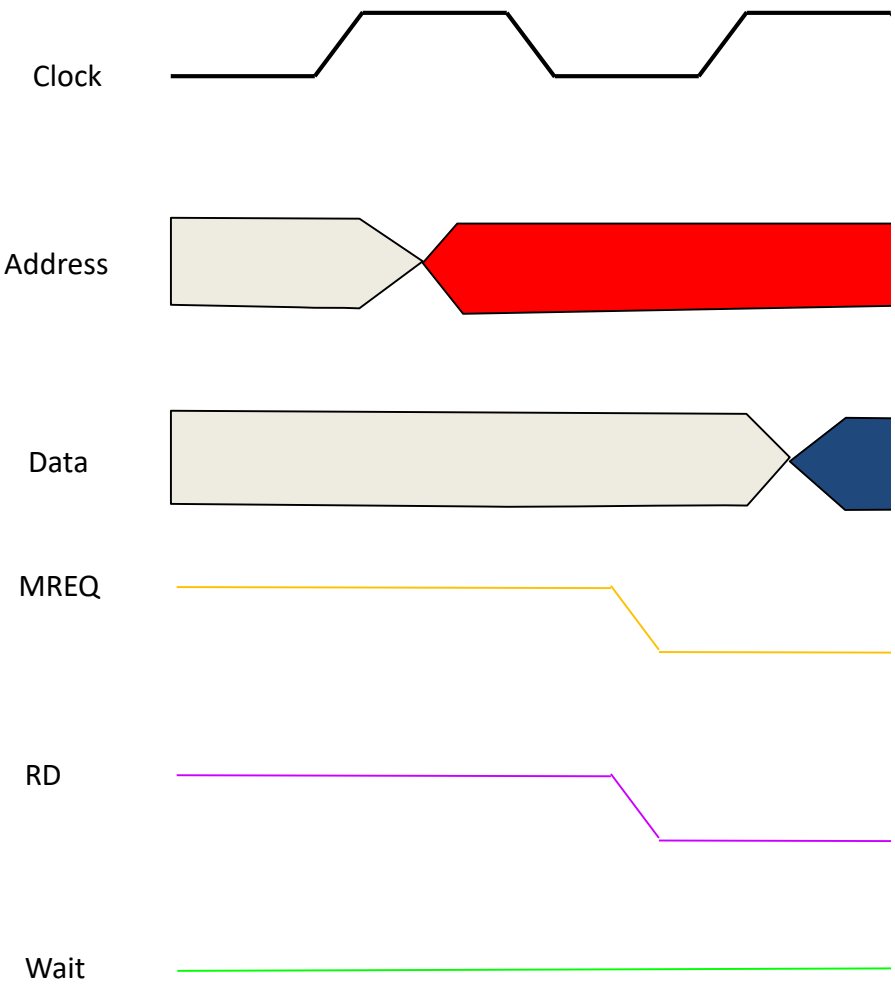

Between them $T_{ML}$ and $T_M$ determine when to commence asserting MREQ. A constraint $T_{RD}$ similar to that of $T_M$ determines the the longest we can wait before asserting RD.



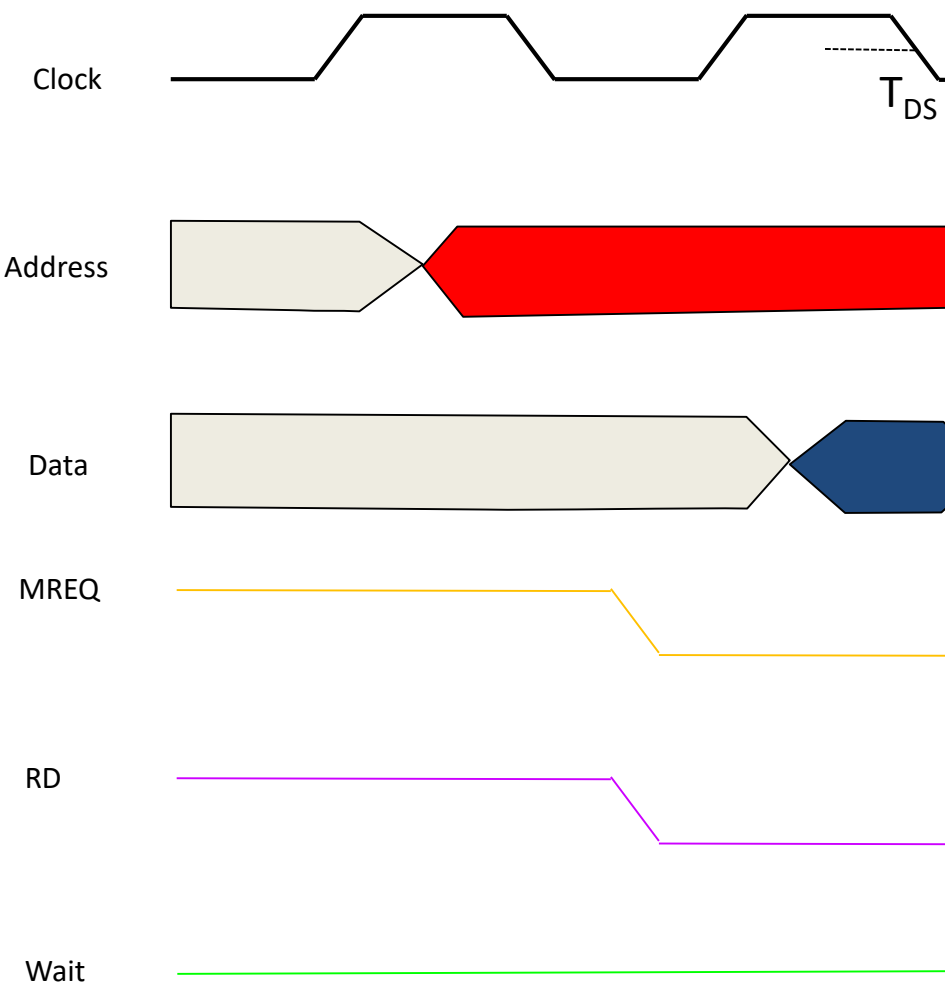

Having a “no wait” read means that we have a memory sufficiently fast that, accounting for other delay times and hold time, we are able to complete our read operation before the start of the third clock pulse



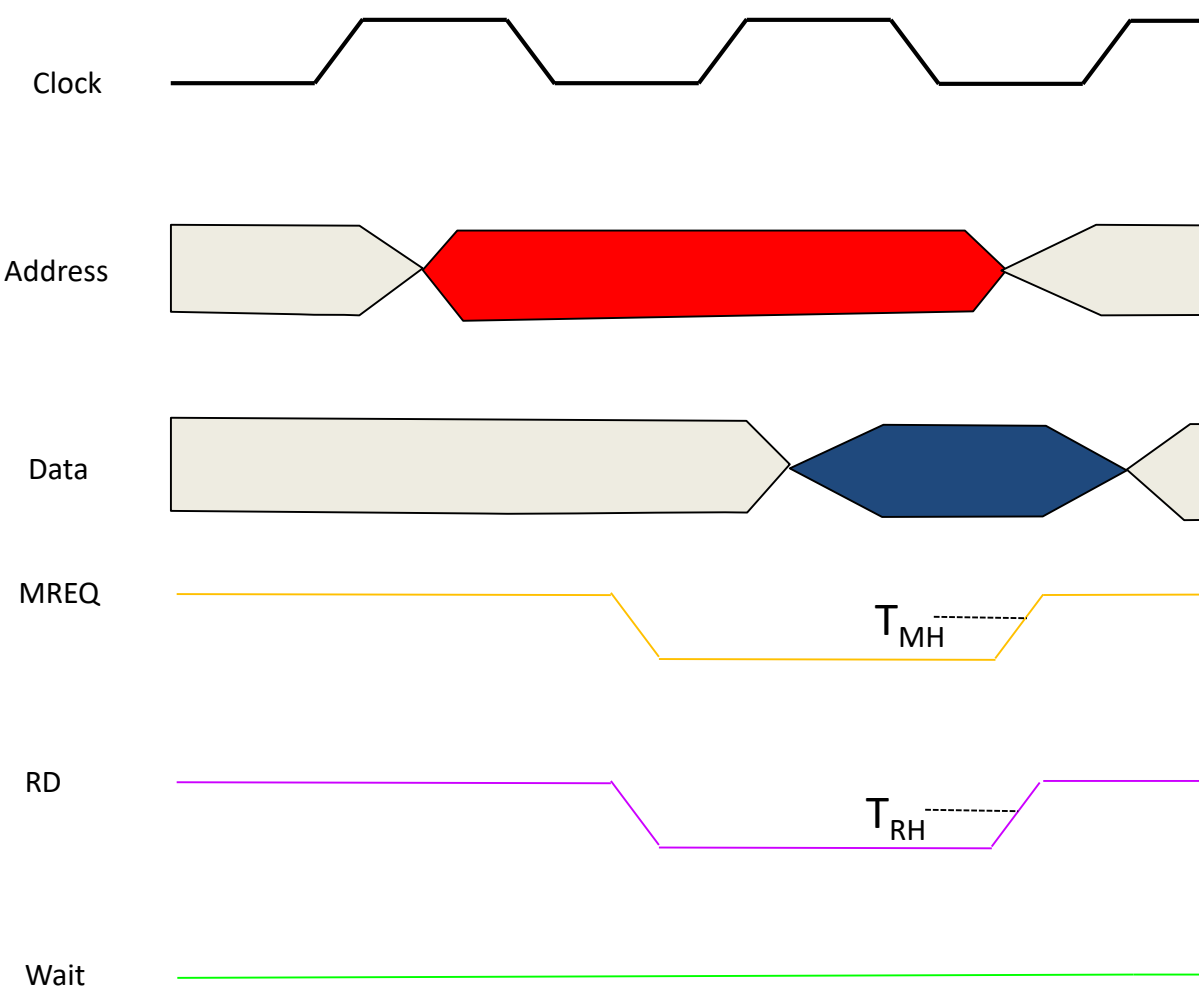

Requested transfer signals have been active for a while, next clock pulse commences.



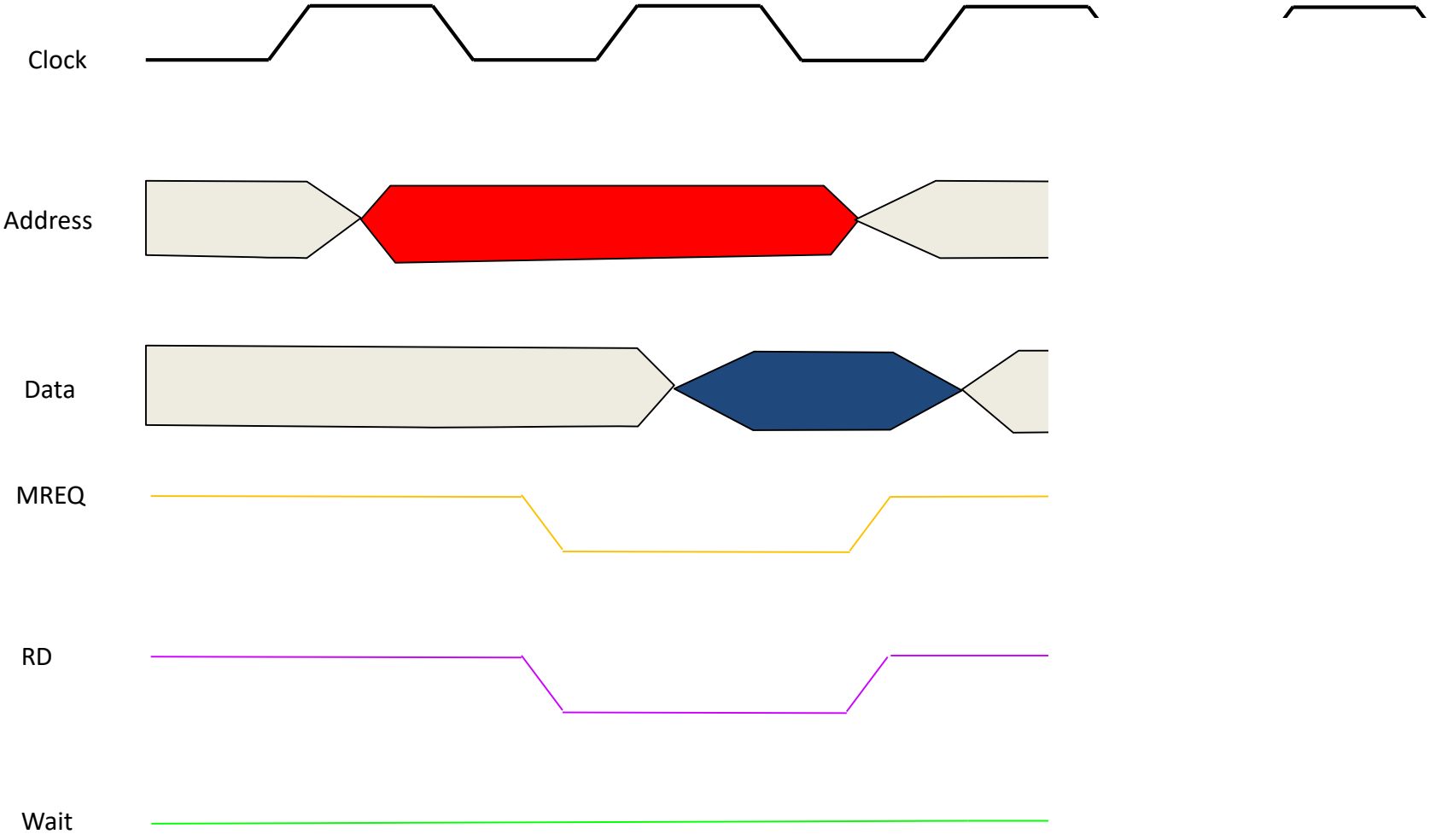

Data read from desired memory address begins appearing on data lines



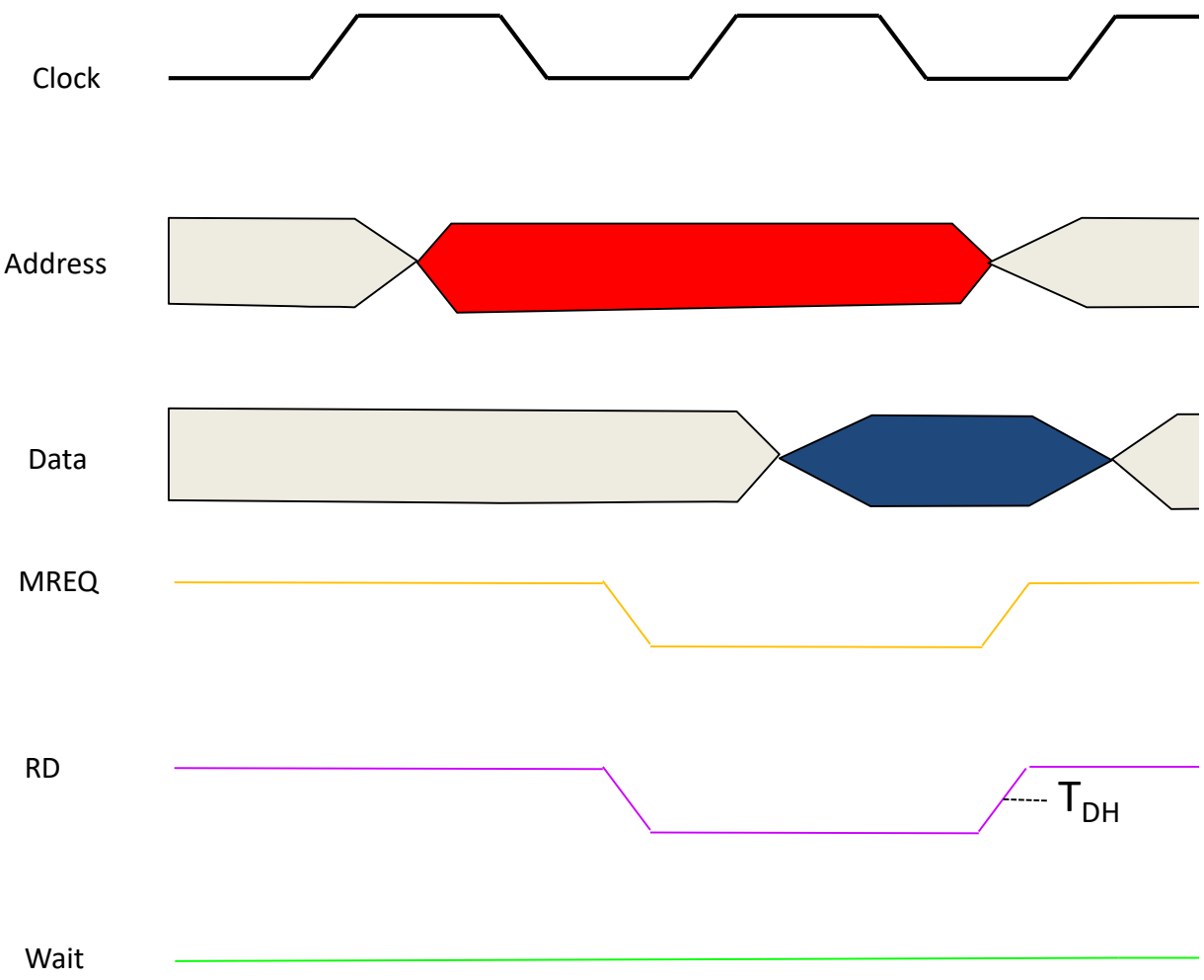

Time constraint $T_{DS}$ indicates the minimum time prior to the falling edge of the clock pulse that the data must be stable on the data lines



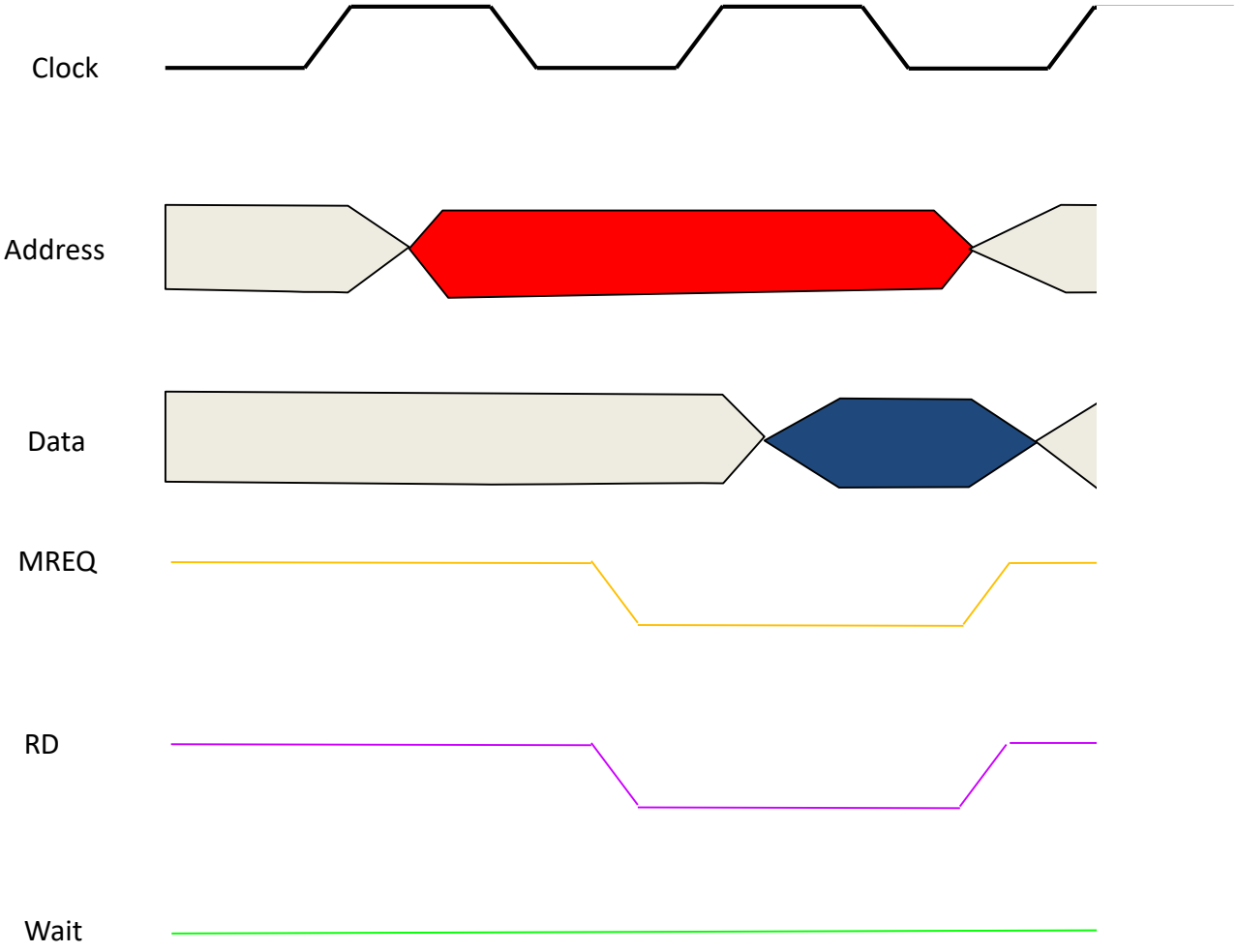

The time conditions $T_{MH}$ and $T_{RH}$ (MH = “memory high”, RH = “read high”) indicate the maximum time from the middle of the falling edge before beginning returning the MREQ and RD lines are returned to their unasserted (“high”) value



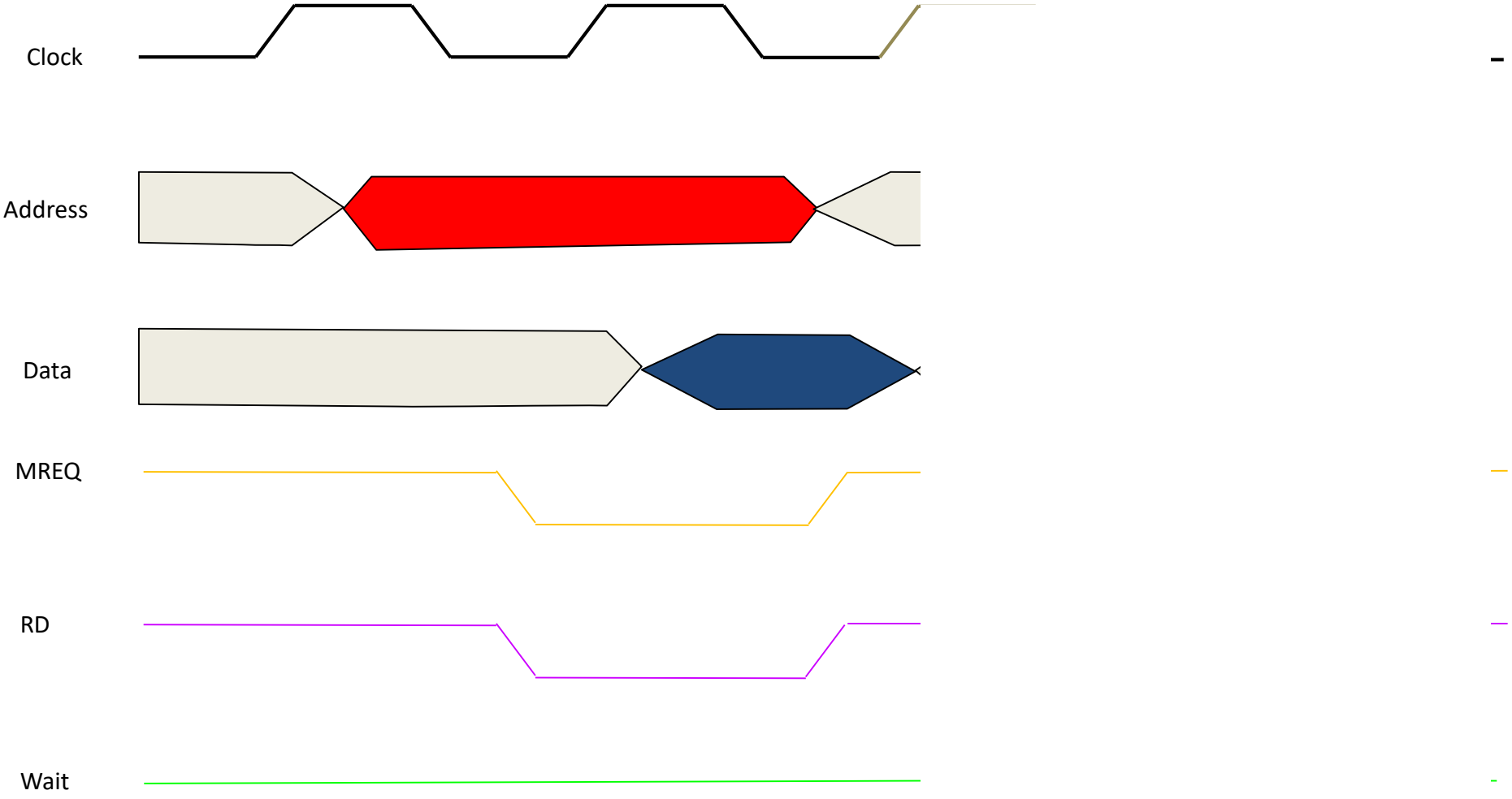

Memory read complete; a new bus activity can commence as soon as the next clock pulse.




The time $T_{DH}$ (DH = “data hold”) indicates how long to keep data on the bus after RD has been deasserted. This could be 0, but some CPUs may need for the data to be there a bit longer.




Memory read complete; a new bus activity can commence as soon as the next clock pulse.




The memory read is complete; a new bus activity can commence as soon as the next clock pulse.