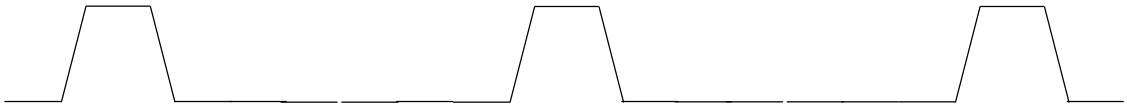
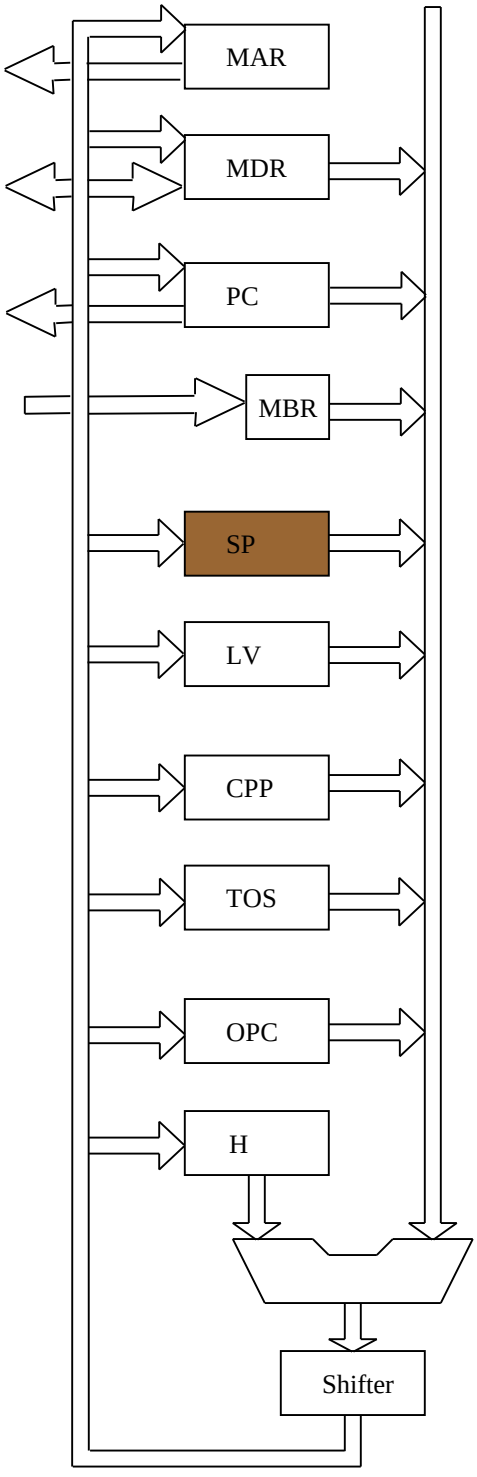
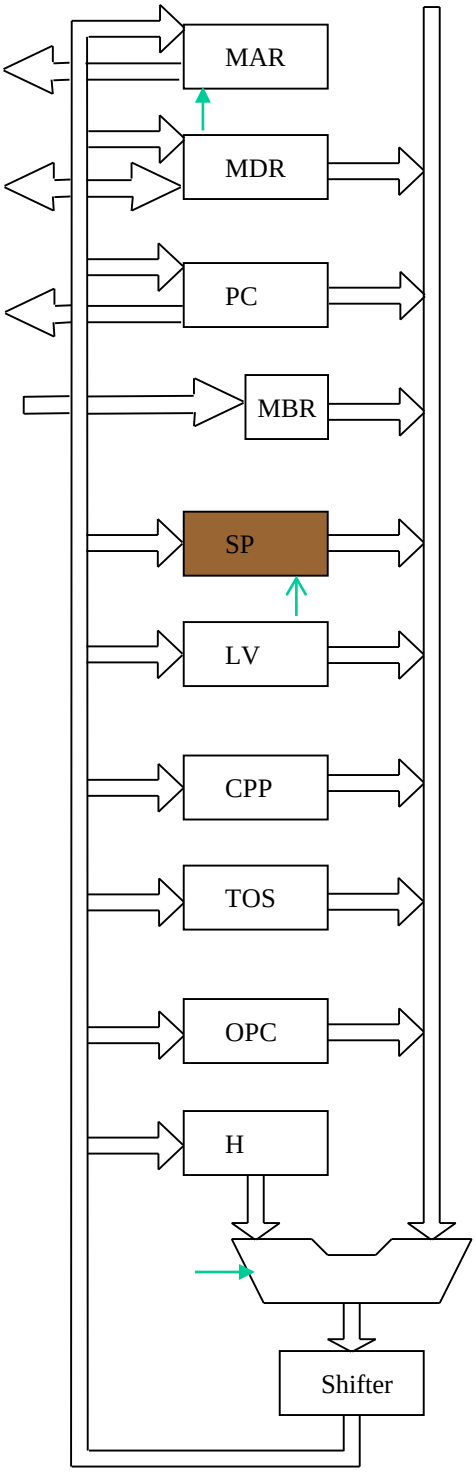


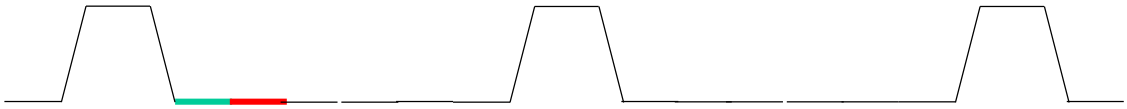


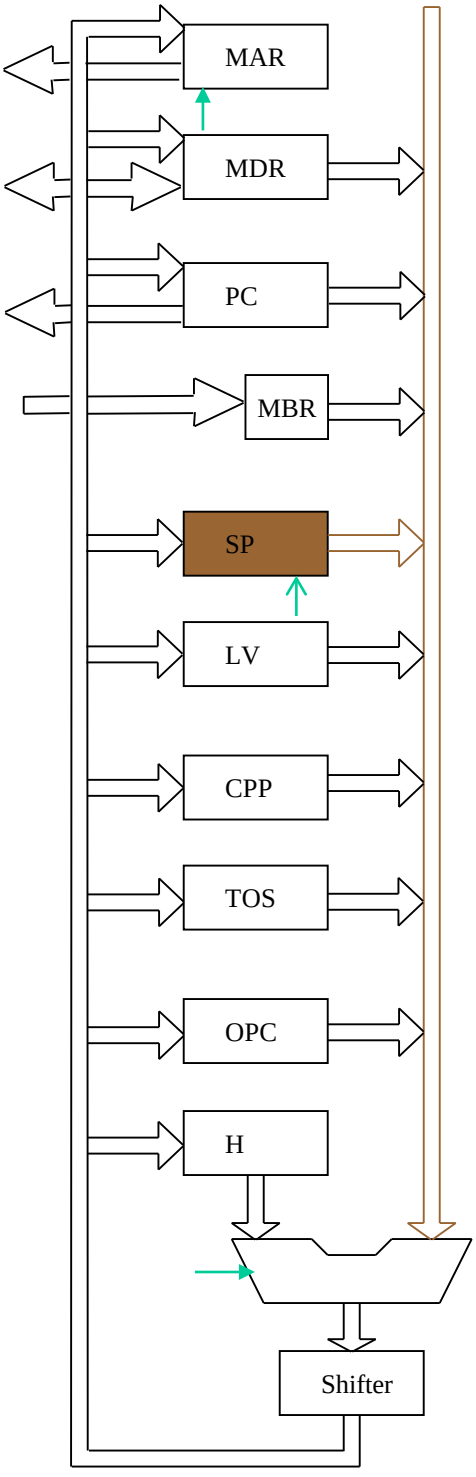
Timing diagram for MDR = M[[SP] + 1]



Control signals are set up

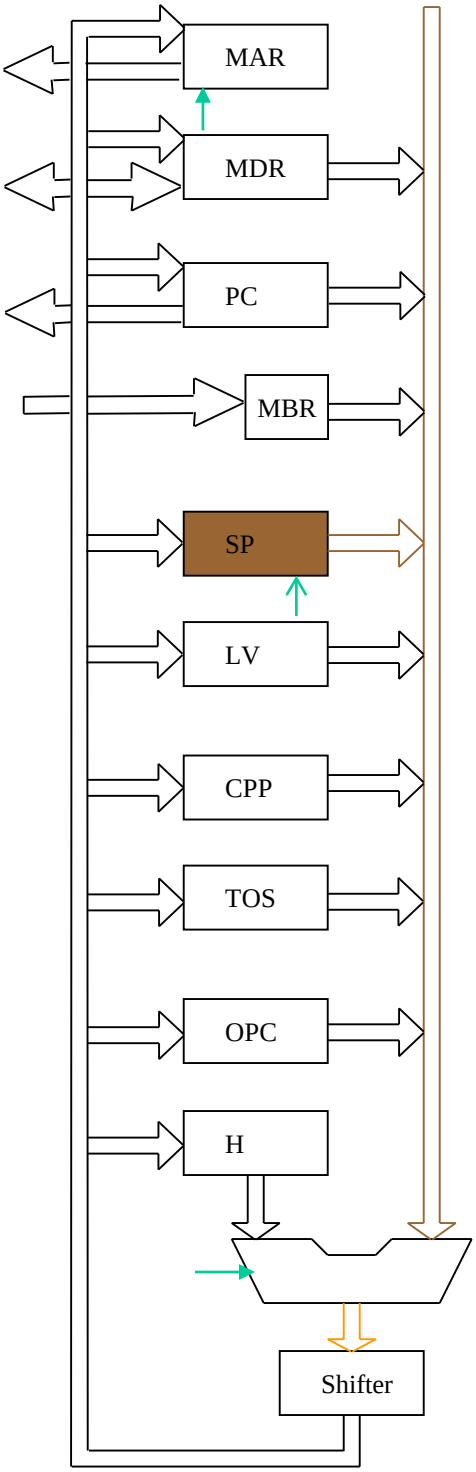
MDR = M[[SP] + 1]





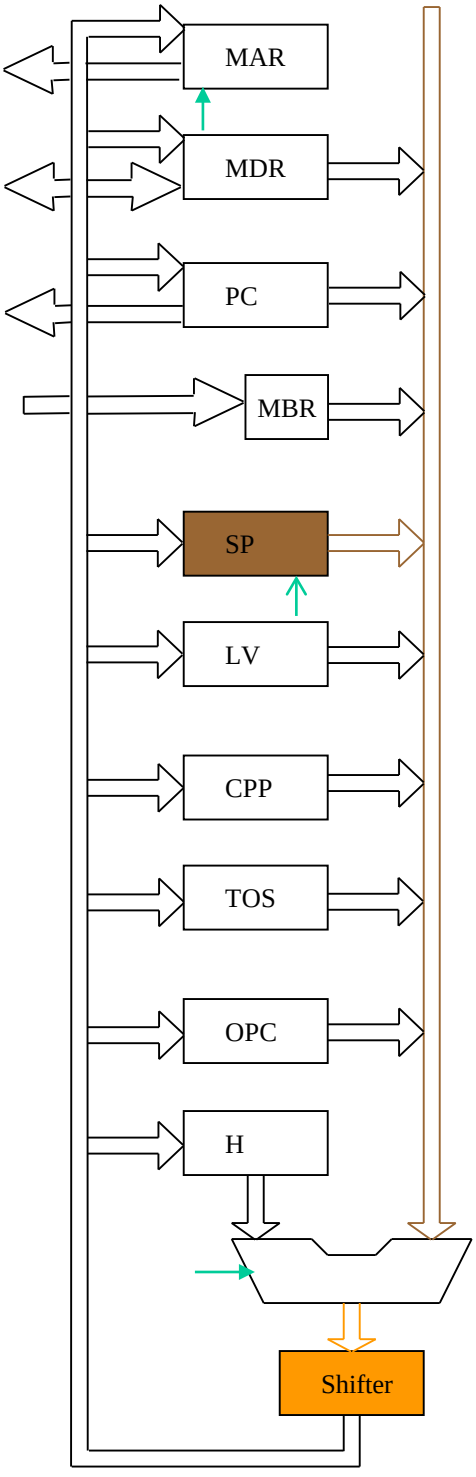
Drive B bus

MDR = M[[SP] + 1]



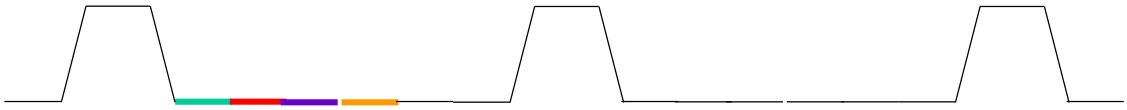
ALU

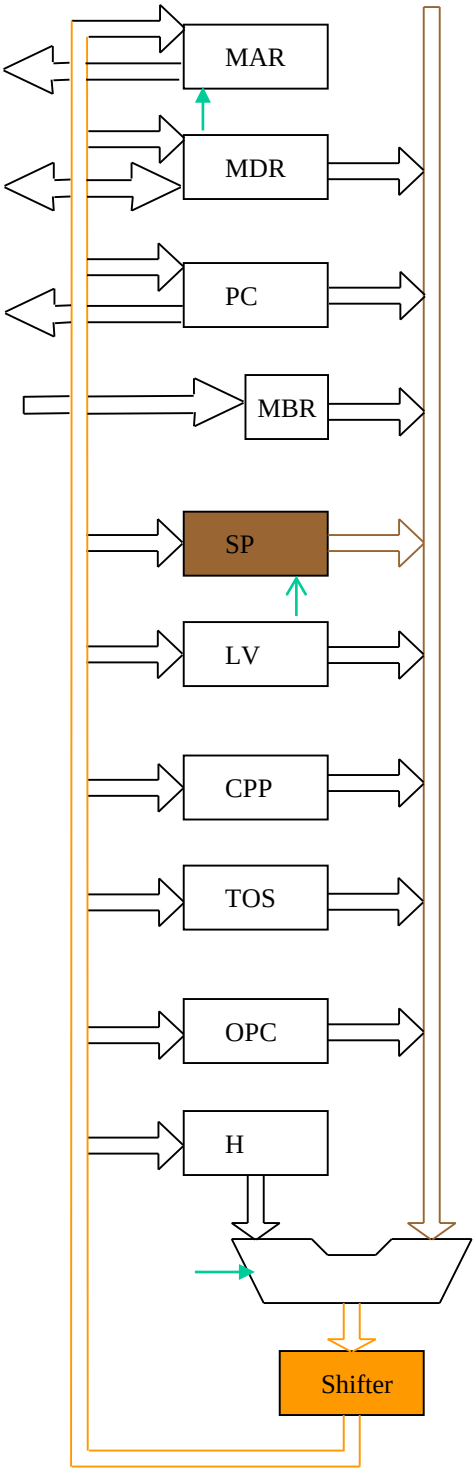
MDR = M[[SP] + 1]



ALU and shifter

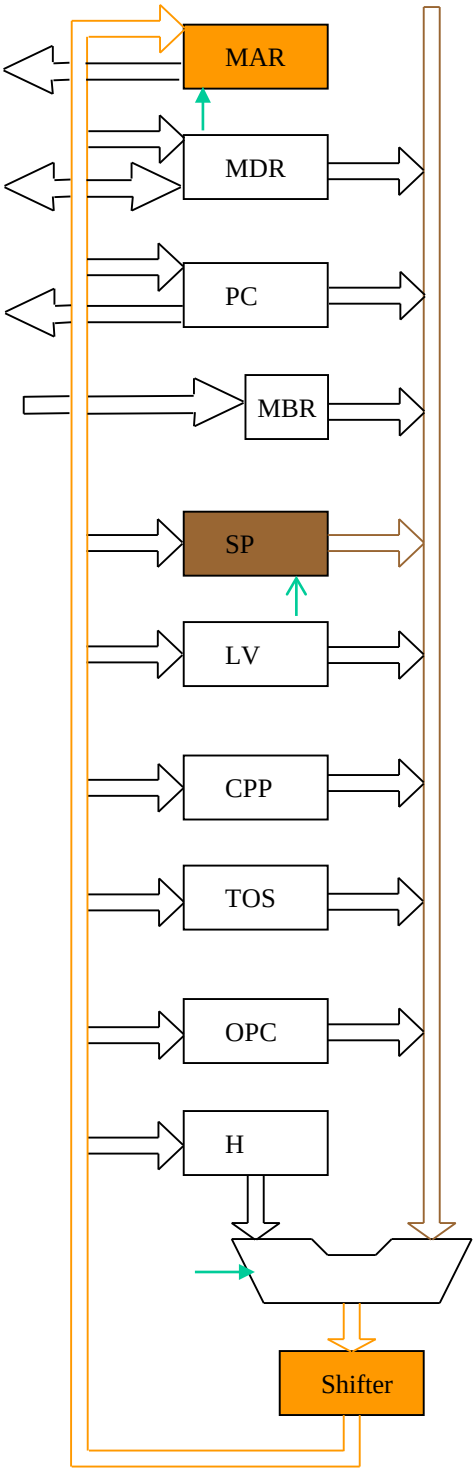
MDR = M[[SP] + 1]





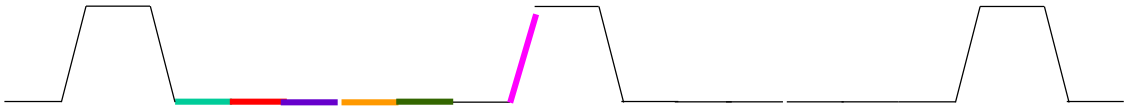
Propagation from shifter to C bus

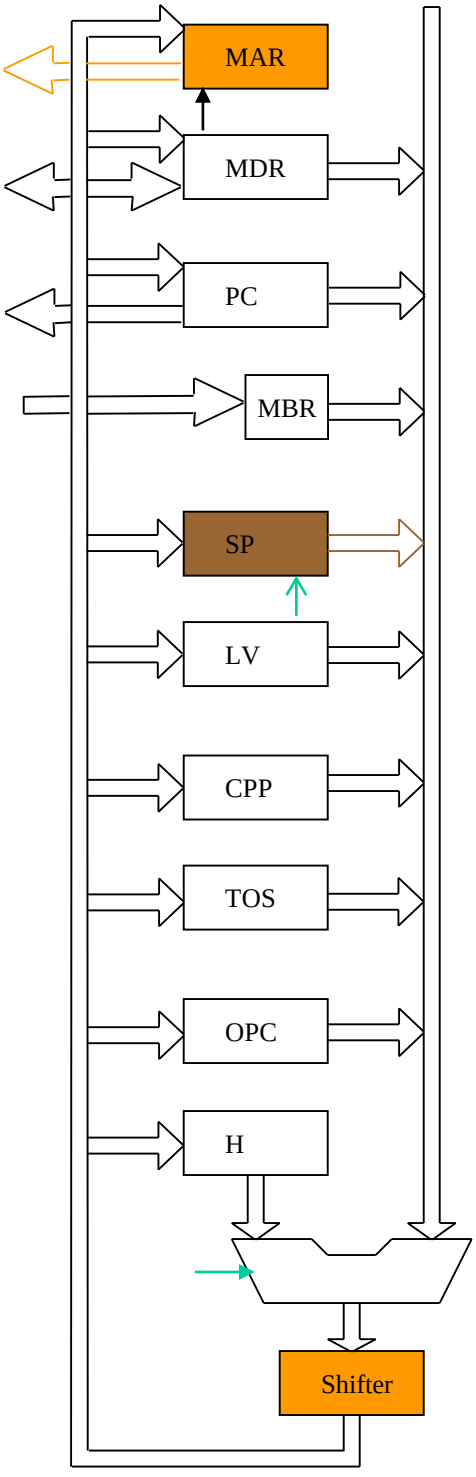
MDR = M[[SP] + 1]



Registers loaded from C bus

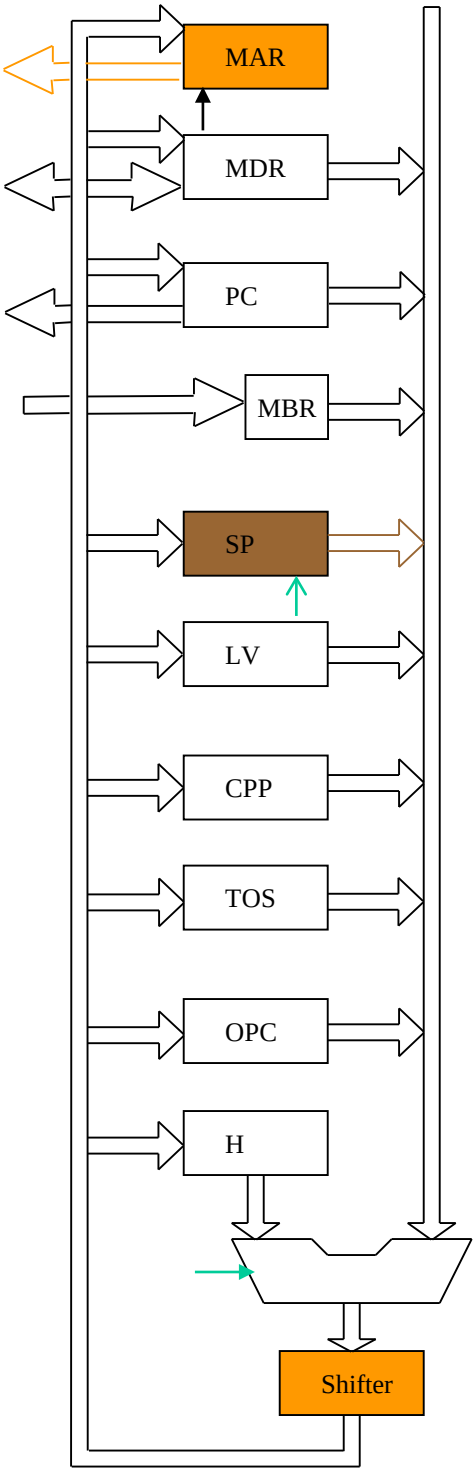
MDR = M[[SP] + 1]





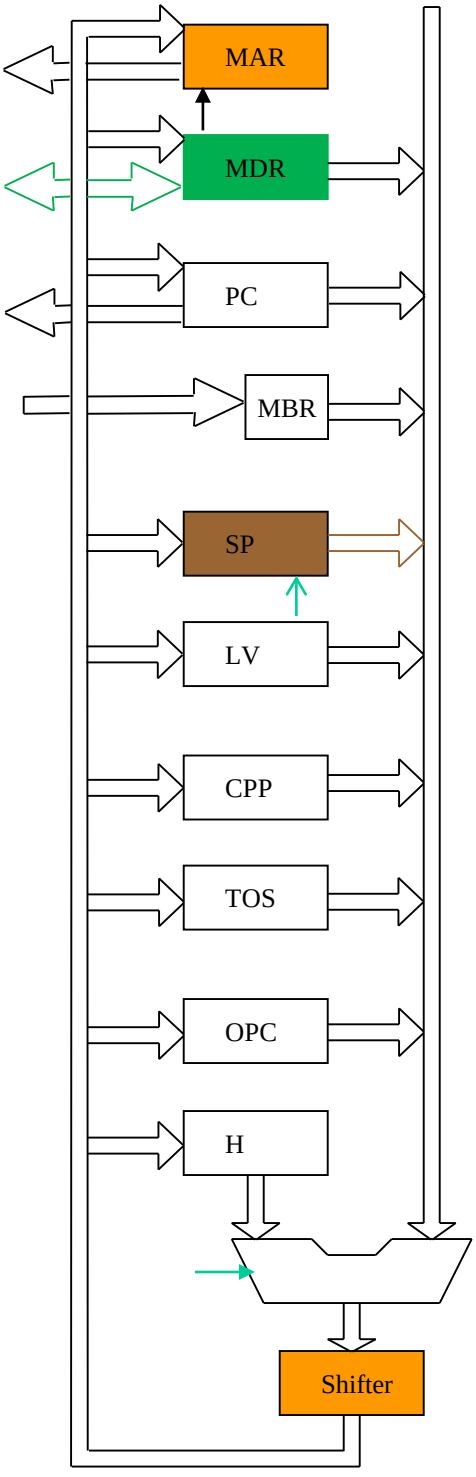
Memory write begins

MDR = M[[SP] + 1]



Waiting for memory read to complete

MDR = M[[SP] + 1]



Value read from memory goes in MDR

MDR = M[[SP] + 1]