Ch 3 HW

College of Charleston
Computer Science Department

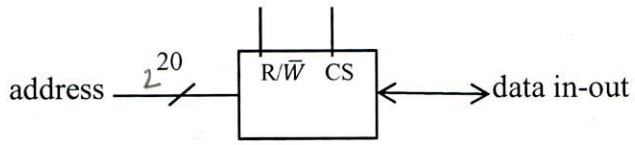
CSCI 350 Digital Logic and Computer Organization
G. Pothering
Spring 2020
Assignment 5 **Due March 12, 2020** when he can start grading

Primary Course Outcomes Being Addressed:

Understand the basic principles behind the design of synchronous and asynchronous buses.
Understand and develop timing diagrams for synchronous and asynchronous read/write.

Assignment Problems

1. Consider the following 1M × 1 bit memory. (in out line)



Construct a 1M × 2 memory using an appropriate number of these modules and any additional circuitry you might need. Assume that when CS is low no data may be stored in the module and no data appears on the data out lines. Also assume a read take place when there is a 1 on the R/$\overline{W}$ line, and a write takes place when there is a 0 on this line.

2. Repeat problem 1, but instead construct a 4M × 1 memory using an appropriate number of these modules and any additional circuitry you might need.

3. Problem 25 on page 239 of your textbook.

4. Problem 26 on page 239 of your textbook.

Assume bus transfers are coordinated by a by 500MHz clock (with equal times while the clock pulse is low and high). Assume further that a memory operation requires 3 nsec from the time a memory address value is available until one can assume a stable output value is available.

5. Give the timing diagram for a synchronous write operation. (Use the sheet on the next page; more copies are available via OAKS if you need them)

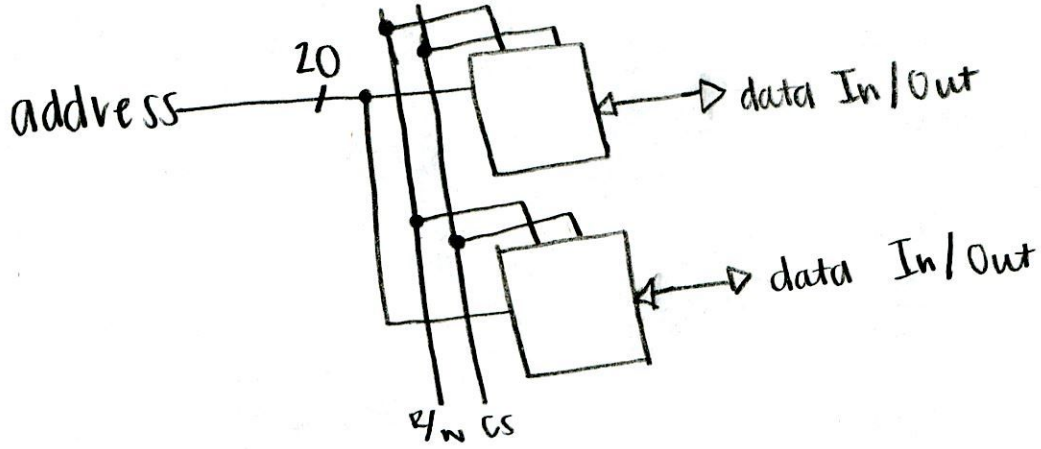
6. Give the timing diagram for an asynchronous write operation. (Use the sheet on the next page)

7. Suppose the memory operation requires 5 nsecs from the time a memory address value is available until one can assume a stable output value is available. Give a timing diagram for a synchronous read operation. (Use the sheet on the next page)

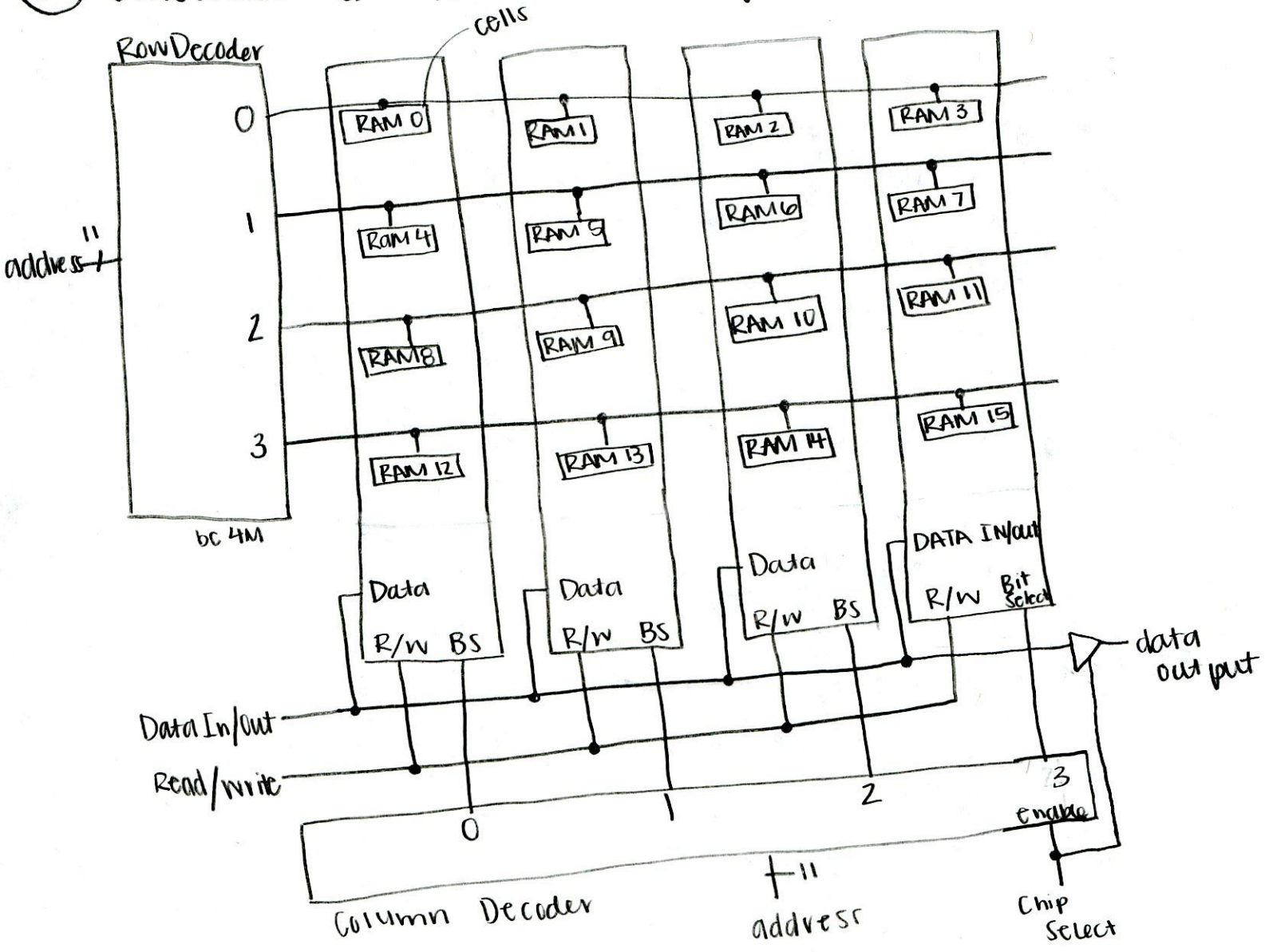
8. Assume that a memory operation requires 4 nsec from the time a memory address value is available until one can assume a stable output value is available and that the maximum time for an address output delay from a rising edge (T_{AD}) and the minimum data setup time prior to the falling edge of a clock pulse (T_{DS}) are both 1/2 nsec. If a system designer wanted to be able to carry out consecutive memory operations without the need for wait states, what is the fastest clock speed (in MHz) that can support this. **You must show all of your work to receive credit on this problem. I will not accept an answer with no work, even if the answer is correct.**

Shefali E

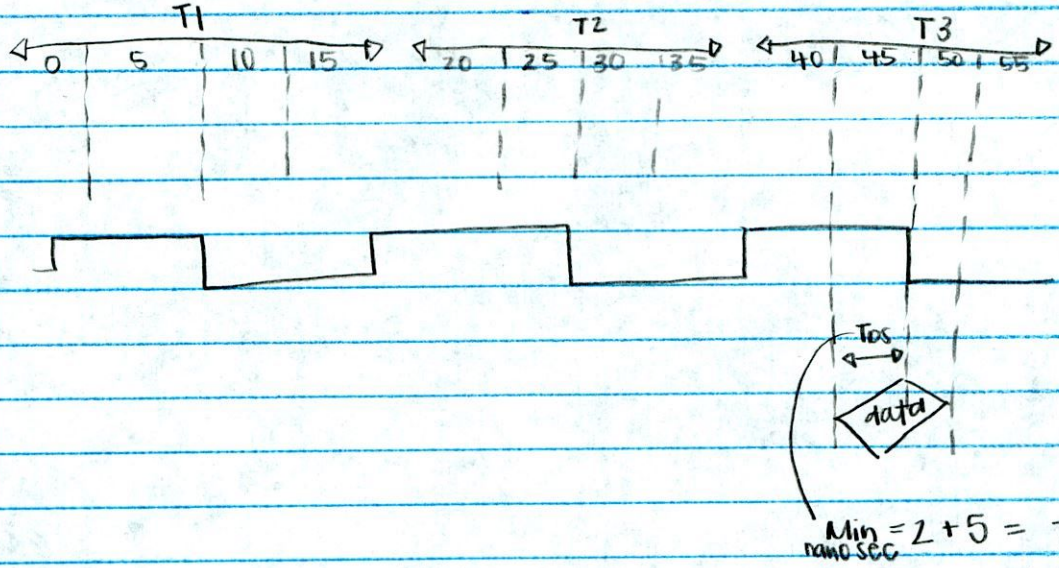
#1 Construct a 1M x 2 memory



#2 Construct a 4M x 1 memory



#3



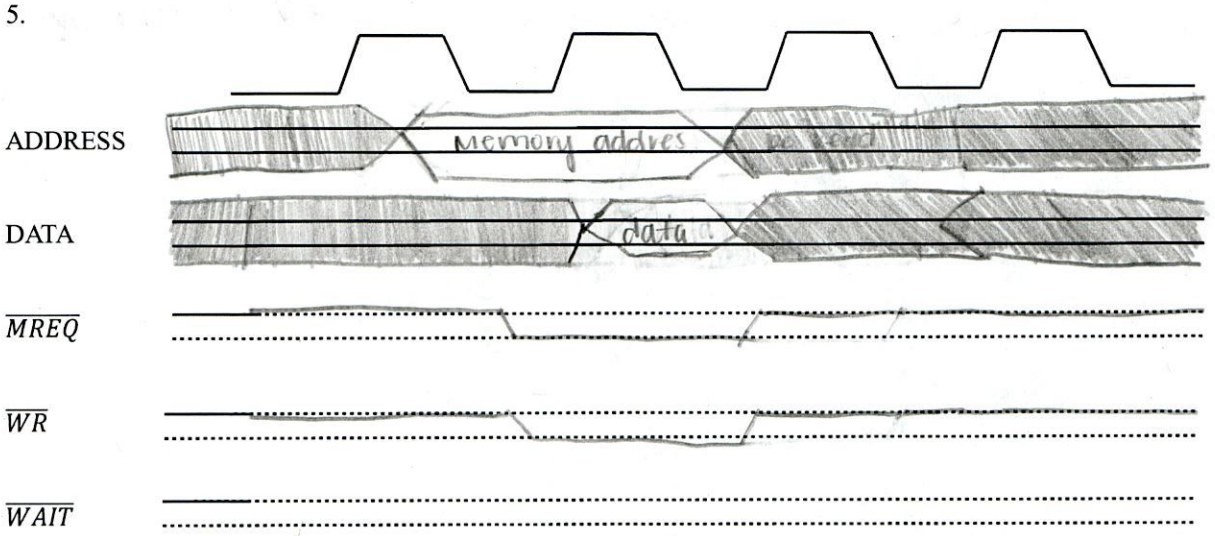
Min nanosec = 2 + 5 = 7 nanosec to get the memory on the bus

as worst case is the least amount of time

#4 NO, if a 10 nanosec memory chip was used > TDS would run for 4 seconds ~~ran~~ ending at 27 nanoseconds which would be AFTER the falling edge

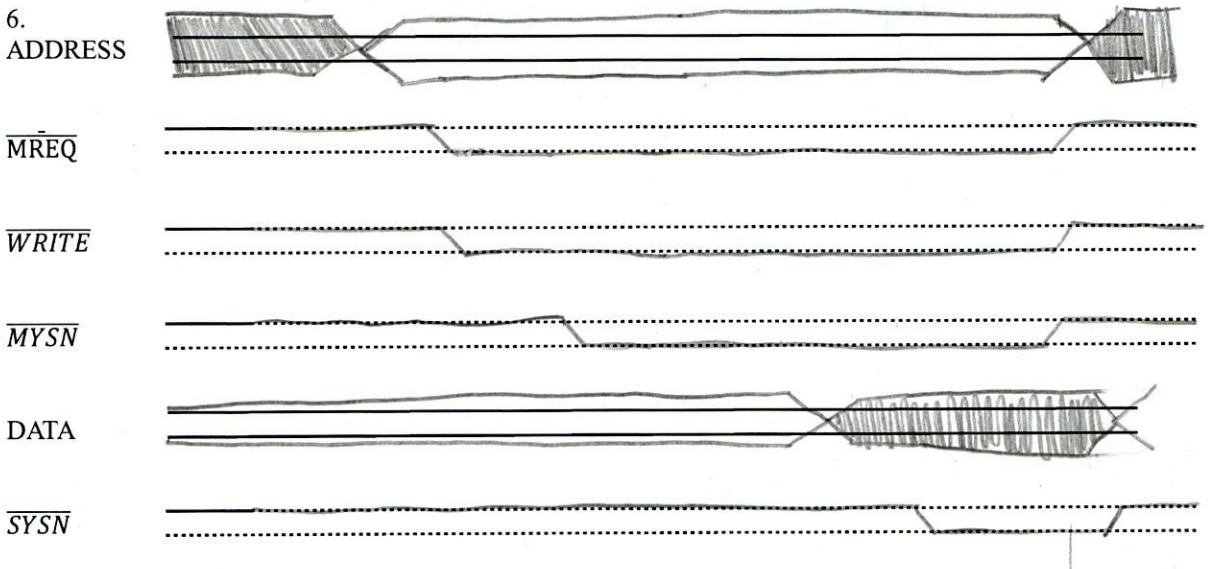
Synchronous Write no wait

5.



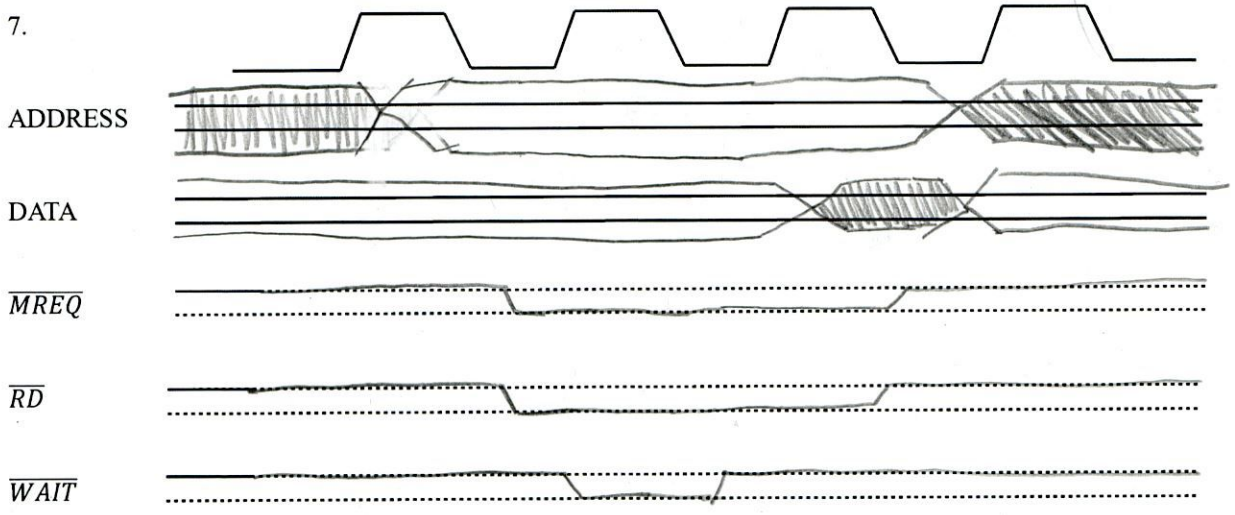
asynchronous Write no wait

6.



Synchronous read wait

7.



(#8) mem operation = 4 nano seconds available → output

T_{AD} = 1/2 nano sec

T_{DS} = 1/2 nano sec

T_{AD} + Memory Operation + T_{DS} = .5 + 4 + .5 = 5 nano seconds