Register transfer	Control signals active
Fetch	
PC = [PC] + 1; fetch	1, fetch, pc, F0, F1, enb, inc
IADD	
MAR, SP = [SP]-1; read	4, read, sp, mar, F0, F1, enb, inva
H = [TOS]; MDR = M[MAR] at end of cycle	7, F1, enb, h
TOS, MDR = [H] + [MDR]; write	0, write F0, F1, ena, enb, tos, mdr
DUP	
MAR, SP = [SP]-1	4, sp, mar, F0, F1, enb, inva
MDR = [TOS], write	7,write,F1, enb, mdr
ILOAD	
H = [LV]	5, h, F1, enb
MAR = [H] + [MBR]$_U$; read	3, mar, F0, F1, ena, enb, read
MAR, SP = [SP] + 1	4, mar, sp, F0, F1, enb, inc
PC = [PC] + 1; fetch; write	1, fetch, write, pc, F0, F1, enb, inc
TOS = [MDR]	0, tos, F1, enb
POP	
MAR, SP = [SP]-1; read	4, read, mar, sp, F0, F1, enb, inva, read
Wait for read to complete	read
TOS = [MDR]	0, tos, F1, enb
