Asynchronous Bus
Read Operation

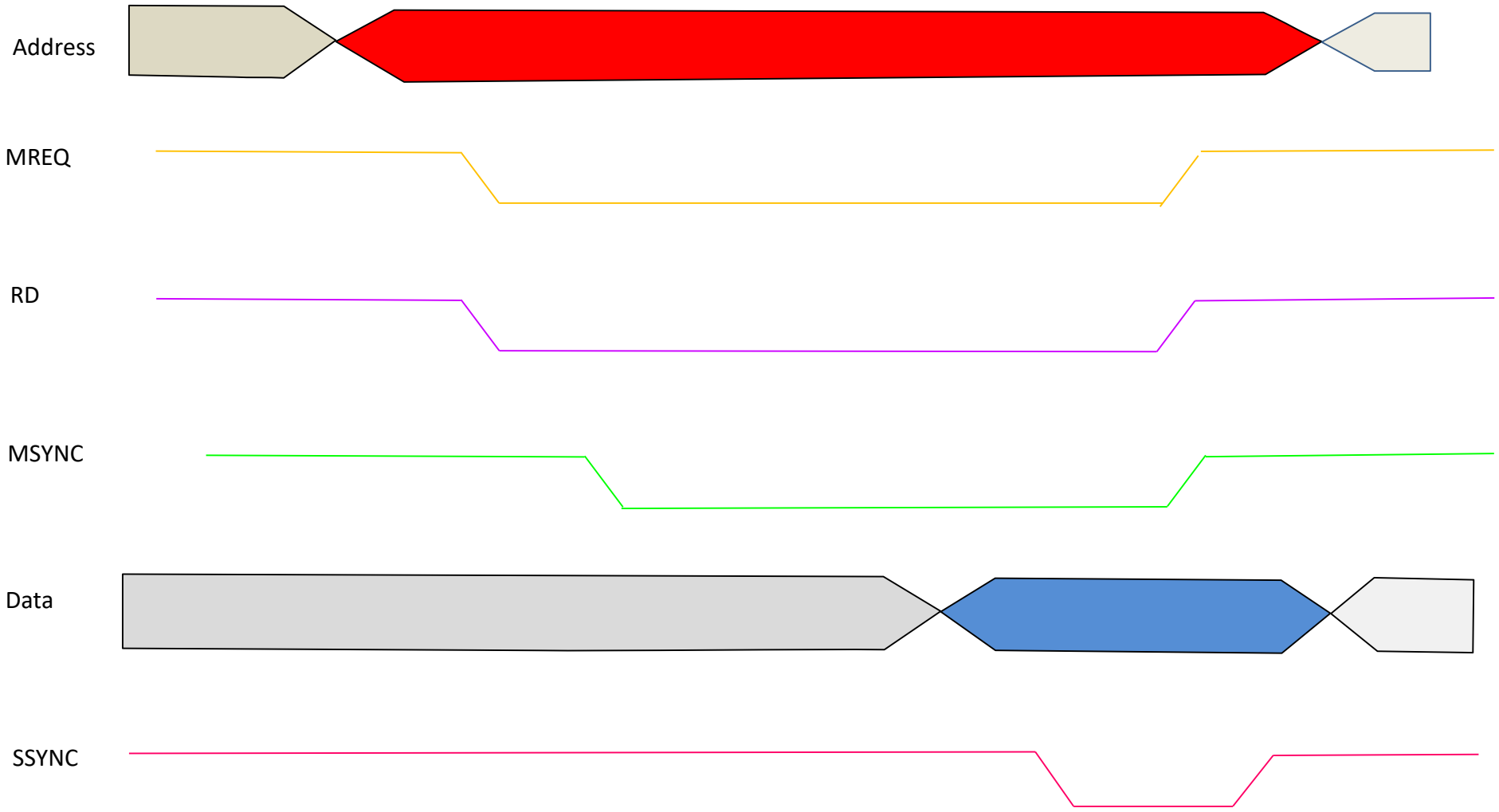
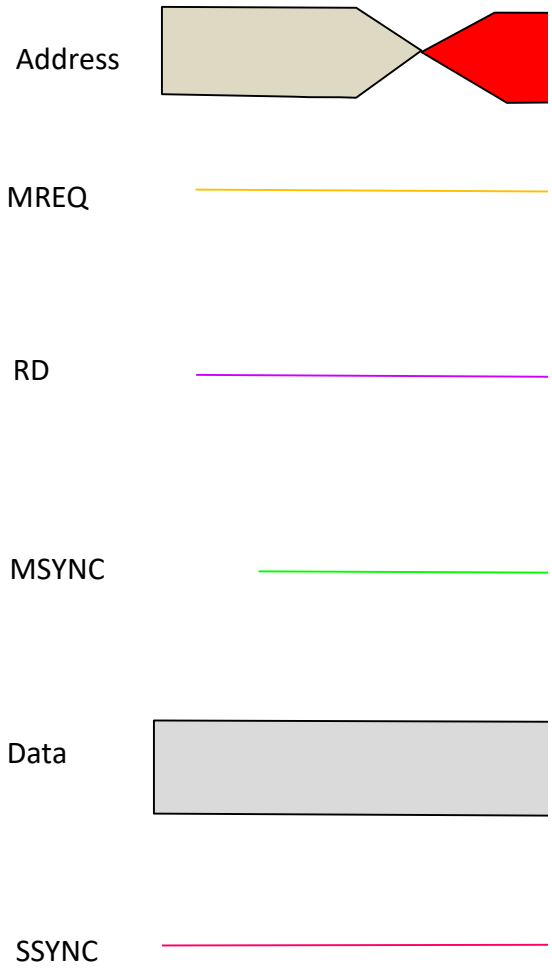
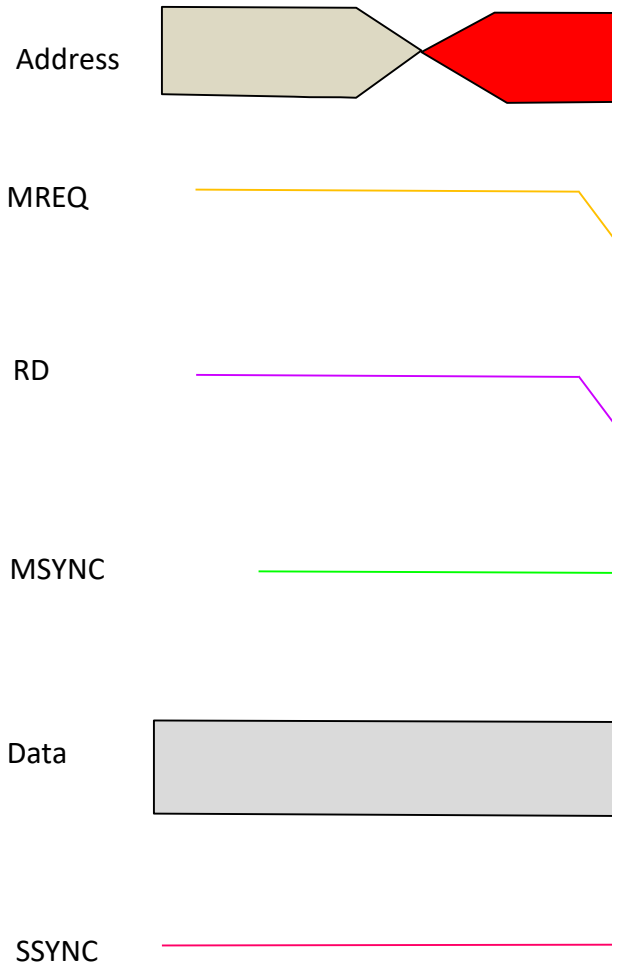


Illustration of a complete asynchronous memory read
We will break this down step-by-step.

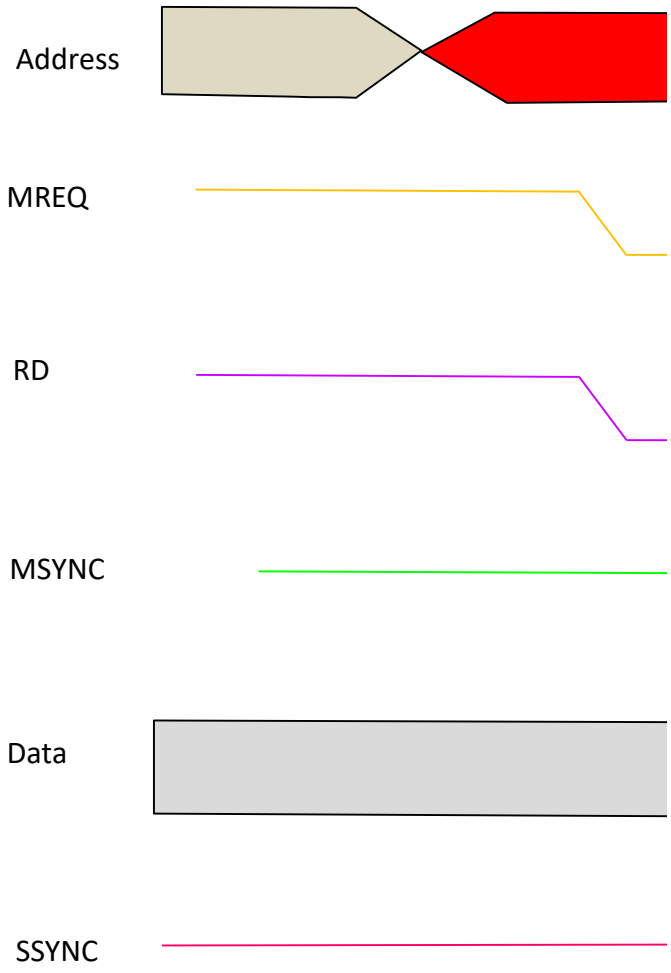
Current values of bus lines. The MREQ, RD, MSYNC and SSYNC lines are all at their "unasserted" values, which in this case is a "high", or "1" signal.



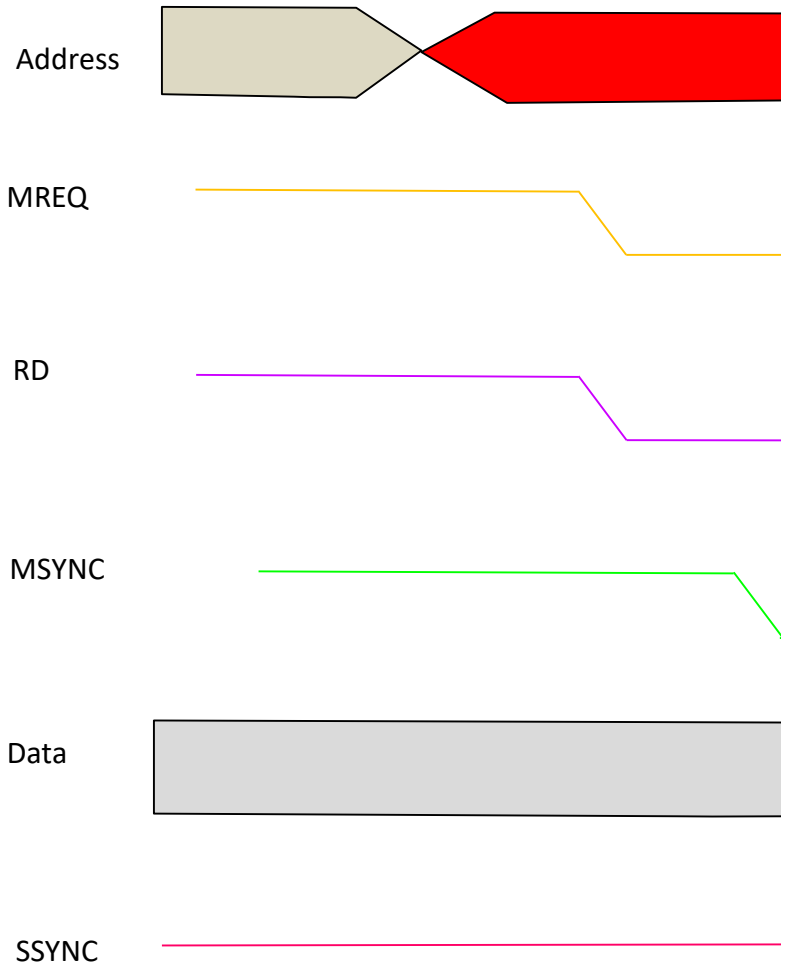
Master device (CPU) begins to place desired address (represented in red) on address lines



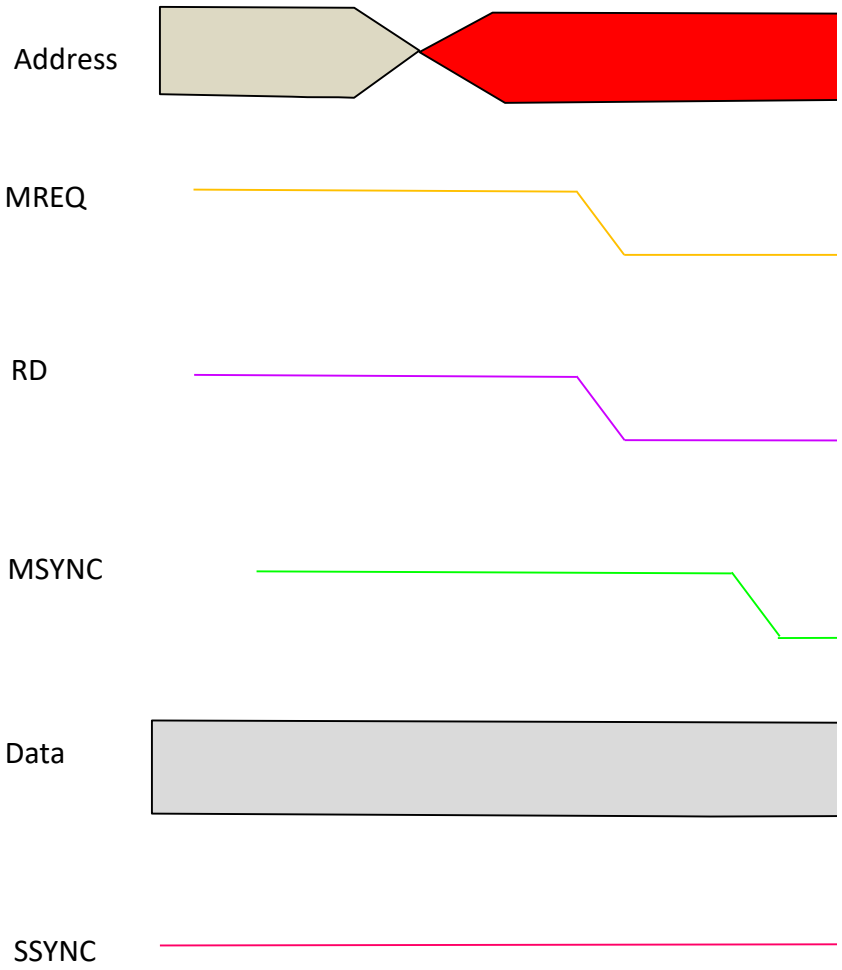
Master device starts to assert MREQ and RD lines low to indicate a memory read is requested. Here “assert” means give a “low” or “0” value



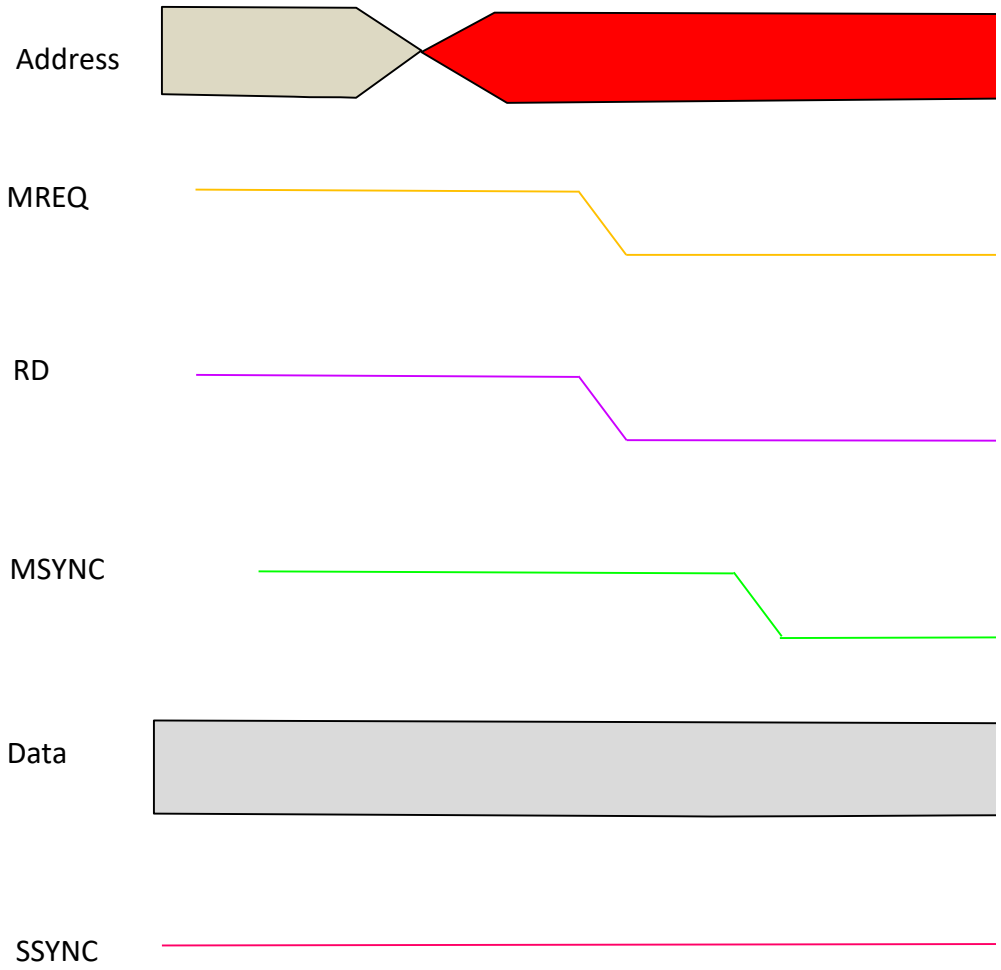
After a short time the changes in MREQ and RD are complete



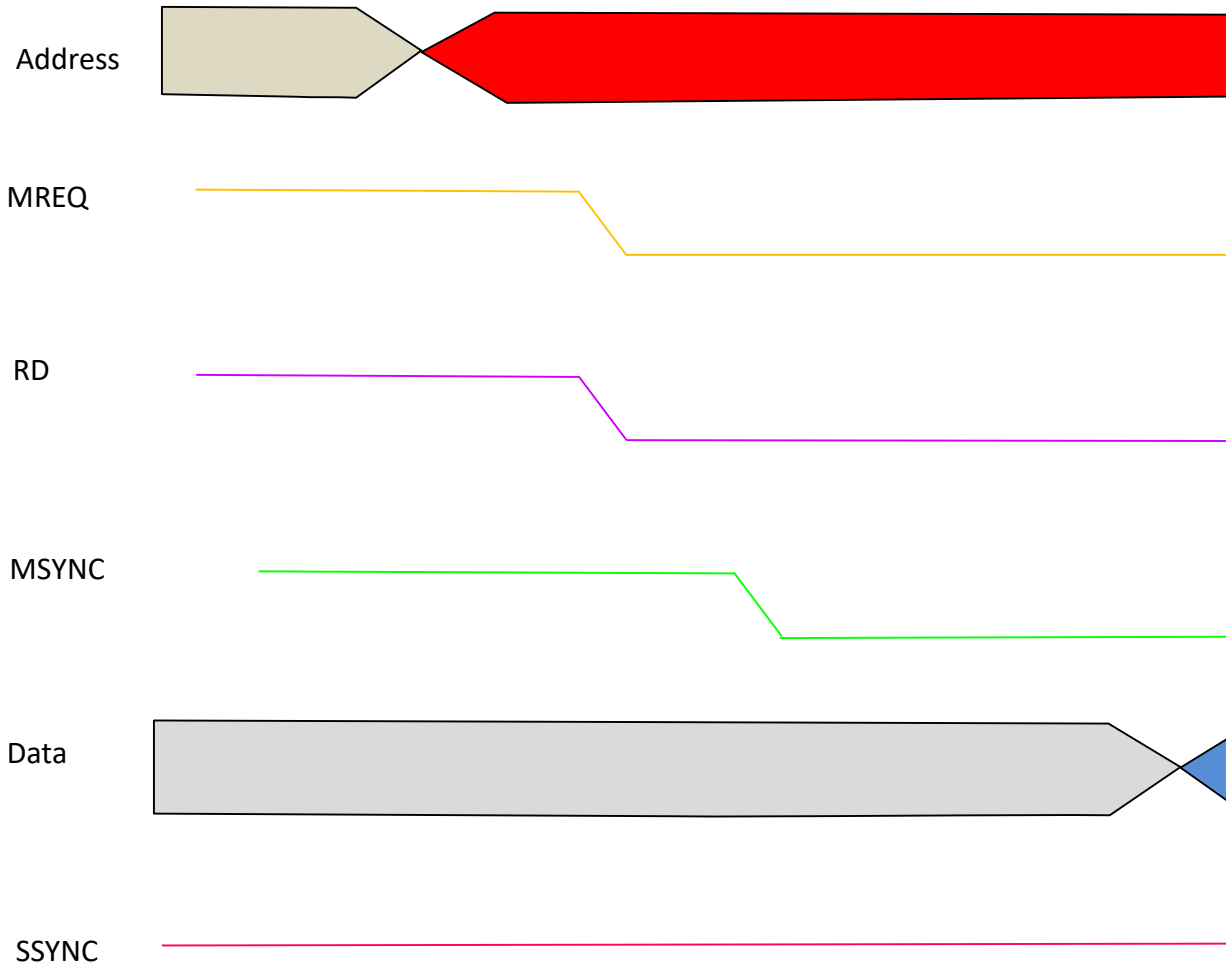
MSYNC (master sync) signal begins to be lowered



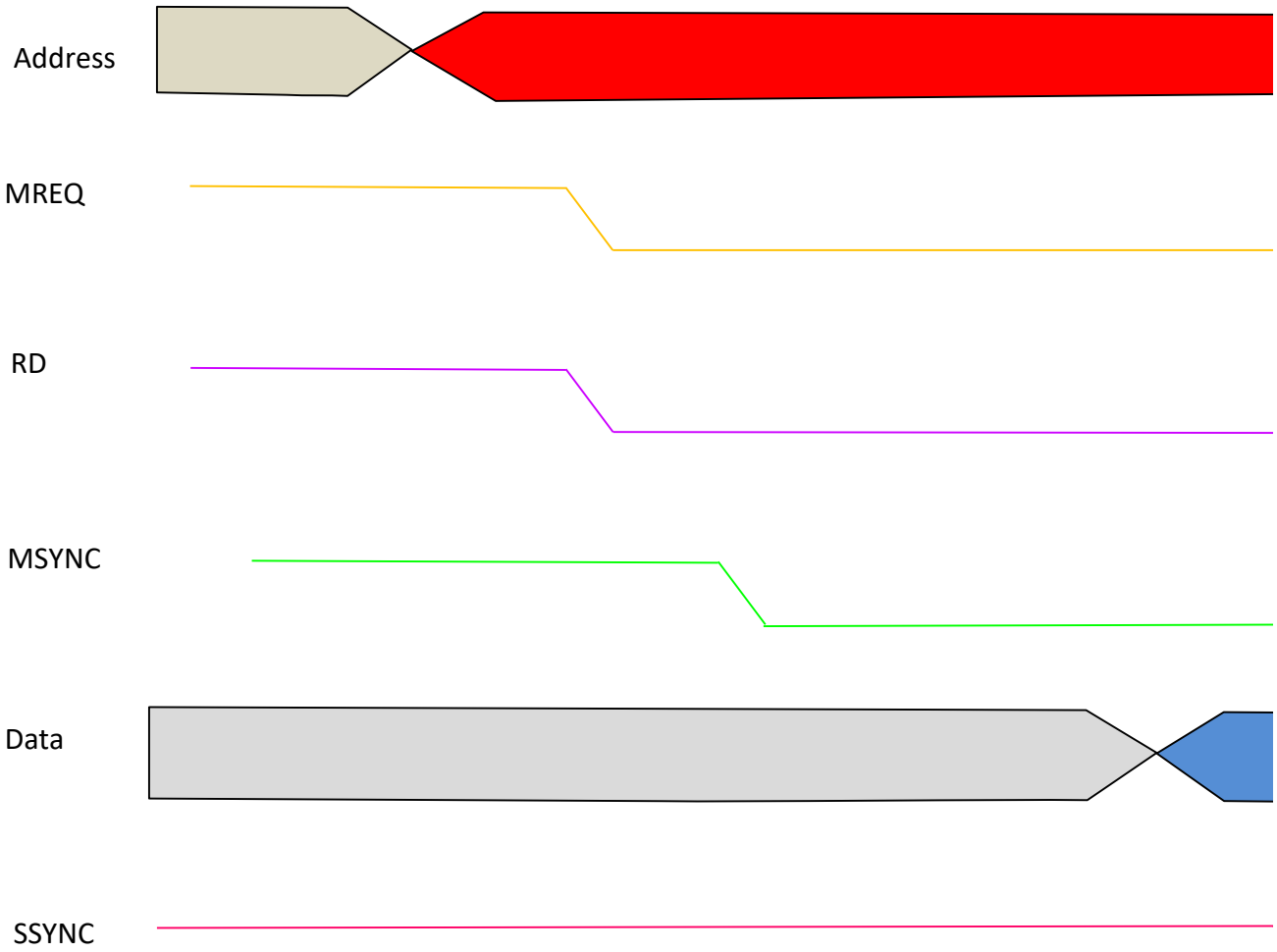
MYSYNC (master sync) signal change is complete indicating that everything is ready and memory can commence the read.



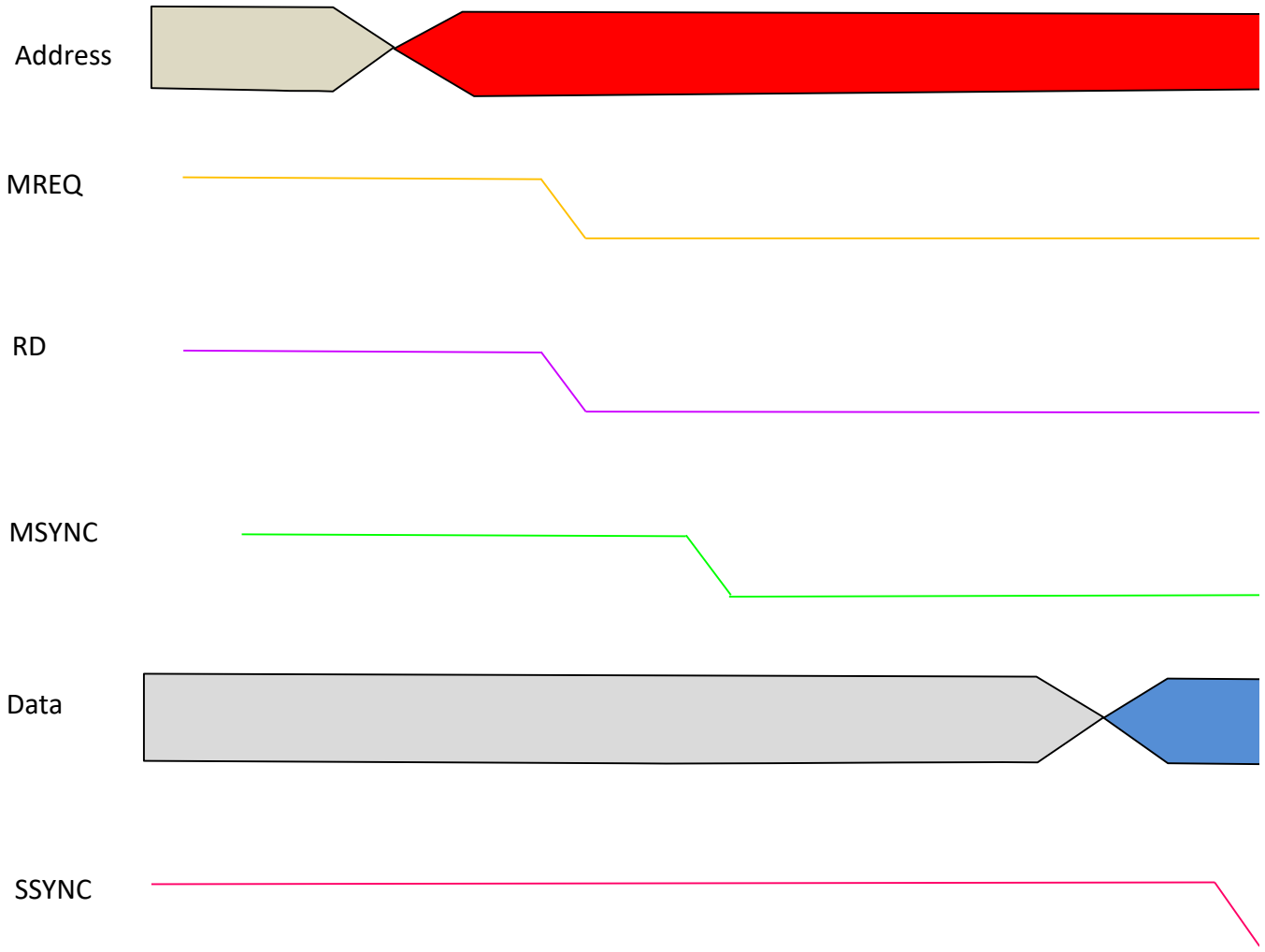
Master device is awaiting a signal from memory (specifically SSYNC will be asserted) that the read is complete and the desired data value is on the data lines.



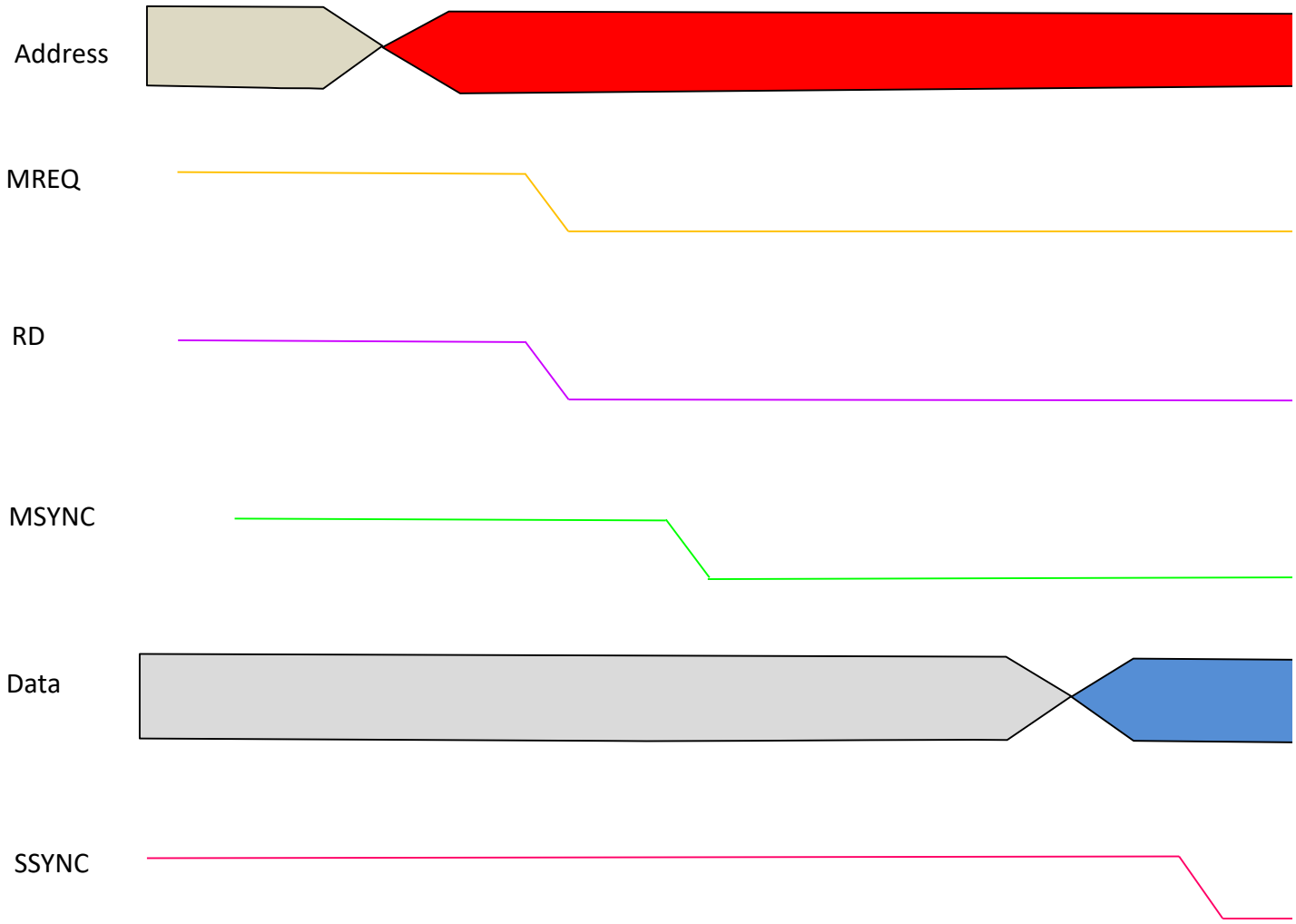
Memory begins placing requested data value (represented in blue) on the bus' data lines



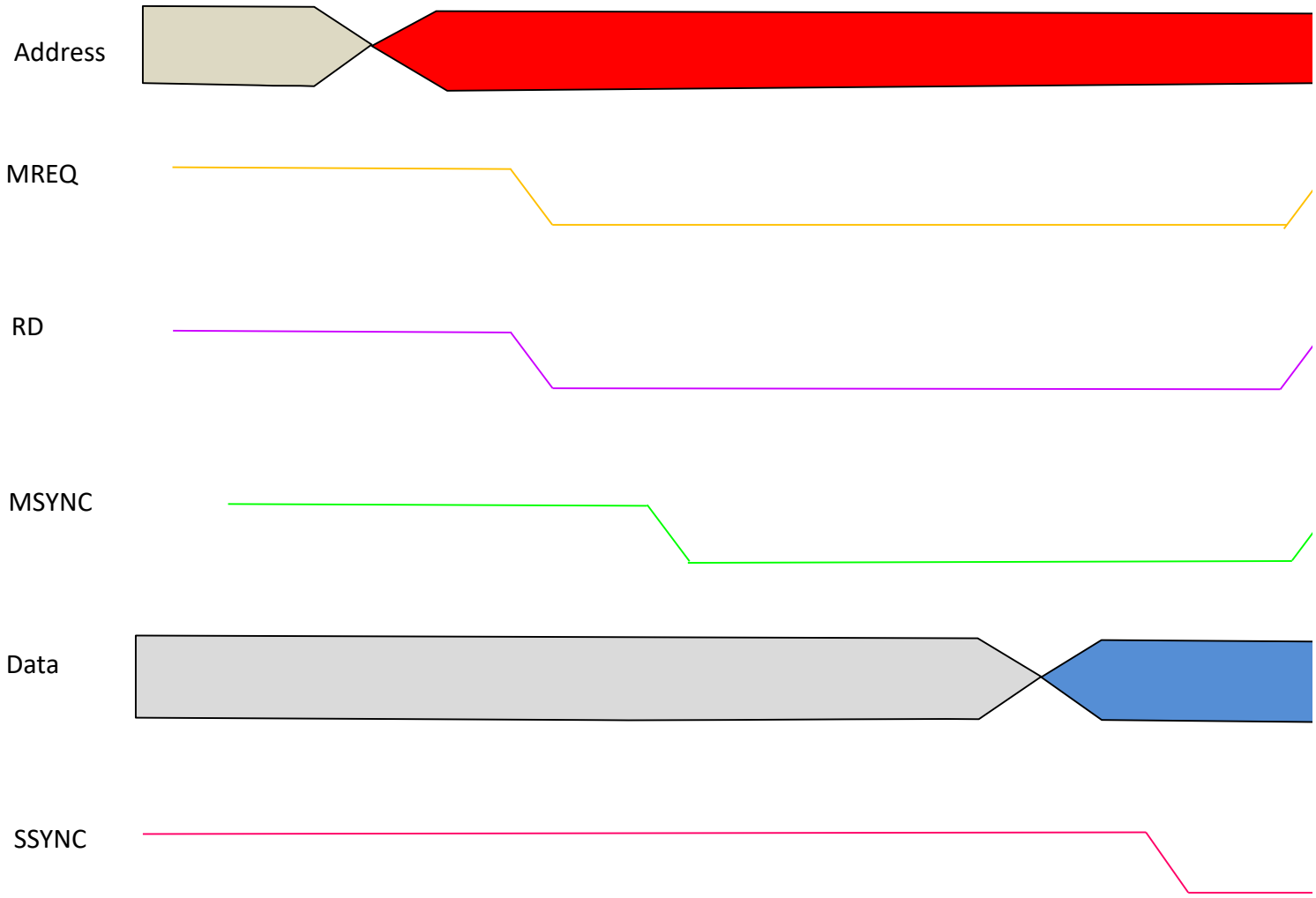
Memory continues loading desired data value onto the data lines



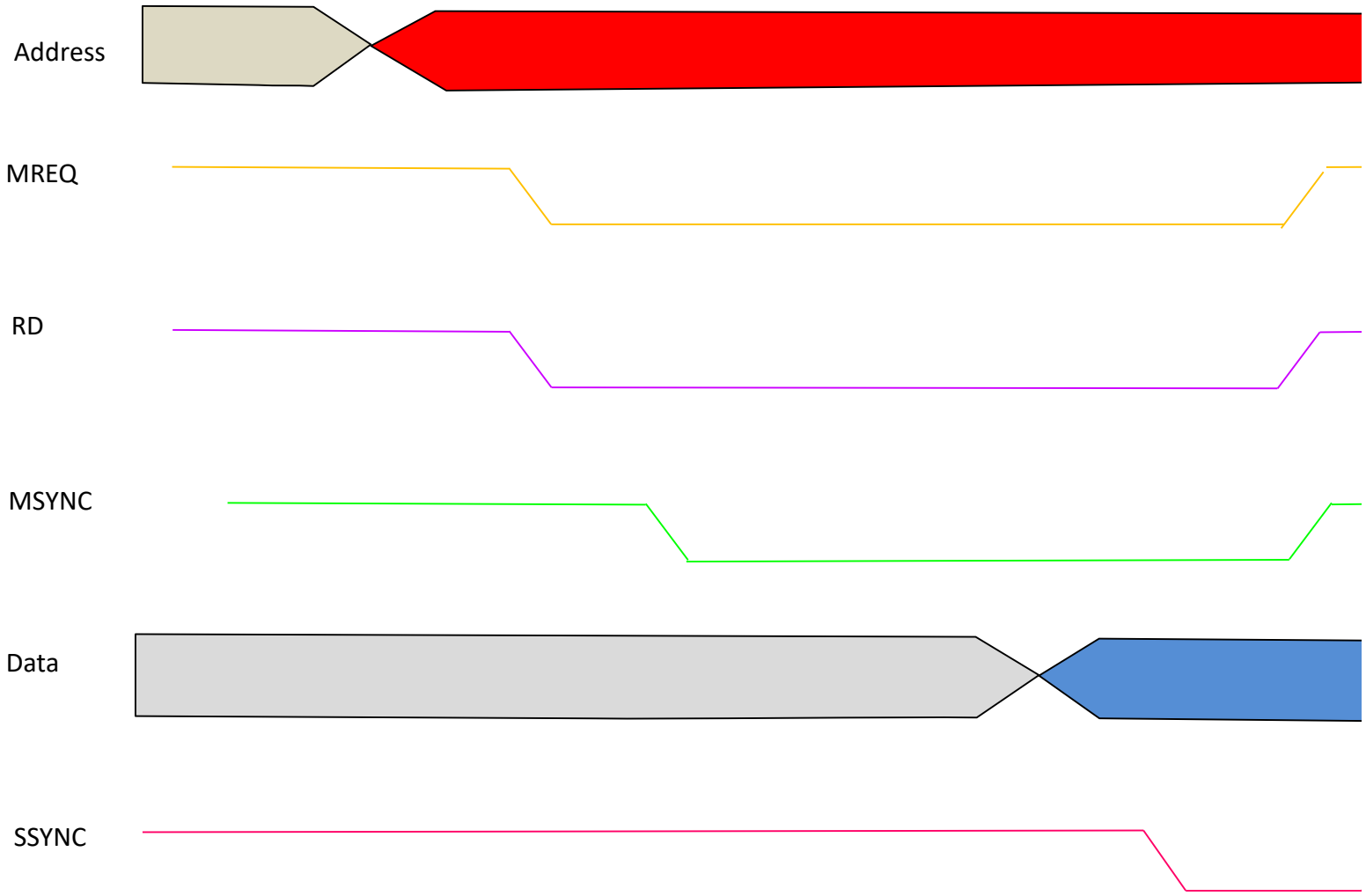
Memory (the slave device) begins to lower the SSYNC (slave sync) line to indicate that memory has completed its part of the memory read. This is the signal that the master device is waiting to see.



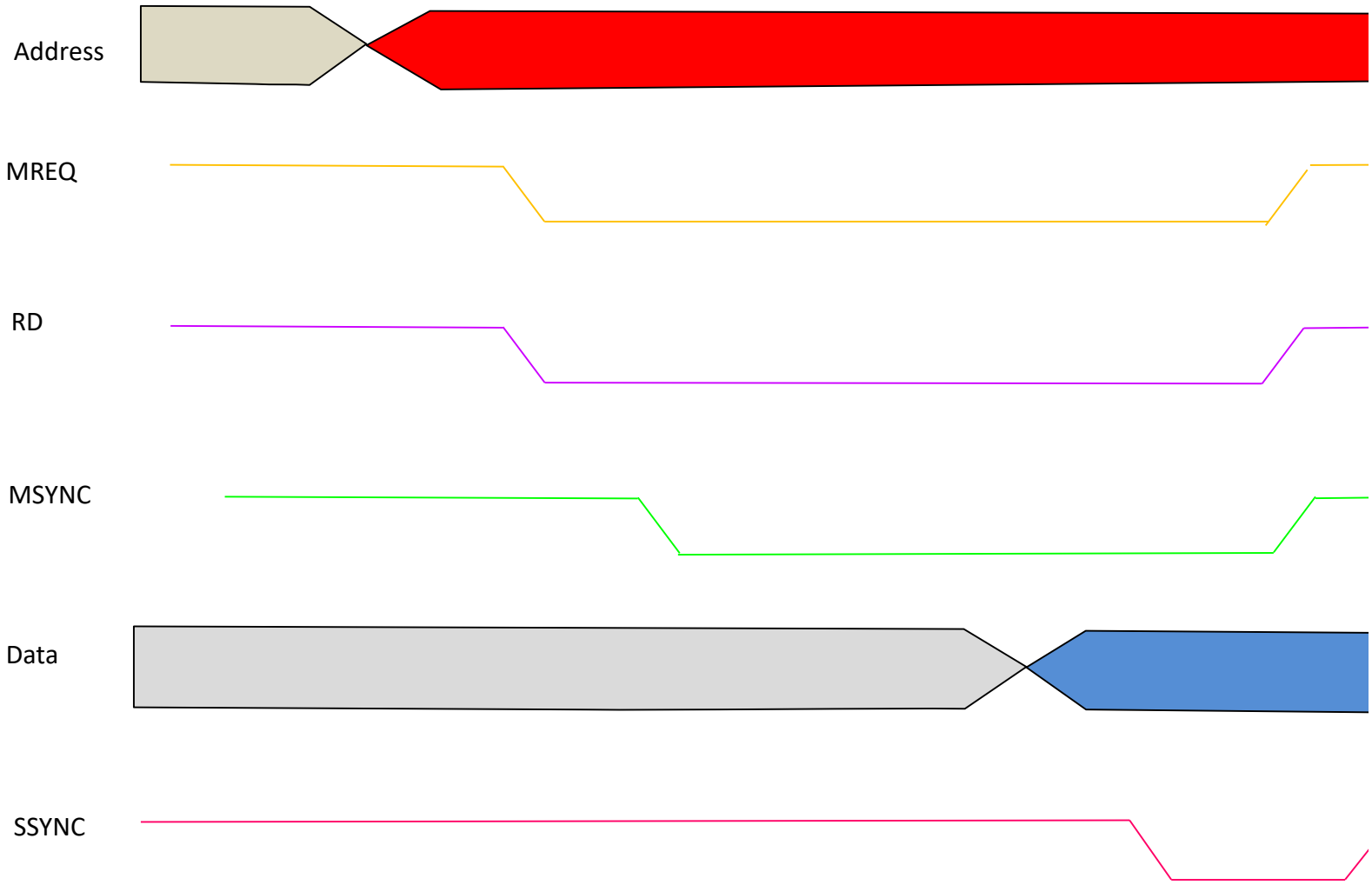
Once the change in the SSYNC value is complete, the CPU can begin transferring the data from the data lines to a desired register.



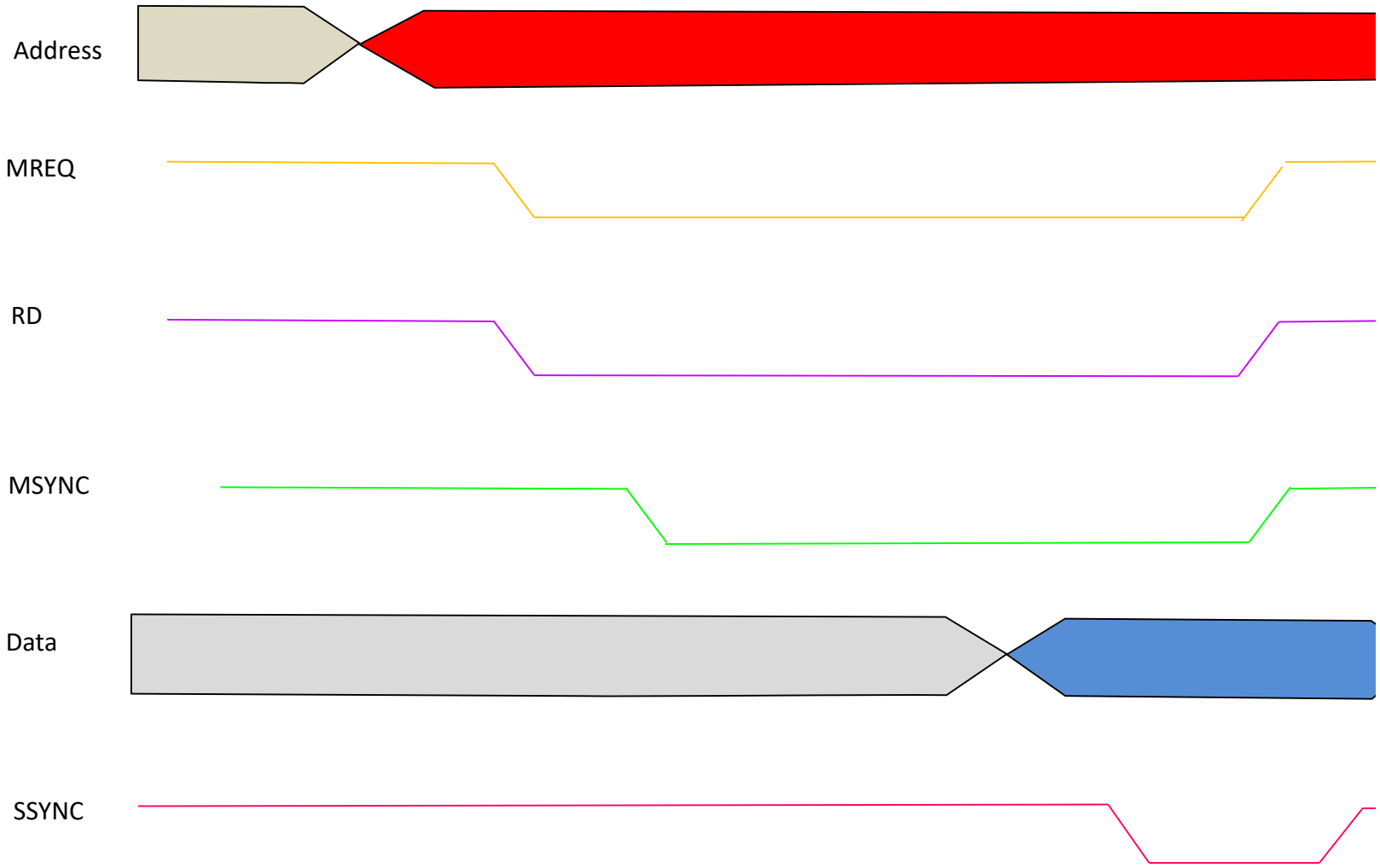
CPU begins to restore the MSYNC line to unasserted status (high). This indicates that it has completed transferring the data from the data lines. The MREQ and RD signals can also be returned to their unasserted status since, from the master device's perspective, the memory read request is complete



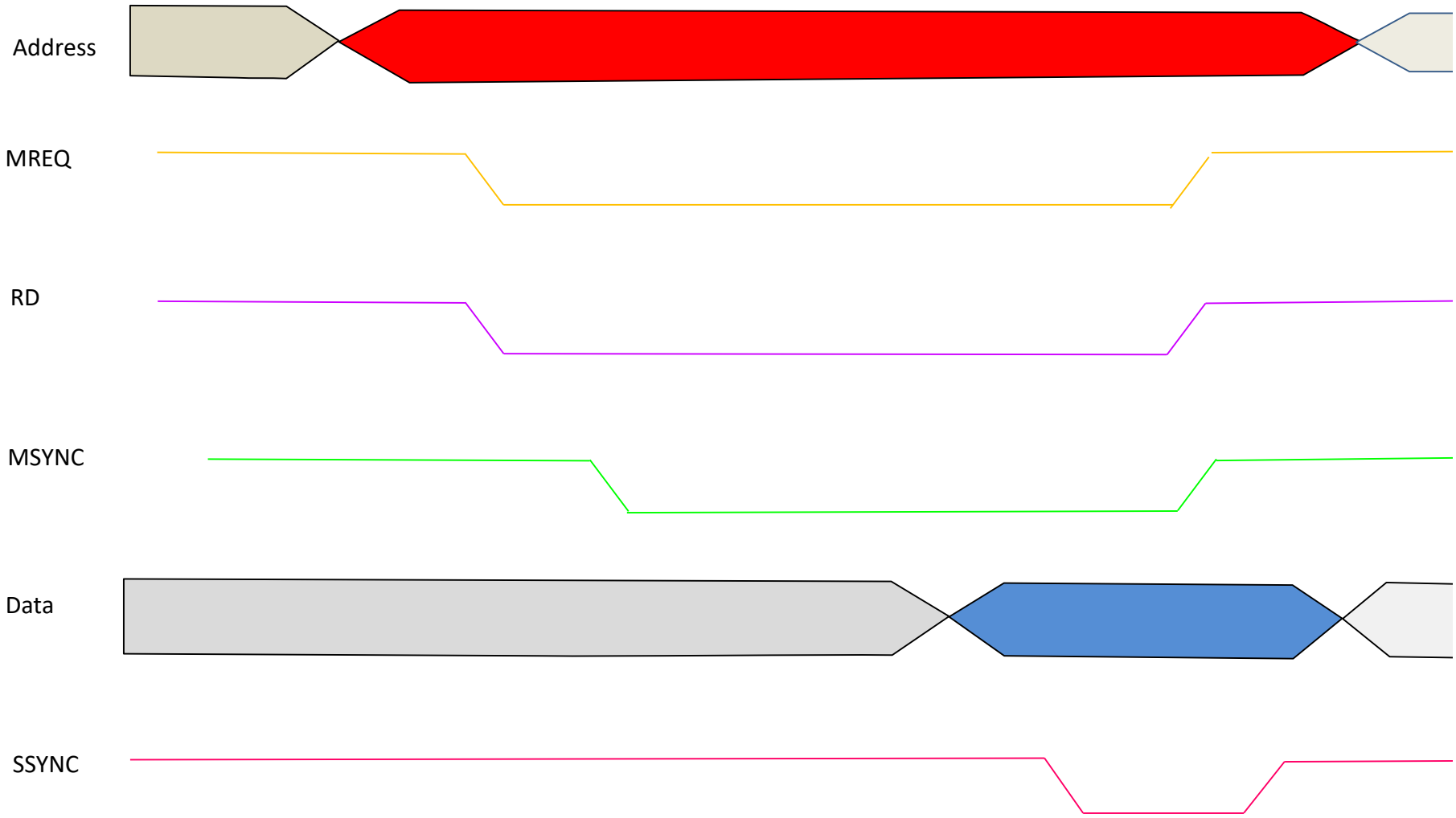
The restoration of the MSYNC, MREQ and RD lines to unasserted status (high) is complete



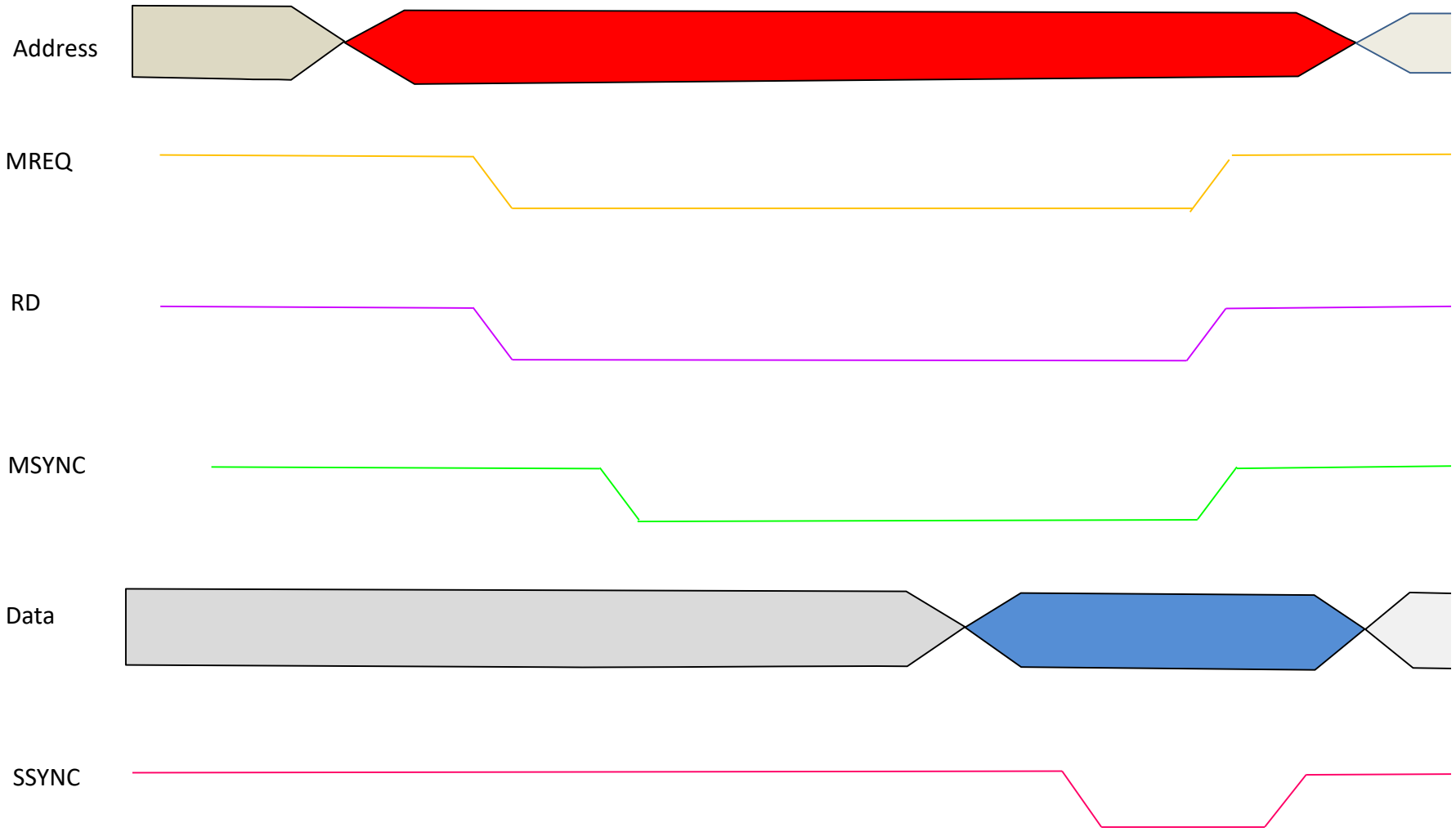
Once memory detects the change in MSYNC it begins restoring the SSYNC signal to the unasserted value



All control signals have now reached “rest state” values; that is their unasserted values.



The bus is ready for another transaction



Actions of a complete asynchronous read at a glance