Analog IC Design (Xschem, Ngspice, ADT)

Lab 05

Simple vs Wide Swing (Low Compliance) Cascode Current Mirror

Part 1: Exploring Sizing Tradeoffs Using SA

2)Sinking current means which device type? NMOS or PMOS?

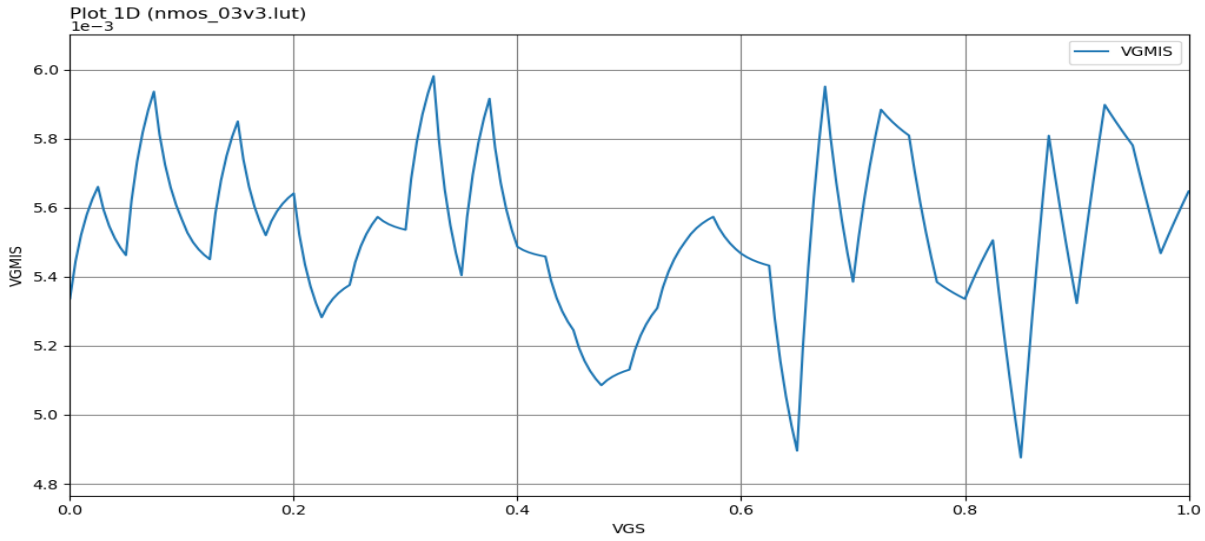
- NMOS

3)The % Change in current translates to a spec on the $\lambda = 1/V_A$ of the device. How much is the required λ?

$$\frac{\Delta i_{out}}{i_{out}} = \lambda \times \Delta V_{out} \longrightarrow \lambda < 0.1$$

```
46989 + par_vth=0.007148
46990 + par_k=0.007008
46991 + par_l=1.5e-7
46992 + par_w=-1e-7
46993 + par_leff='l-par_l'
46994 + par_weff='par*(w-par_w)'
46995 + p_sqrtarea='sqrt((par_leff)*(par_weff))'
46996
46997 .param
46998 + var_k='0.7071*par_k* 1e-06 / p_sqrtarea'
46999 + mis_k=agauss(0,var_k,1)
47000
47001 .param
47002 + var_vth='0.7071*par_vth* 1e-06 / p_sqrtarea'
```

From the model file :
Var_VTH=0.007148×0.0701= 5.05 mV



From ADT average here almost= 5.5mV, so ADT is higher The ADT value is higher because it often includes additional systematic variations or design-specific margins added for safety and robustness in real design scenarios, while the model file value represents more idealized or intrinsic process variation (σVt) without extra design overheads.

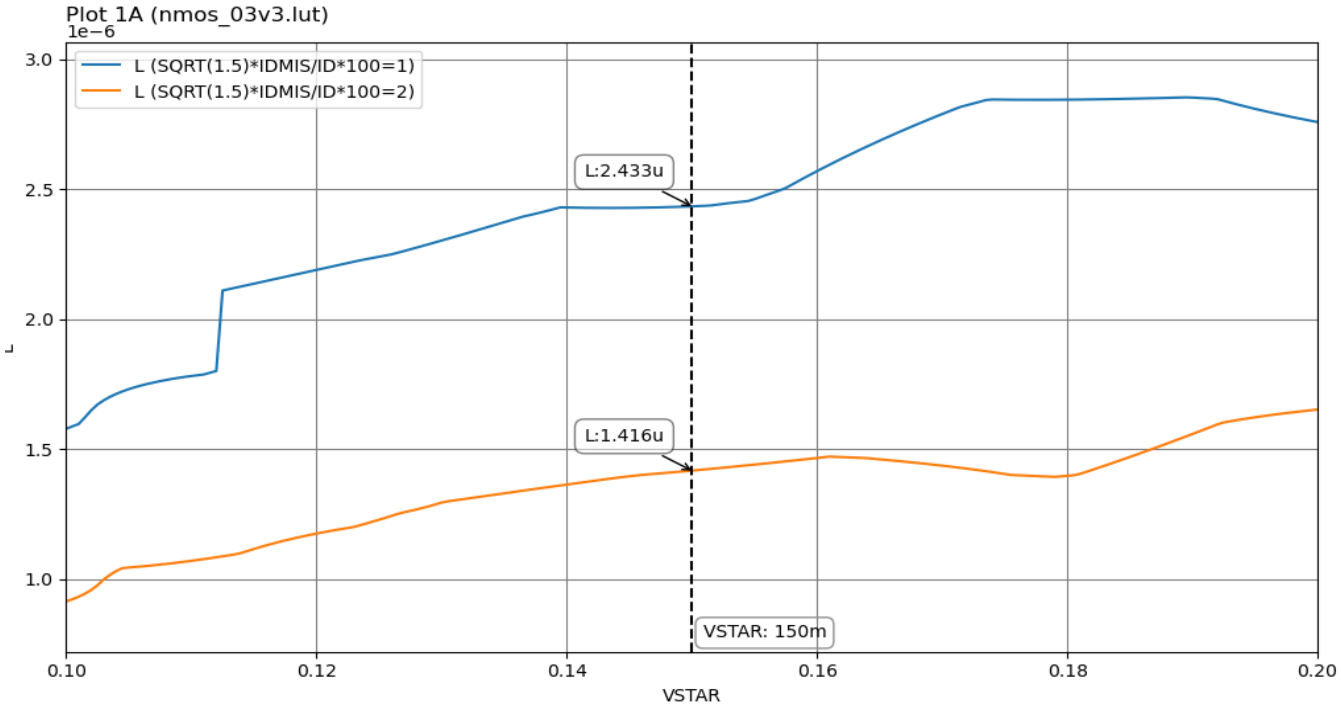


Figure 1;: L VS Vstar

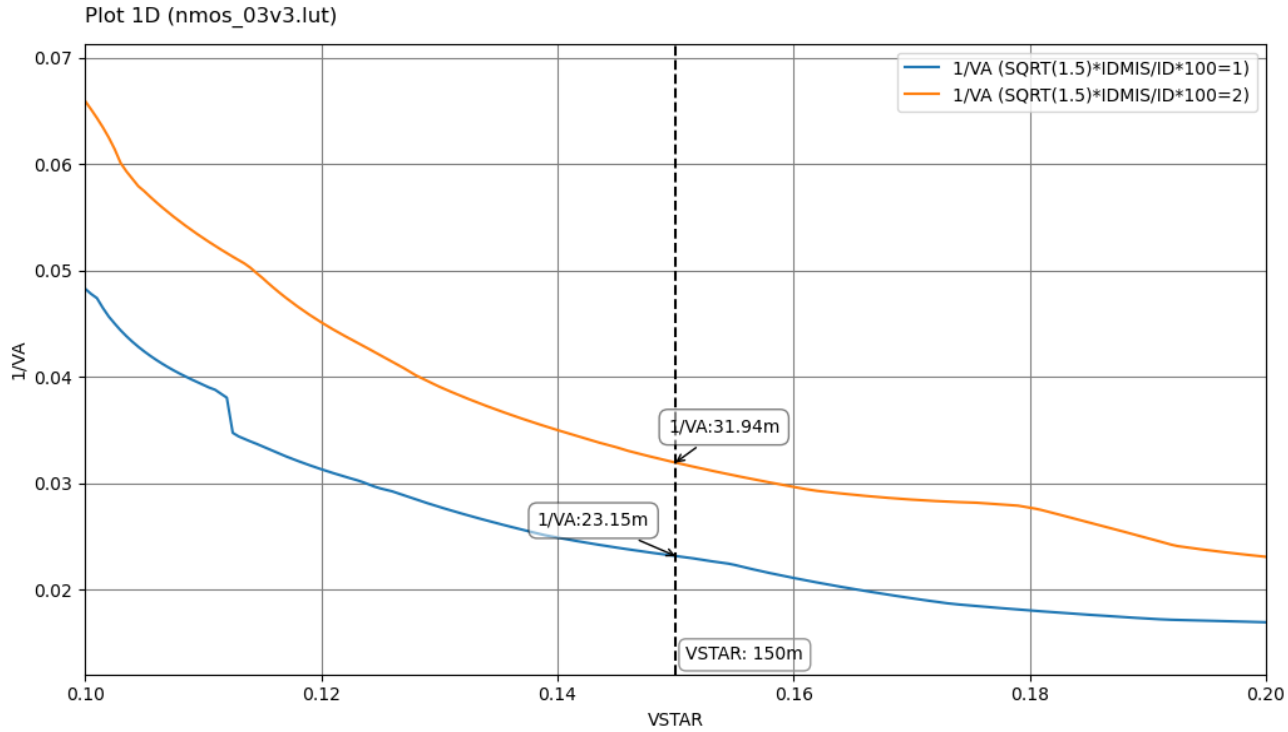


Figure2 : λ VS Vstar

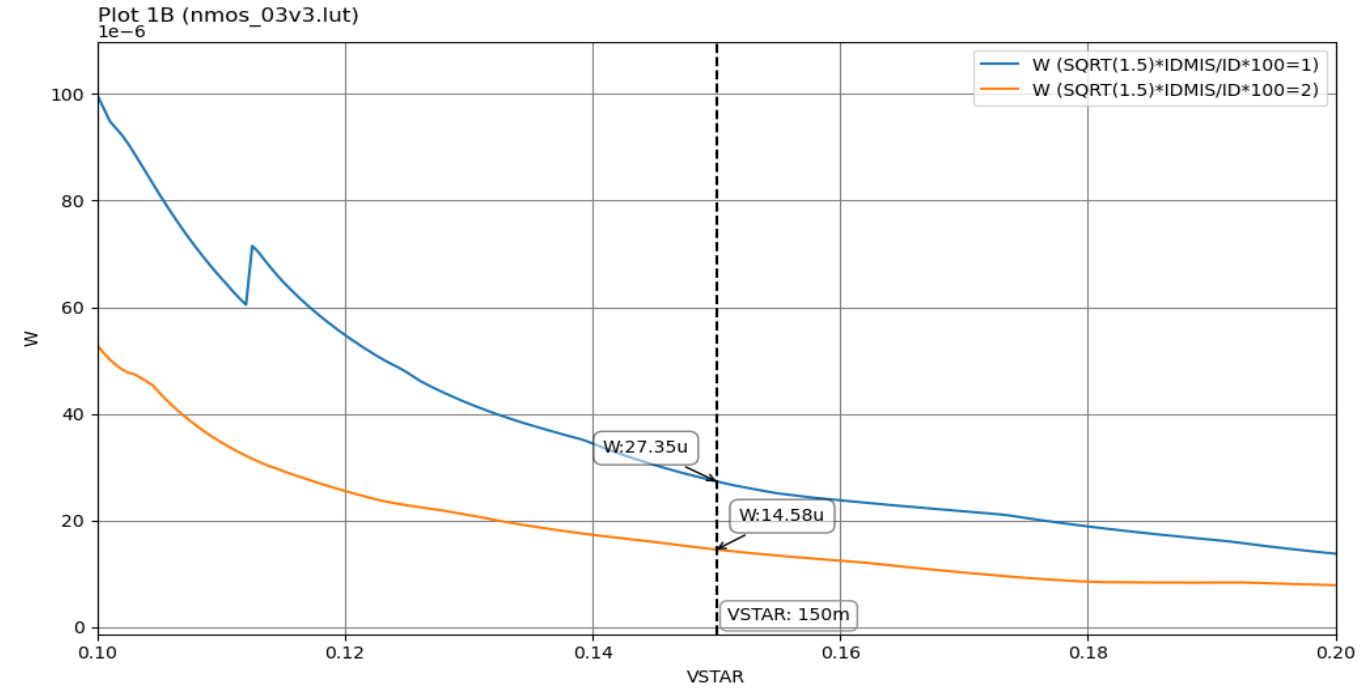


Figure 3: W VS vstar

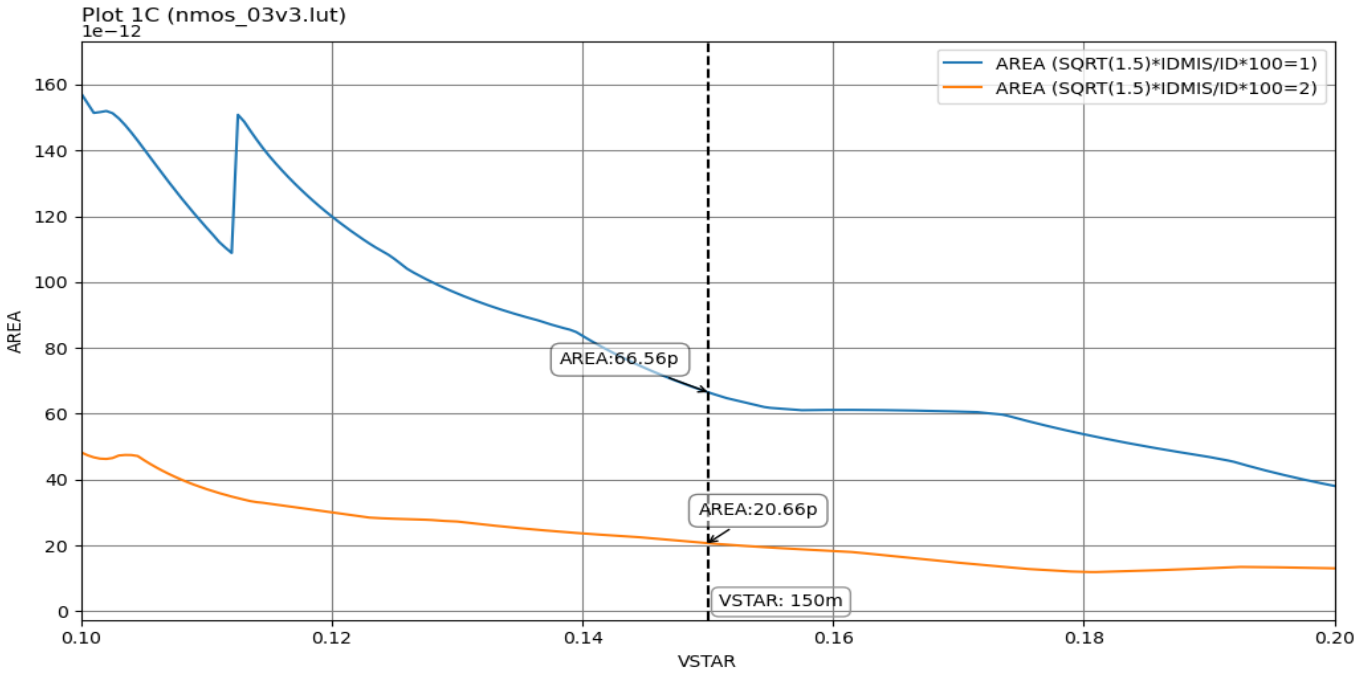


Figure 4: AREA VS Vstar

i will choose 1% Mismatch: Better Performance, But Costs More where Less sensitive to VOUT*VOUT* changes. More stable over process/temperature variations and achieve specs so we will find W=27,35u L=2.4334u λ=0.02315 V^{-1}

SO I don't have to make check in 2% Mismatch in Q 10,11

Part 2: Current Mirror Simulation

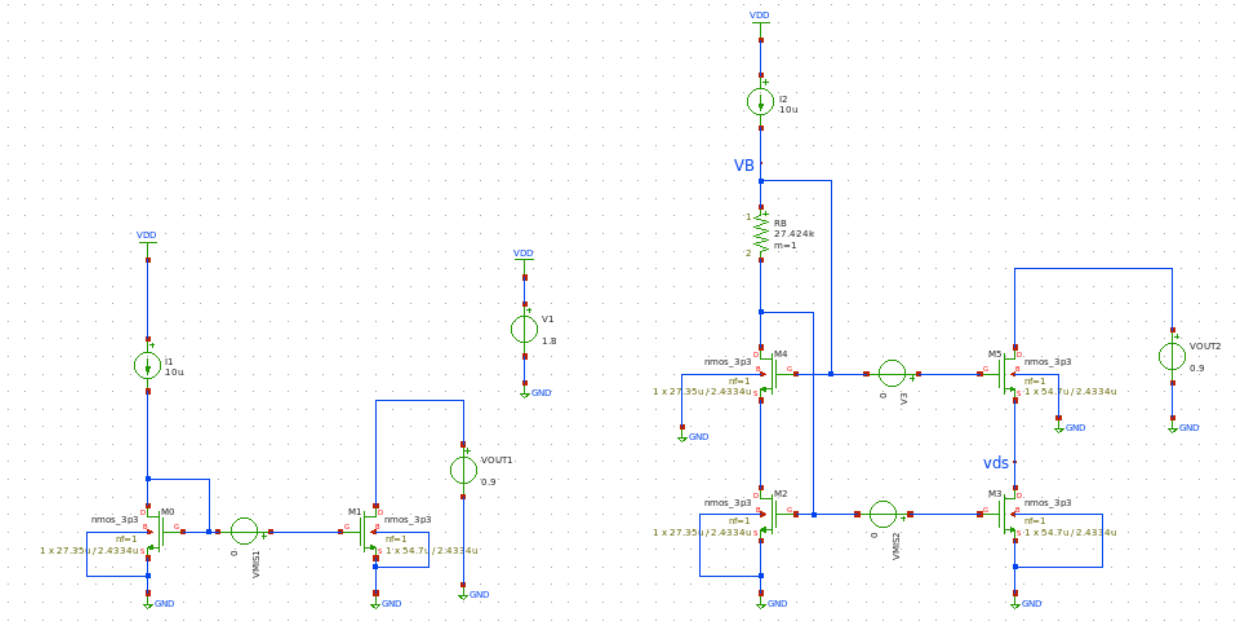


Figure 5:SHCEMATIC

1. Design and OP (Operating Point) Analysis

$$R_B = \frac{V_{GS4}+V_{DS2}-V_{GS2}}{I_B} \approx \frac{V_{DS2}}{I_B} \quad VDS2 \approx VDS3 \approx V* + 50mV \longrightarrow \text{RB=20KΩ}$$

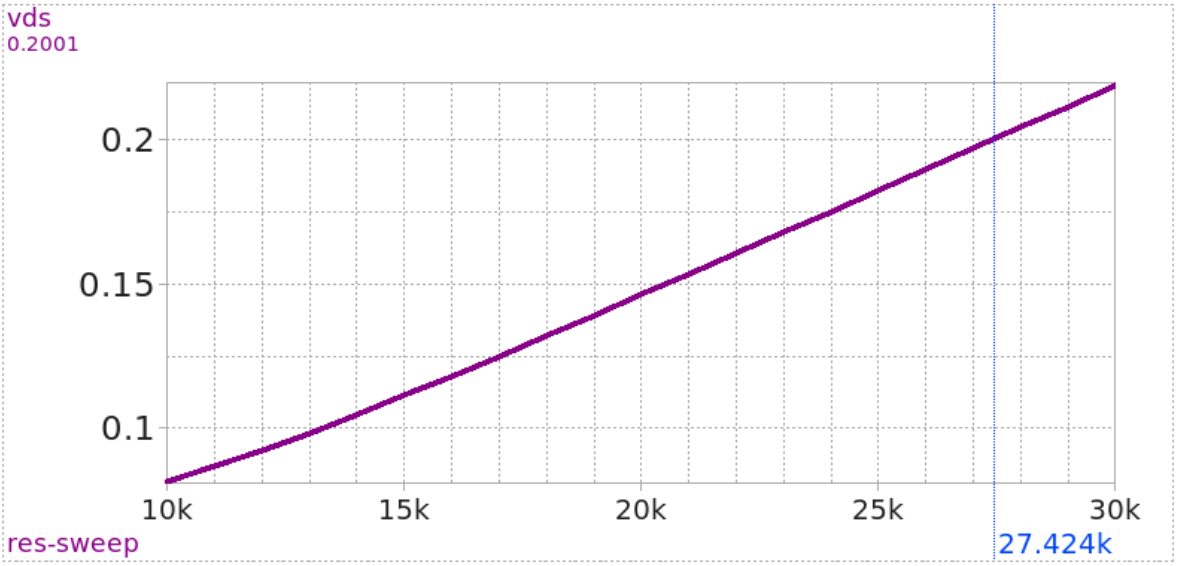
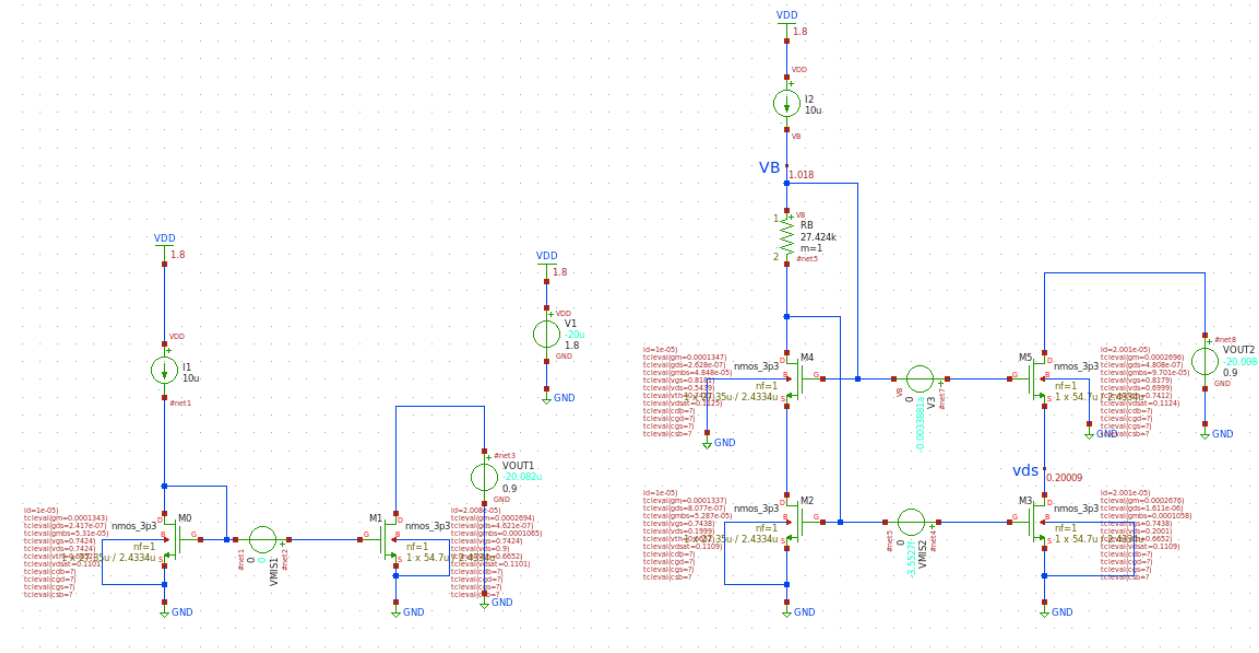
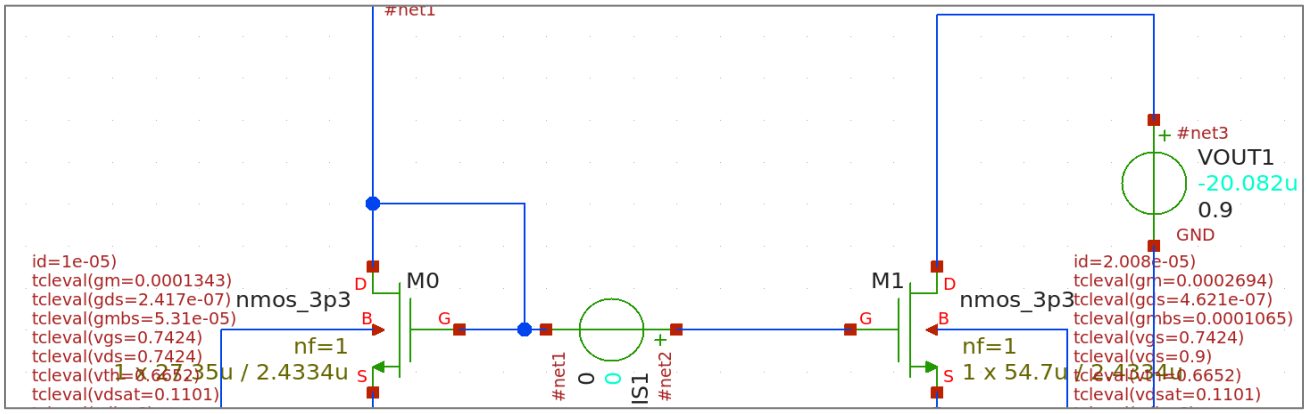


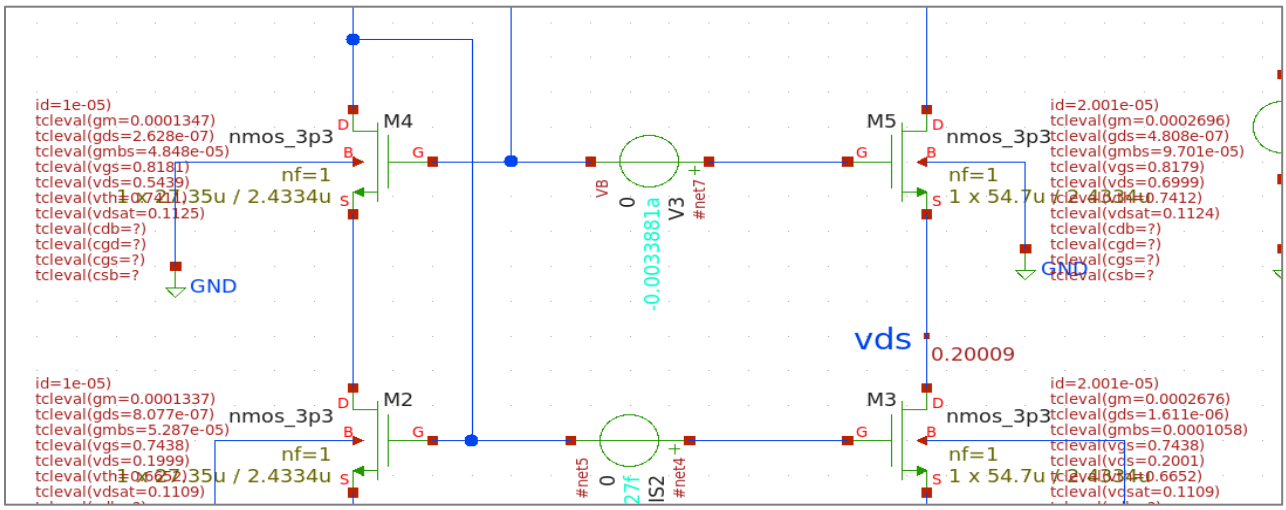
Figure 6: VDS VS RB

AS show from simulation RB=27.424K , Simulation accounts for real-world effects missed in hand calculations as Body Effect which Increases VTH of cascode devices, requiring higher VGS (and thus larger *RB*). so RB must be bigger in simulation

1) Simulate the OP point. Report a snapshot clearly showing the following parameters.







All transistors have VDS>VDSAT , so all work in saturation

2. DC Sweep (I_{out} vs VOUT)

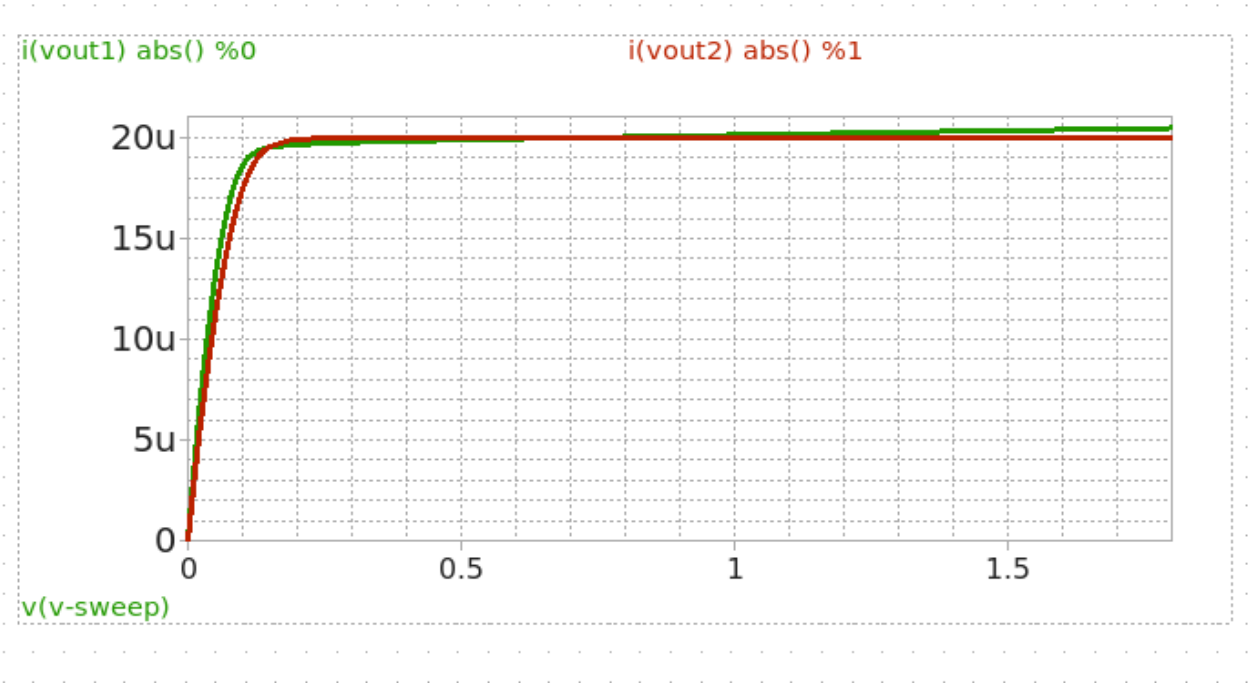
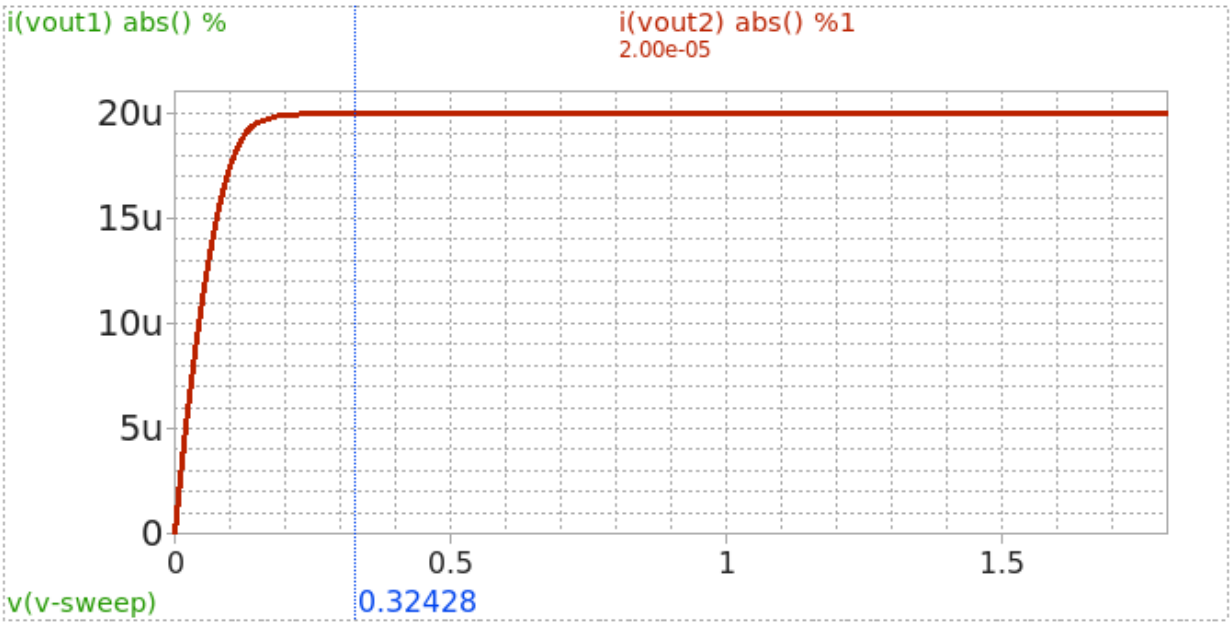
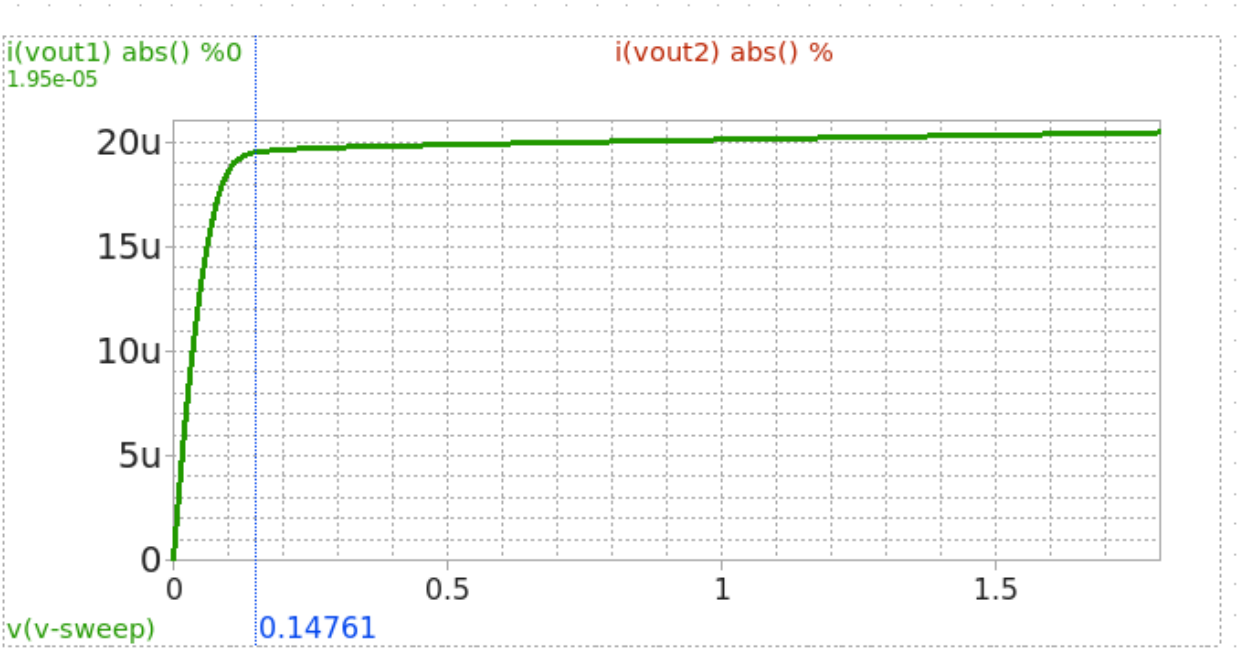


Figure 1: id1(simple cm) & id2(wide swing) VS VOUT

find an estimate for the compliance voltage of each current mirror.



Vcomp(wide swing) almost = 0,32428V



Vcomp(simple CM) almost = 0.14761 V

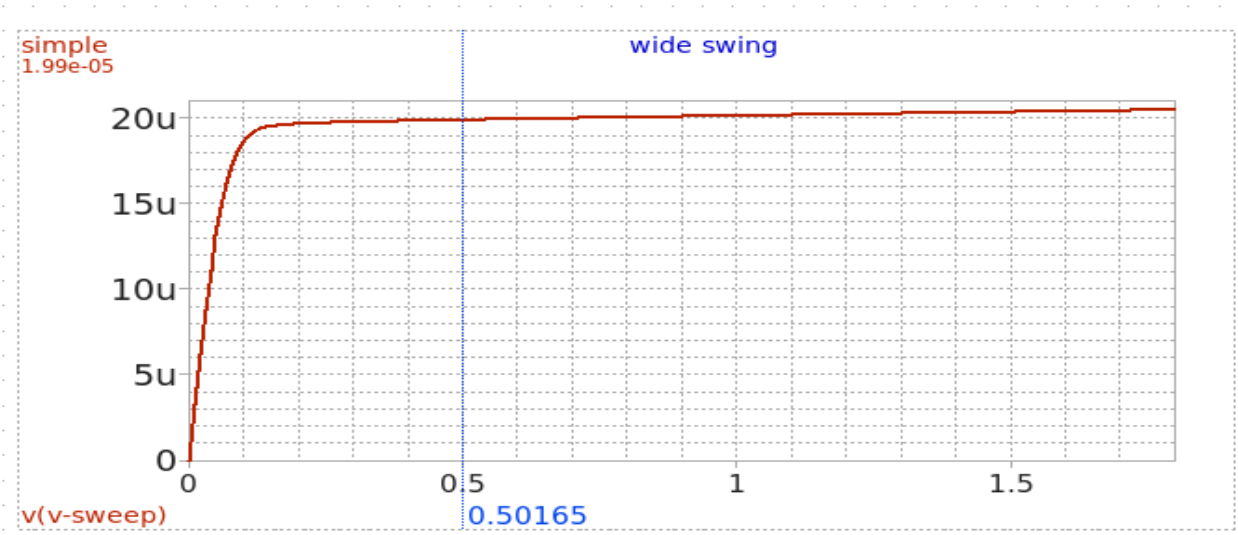
Comment on the difference between the two circuits

The wide-swing mirror has a larger compliance voltage than the simple mirror, but maintains more stable current by suppressing channel-length modulation through its cascode structure. The simple mirror operates at lower voltage but shows greater current variation

I_{out} of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?

Due to accurate mirroring where vgs1=vgs0 and W1=2*W0 , SO Iout=2*IB

2)



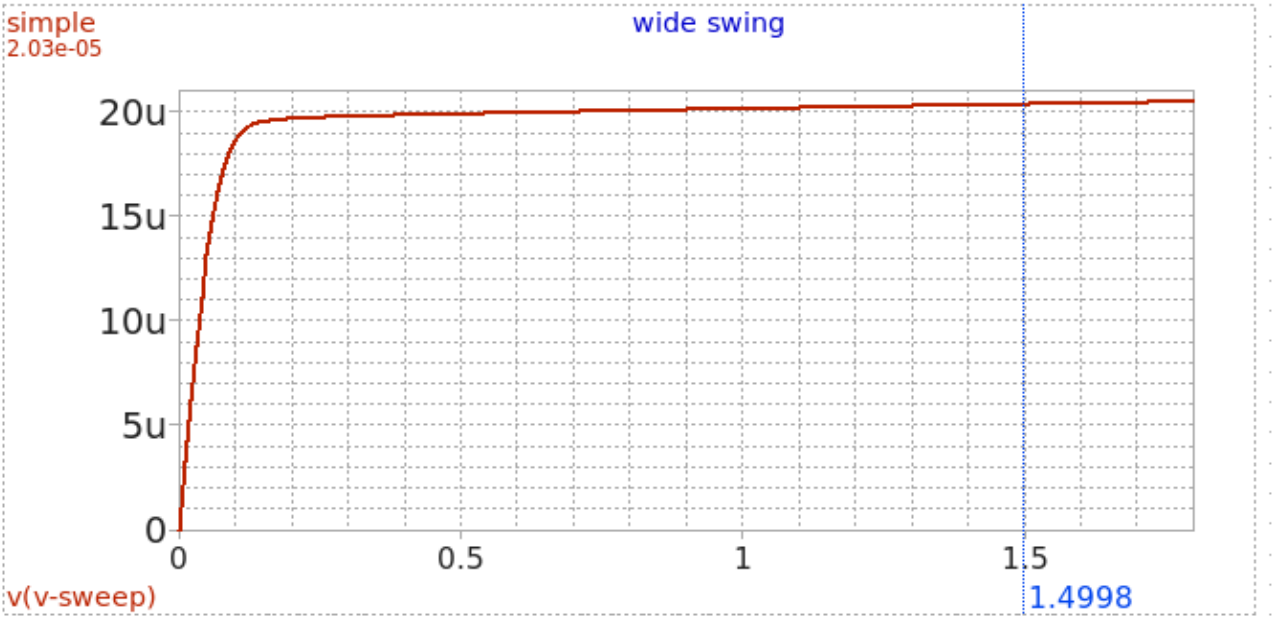


Figure: ID VS VOUT AT 1.5V

so from 2 previous graphs:

$$\frac{i_d(1.5V)\text{-}i_d(0.5V)}{i_d(0.5V)} \times 100 = \frac{20.3\text{-}19.9}{19.9} \times 100 = 2.01\% < 10\%$$

expected from Part 1:

$$\frac{\Delta i_{out}}{i_{out}} \times 100 = \lambda \times \Delta V_{out} \times 100 = 0.02315 \times 1 \times 100 = 2.32\%$$

3)

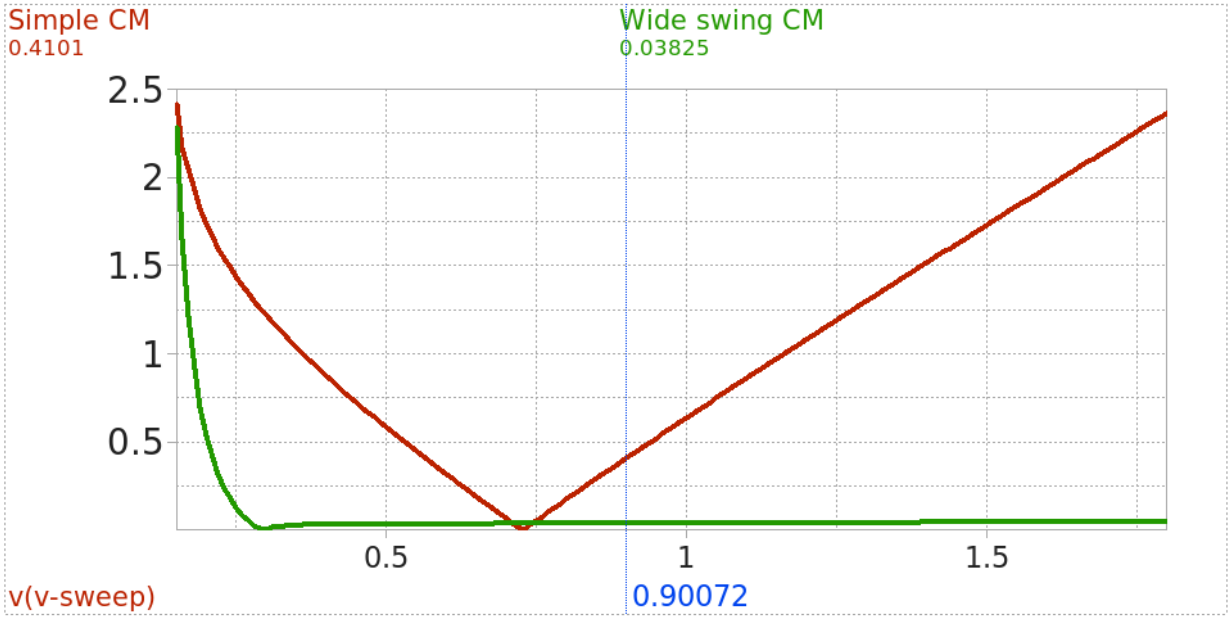


Figure 2: percentage of error iout vs vout

AS shown error from simulation :

Simple CM = 0.4101% wide swing cm =0.03825%

Error analytical:

Simple cm = $\frac{20.08-20}{20} \times 100 = 0.4\%$ wide swing cm=$\frac{20.01-20}{20} \times 100 = 0.05\%$

The wide-swing current mirror's smaller error (0.05% vs. 0.4%) comes from its cascode transistor suppressing channel-length modulation (CLM) Simple Mirror :Output transistor's drain voltage (VDS) varies with VOUT and Wide-Swing Mirror :Cascode fixes the drain voltage of the output transistor

4)

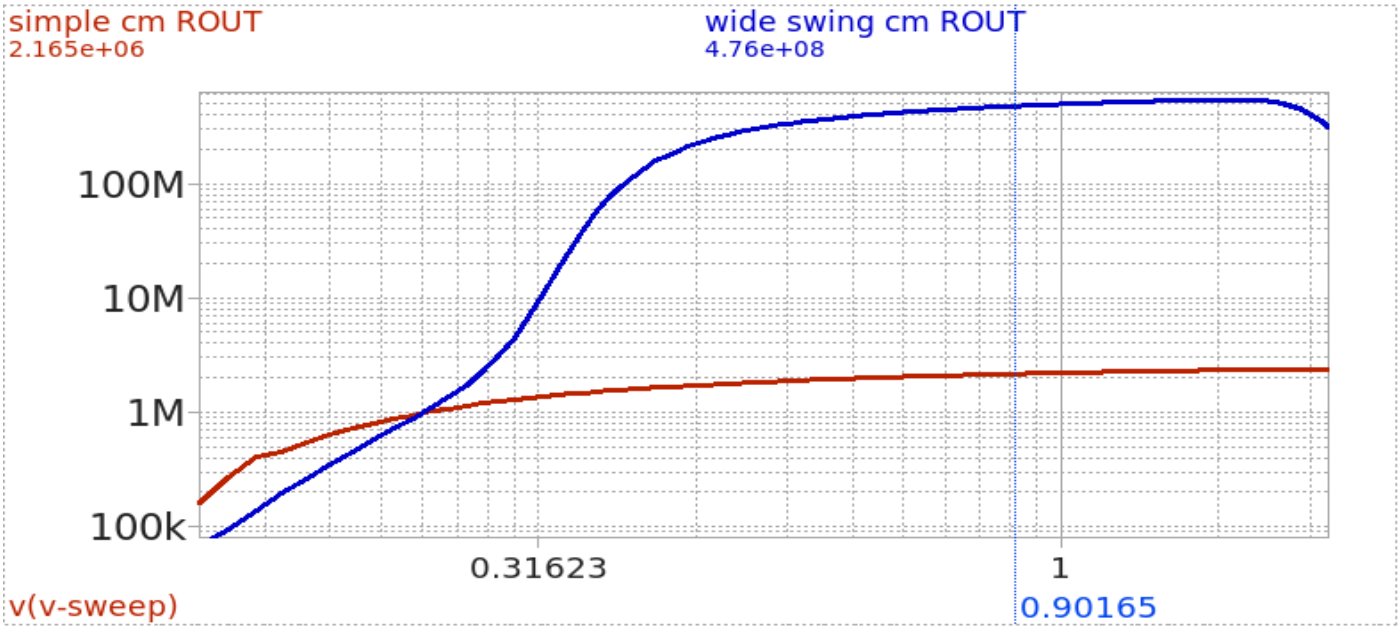


Figure: ROUT VS VOUT (LOG X LOG Y SCALE)

AS shown FROM SIMULATION:

Simple cm ROUT=2.165 MΩ Wide swing cm ROUT = 476 MΩ

Analytically :

Simple cm ROUT = $\frac{1}{gds1}$ =2.164 MΩ Wide swing cm ROUT =ro5 + ro3 [1+ (gmbs5 + gm5)*ro5] = 476.01 MΩ

Accuracy very high

Comment on the difference between the two circuits.

Wide-swing Rout is bigger because:Cascode adds its own ro in series and Blocks VOUT variations from output transistor

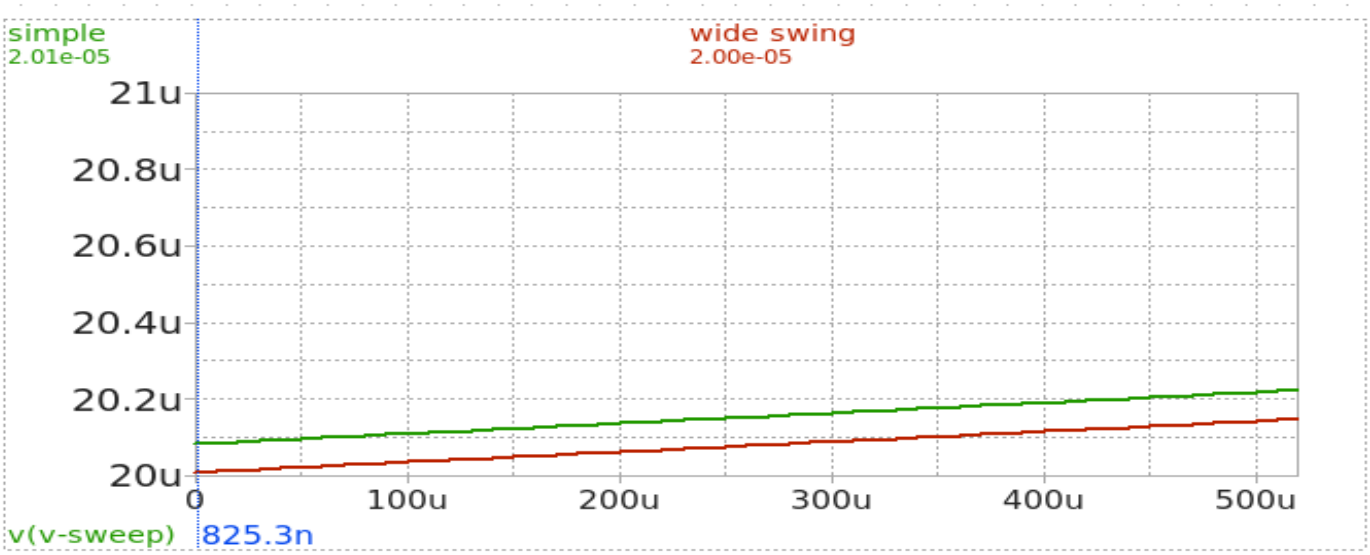
Does Rout change with VOUT? Why?

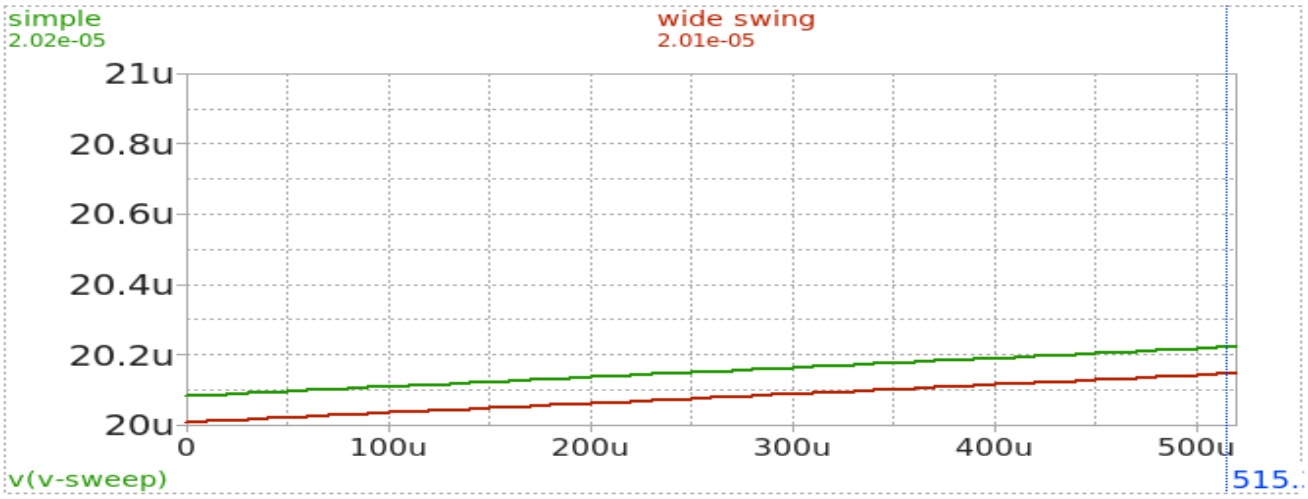
Yes, because output resistance (Rout) depends on VDS (vout) where Rout ∝ 1/λ(VDS) vds= vout

3. Mismatch

sqrt(1.5)*3.5m/sqrt(W*L*1e12) = 0.525 mV

1) id vs vmis1 dc sweep from 0 to 0.525mV :





from simulation :

percentage of error in id(simple cm) = $\frac{20.2\text{-}20.1}{20.1} \times 100 = 0.4975\%$

percentage of error in id(wide swing cm) = $\frac{20.1\text{-}20}{20} \times 100 = 0.5\%$

analytical:

percentage of error in id(simple cm) = $\frac{\Delta Vmis1 \times gm1}{id} = 0.6924\%$

percentage of error in id(wide swing cm) = $\frac{\Delta Vmis1 \times gm3}{id} = 0.68769\%$

id vs vmis2 dc sweep from 0 to 0.525mV

I used this code to detect ymin and ymax ;

s8 .endc

```
.control
save all
dc VMIS3 0 0.525m 0.01m
run

* Create absolute value vector first
let iout_abs = abs(i(vout2))

* Measure using the pre-defined vector
meas dc ymin_val MIN iout_abs
meas dc ymax_val MAX iout_abs

write lab_05_DC.raw
.endc
```

And the result was :

```
ymin_val                =  2.000765e-05 at=  0.000000e+00
ymax_val                =  2.000826e-05 at=  5.200000e-04
```

simulation

percentage of error in id(wide swing cm) = $\frac{y_{max}-y_{min}}{y_{min}} \times 100$ = 0.003049%

analytical:

percentage of error in id(wide swing cm) = $\frac{\Delta Vmis2\times(gm5+gmb3)}{id(1+(gm5+gmb5)ro3}$ =0.0041%

5)Which mismatch contribution is more pronounced? Why?

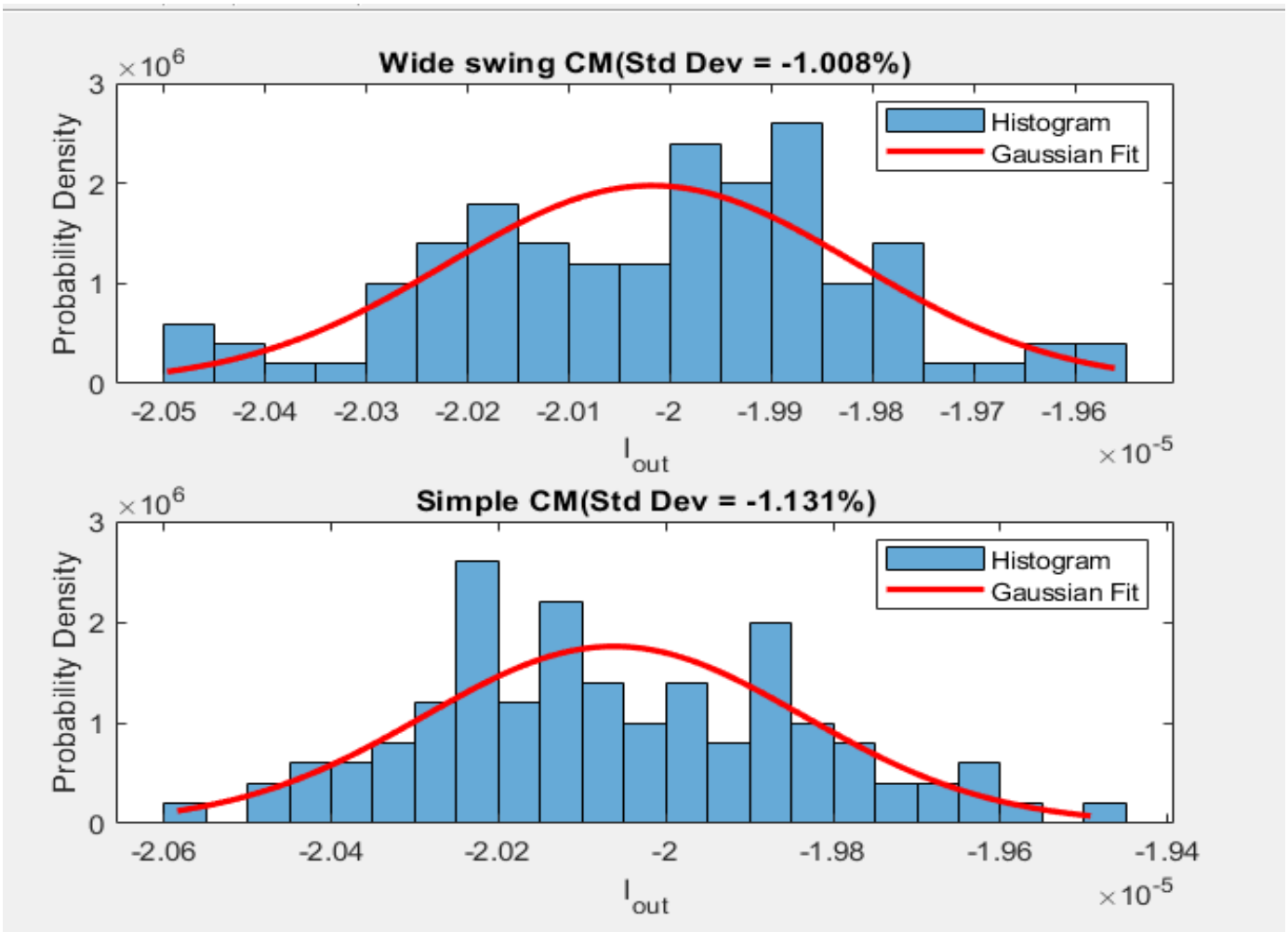
VMIS1 (mirror device mismatch) dominates because:

Direct current control - VMIS1 affects VGS(strong voltage), which exponentially governs current (ΔIout ≈ gm·ΔVTH).

Weak cascode influence - VMIS2 only modulates VDS(weak voltage), causing minor current variation through channel-length modulation.

6) Using larger W/L for the mirror devices is superior because: Cascodes can use minimum sizes (saving area) since their mismatch matters lessMaintains high output resistance while optimizing area

4. Monte Carlo (MC) Simulation



Expected Mismatch: 1% Simulated Mismatch: 1.008% (Standard Deviation) Agreement: Excellent (only 0.008% deviation) so MC confirms our analytical models are reliable for this design.

THE END .....