Analog IC Design
Lab 09 (Mini Project 01) Two-Stage Miller OTA

Part 1: gm/ID Design Charts

1) For L = 0.28u

PMOS:

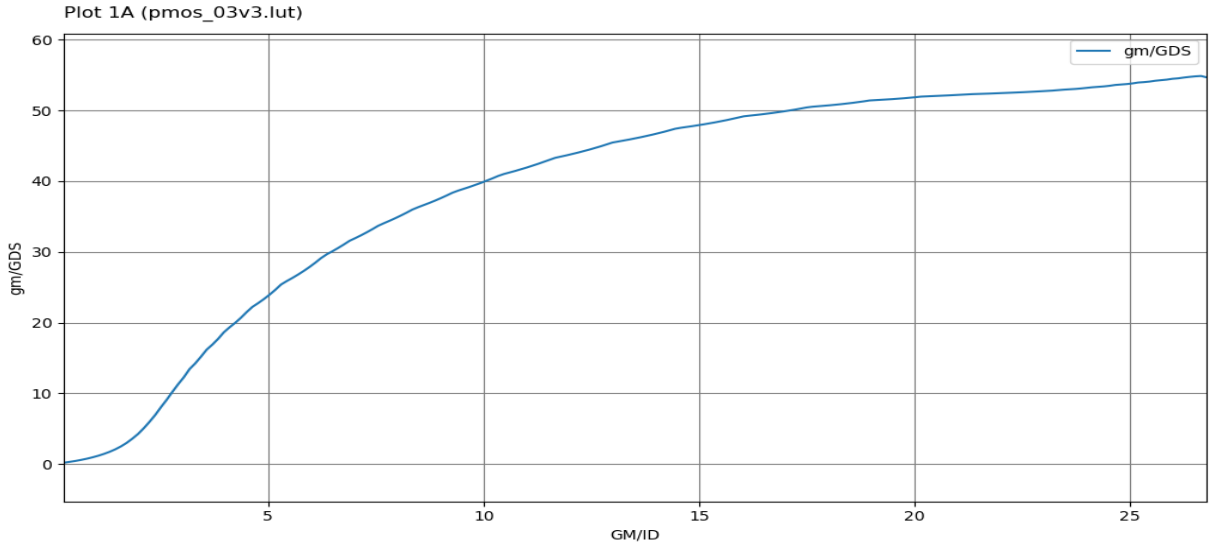


Figure 1: intrinsic gain

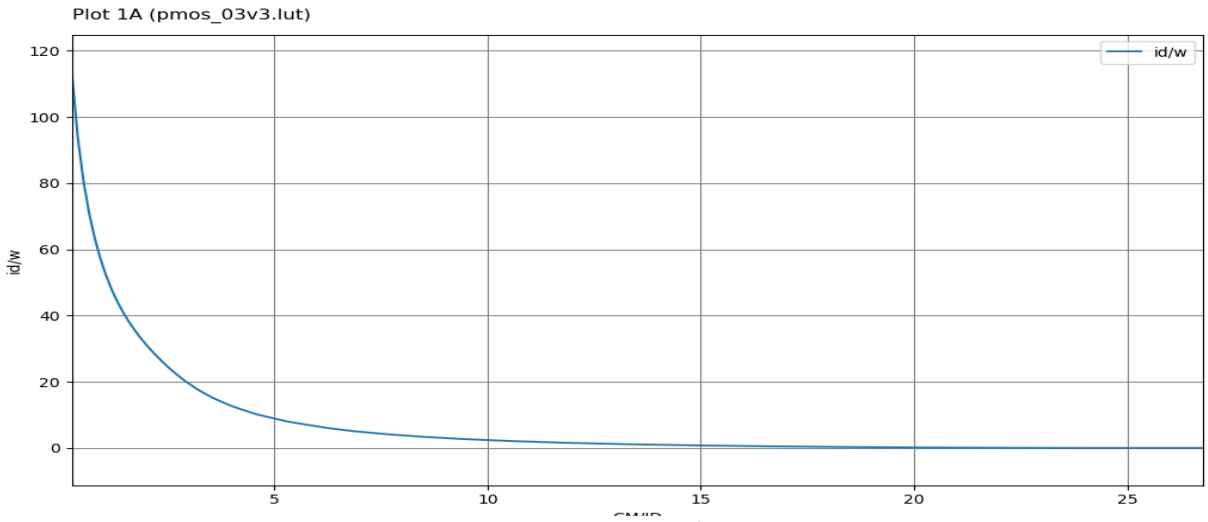


Figure 2: ID/W

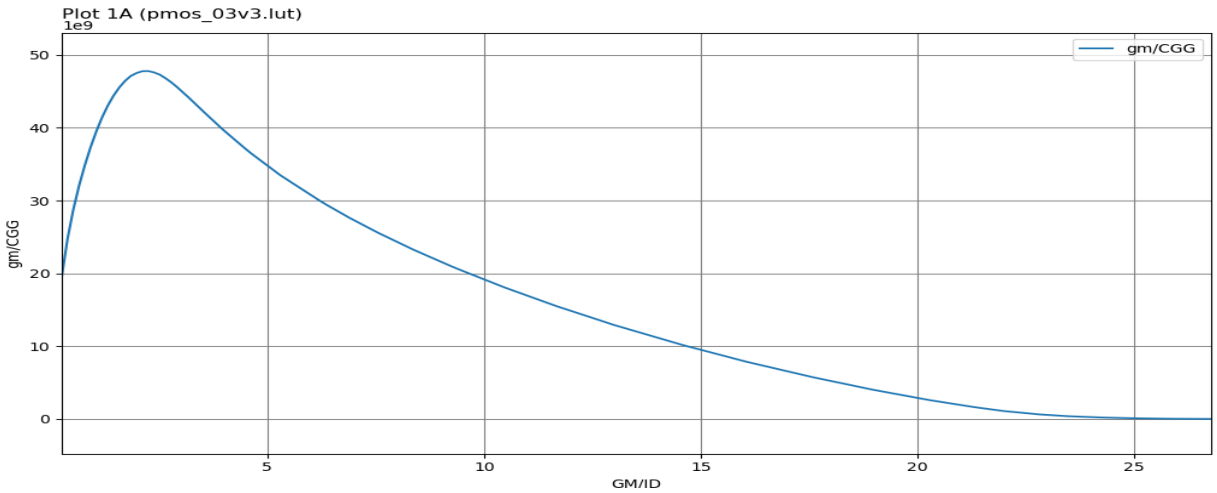


Figure 5:GM/CGG

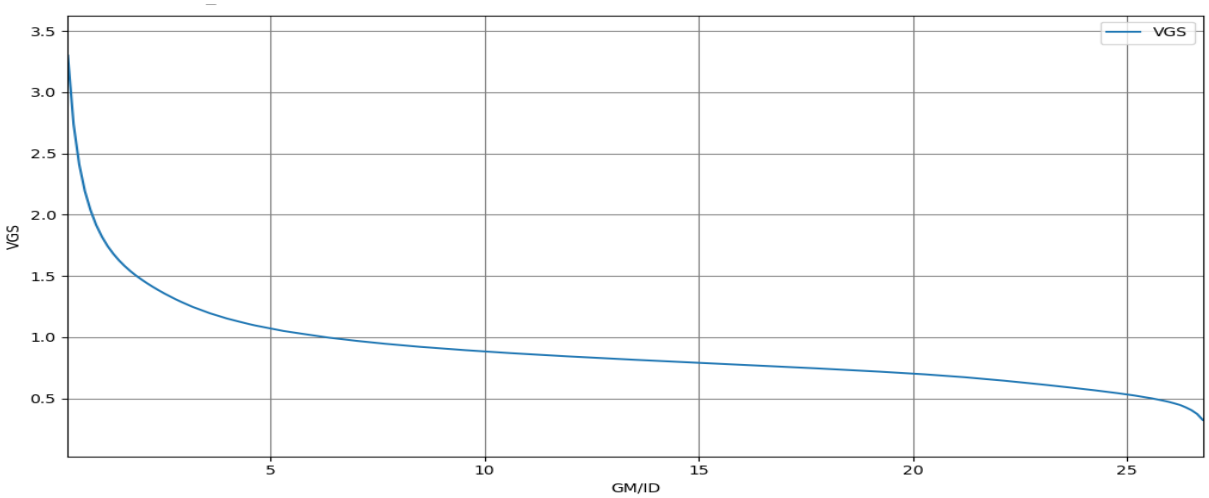


Figure 4:VGS

NMOS

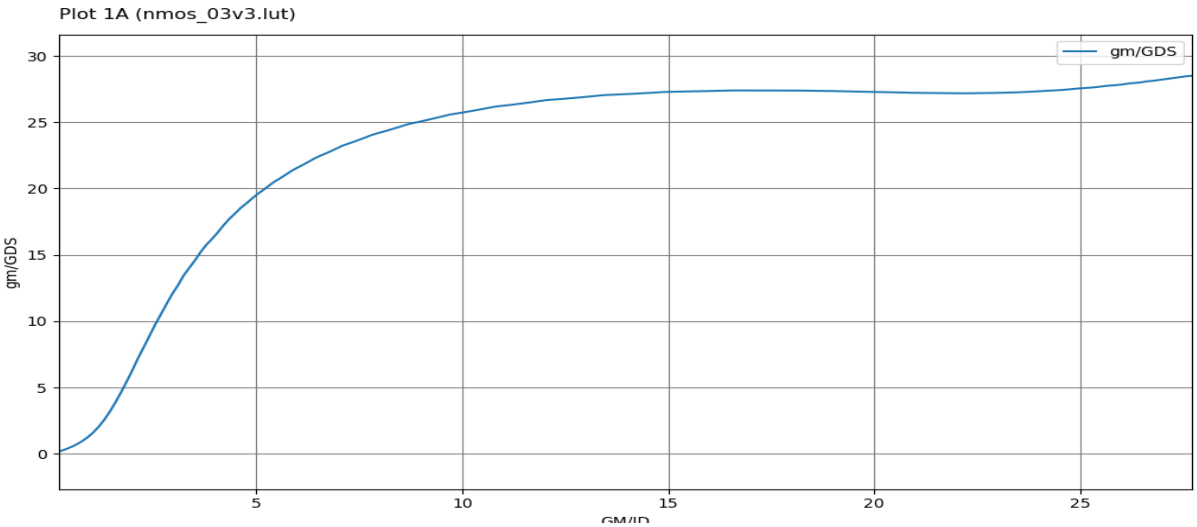


Figure 3: intrinsic gain

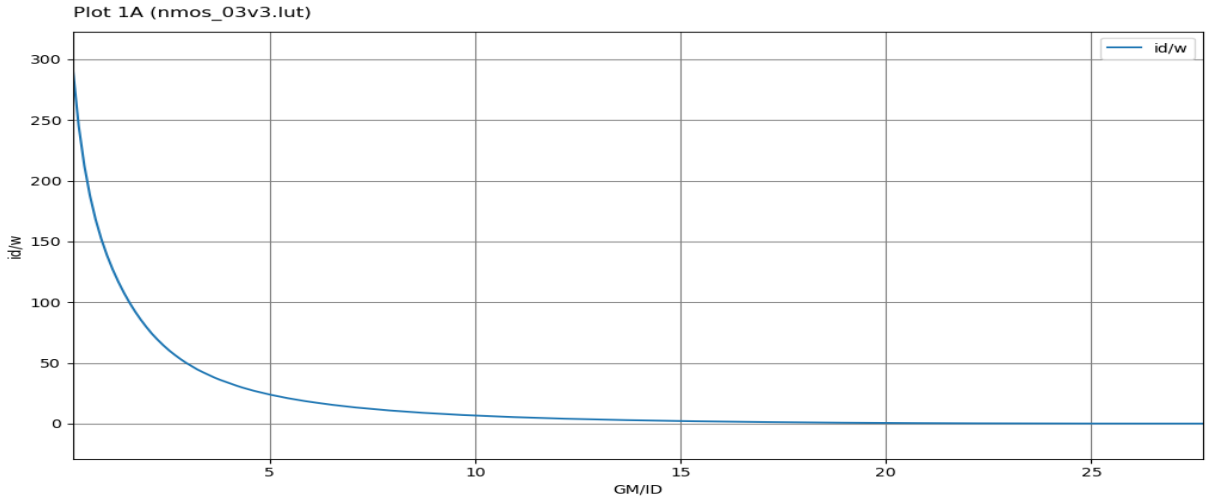


Figure 8:ID/W

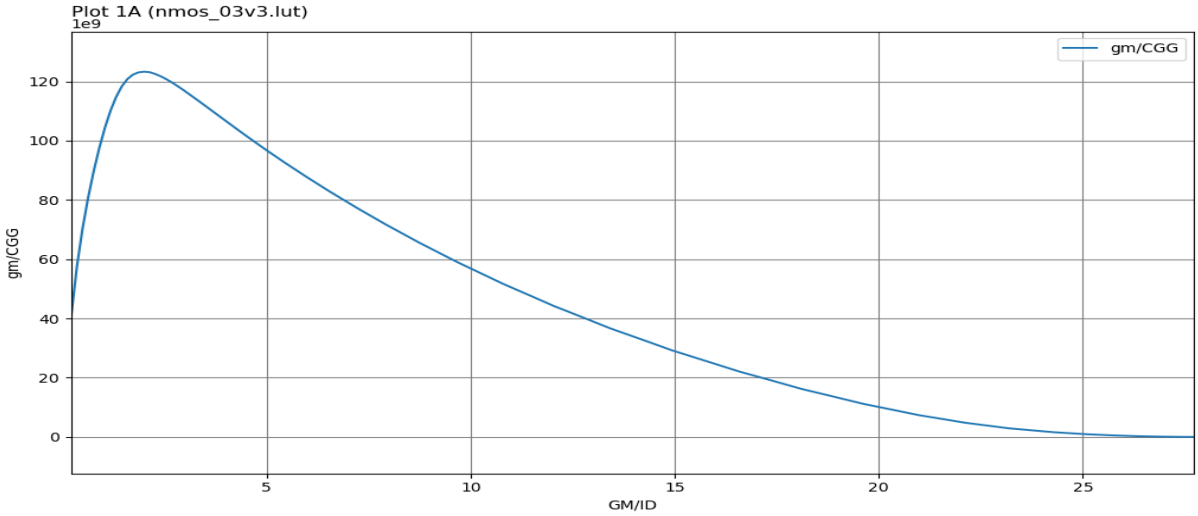


Figure 7:GM/CGG

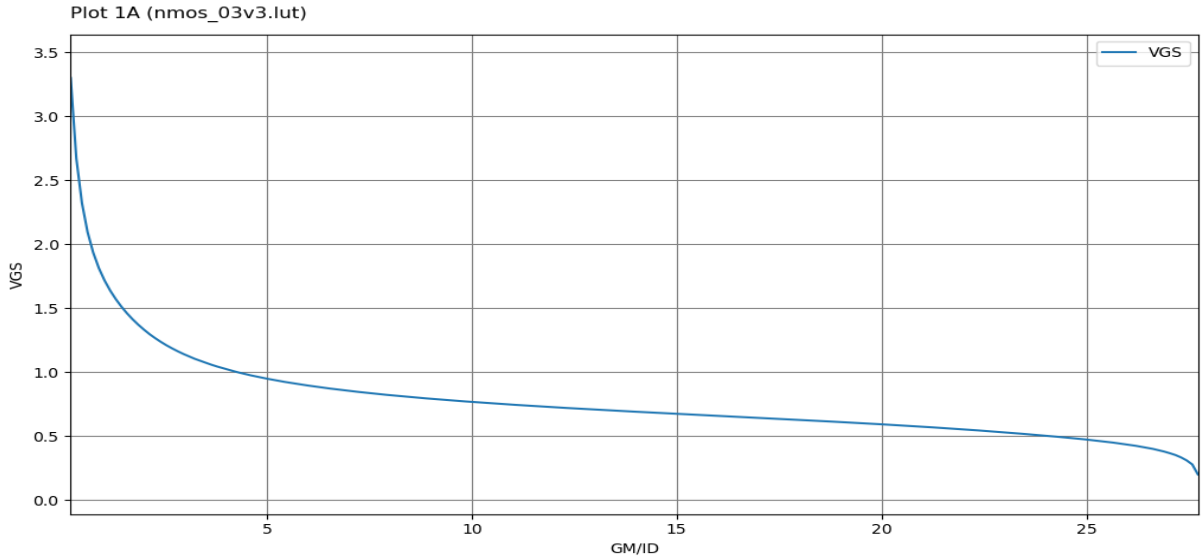


Figure 6:VGS

For L=0.4u:0.4u:2u

PMOS:

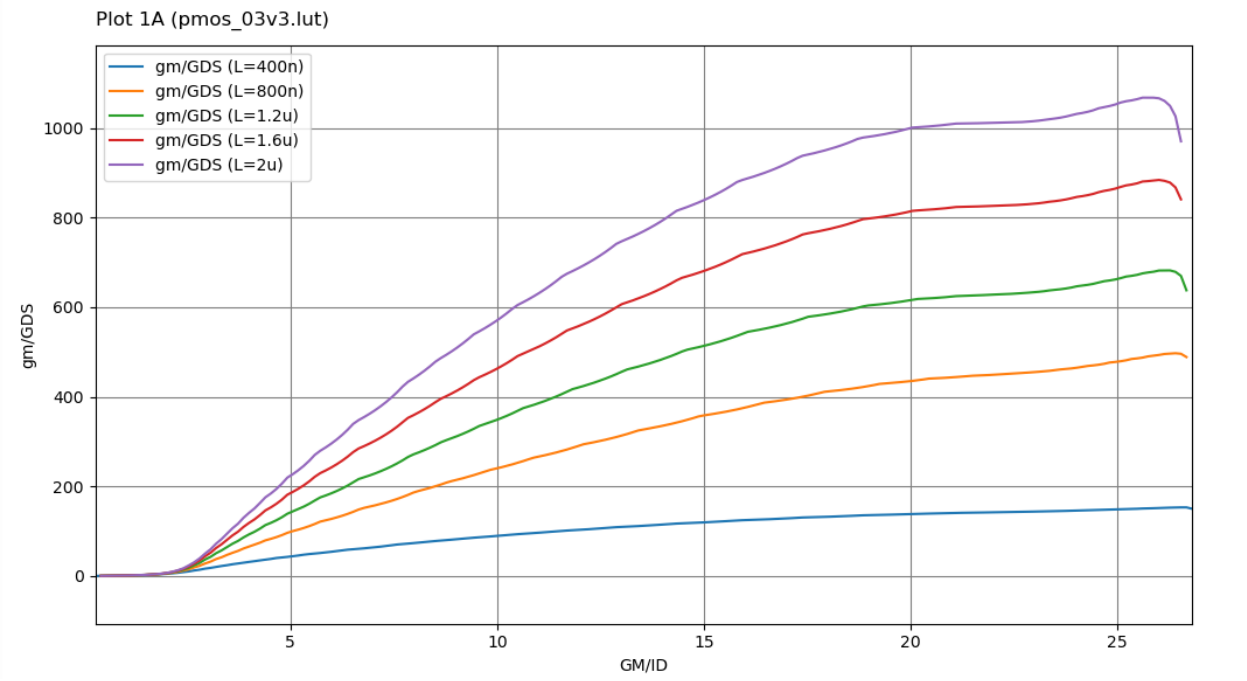


Figure 9:intrinsic gain

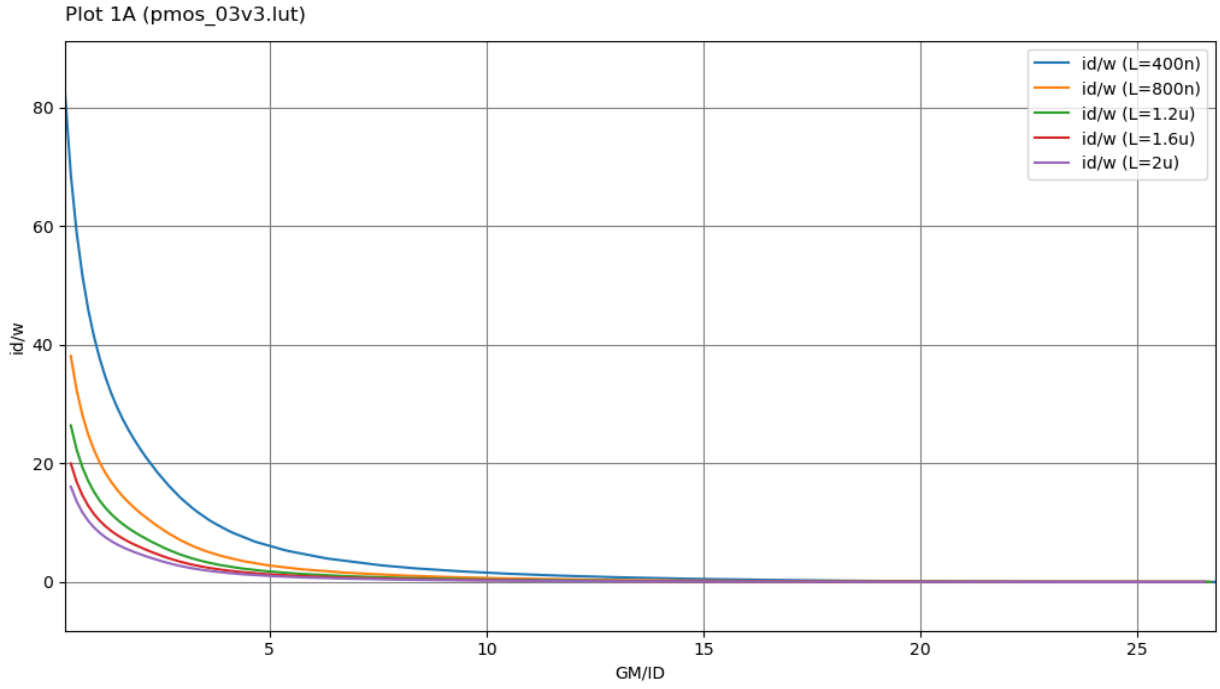


Figure 10:ID/W

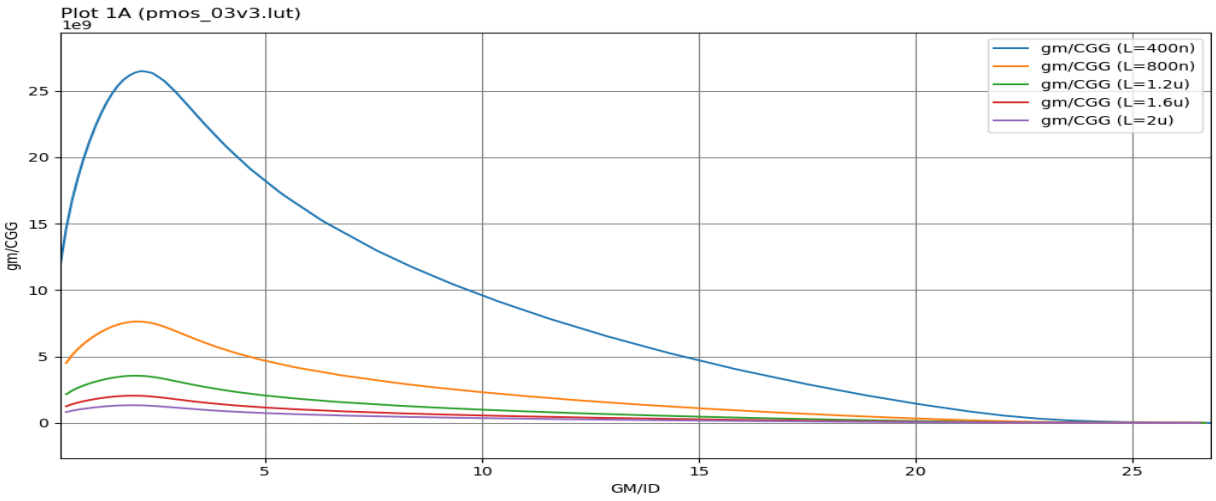


Figure 12:GM/CGG

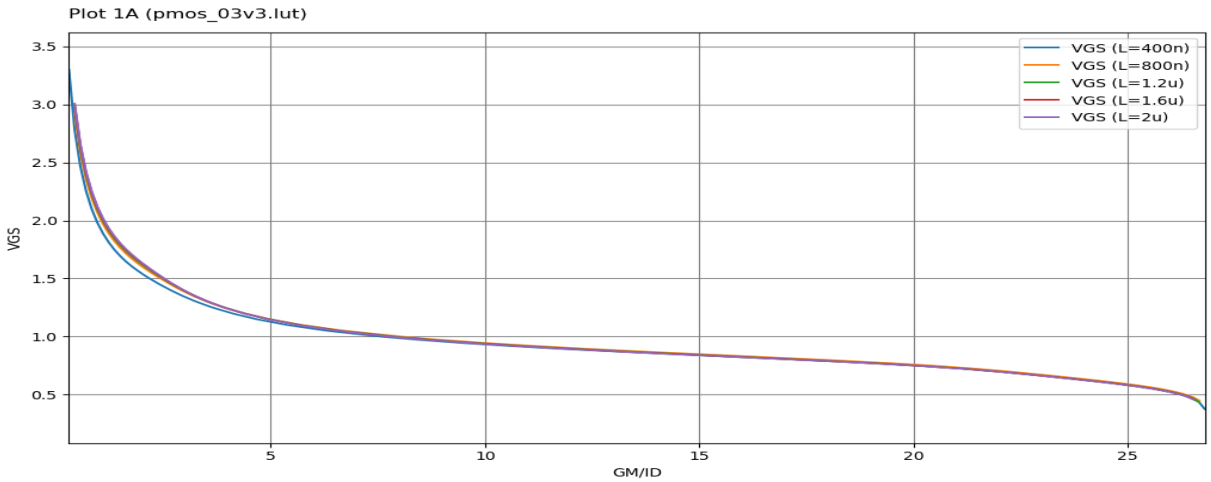


Figure 11:VGS

NMOS:

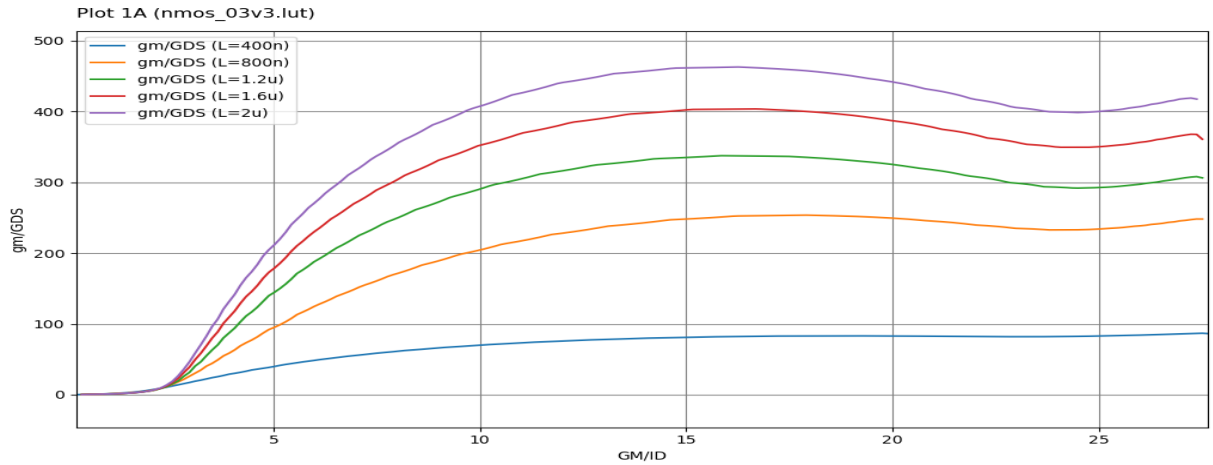


Figure 13: intrinsic gain

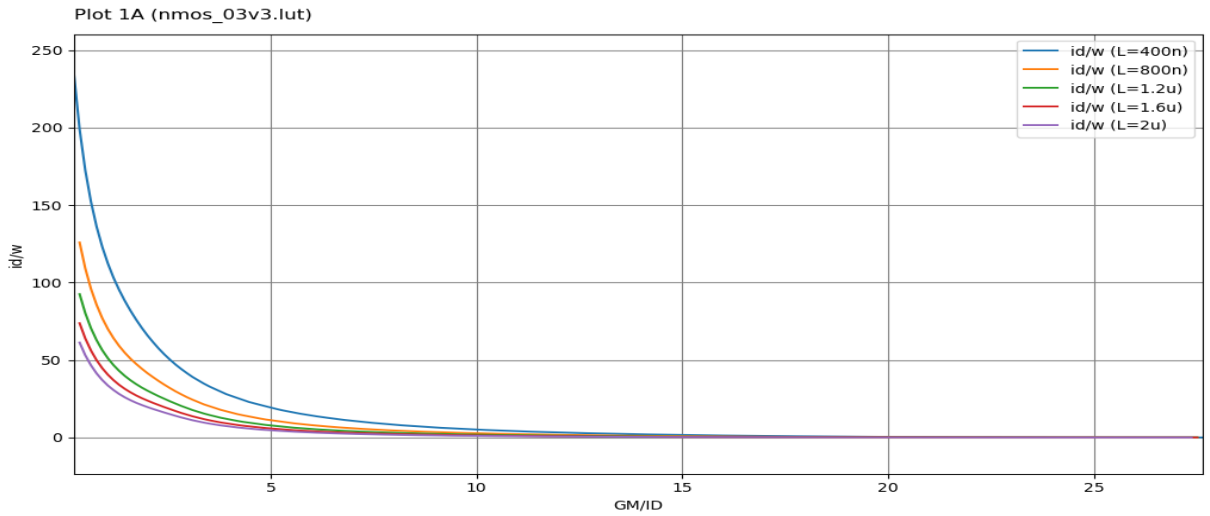


Figure 16:id/w

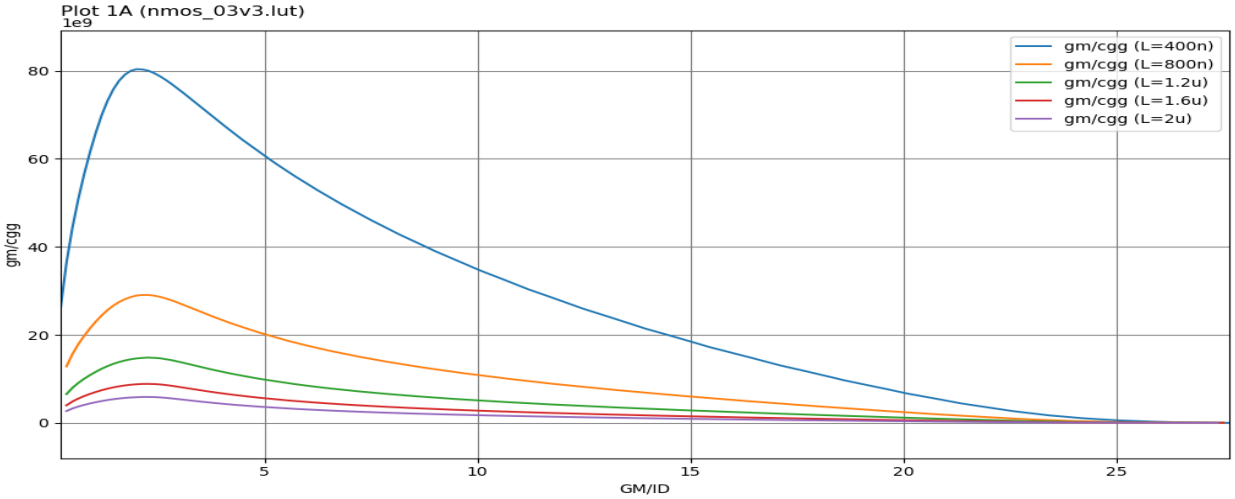


Figure 15:GM/CGG

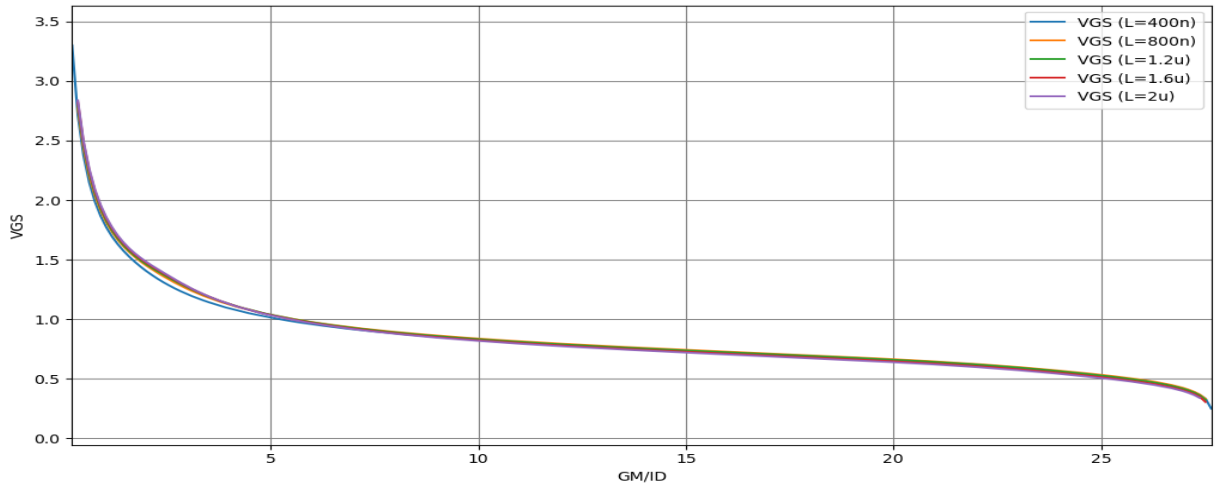


Figure 14:VGS

Part 2: OTA Design :

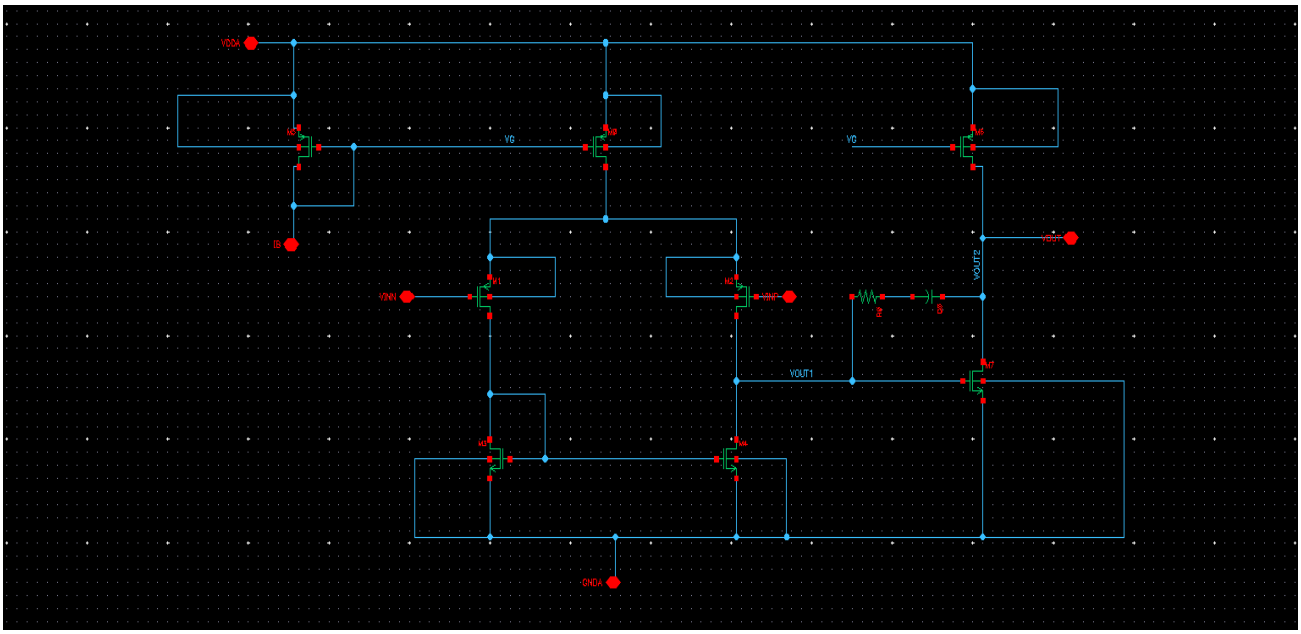


Figure 17: schematic

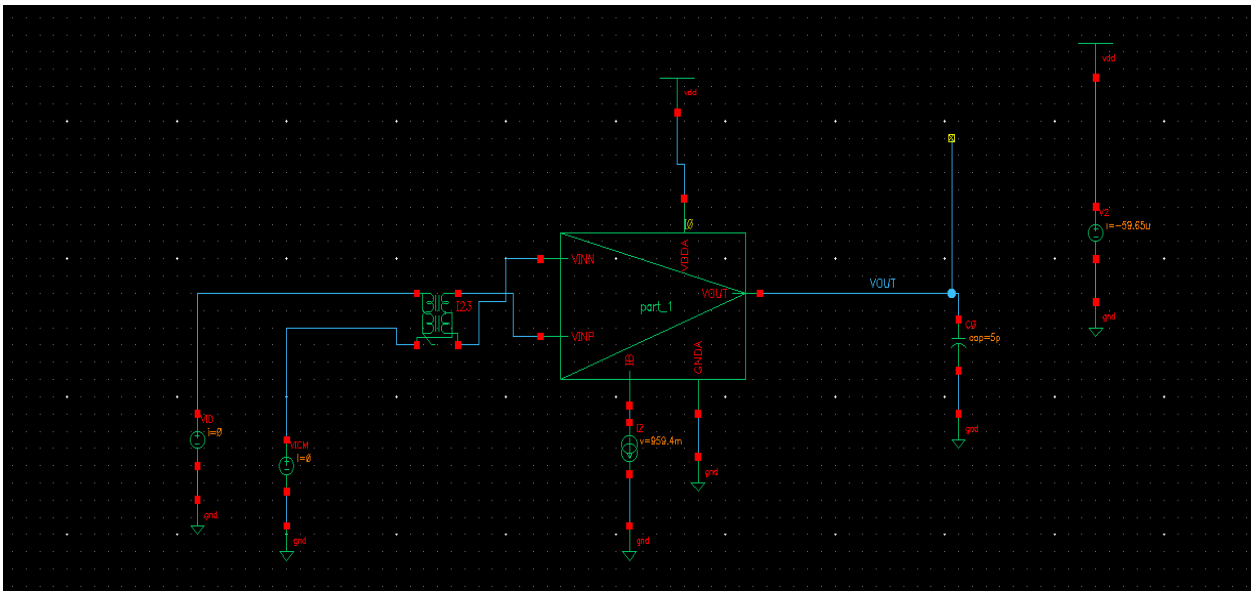


Figure 18: schematic with symbol

Design for input pair (PMOS):

PMOS input pair naturally supports low-end CMIR (towards GND)

Static gain error <= 0.05% ⟶ A_{OL} <= **2000** ($for\ 2\ stages$)

So assume $A_{OL(1st\ stage)} = 64$, $A_{OL(2nd\ stage)} = 32$, Assume $i_{dM1} = 5u$, $i_{dM6} = 40u$

CC=2p , $t\ r\ i\ s\ e\ = 2.2\tau$ ⟶ GBW $= \frac{1}{2\pi\tau} = 5\ MHZ$

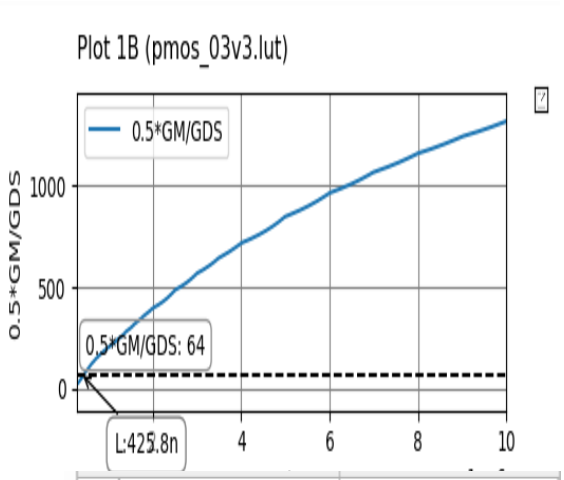
$gm_{1,2} = 2\pi \times$GBW$\times$ CC =62.83u ⟶ $\frac{gm_{1,2}}{i_{dM1}} =$ 12.57

≈ 14 (for some margin)

$0.5 \times \frac{gm_{1,2}}{gds} = 64$

And from SA :

L=425.8n ≈ 440n (for some margin)



4	W	8.91u
5	VGS	862.1m
6	VDS	600m
7	VSB	0
8	gm/ID	13.74
9	Vstar	145.5m
10	fT	747.1MEG
11	gm/gds	137.5
12	VA	10

Figure 19: VALUES FROM SA

.

W = 8.91u, VSG=862.1mV,

vthp= 781.6mV r_{on}= 2MΩ

We assign **larger gain to stage-1** because it:

reduces input-referred offset & noise, and leaves stage-2 mainly for providing swing & driving CL.

Design for load (NMOS):

We use **NMOS** load because it provides high gain, better headroom, easier biasing for the NMOS 2nd stage, and systematic offset cancellation

$Assume\ VINM_{MIN} = V_{GS} - V_{THP} = 0.03V$ ⟶ V_{GSn} =810m

And assume $r_{on} = r_{op}$ =2MΩ

From SA I found:

L = 500n W=1.69u

gm/id=11.58 $g_{mn} = 56.91u$

3	L	500n
4	W	1.69u
5	VGS	810m
6	VDS	600m
7	VSB	0
8	gm/ID	11.58
9	Vstar	172.7m
10	fT	3.321G
11	gm/gds	117.5

Lab 09 (Mini Project 01) Two-Stage Miller OTA

Design for the tail current source (PMOS):

PMOS inputs require a PMOS tail source at the top.

$\boldsymbol{CMRR(db) = A_{VD}(db) - A_{vcm}(db)}$ $\boldsymbol{A_{vcm} = -39db = 0.01122}$

$\boldsymbol{A_{vcm} = \frac{1}{g_m \times R_{ss}}}$ → $\boldsymbol{R_{ss} = 783K}$

V*= VDD-VSG- $VINM_{MAX}$ V*=130m (for some margin)

L= 400n W= 22.17u

gm/id=15.1 gm=151 u

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	400n
4	W	22.17u
5	VGS	834.6m
6	VDS	600m
7	VSB	0
8	gm/ID	15.1
9	Vstar	132.5m

Figure 20:VALUES FROM SA

Design for the 2ND input pair (NMOS):

we want VGS of 1st stage load = VGS of 2nd stage input= 810 mV
to eliminate systematic input-referred offset voltage

$\boldsymbol{i_{dM6} = 40u}$, $\boldsymbol{A_{OL(2nd\ stage)} = 32}$

SO, L= 360n W= 7.1u

gm/id=9.862 gm=400.6u

In a 2-stage Miller OTA, the compensation capacitor CC creates a right-half plane (RHP) zero if connected directly By putting a resistor RZ in series with CC, you can move that zero ,

So RZ = $\frac{1}{\text{gm (input transistor of this second stage)}}$ =2.496k

	Name	TT-27.0
3	L	360n
4	W	7.1u
5	VGS	810m
6	VDS	900m
7	VSB	0
8	gm/ID	9.862
9	Vstar	202.8m
10	fT	6.712G
11	gm/gds	59.94

Figure 21:VALUES FROM SA

Important Note :

I made some changes to some sizes to adjust some specs , the most important of which are :

- $\mathbf{W_{second\ input\ pair}}$ **increased to** → boosted gm, improved phase margin.
- $\mathbf{W_{second\ input\ pair}}$ **increased to 3.2959u as shown** → set VDSV of 2nd-stage NMOS ≈ 0.9 V for proper bias.
- $\mathbf{L_{tail}}$ **increased to 420n** → reduced gds, raised output resistance, improved CMRR

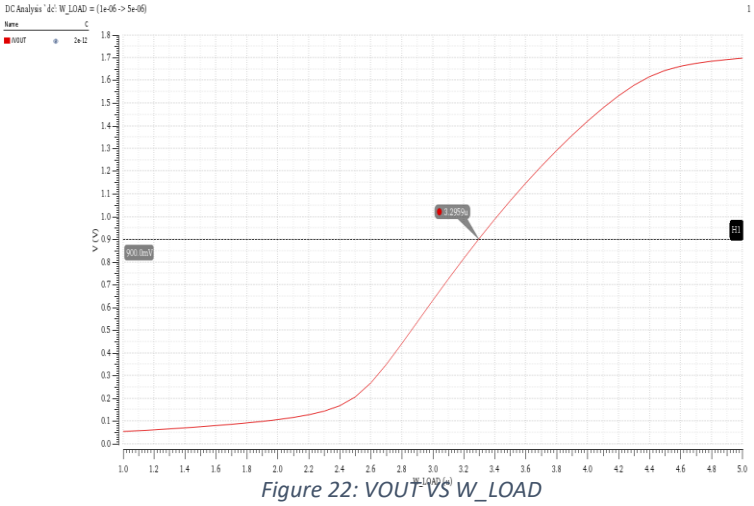


Figure 22: VOUT VS W_LOAD

part3: open loop OTA simulation

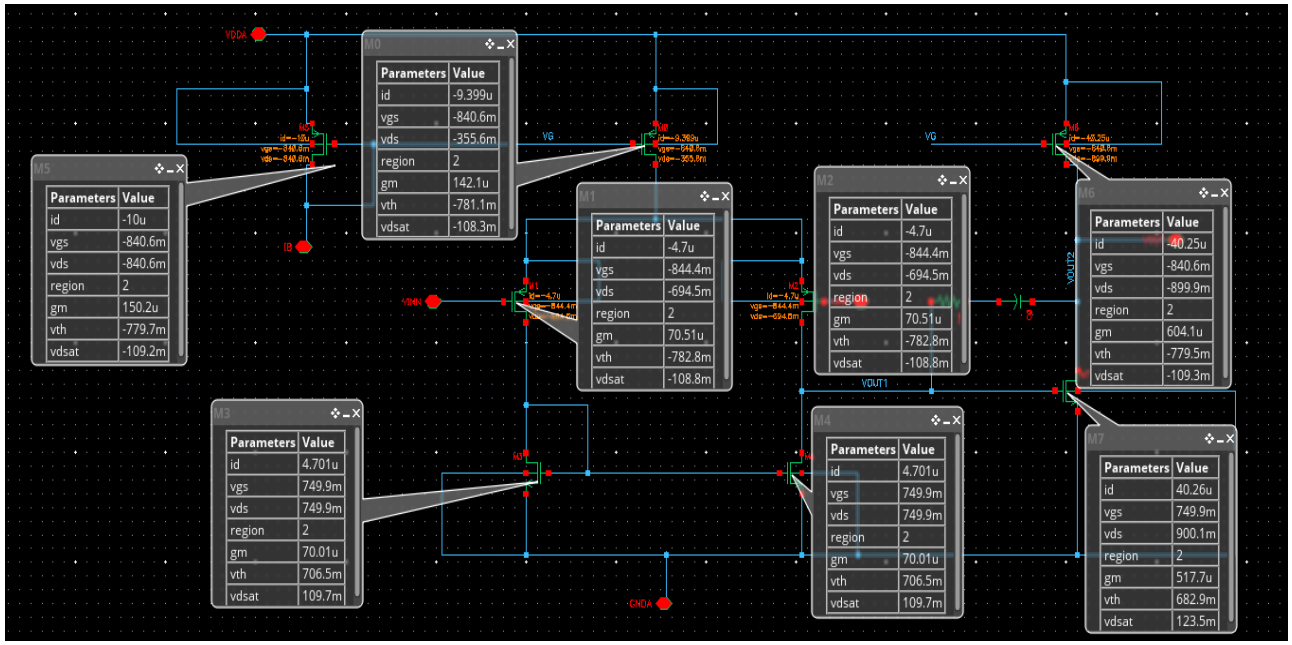


Figure 24:schematic with ballons annotated

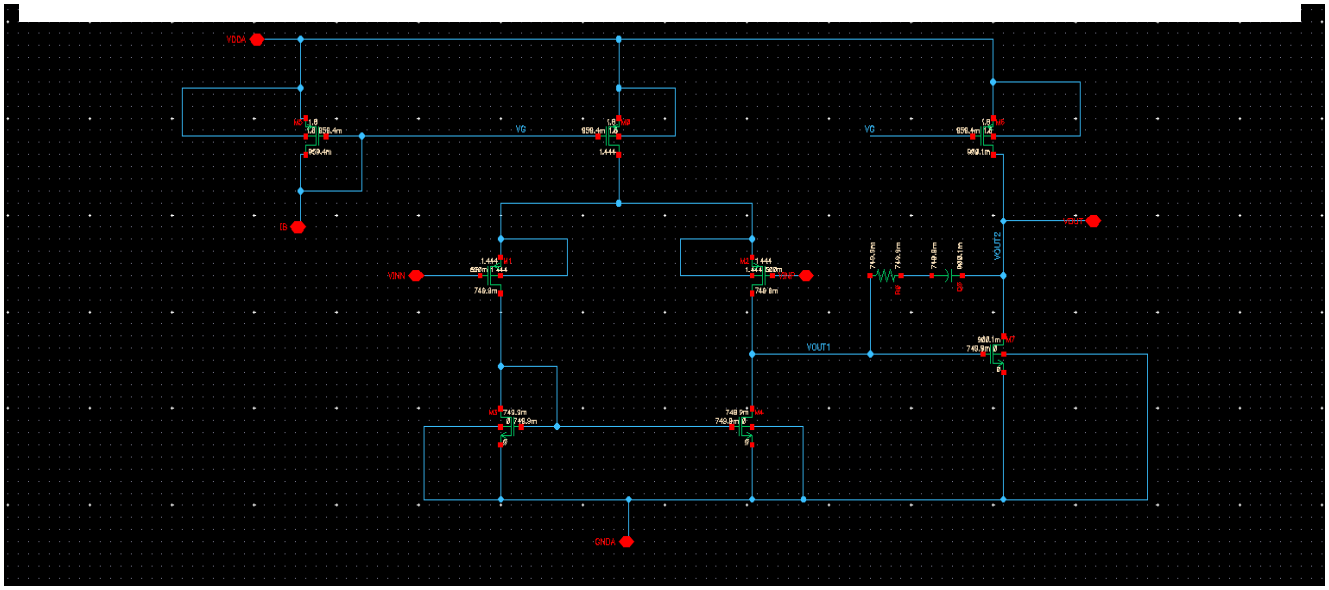


Figure 23:schematic with dc node voltages annotated

Is the current (and gm) in the input pair **exactly** equal?

- Yes — the currents (and therefore **gm**) in the input pair are exactly equal, since there's no mismatch. The two transistors in the input pair have the same VGS, VDS, and identical W/L

What is DC voltage at the output of the first stage? Why?

- Vout1= 749.9m, there's no mismatch, Vout1= vgs_tail=749.9m

What is DC voltage at the output of the second stage? Why?

- VOUT2= 0.9V, there's no mismatch VOUT2=VDD-VDSP=0.9V

2)Diff small signal ccs:

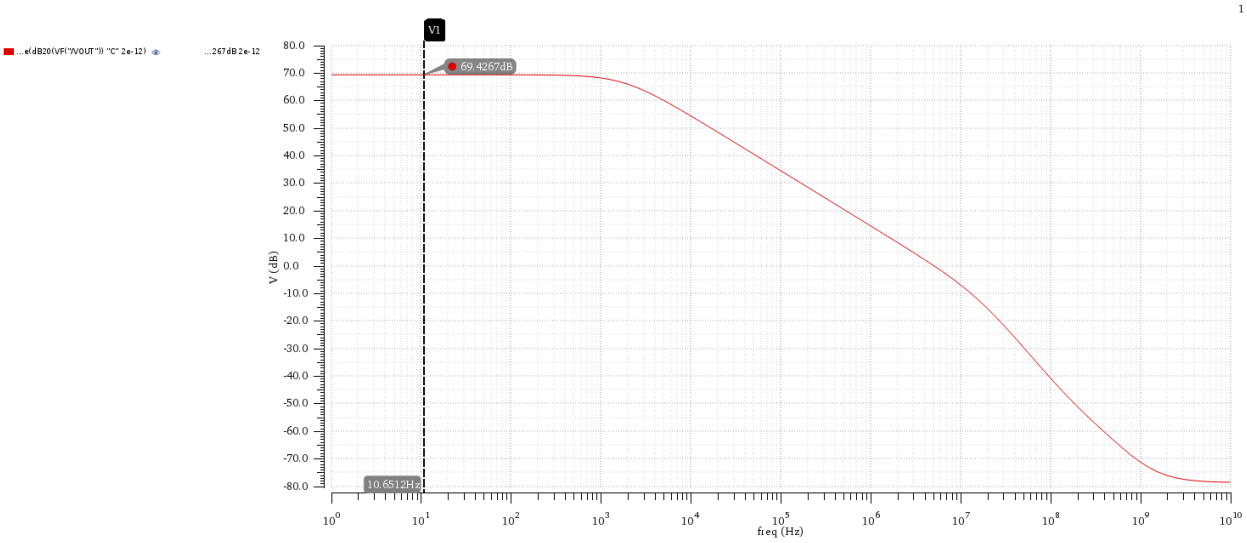


Figure 25:DIFF GAIN VS FREQ (in dB)

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab_9_mini_project:part_2:1	AO	2.96k			
lab_9_mini_project:part_2:1	AO_dB	69.43			
lab_9_mini_project:part_2:1	BW	1.823k			
lab_9_mini_project:part_2:1	Fu	5.173M			
lab_9_mini_project:part_2:1	GBW	5.41M			

Figure 26: RESULTS FROM SIMULATION

Hand analysis:

$|A_{Vdiff}| = gm_1 \times (r_{o1}//r_{o3}) \times gm_7 \times (r_{o6}//r_{o7}) = 2965.41 = 69.441$ dB

$BW = \frac{1}{2\pi \times C_c \times (r_1//r_3) \times (1+gm_7 \times (r_{06}//r_{o7})} = 1848.8\ HZ$

$GBW = \frac{gm1,2}{2\pi \times C_c} = 5.611\ MHZ > 5MHZ$ almost equal UGF

	GAIN	BW	UGF	GBW
From simulation	69.43 dB	1823 HZ	5.173M	5.41M
From hand analysis	69.441 dB	1848.8 HZ	5.611M	5.611M

3)CM small signal ccs:

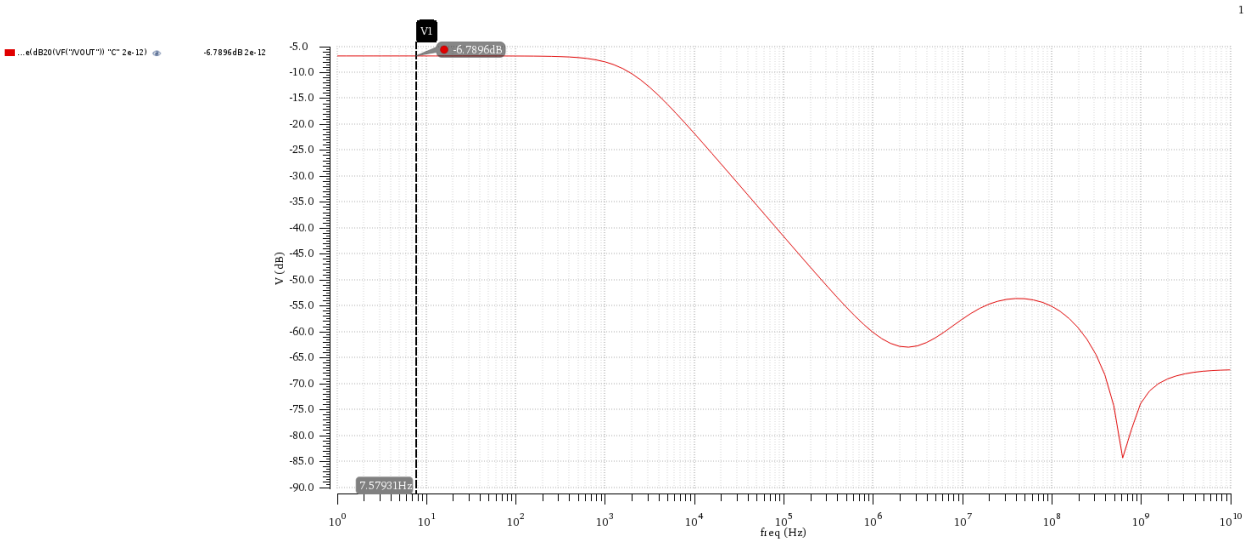


Figure 27: CM GAIN VS FREQ (In dB)

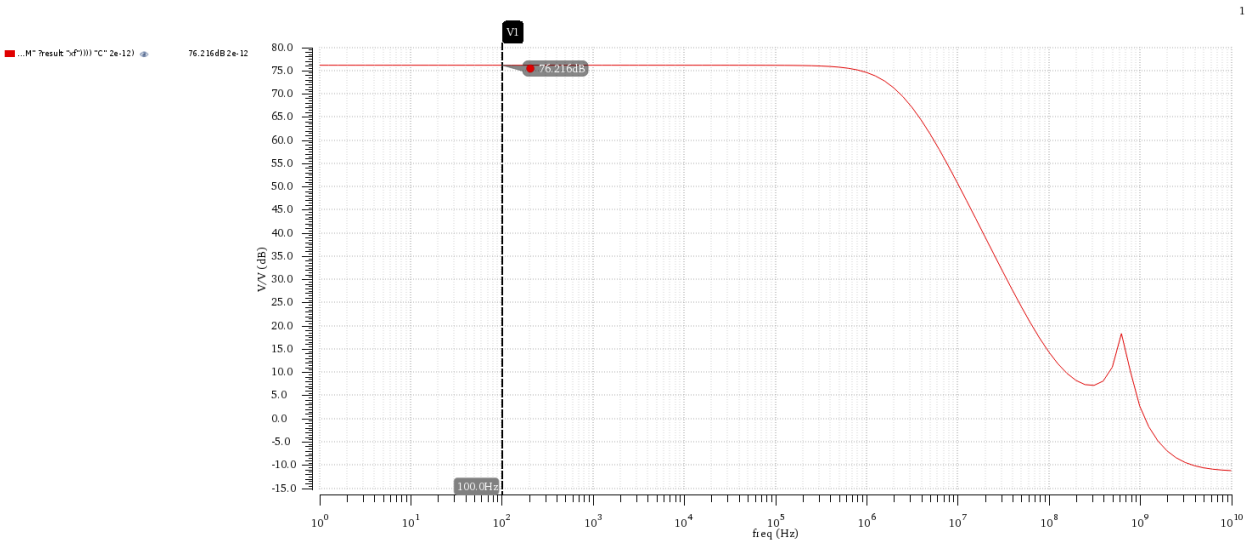
Test	Output	Nominal	Spec	Weight	Pass/Fail
lab_9_mini_project:part_2:1	AO	457.6m			
lab_9_mini_project:part_2:1	AO_dB	-6.789			

Hand analysis:

$$|A_{Vcm}| = \frac{1}{2 \times g_{mn} \times r_{o\ tail}} \; gm_7 \times (r_{o6} // r_{o7}) = 0.4649 = -6.6522\ dB$$

	Simulation	Hand analysis
$\|A_{Vcm}\|$	-6.789 dB	-6.6522 dB

4)CMRR:



From simulation:

CMRR =76.216 dB > 74 dB

Hand analysis:

CMRR (db)= AVD(db)-AVCM(db) =76.0932 db

	Simulation	Hand analysis
CMRR	76.216 dB	76.0932 dB

5) (Optional) Diff large signal ccs:

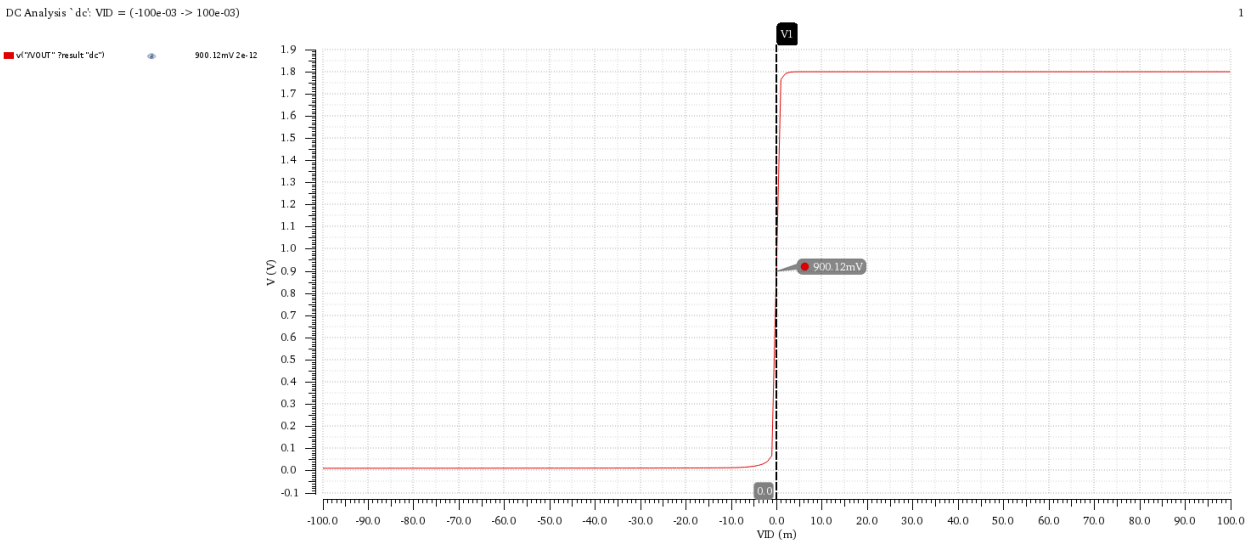


Figure 28:vout vs vid

VOUT(From simulation) =900.12 mV

VOUT(From DC OP) =900.1 mV

This is expected because when the differential input is zero, both input transistors carry equal current, so the circuit settles to its DC bias point

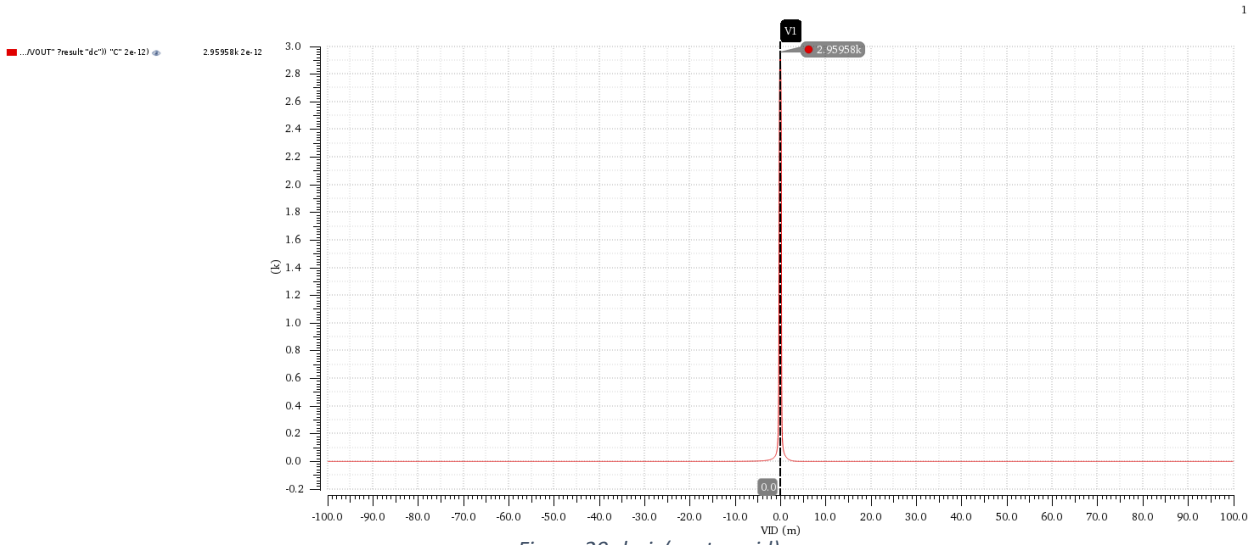


Figure 29:deriv(vout vs vid)

Peak = 2.95958 KV which almost = Avd

Comment: The peak gain from the transient test is almost the same as the gain from the AC analysis because both are measuring the small-signal behavior of the circuit around its bias point. They are not identical since the transient method depends on the input signal amplitude and FFT calculation, which can cause small differences compared to the direct AC analysis.

6)CM large signal ccs (region vs VICM):

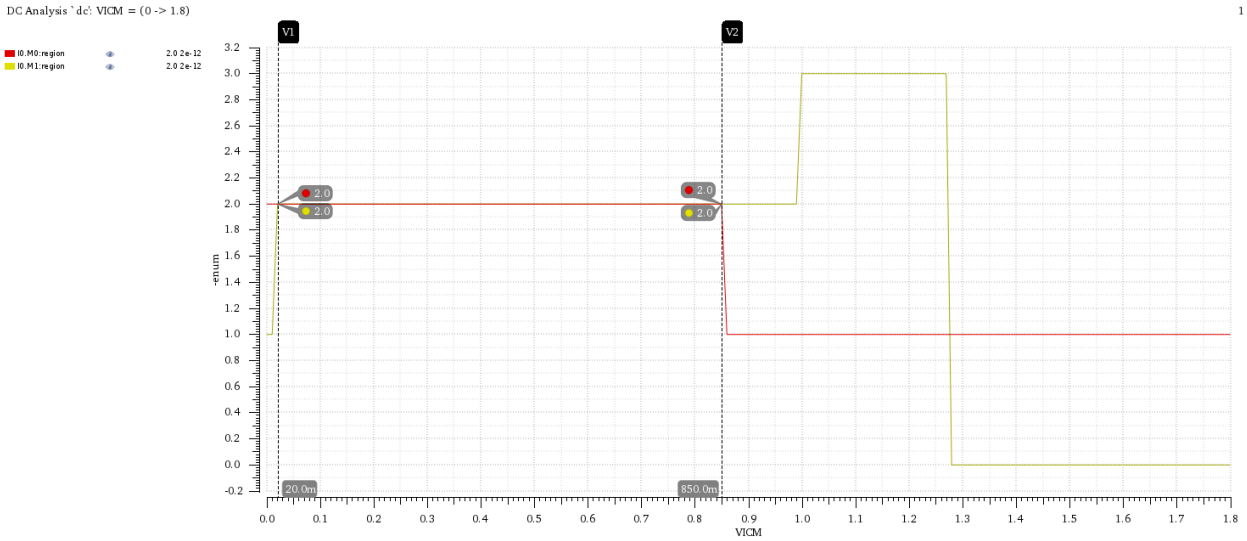


Figure 30: REGIONS VS VICM

From graph :20m < VICM < 850m Which achieves our specs in the first

Hand analysis

Vincmax = -Vdsat0-vgs1+vdd=847.3 mV

VINCmin = vgs3-vgs1+vdsat1= 15.2 mV

	Hand	simulation
VICMmin	15.2 mV	20 mV
VICMmax	847.3 mV	850 mV

7)(Optional) CM large signal ccs (GBW vs VICM):

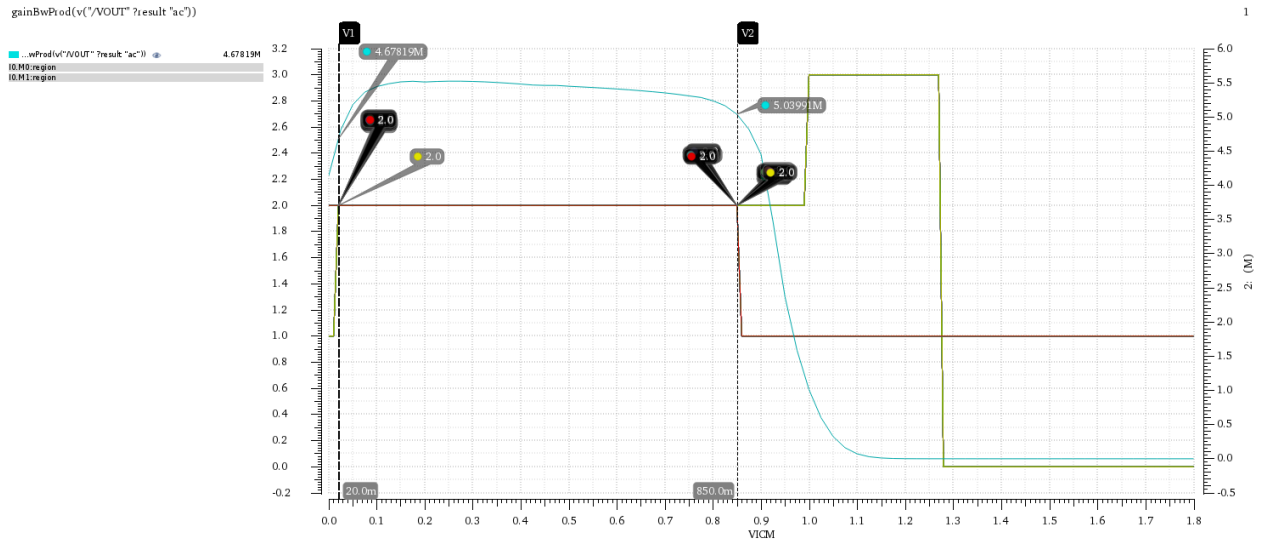


Figure 31: regions &gbw vs vicm

From graph :20m < VICM < 850m Which achieves our specs in the first

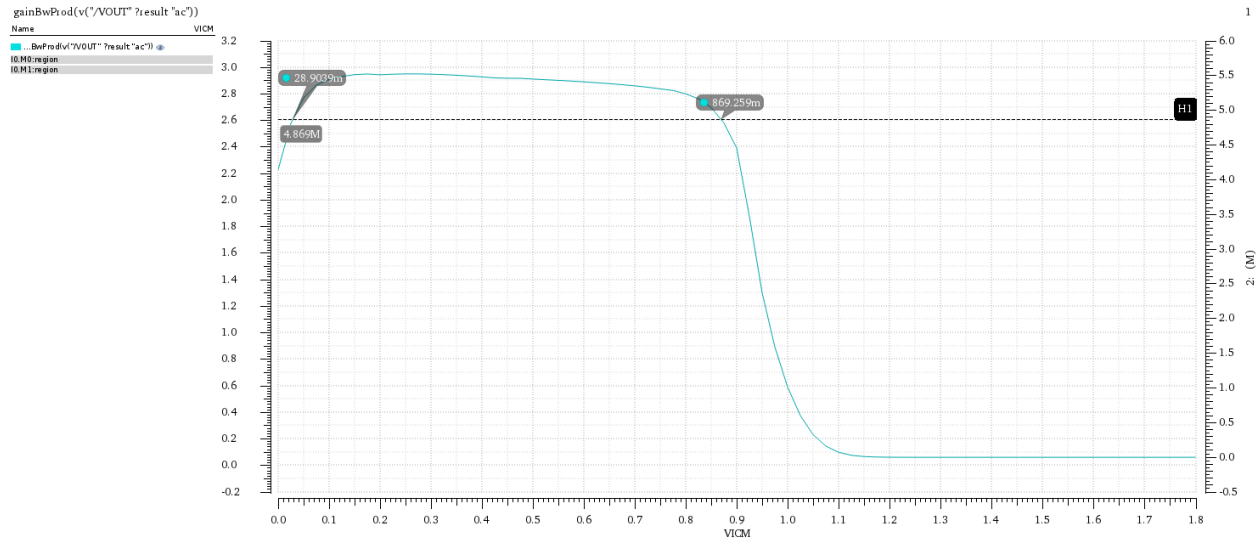


Figure 32:90% of max GBW VS VICM

From graph :28.903m < VICM < 869.259m Which achieves our specs in the first

PART 4: Closed-Loop OTA Simulation

1)Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.

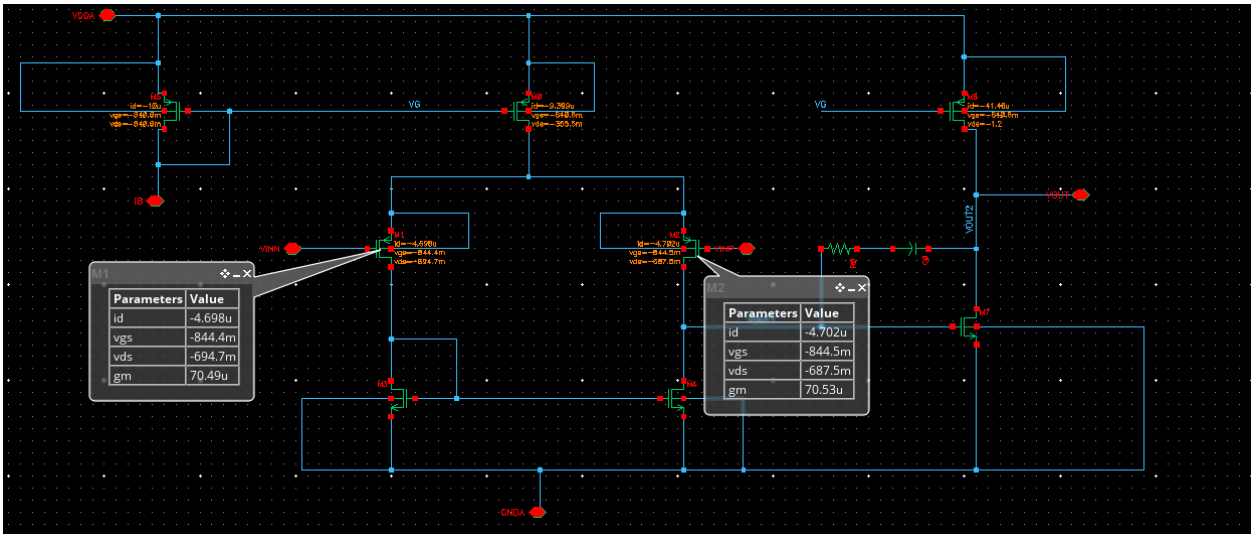


Figure 34:schematic with dc op annotated

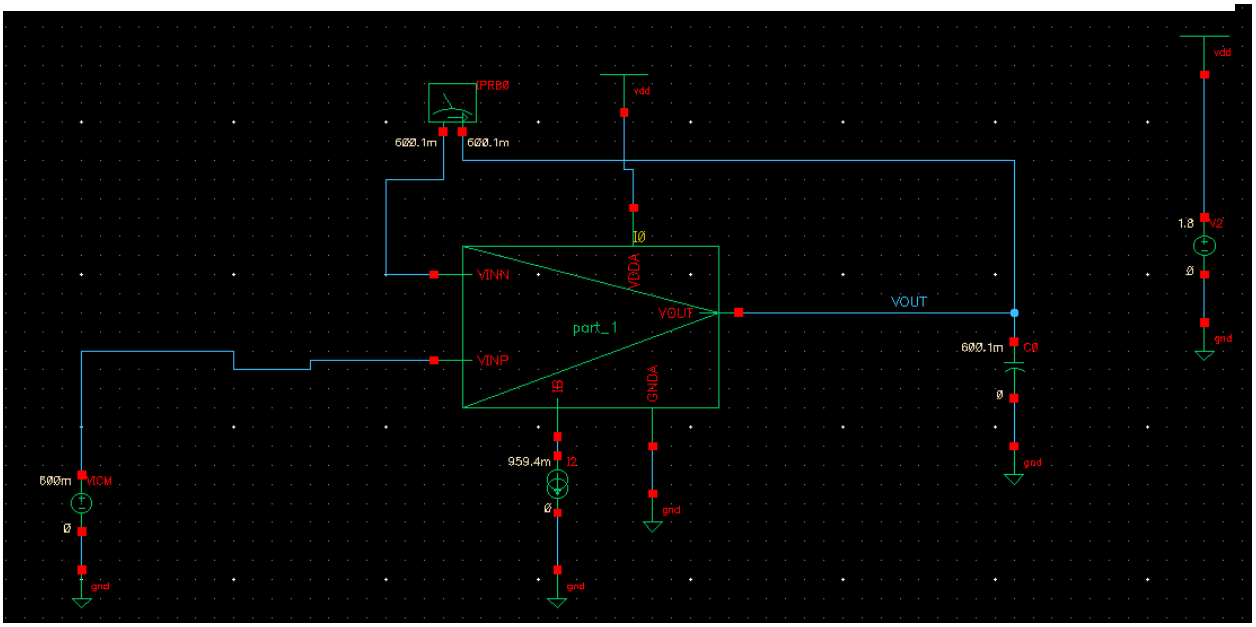


Figure 33: symbol voltages

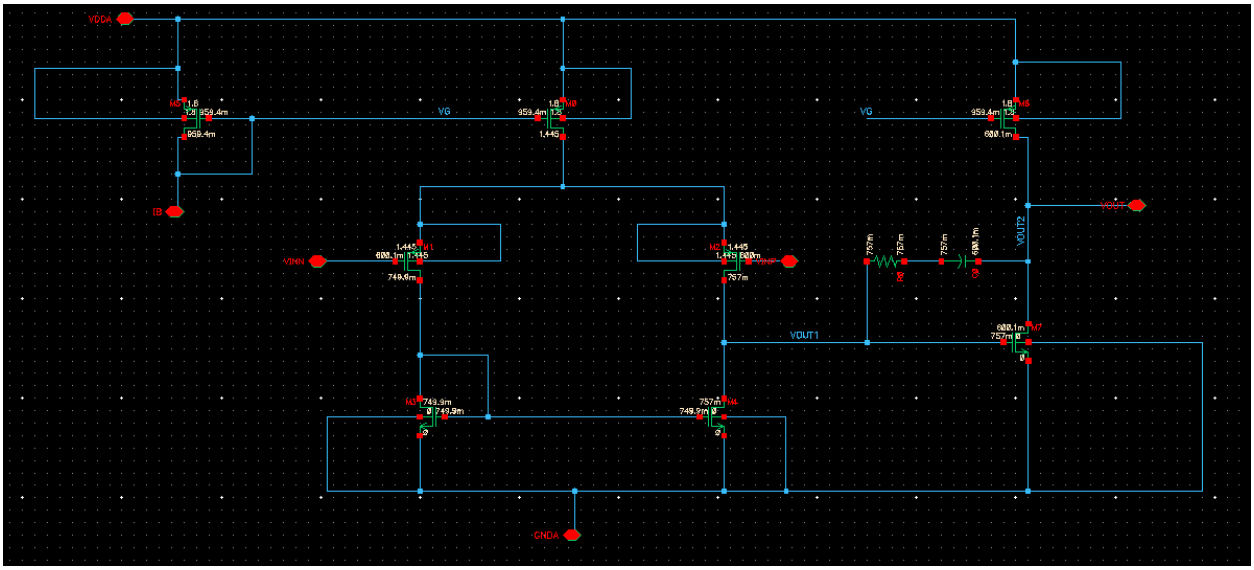


Figure 35 : schematic node voltages

Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

- Approximately Yes — in closed loop the DC voltages at the op-amp inputs are (almost) equal. This is because negative feedback forces the op-amp to adjust its output until the differential input voltage is nearly zero. With high open-loop gain, even a tiny difference between the inputs produces a large output change, so at steady state the inputs sit at the same DC potential.

Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

- No , Closed loop introduces a small input error and shifts the common-mode, so the first-stage DC node moves from its open-loop value.”

Is the current (and gm) in the input pair exactly equal? Why?

- No — in closed-loop operation, a small differential input voltage is required due to the OTA’s finite gain, which creates an effective mismatch between the two input transistors. This mismatch causes their drain currents — and therefore their gm — to be slightly different.

2)Loop gain:

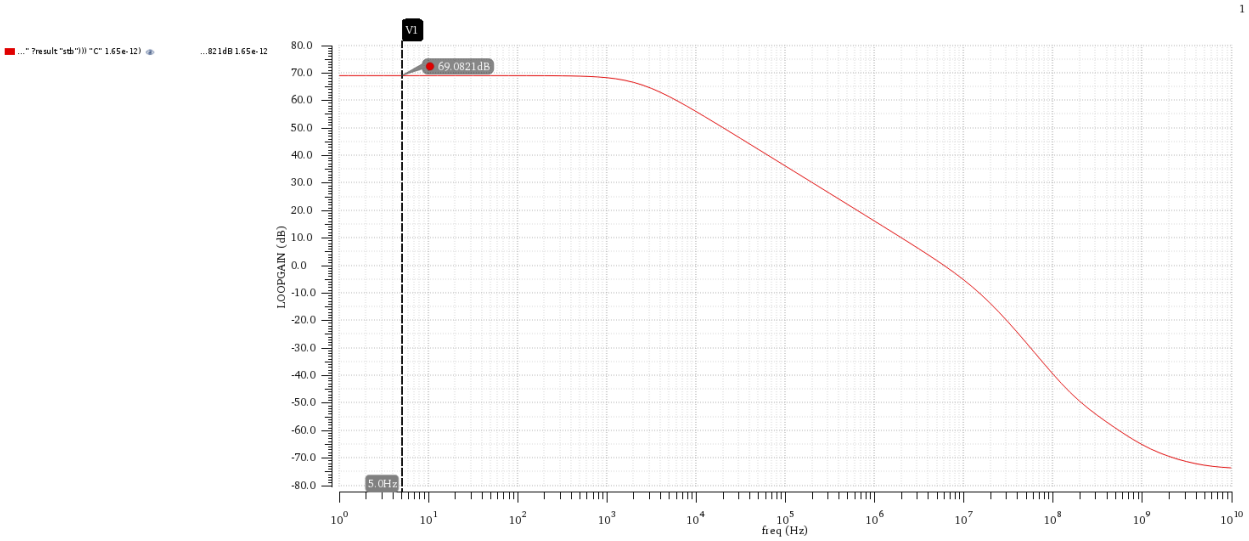


Figure 37:LOOP GAIN VS FREQ

Parameters: C=2p						
1	lab_9_mini_project:part_2:1	A01	2.845k			
1	lab_9_mini_project:part_2:1	AO1_dB	69.08			
1	lab_9_mini_project:part_2:1	GBW1	5.401M			
1	lab_9_mini_project:part_2:1	Fu1	5.176M			
1	lab_9_mini_project:part_2:1	phase margin DEG	73.4			

*Figure 36:Result from simulation **(contains PM)***

Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment

	GAIN	UGF	GBW
Open loop	69.43 dB	5.173M	5.41M
Loop gain	69.08 dB	5.176M	5.401M

DC gain is nearly the same in both cases with only a slight drop in Loop gain, while UGF and GBW are almost identical. This shows feedback has little effect on the frequency response, and differences come only from small bias/loading changes and there is mismatch when I closed the loop

Hand analysis:

$|A_{Vdiff}| = gm_1 \times (r_{o1}//r_{o3}) \times gm_7 \times (r_{o6}//r_{o7}) = 2847.41 = 69.089$ dB

$BW = \frac{1}{2\pi \times C_c \times (r_1//r_3) \times (1+gm_7 \times (r_{06}//r_{o7})} = 1896.88\ HZ$

$GBW = \frac{gm1,2}{2\pi \times C_c} = 5.4MHZ$ > 5MHZ almost equal UGF

$w2 = \frac{gm(input\ second\ stage)}{2*pi*cl}$

$PM = 90 - tan^{-1}(\frac{wu}{w2}) = 72.686\ deg$

The formula $PM = 90 - tan^{-1}(\frac{wu}{w2})$ assumes only two poles and no zeros. In the real OTA, extra poles/zeros, finite gain, and bias shifts are present, so the phase at unity-gain differs. That's why the simulated PM is not exactly the same as the formula result

	GAIN	PM	UGF	GBW
From simulation	69.08 dB	73.4 DEG	5.176M	5.401M
From hand analysis	69.089 dB	72.686 DEG	5.4M	5.4M

3)Slew rate:

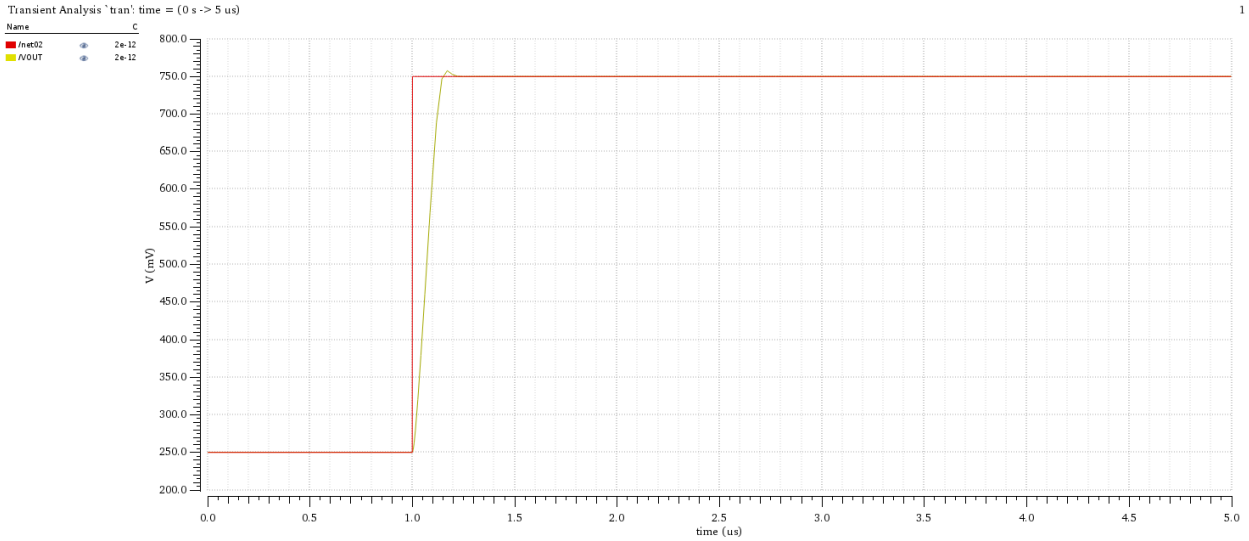


Figure 38: VOUT VS VIN

Report the slew rate

Parameters: C=2p						
1	lab_9_mini_project:part_2:1	phase margin DEG	73.62			
1	lab_9_mini_project:part_2:1	slew rate	4.294M			

As shown slew rate didn't achieve our specs at CC=2p , so I will sweep on CC to see when achieve our specs and PM is correct also :

Parameters: C=1.6p						
1	lab_9_mini_project:part_2:1	phase margin DEG	69.93			
1	lab_9_mini_project:part_2:1	slew rate	5.13M			
Parameters: C=1.65p						
2	lab_9_mini_project:part_2:1	phase margin DEG	70.46			
2	lab_9_mini_project:part_2:1	slew rate	5.013M			
Parameters: C=1.7p						
3	lab_9_mini_project:part_2:1	phase margin DEG	70.98			
3	lab_9_mini_project:part_2:1	slew rate	4.899M			
Parameters: C=1.75p						
4	lab_9_mini_project:part_2:1	phase margin DEG	71.47			
4	lab_9_mini_project:part_2:1	slew rate	4.79M			
Parameters: C=1.8p						
5	lab_9_mini_project:part_2:1	phase margin DEG	71.93			
5	lab_9_mini_project:part_2:1	slew rate	4.684M			
Parameters: C=1.85p						
6	lab_9_mini_project:part_2:1	phase margin DEG	72.38			
6	lab_9_mini_project:part_2:1	slew rate	4.581M			
Parameters: C=1.9p						
7	lab_9_mini_project:part_2:1	phase margin DEG	72.81			
7	lab_9_mini_project:part_2:1	slew rate	4.482M			
Parameters: C=1.95p						
8	lab_9_mini_project:part_2:1	phase margin DEG	73.22			
8	lab_9_mini_project:part_2:1	slew rate	4.387M			

As shown PM & SR will achieve our spec at CC=1.65p

Hand analysis

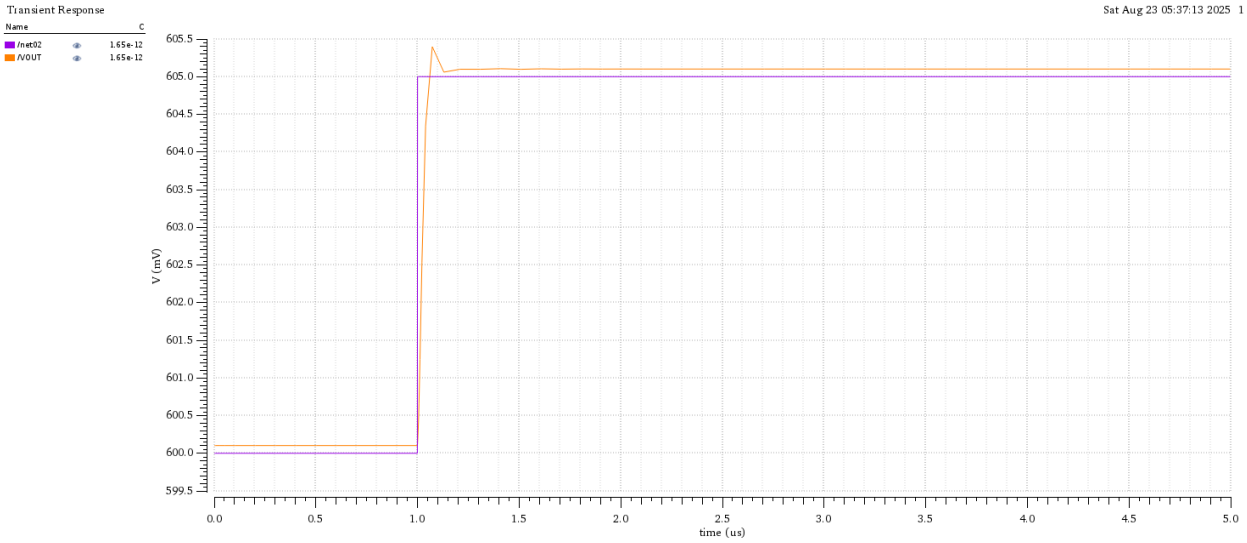
Slew_rate = $\frac{I_B}{CC} = 5.7\ M$

	Simulation	Hand analysis
Slew_rate	5.013 M	5.7 M

4)Settling time:

Calculate the output rise time from simulation.

	C	riseTim...time")
1	1.650E-12	39.01E-9



Do you see any ringing? Why?

just a tiny overshoot with no sustained ringing because the **closed-loop step response reflects limited phase margin**. The second pole and parasitic poles/zeros add lag, so the feedback loop overshoots and rings before settling and the phase margin < 76 DEG

Compare simulation results with hand calculations in a table

HAND ANALYSIS: T_rise = $\frac{2.2}{2\pi \times GBW} = 64.84\ ns$

The simulation result will be better than expected. Why? Using trise = 2.2τ is based on first-order model but our second order sysem is faster and that clarify the difference between simulation and hand analysis

	Simulation	Hand analysis
T_rise	39.01 ns	64.84 ns

	Specs	Achieved specs	
Static gain error	**<= 0.05%**	0.03%	✓
CMRR @ DC	**>= 74dB**	76.216dB	✓
Phase margin (avoid pole-zero doublets)	>= 70°	73.62 °	✓
OTA current consumption	**<= 60uA**	49.65 uA	✓
CMIR – high	**>= 0.8V**	0.85 V	✓
CMIR – low	**<= 0.2V**	0.02 V	✓
Buffer closed loop rise time (10% to 90%)	**<= 70ns**	64.84 ns	✓
Slew_rate	**5V/ μs**	5V/ μs	✓

Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation

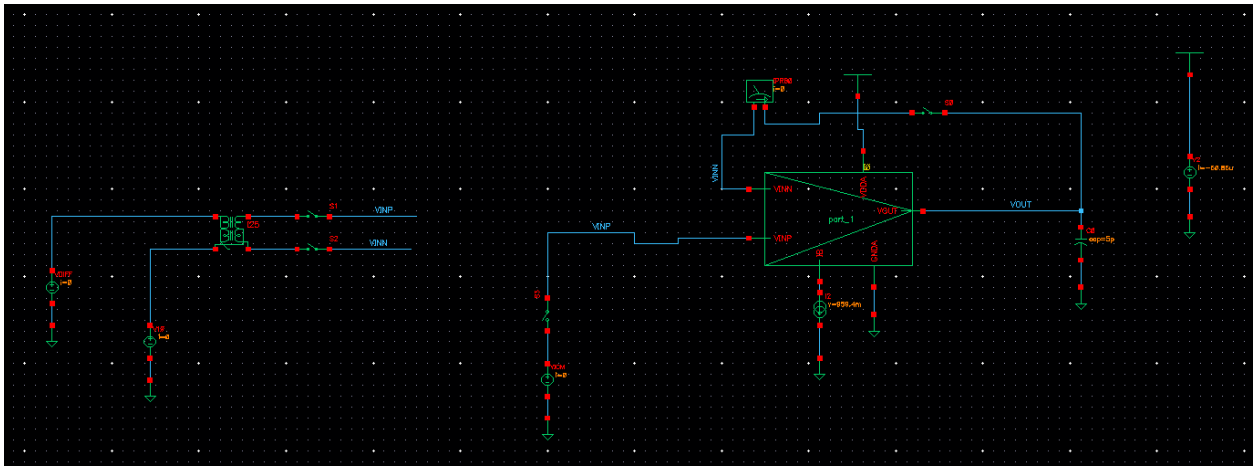


Figure 39:schematic

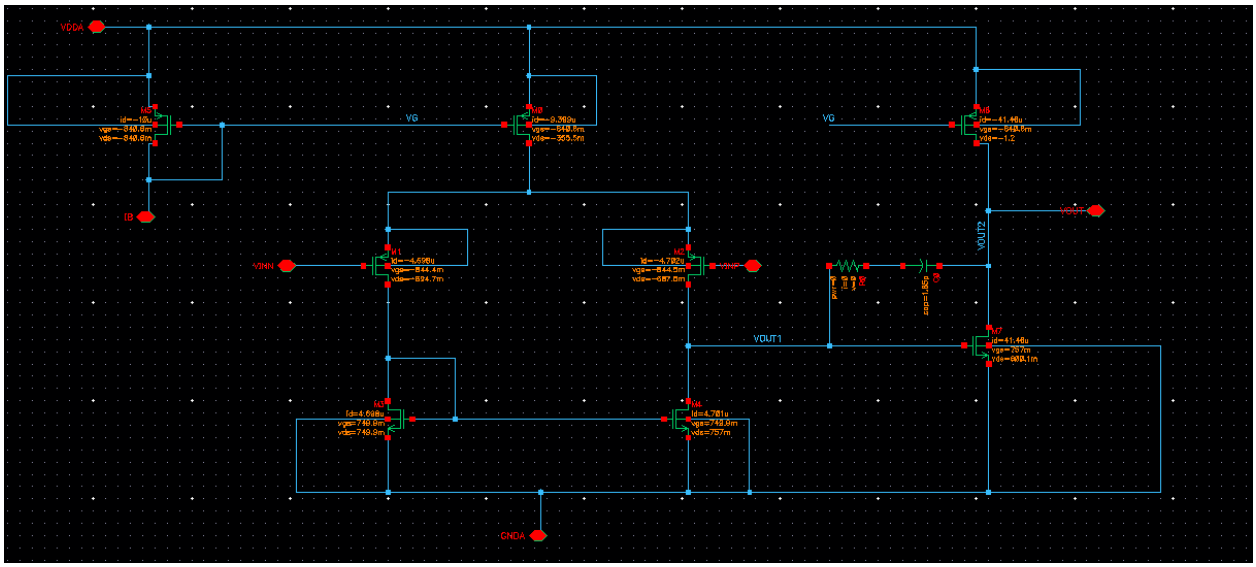


Figure 40: dc op annotated

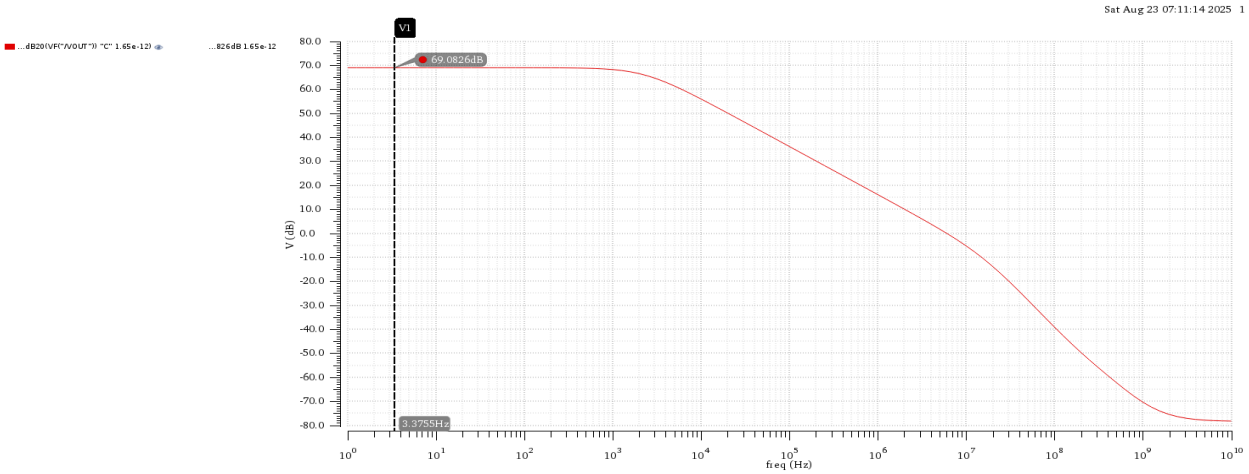


Figure 43:AVDIFF vs FREQ

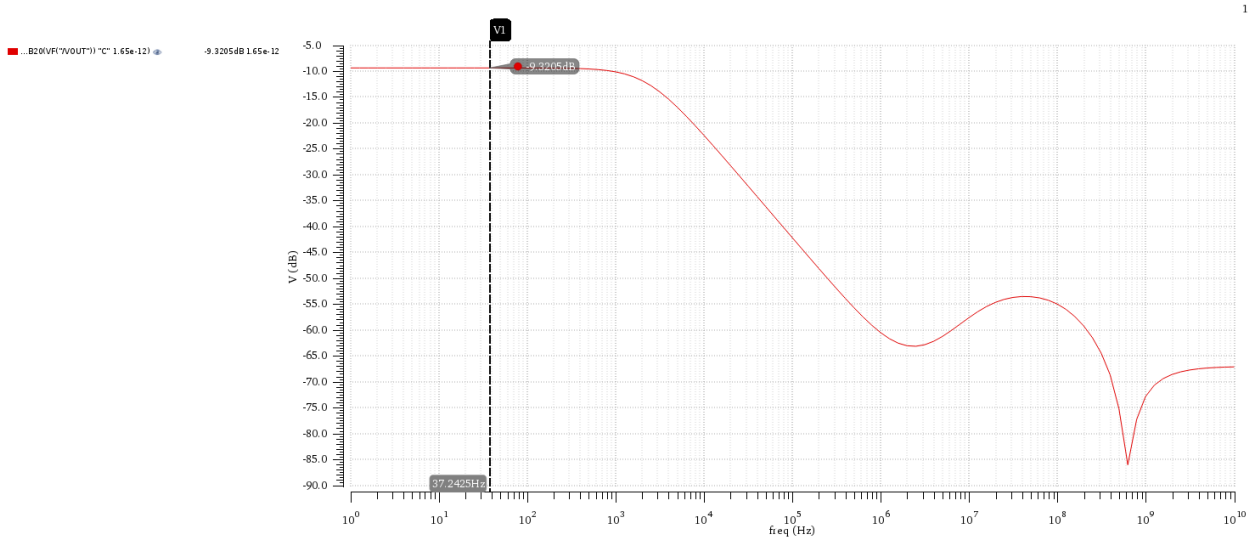


Figure 42: AVcm VS freq

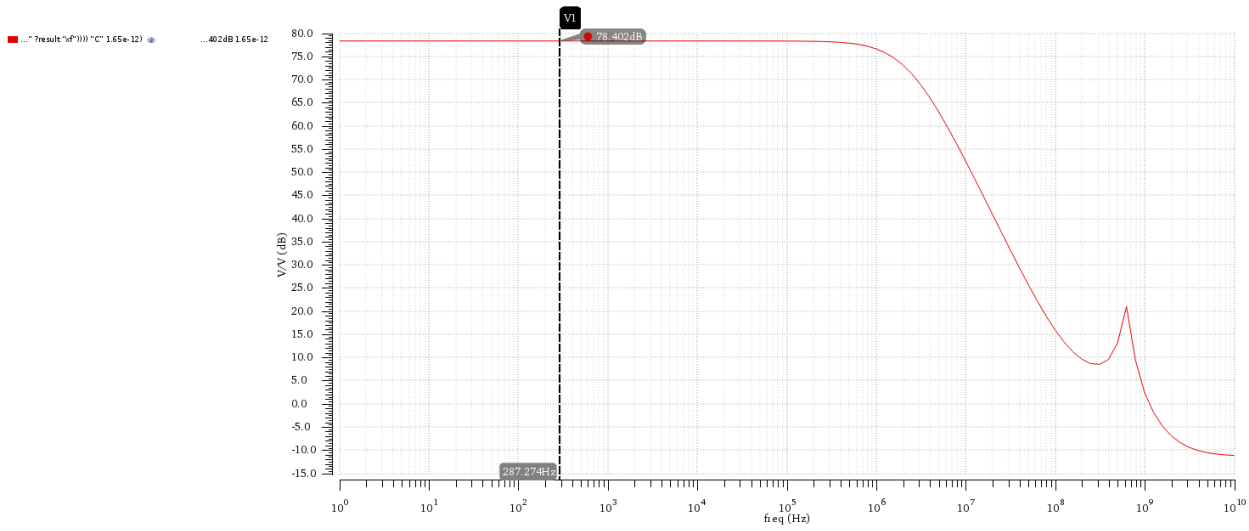


Figure 41:CMRR

Acm dropped because closing the loop for the DC operating point changed the amplifier's bias and loop action so the circuit responds less to common-mode inputs and mismatch

Part 6 (optional): RZ Implementation

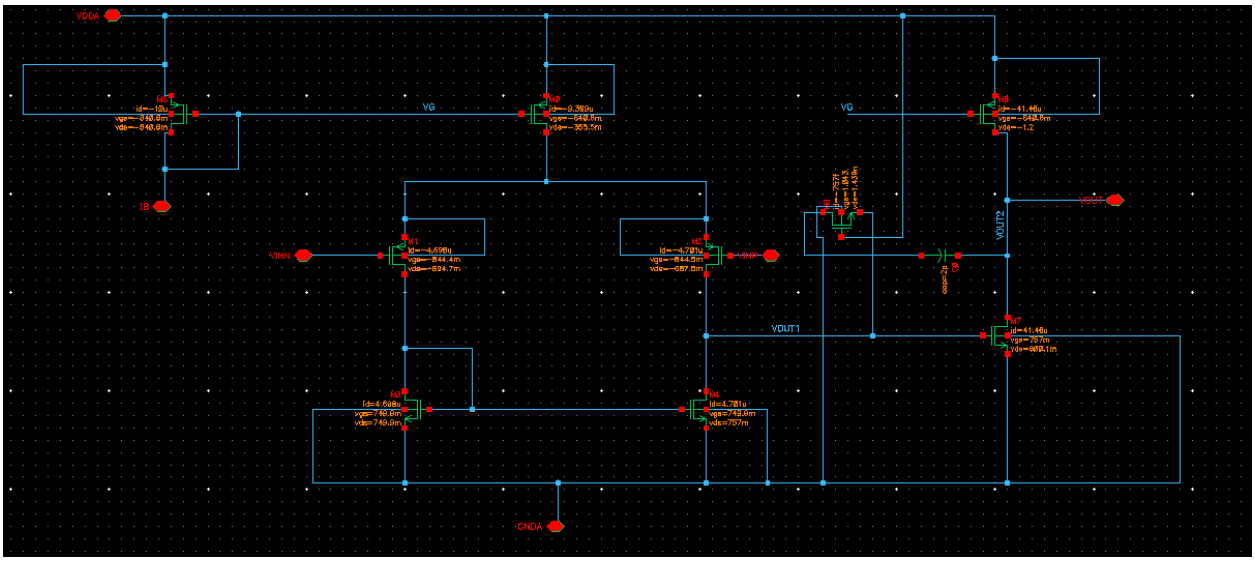


Figure 44: schematic with dc op

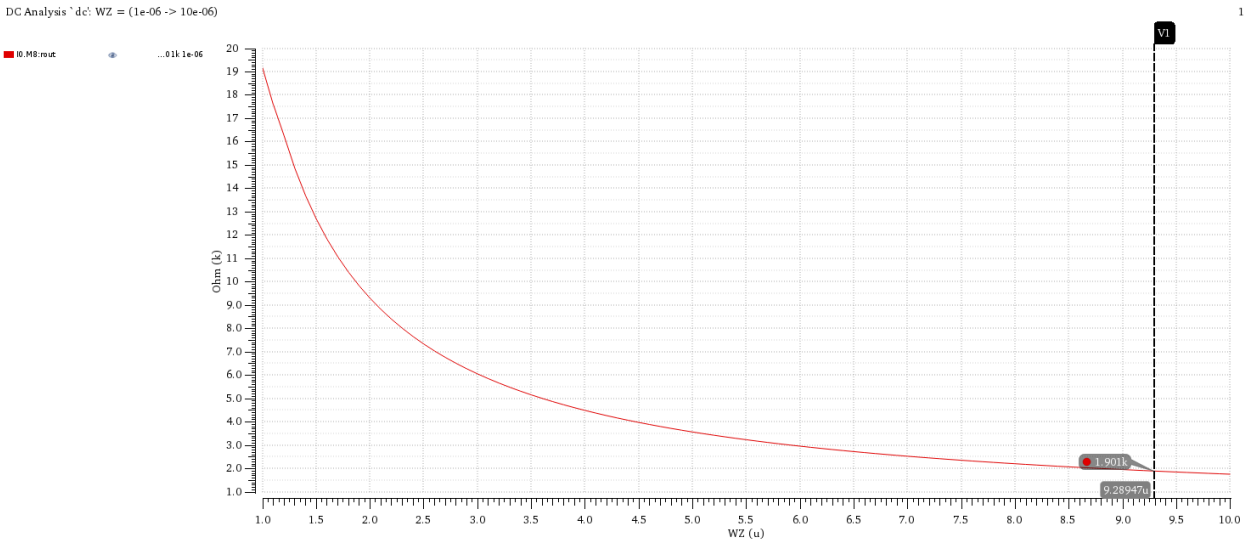


Figure 45: ROUT VS W

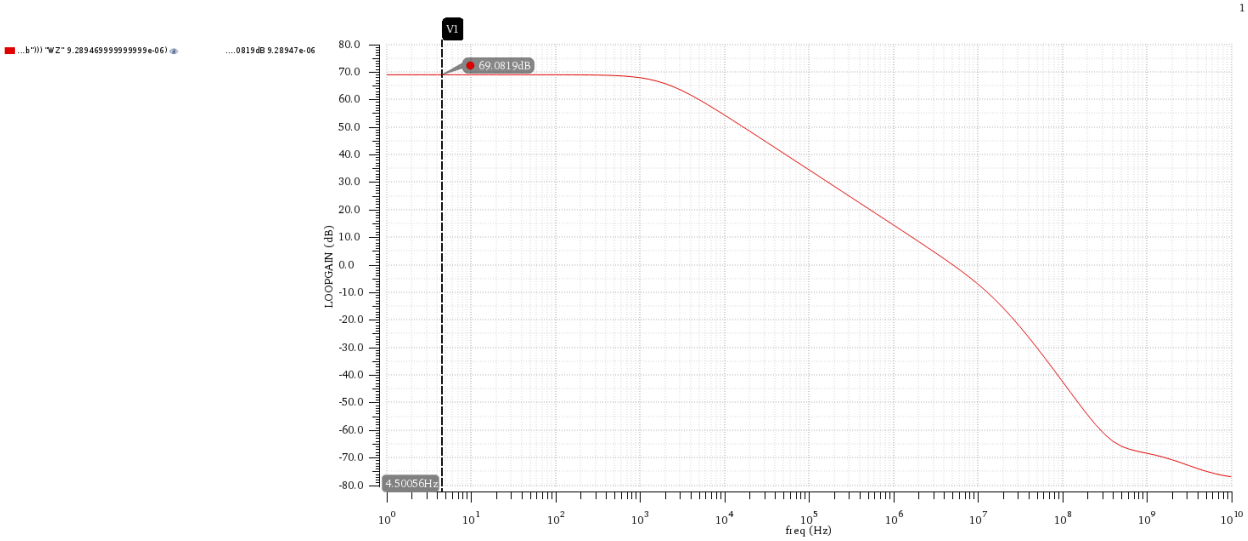


Figure 46: LOOP GAIN VS FREQ

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab_9_mini_project:part_2:1	A01	2.845k			
lab_9_mini_project:part_2:1	AO1_dB	69.08			
lab_9_mini_project:part_2:1	GBW1	5.398M			
lab_9_mini_project:part_2:1	Fu1	5.161M			
lab_9_mini_project:part_2:1	phase margin DEG	73.43			

NOTE I calc these values at CC=2p , as before changing it