Analog IC Design (Xschem, Ngspice, ADT) Lab 04

Common Drain Frequency Response

Part 1: Device Sizing Using SA

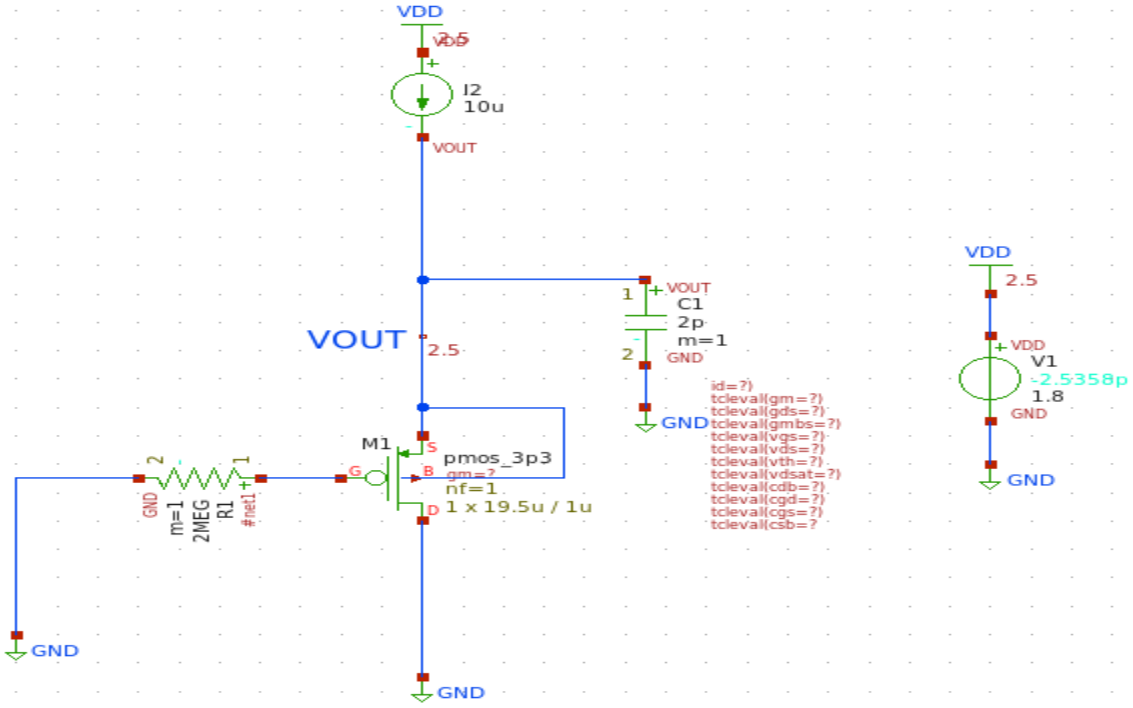
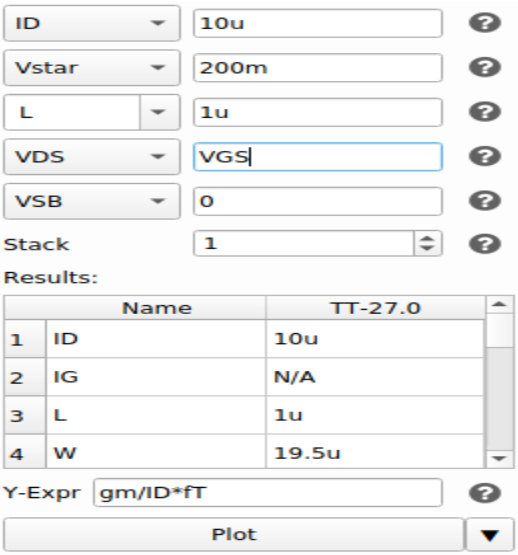


Figure 1: schematic



AS shown, after applying given specs on ADT because values on x_schem not accurate we see the width(W) of PMOS = 19.5 u

Part 2: CD Amplifier

1. OP (Operating Point) Analysis

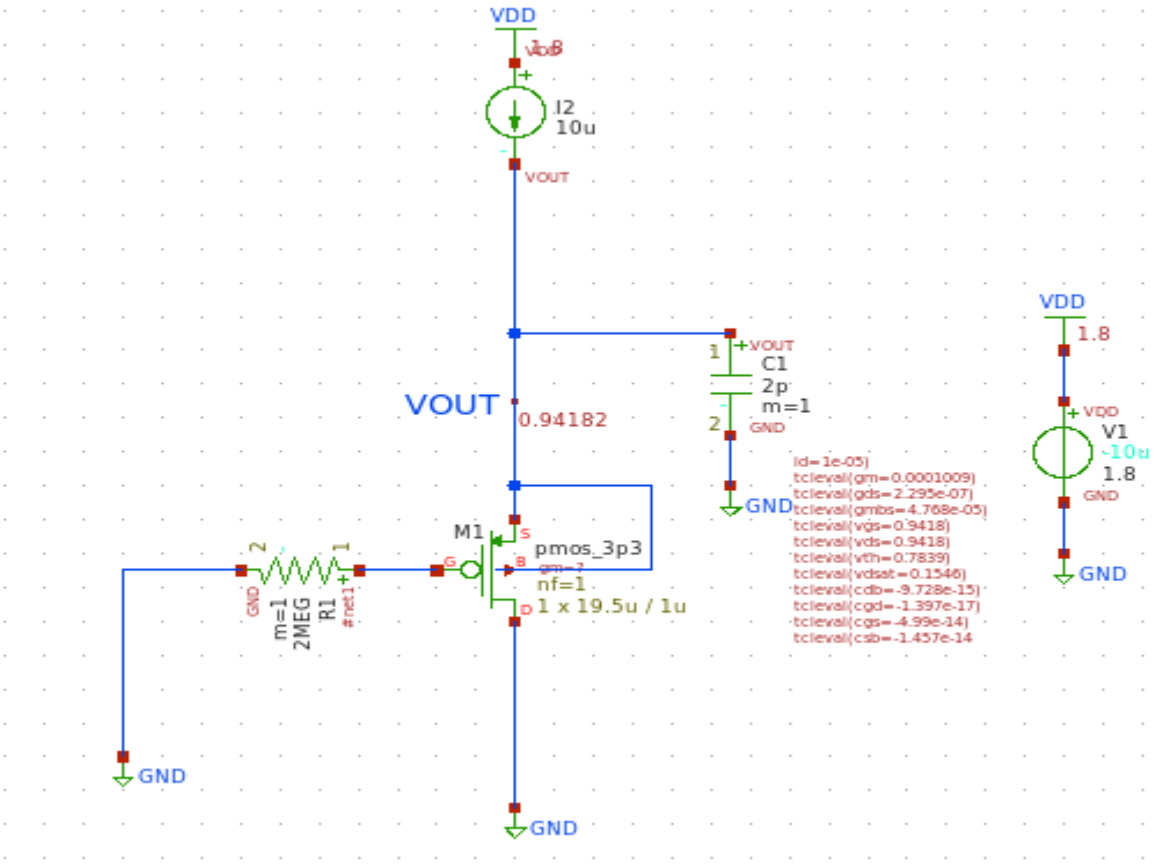


Figure 2: schematic

3) Check that the transistor operates in saturation

AS shown from fig (3) VDS>VDSAT, SO the TRANSISTOR work In saturation

```
id=1e-05)
tcleval(gm=0.0001009)
tcleval(gds=2.295e-07)
tcleval(gmbs=4.768e-05)
tcleval(vgs=0.9418)
tcleval(vds=0.9418)
tcleval(vth=0.7839)
tcleval(vdsat=0.1546)
tcleval(cdb=-9.728e-15)
tcleval(cgd=-1.397e-17)
tcleval(cgs=-4.99e-14)
tcleval(csb=-1.457e-14
```

snapshot clearly showing parameters.

2. AC Analysis

1) Report the Bode plot magnitude.

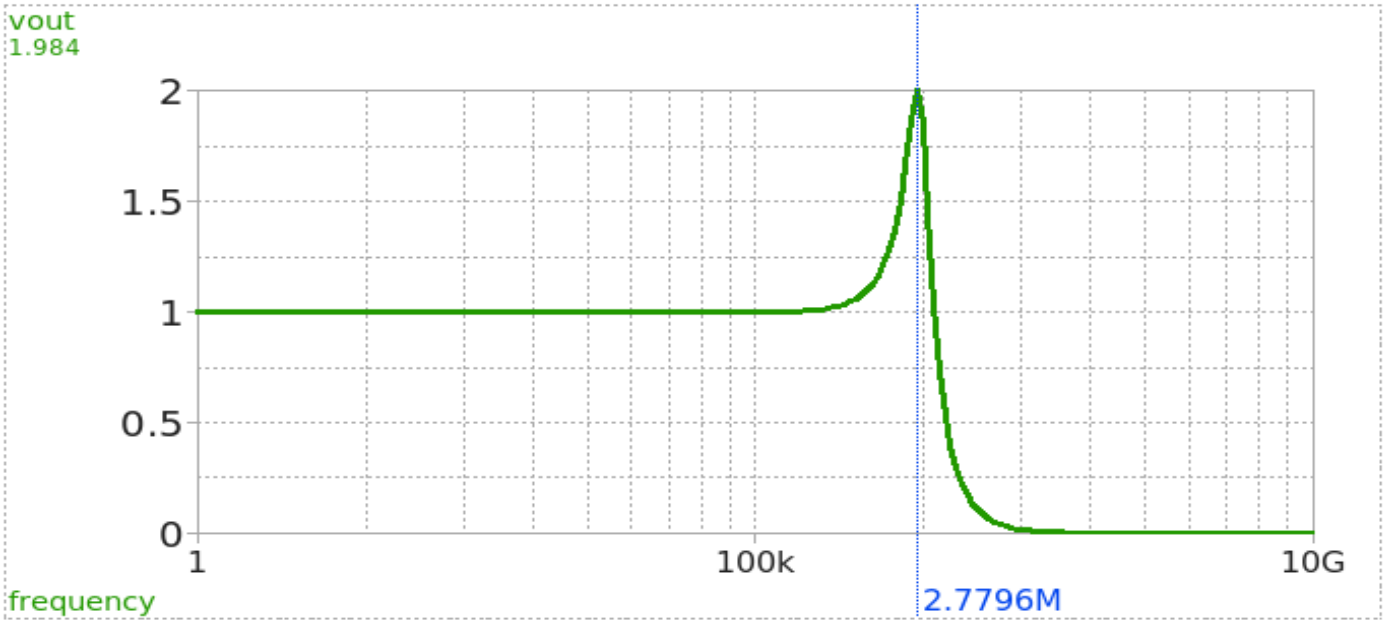


Figure 3: VOUT VS freq (linear scale)

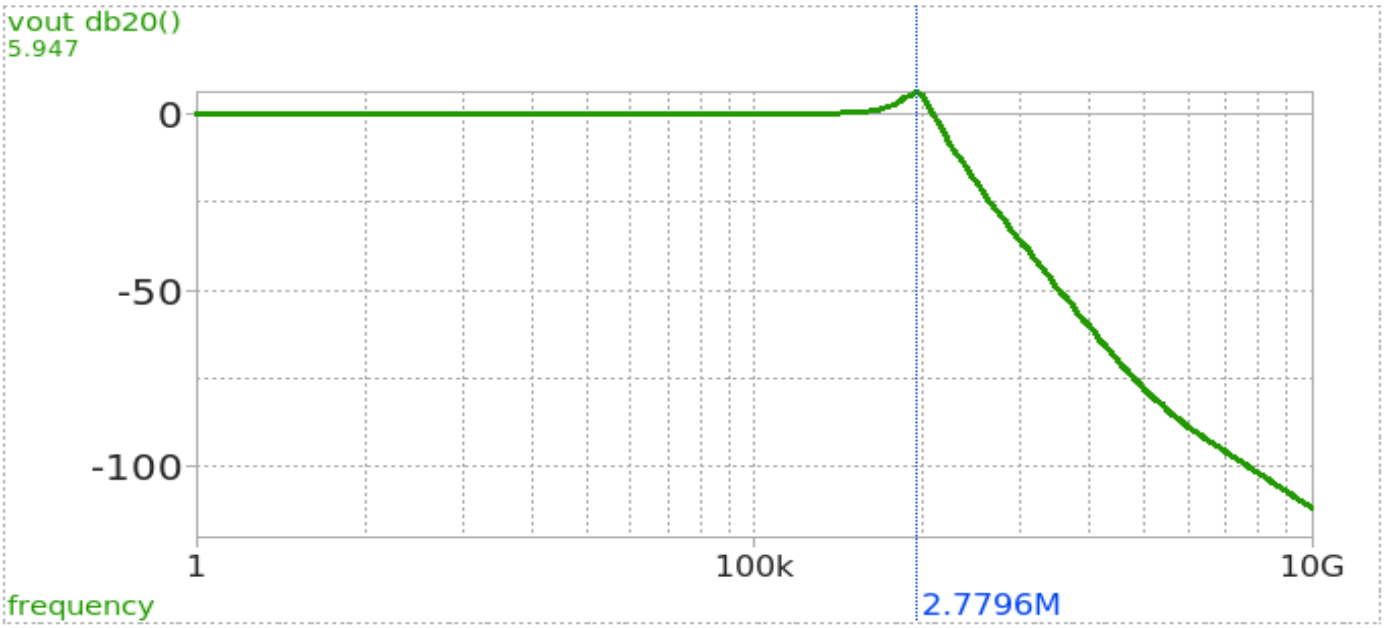


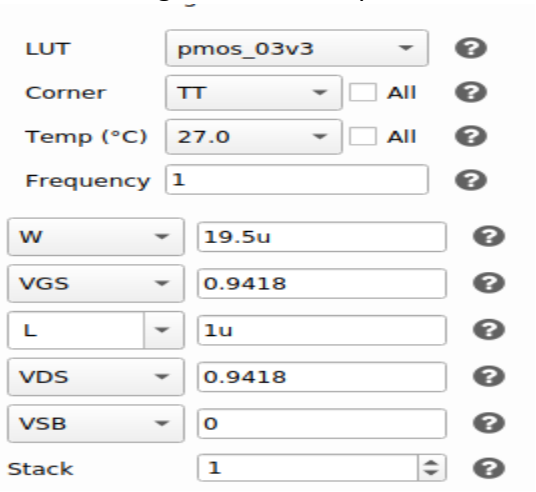
Figure 4: VOUT VS freq(db scale)

3) Do you notice frequency domain peaking? How much is the peaking?

Yes, there is noticeable frequency domain peaking, Peak magnitude: ≈2V(linear scale) and ≈6db(db scale) (at ≈2.78 MHz)

4) Analytically calculate the quality factor (use approximate expressions). Is the system underdamped or overdamped?

I got values of caps from ADT as shown in next photo



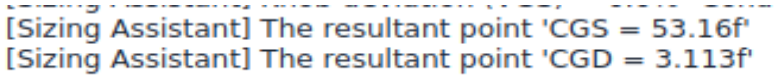


Figure 5: value of Cgs &Cgd

Approximated: $Q = \frac{\sqrt{b_2}}{b_1} = \sqrt{\frac{g_{m(C_{gs}+C_{gd})R_{sig}}}{C_L}} = 2.3828$

Exact: $b_1 = C_{gd}R_{sig} + \frac{C_{gs}+C_L}{g_m}$

$b_2 = \left(\frac{(C_{gs}+C_{gd})C_L + C_{gs}C_{gd}}{g_m}\right)$

$Q = \frac{\sqrt{b_2}}{b_1} = 1.7677$ Q>0.5, SO underdamped

5)

- Report Bode plot magnitude overlaid on same plot.

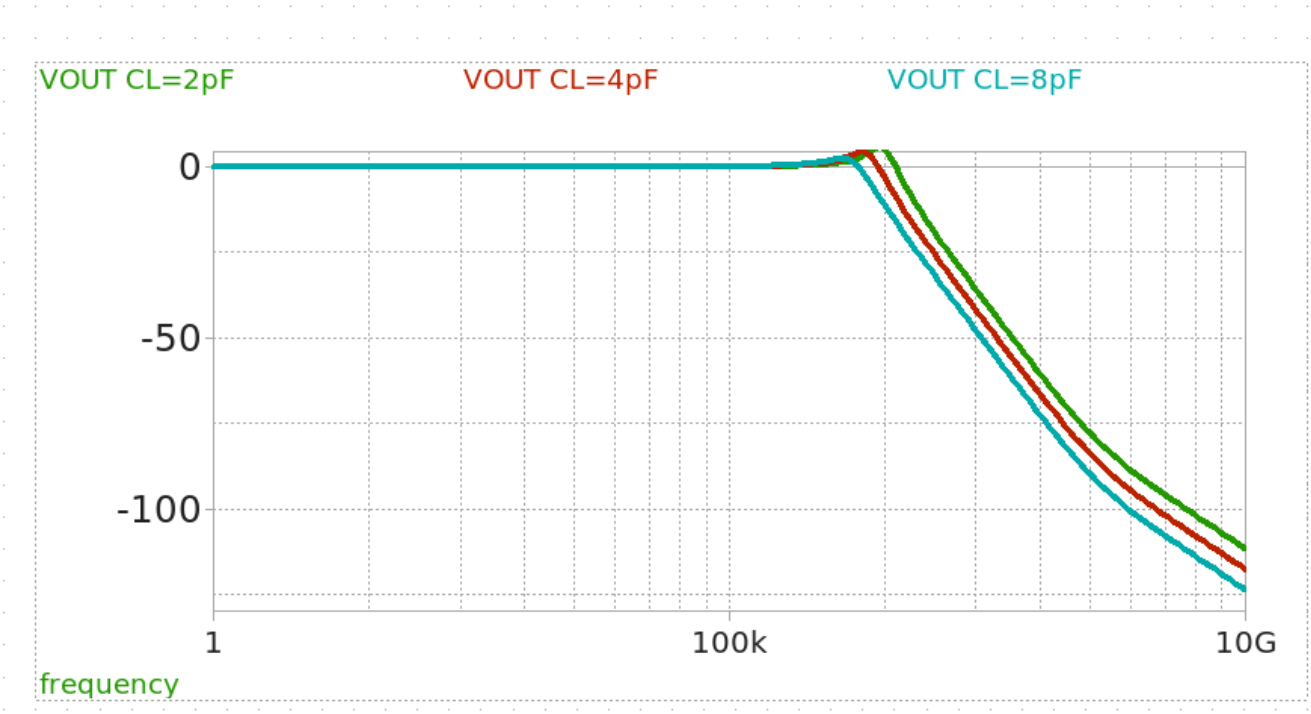


Figure 5: vout for given values of CL (db scale)

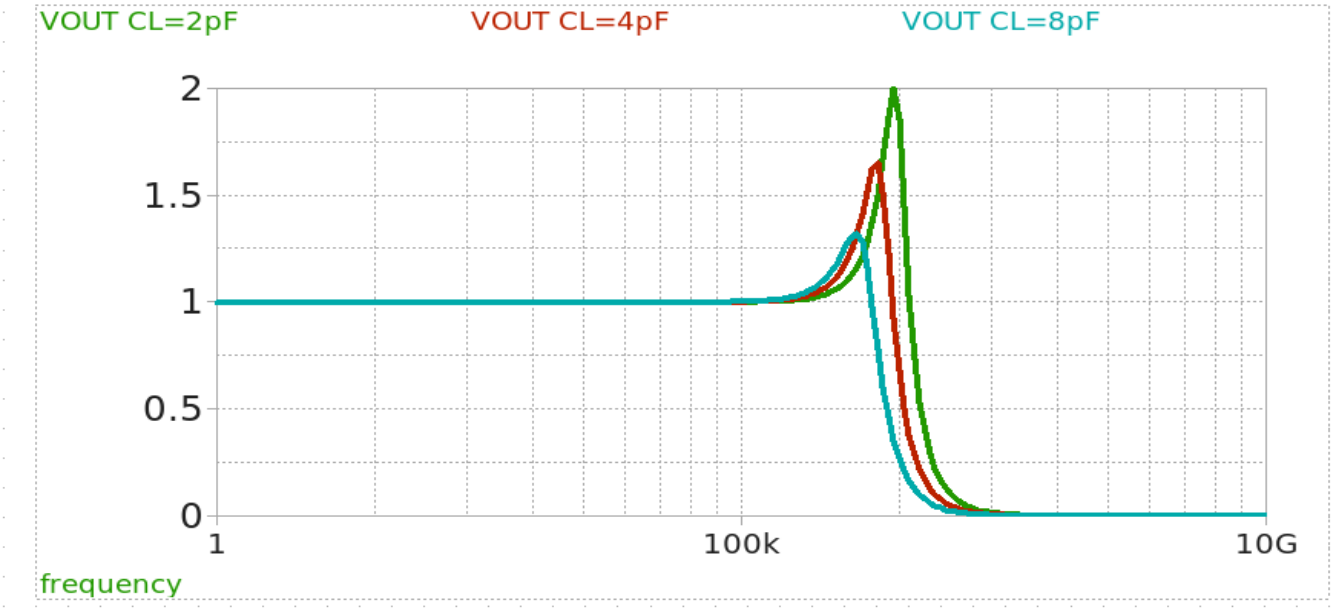


Figure 6:vout for given values of CL (linear scale)

- Report the peaking vs CL.

```
1 peaking = 1.999430e+00
2 peaking = 1.651603e+00
3 peaking = 1.320388e+00
```

→ Values from simulation on xschem

Cl (pF)	Peaking (V)	Peaking (dB)*
2p	1.999430	≈6.02 dB
4p	1.651603	≈4.36 dB
8p	1.320388	≈2.41 dB

Figure 7:Peaking vs. Cl values

Comment on the previous results:

The results show that higher C_L (capacitance) reduces peaking, indicating less resonant behavior. The strongest peaking occurs at 2pF, while 8pF provides the most stable response.

6)

- Report Bode plot magnitude overlaid on same plot.

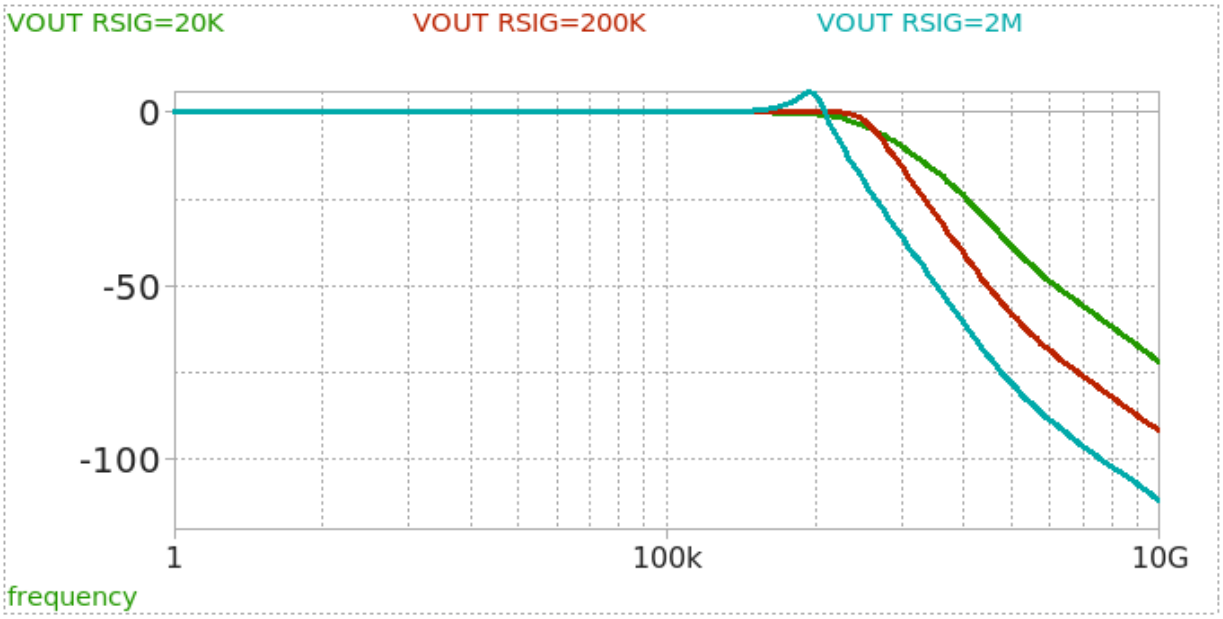


Figure 8:vout for given values of CL (db scale)

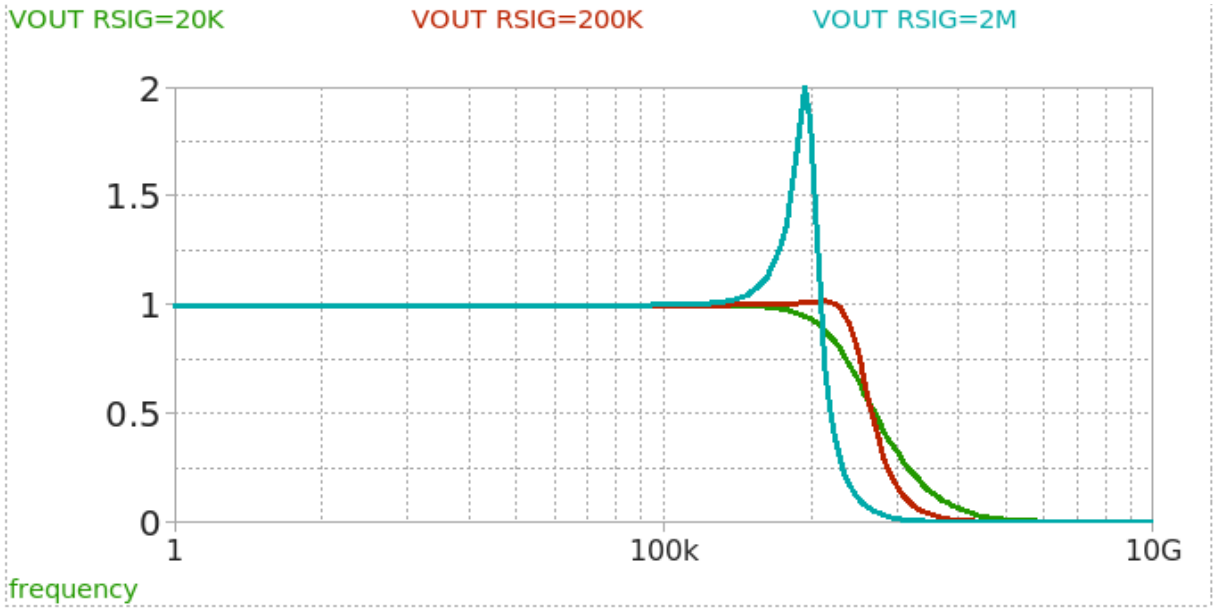


Figure 9:vout for given values of Rsig (linear scale)

- Report the peaking vs Rsig.

```
peaking = 9.977310e-01
peaking = 1.015393e+00
peaking = 1.999430e+00
```

→ Values from simulation on xschem

Rsig (Ω)	Peaking (V)	Effect
20k	0.9977 (~1.00)	**Minimal peaking** (stable)
200k	1.0154 (~1.02)	**Slight peaking**
2M	1.9994 (~2.00)	**Strong peaking** (resonant)

Figure 10:Peaking vs. Rsig values

Comment on the previous results:

The results show that higher Rsig (resistance) increases peaking, indicating stronger resonant behavior. The weakest peaking occurs at 20kΩ, while 2MΩ produces the most pronounced response. This suggests lower Rsig dampens oscillations, making the circuit more stable, while higher Rsig allows sharper resonance.

3. Transient Analysis

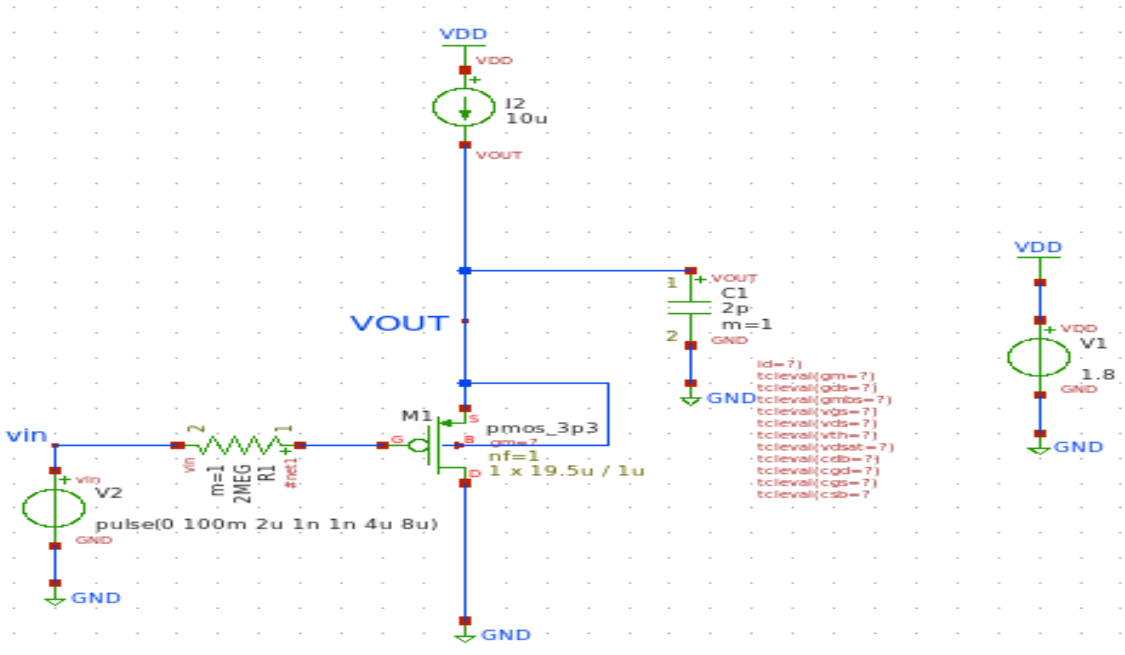


Figure11: schematic

3) Report Vin and Vout overlaid vs time.

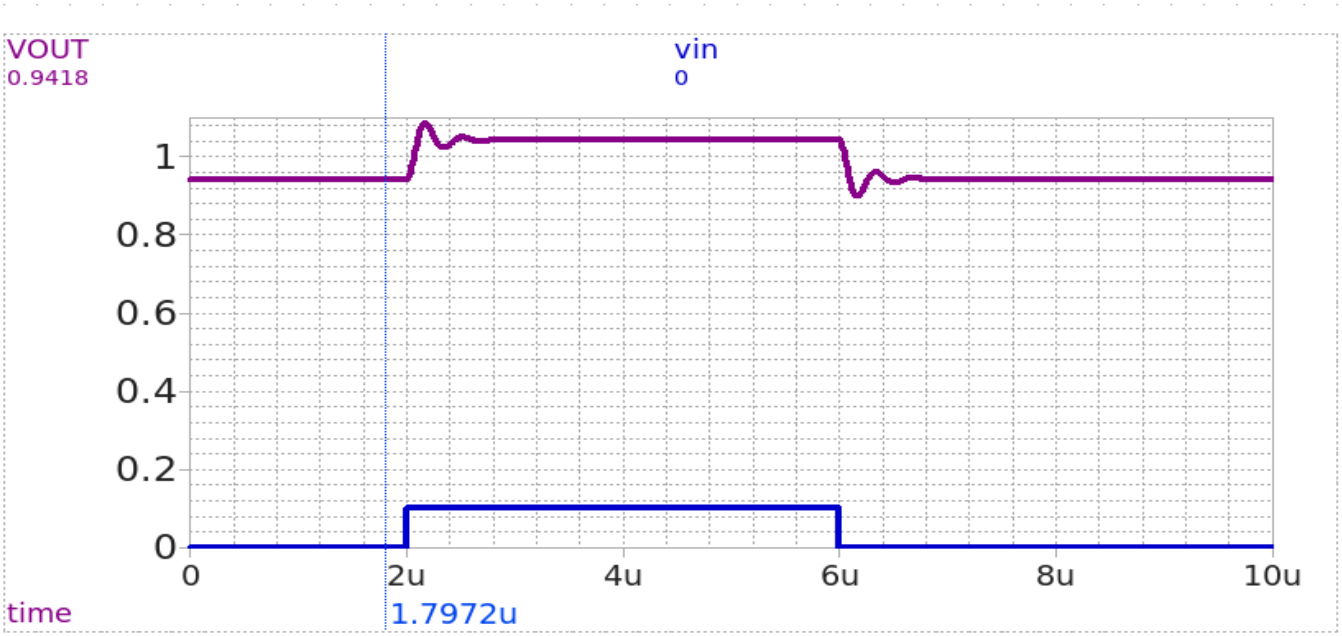


Figure 12: vout&vin VS time

4)

- Calculate the DC voltage difference (DC shift) between Vin and Vout.

From graph: Vin= 0 , Vout= 0.9418 V ⟶ DC Shift = Vout – Vin = 0.9418 V

- What is the relation between the DC shift and VGS of the transistor?

Equals Vgs because PMOS always shifts DC level up by its |VGS|

- How to shift the signal down instead of shifting it up?

Use an NMOS (instead of PMOS)

5) Do you notice time domain ringing? How much is the overshoot?

YES, IT is percentage = 43.101%

6) Perform parametric sweep: CL = 2p, 4p, 8p

- Report Vout vs time overlaid on same plot.

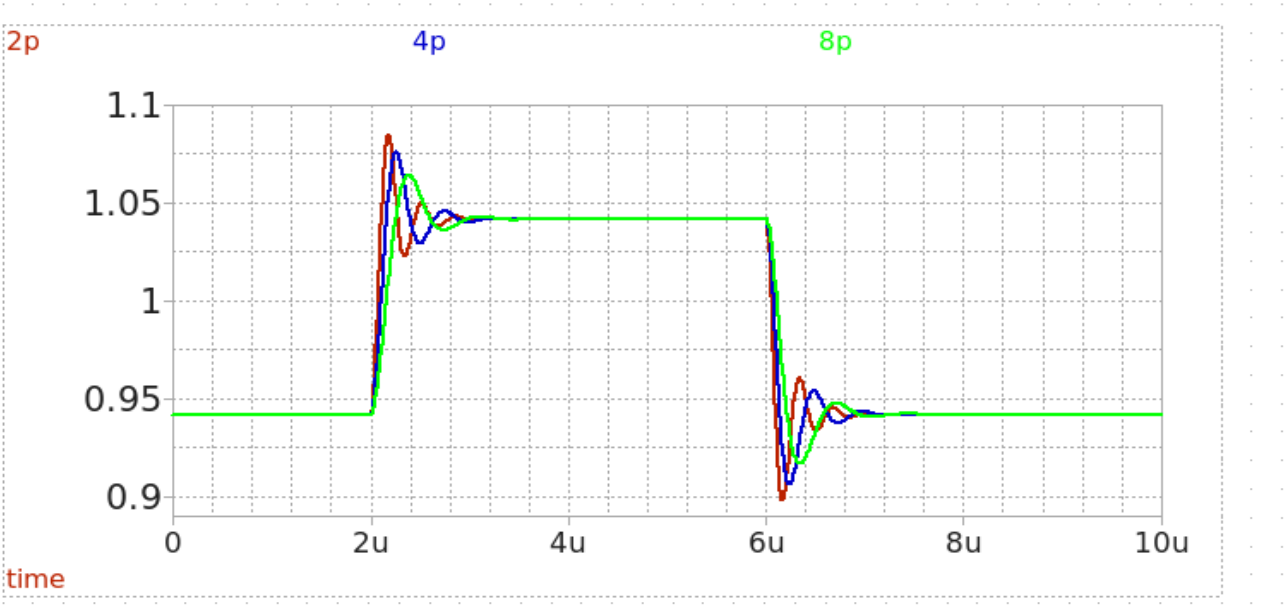


Figure 13: vout at diff values of CL

- Report the overshoot vs CL.

```
1 overshoot = 4.310105e+01
2 overshoot = 3.424372e+01
3 overshoot = 2.259353e+01
```

→ Values from simulation on xschem

C_L (pF)	Overshoot (%)	Effect
2p	43.1%	**Severe ringing** (underdamped)
4p	34.2%	Moderate ringing
8p	22.6%	**Improved stability**

Figure 14:OVERSHOOT vs. CL values

Comment on the previous results:

The results show that higher CL (capacitance) reduces overshoot, indicating improved damping of transient oscillations. The strongest overshoot (43.1%) occurs at CL=2pF (underdamped), while CL=8pF delivers the most stable response (22.6% overshoot). This confirms that larger CL suppresses ringing by lowering the circuit's effective Q-factor

7) Perform parametric sweep: Rsig = 20k, 200k, 2M.

- Report Vout vs time overlaid on same plot.

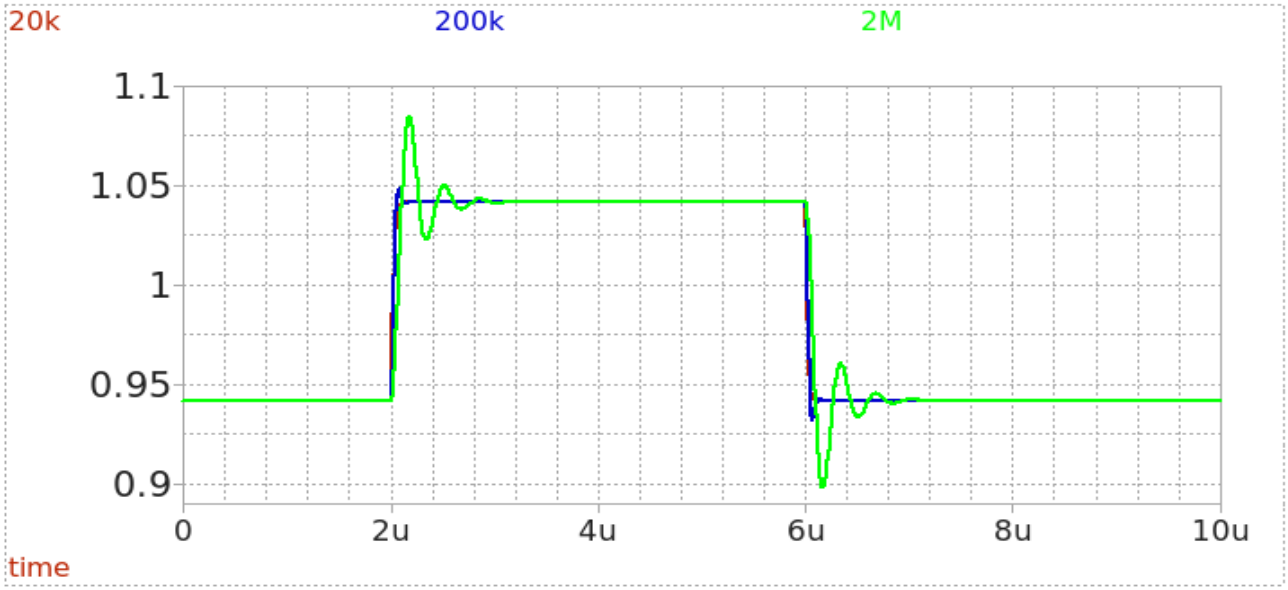


Figure 15: VOUT at diff valuesoif Rsig

- Report the overshoot vs Rsig.

```
1 overshoot = 0.000000e+00
2 overshoot = 6.725675e+00
3 overshoot = 4.310105e+01
```

→ Values from simulation on xschem

R_{sig} (Ω)	Overshoot (%)	Effect
20k	0%	**Critical damping** (no overshoot)
200k	6.7%	**Moderate damping** (minimal overshoot)
2M	43.1%	**Underdamped** (severe ringing)

Figure 16:OVERSHOOT vs. Rsig values

Comment on the previous results:

The results demonstrate that lower Rsig (resistance) reduces overshoot, indicating stronger damping of transient oscillations. The worst overshoot (43.1%) occurs at Rsig=2MΩ (underdamped), while Rsig=20kΩ completely eliminates overshoot (0%), providing perfect stability. This confirms that smaller Rsig suppresses ringing by increasing damping in the circuit.

4. Z_{out} (Inductive Rise)

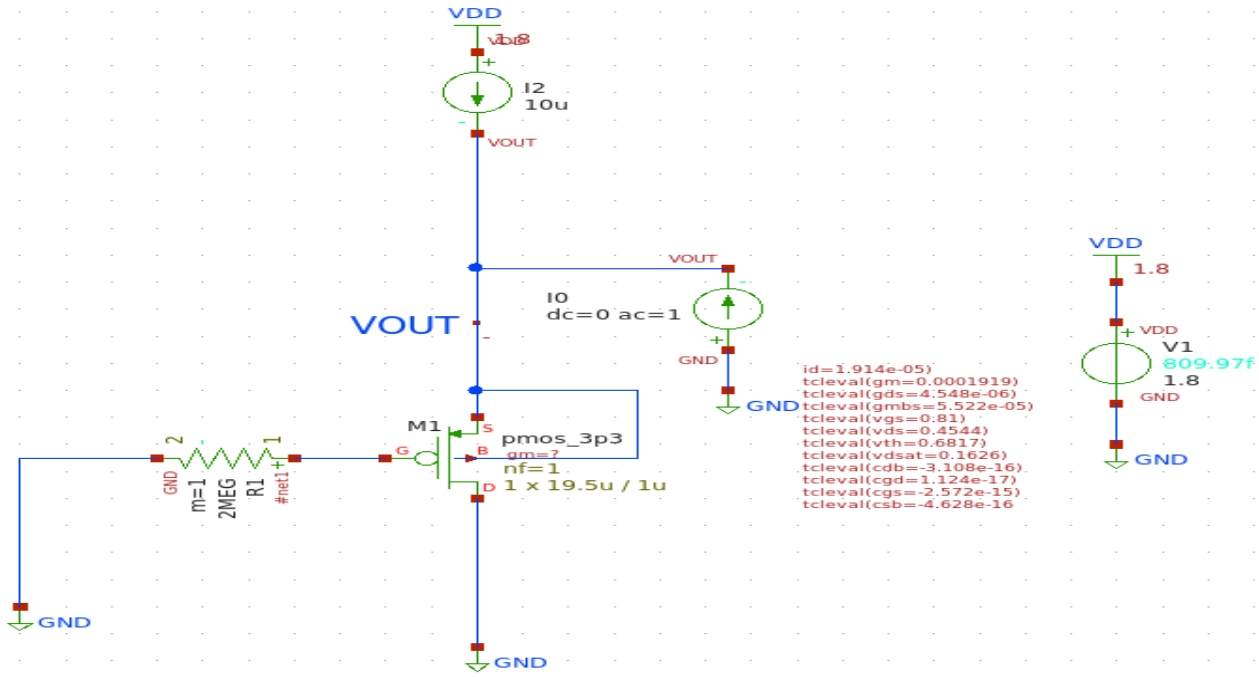


Figure 17: SCHEMATIC

3)Plot the output impedance (magnitude and phase) vs frequency

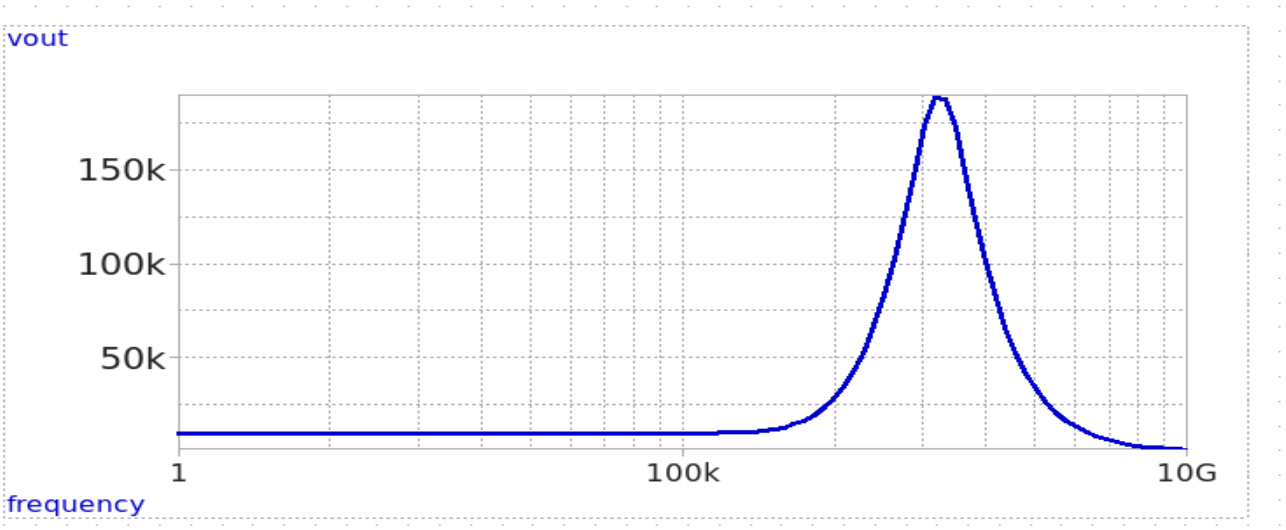


Figure 18: Zout(mag) VS freq

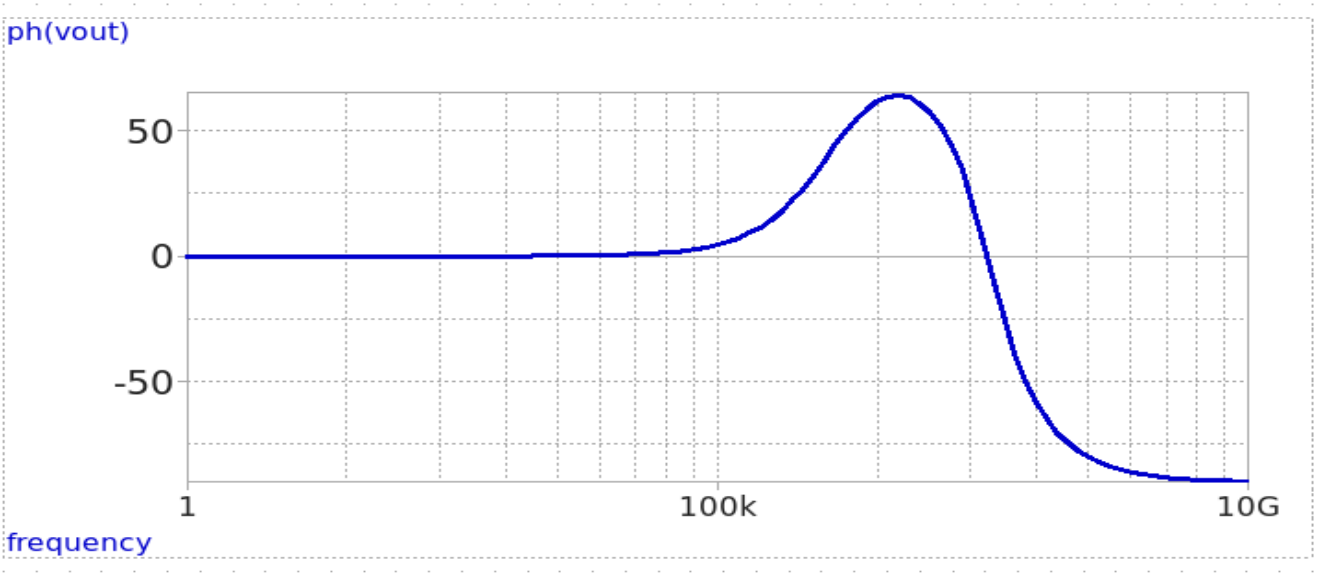


Figure 19: Zout(phase) VS freq

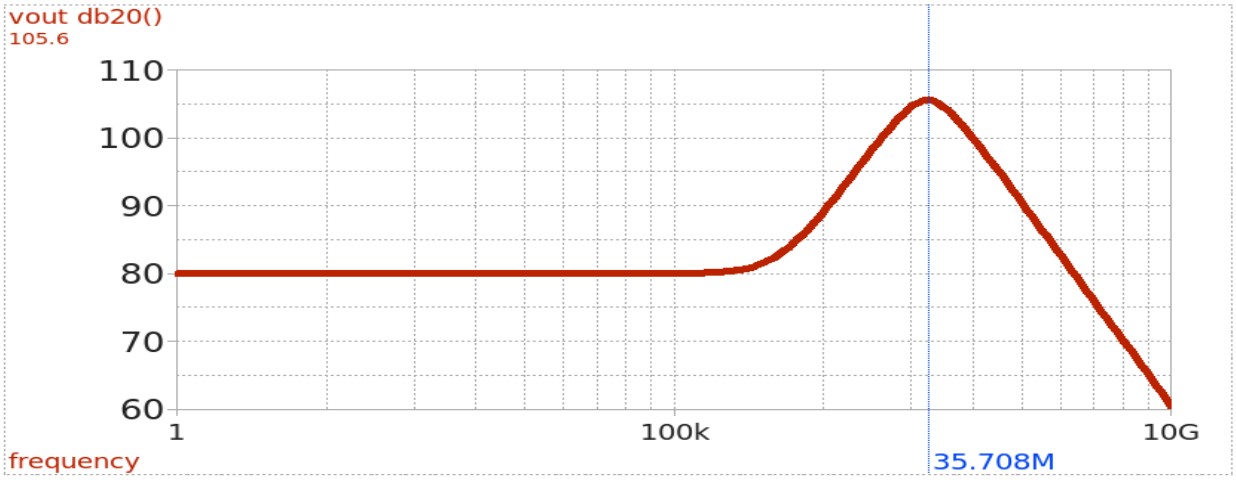
Do you notice an inductive rise? Why?

Yes, there is an inductive rise in the output impedance (ZOUT) , This is caused by the PMOS transistor's parasitic capacitances (Cgd, Cgs) interacting with the circuit

4)Does Z_{out} fall at high frequency? Why?

Yes, Zout falls at high frequency because C_{gd} dominates: At high frequencies, C_{gd}shunts Rsig, creating a low-impedance path ($Z \approx \frac{1}{R_{sig} C_{gd}}$)

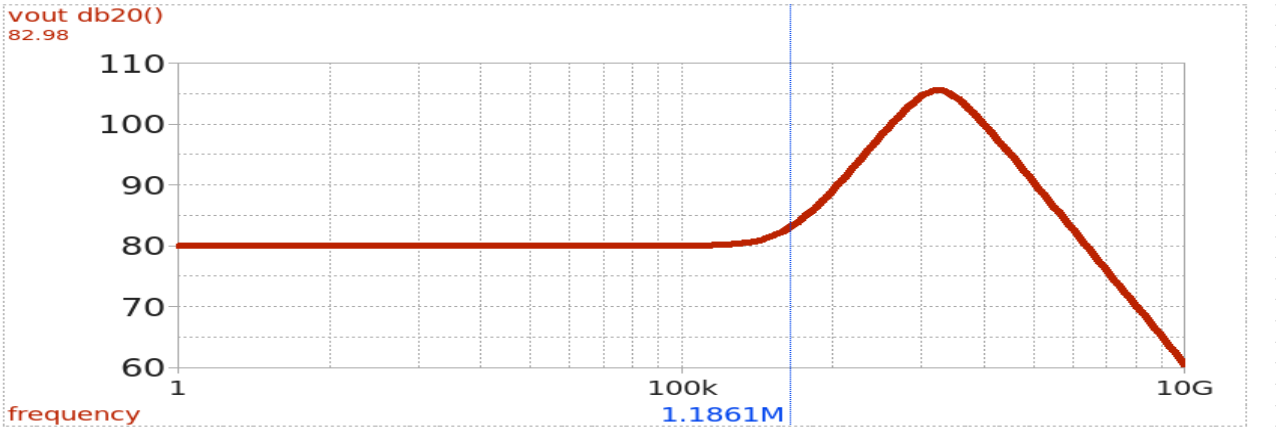
5) Analytically calculate the zeros, poles, and magnitude at low/high frequency for Z_{out}. Compare with simulation results in a table.



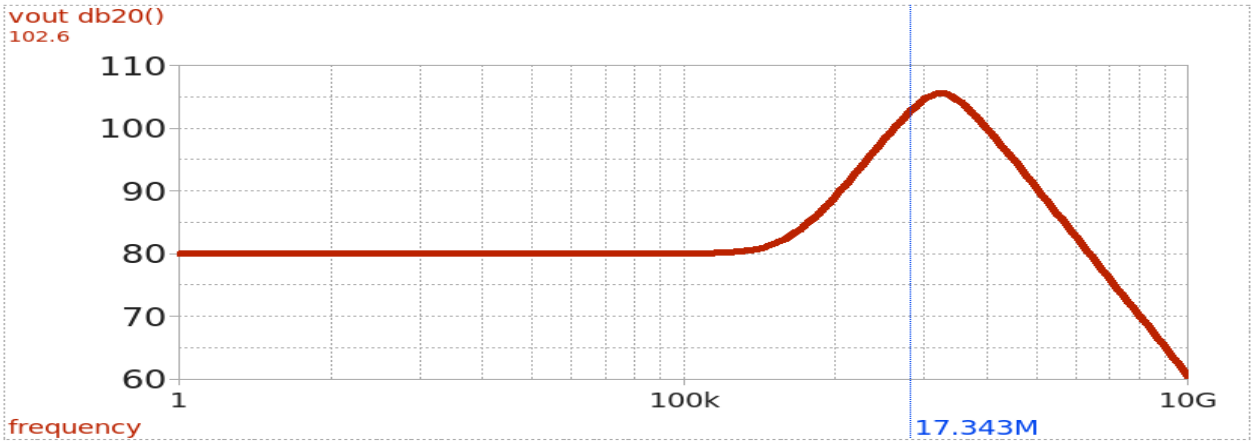
comment

As we see the curve starts at 80 db then increase until it reaches max value approximately at 105.6 db so we have one zero and 2 poles the first zero we will find around at 83 db and first pole approximately at 102.6 db from the left of max value and second pole approximately at 102.6 db

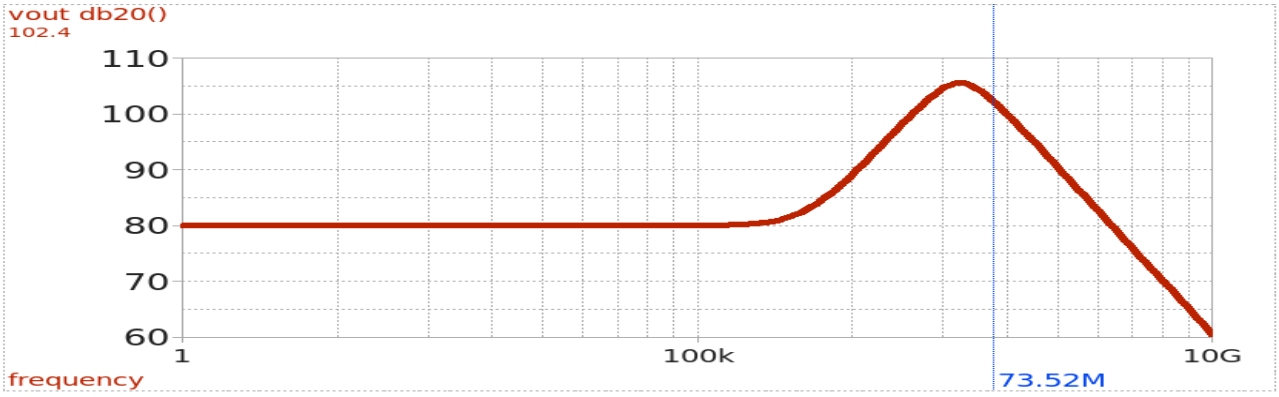
- ZERO:



- THE FIRST POLE:



- THE SECOND POLE:



HAND ANALYSIS

$$.Z_{sig} = R_{sig} // \frac{1}{C_{gd}} \longrightarrow i_x = \frac{v_x}{\frac{1}{sC_{gs}} + Z_{sig}} + g_m \times \frac{v_x}{\frac{1}{sC_{gs}} + Z_{sig}} \times \frac{1}{sC_{gs}}$$

$$.Z_{out} = \frac{i_x}{v_x} = \frac{1}{g_m}\left(\frac{1+sz_{sig}C_{gS}}{\left(1+S\frac{C_{gs}}{g_m}\right)}\right) = \frac{1}{g_m}\left(\frac{1+sR_{sig}\left(C_{gS}+C_{gd}\right)}{\left(1+S\frac{C_{gs}}{g_m}\right)\left(1+SC_{gs}R_{sig}\right)}\right)$$

- $F_Z = \frac{1}{2\pi \times R_{sig}\left(C_{gS}+C_{gd}\right)}$ = 1.414 MHZ
- $F_{p1} = \frac{1}{C_{gs}R_{sig}} = 25.563$ MHZ
- $F_{p2} = \frac{g_m}{C_{gs}} = 302.08$ MHZ

By intuition: $\omega \downarrow\downarrow$ (LOW frequency): $Zout \approx 1/gm \approx$ 9.912 KΩ

$\omega \uparrow\uparrow$ (HIGH frequency): $Zout \approx \frac{SR_{sig}(C_{gs}C_{gd})}{SR_{sig}C_{gs}g_m} = \frac{(C_{gs}C_{gd})}{C_{gs}g_m} \approx$ 0.17916 MΩ

	F_Z	F_{p1}	F_{p2}	(LOW frequency): $Zout$	(HIGH frequency): $Zout$
Hand analysis	1.414 MHZ	25.563 MHZ	302.08 MHZ	9.912 KΩ	0.17916 MΩ
From simulation	1.1861 MHZ	17.343 MHZ	73.52 MHZ	9.888 KΩ	0.1893 MΩ

Important NOTE:

The simplified hand analysis presented earlier provides useful intuition but lacks full accuracy because it neglects two critical components:

Drain-Bulk Capacitance (Cdb): This parasitic capacitance appears between drain and substrate.

Output Resistance (ro): The transistor's finite output resistance.

If i took both Cdb and ro into account, the equation becomes huge like this:

$$\frac{V_x}{i_x} = \frac{\left(1 + SR_{sig}\left(C_{gs} + C_{gd}\right)\right) r_0}{S^2\left[R_{sig}\left(C_{gs} + C_{gd}\right)C_{dB}r_0 + R_{sig}C_{gd}r_0C_{gs}\right] + S\left[C_{dB}r_0 + R_{sig}\left(C_{gs} + C_{gd}\right) + C_{gs}r_0 + g_m r_0 C_{gd}R_{sig}\right] + g_m r_0 + 1}$$

Figure 20: exact expression for Zout

5. [Optional] How to solve the peaking/ringing problem?

1) The simple solution is to place the input/output poles away from each other (as we did when we swept CL and Rsig).

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2) Alternatively, a compensation network can be used to compensate for the negative input impedance and prevent overshoots

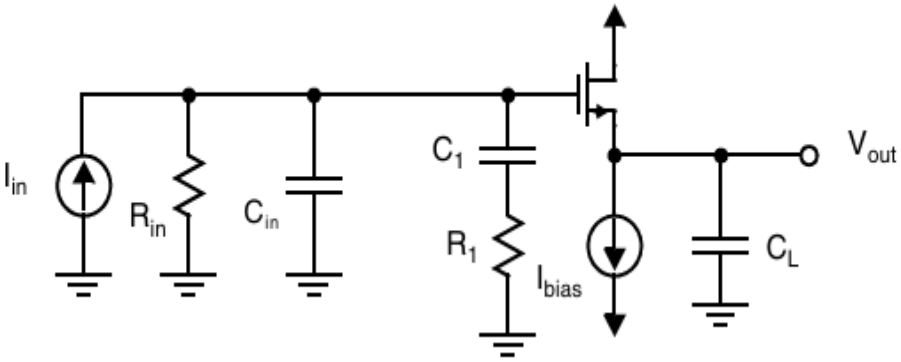

Figure 21: schematic after adding compensation network

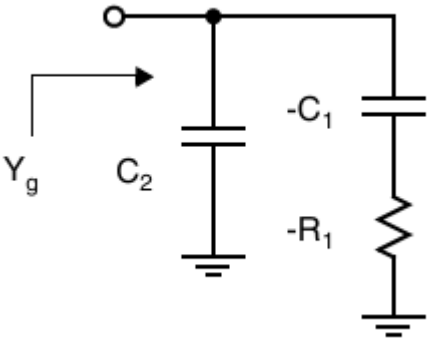

Figure 22: compensation network

Adding a compensation network (C1 and R1) to compensate for the negative components of the admittance looking into the gate of the source-follower

$$R_1 = \frac{(C_{gs}+C_L)^{\wedge}2}{g_m C_{gs} C_L} = 392.952\ K\Omega \qquad C_1 = \frac{C_{gs} C_L}{(C_{gs}+C_L)} = 51.78\ fF$$

schematic:

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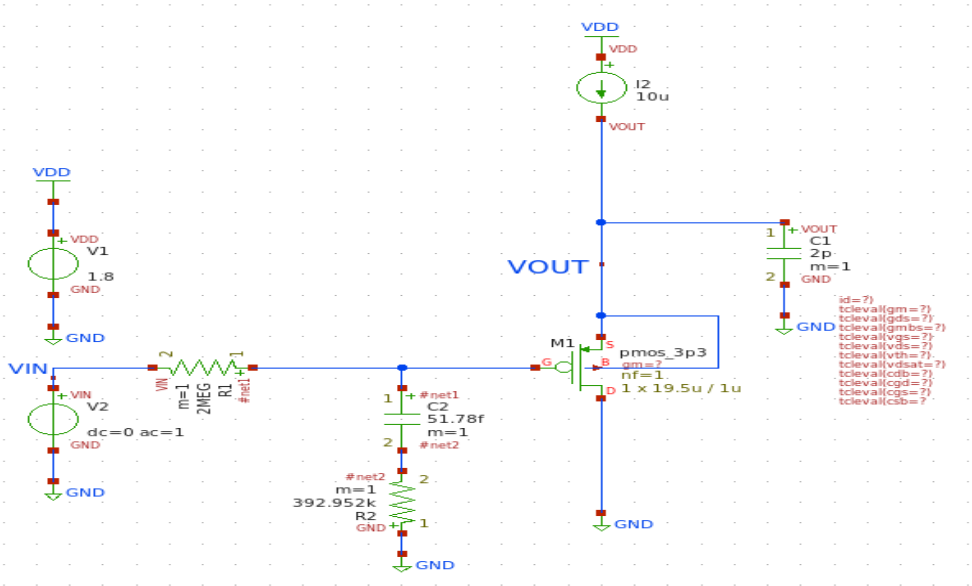

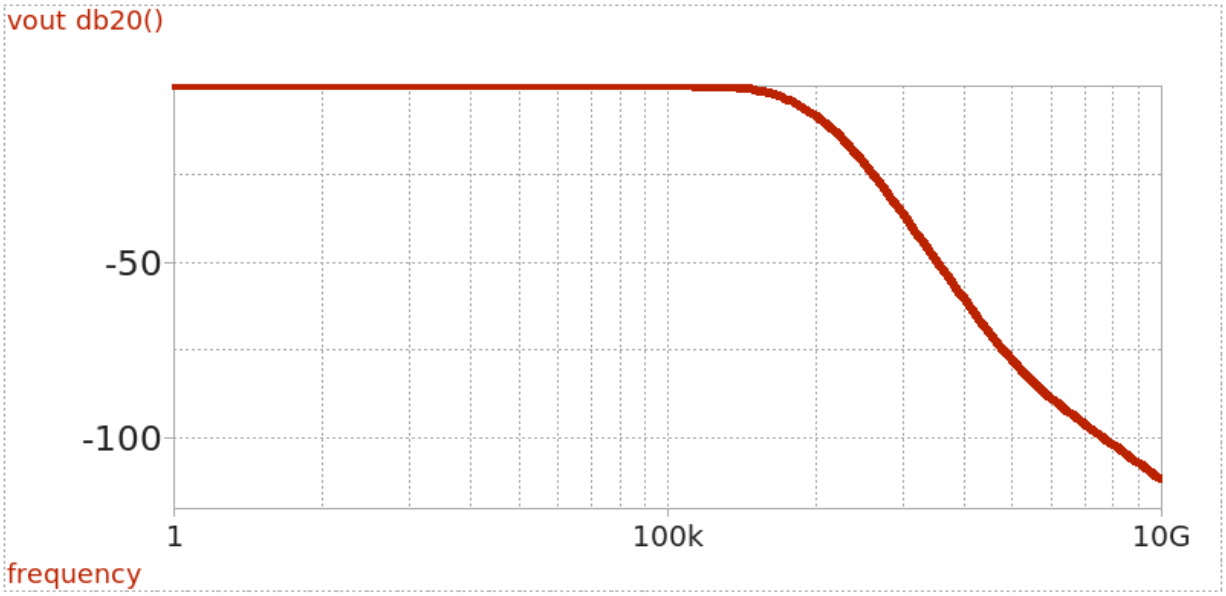

Figure 23: vout vs dreq (ac analysis)

- There is no peaking at frequency domain

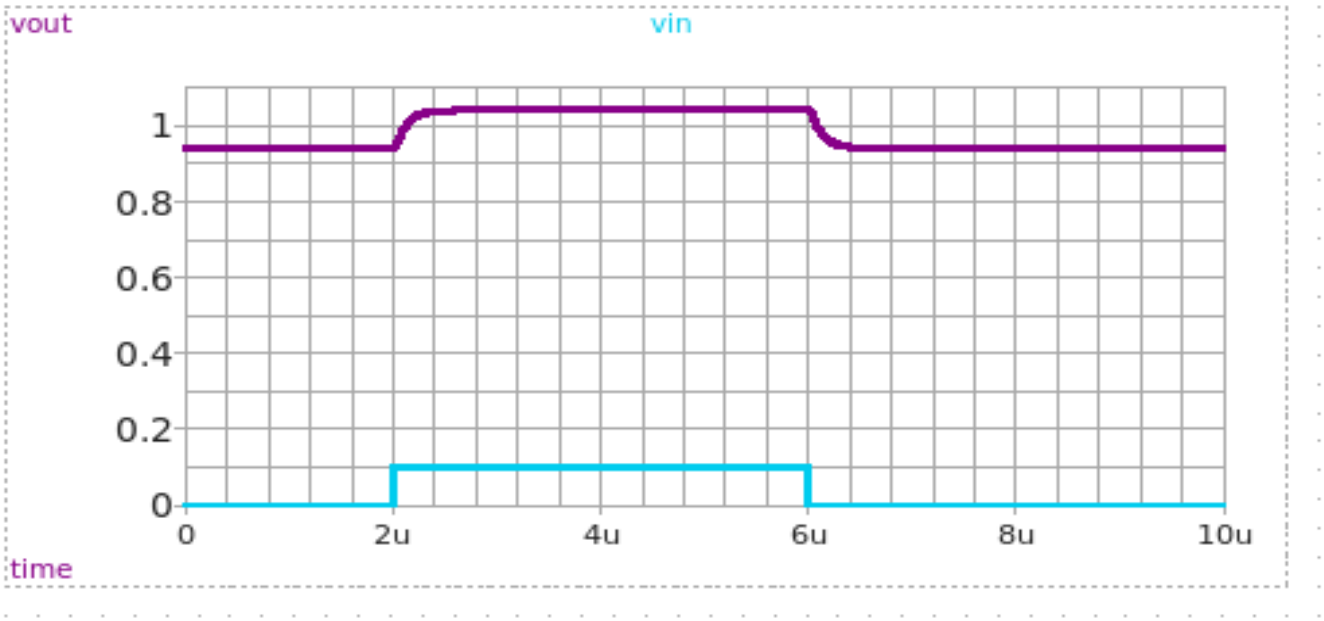

Figure 24: vout&vin VS time (transient analysis)

- There is no ringing at time domain