Analog IC Design – Xschem and Master Micro Tools Lab
07

gm/ID Design methodology

Part 1: gm/ID Design Charts

1) For L = 0.28u

PMOS:

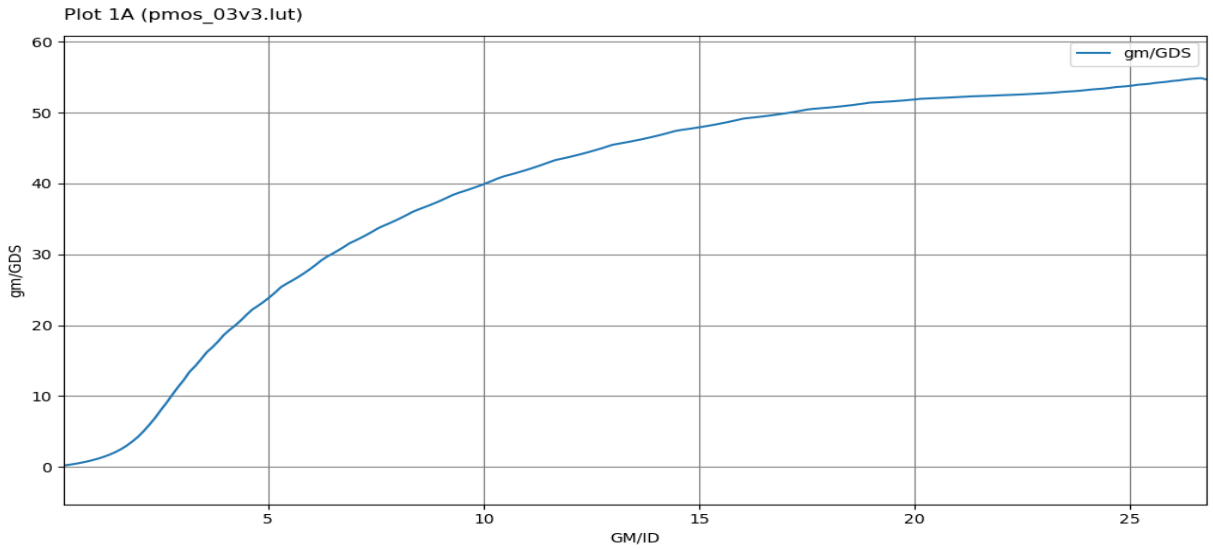


Figure 1: intrinsic gain

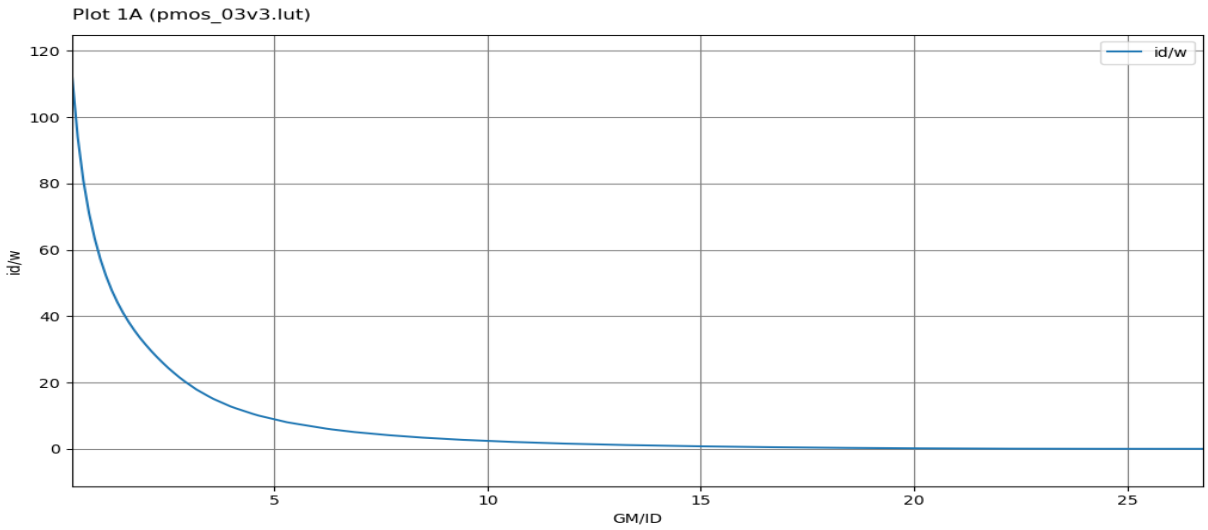


Figure 2: ID/W

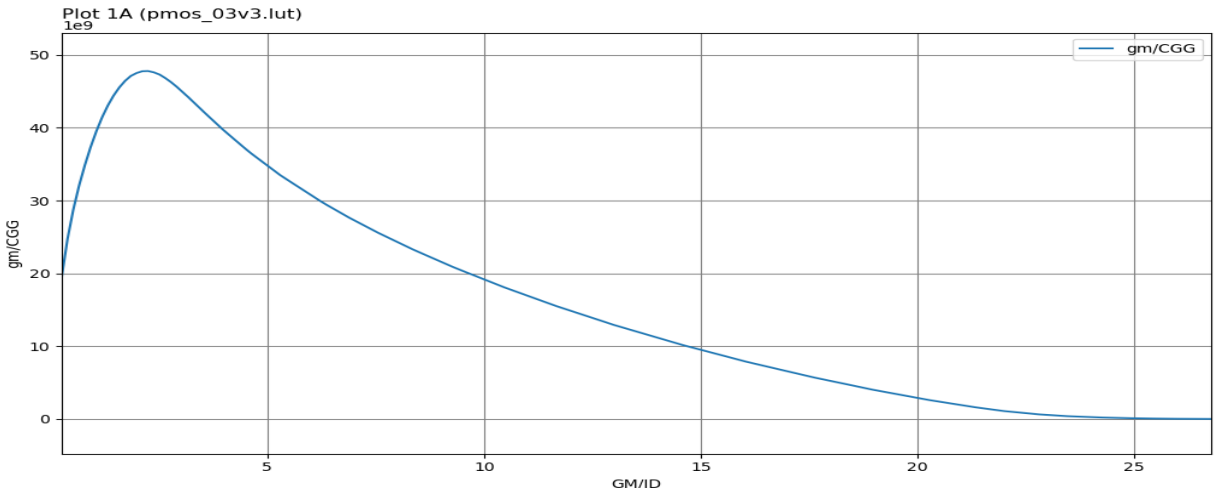


Figure 5:GM/CGG

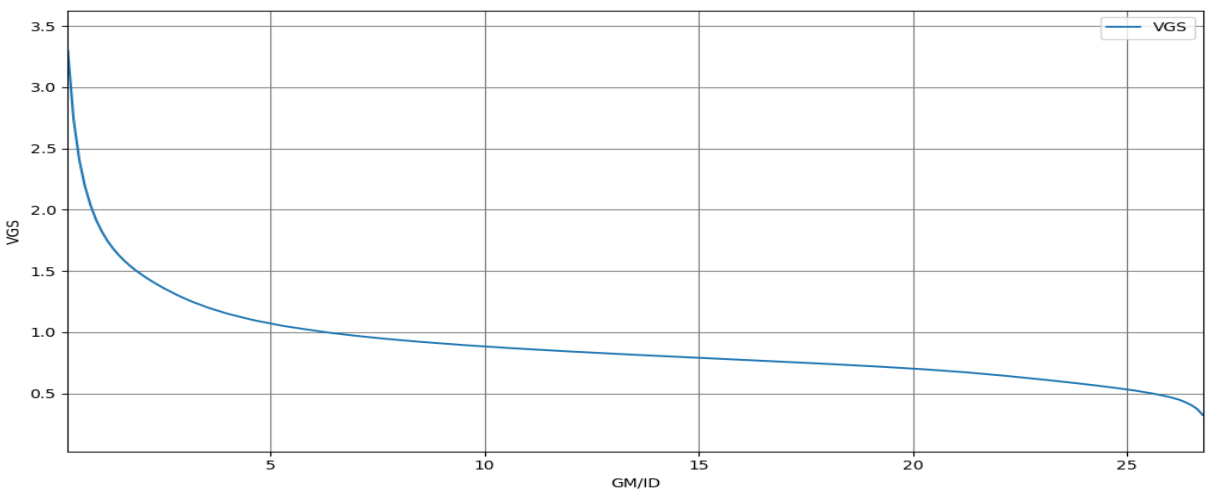


Figure 4:VGS

NMOS

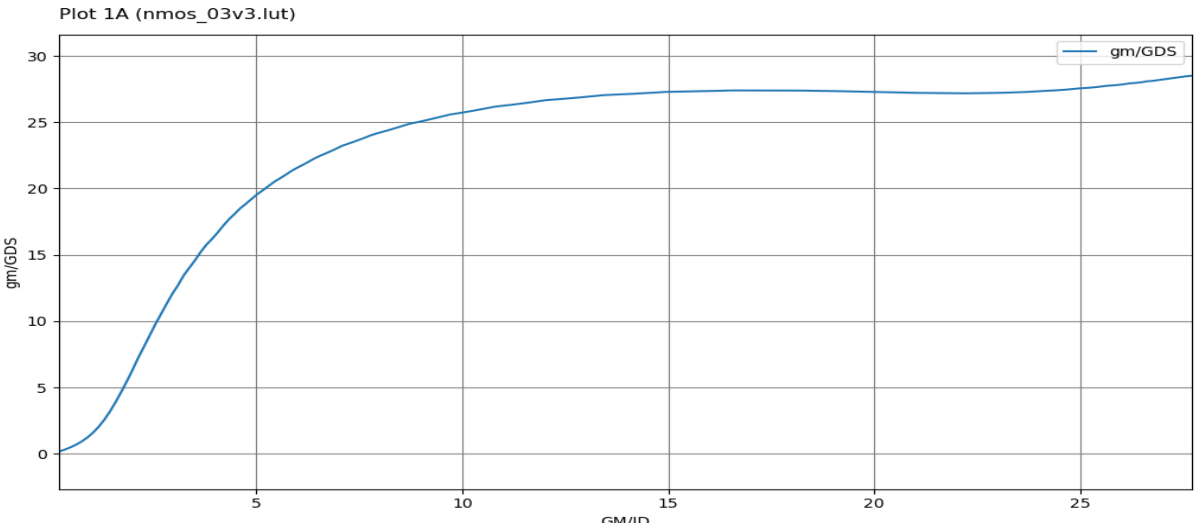


Figure 3: intrinsic gain

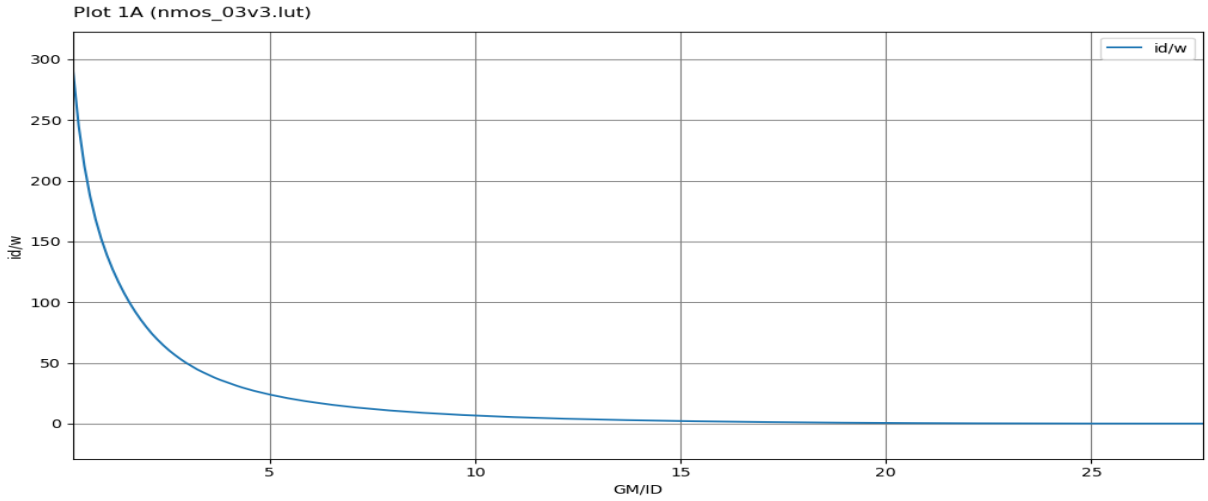


Figure 8:ID/W

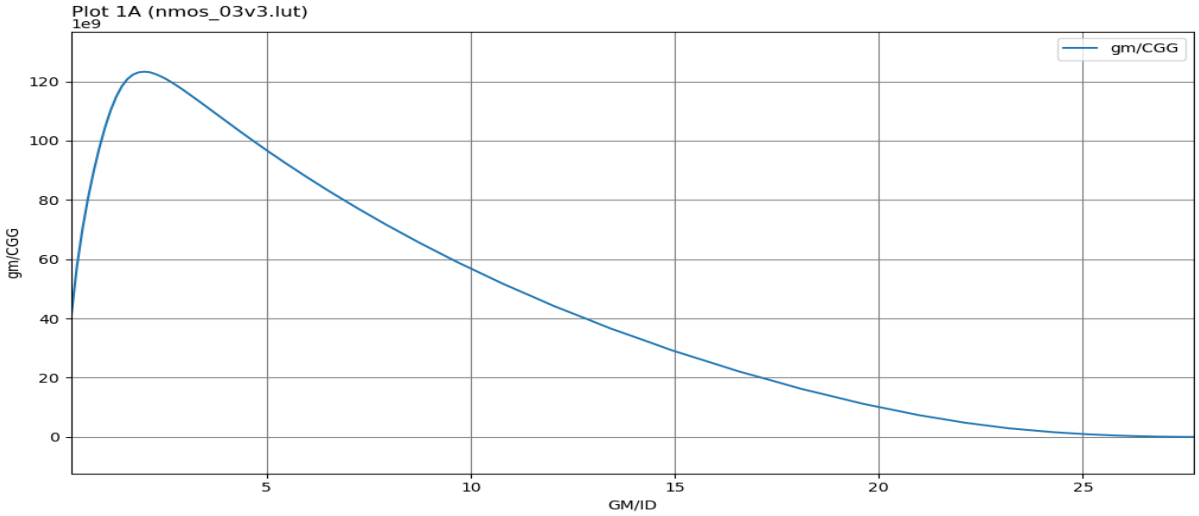


Figure 7:GM/CGG

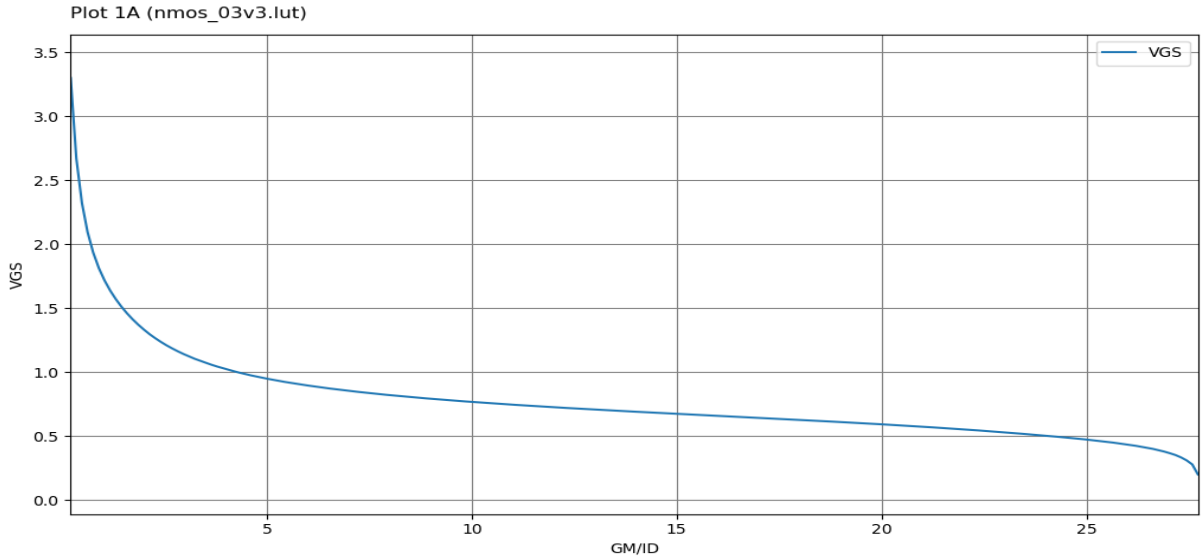


Figure 6:VGS

For L=0.4u:0.4u:2u

PMOS:

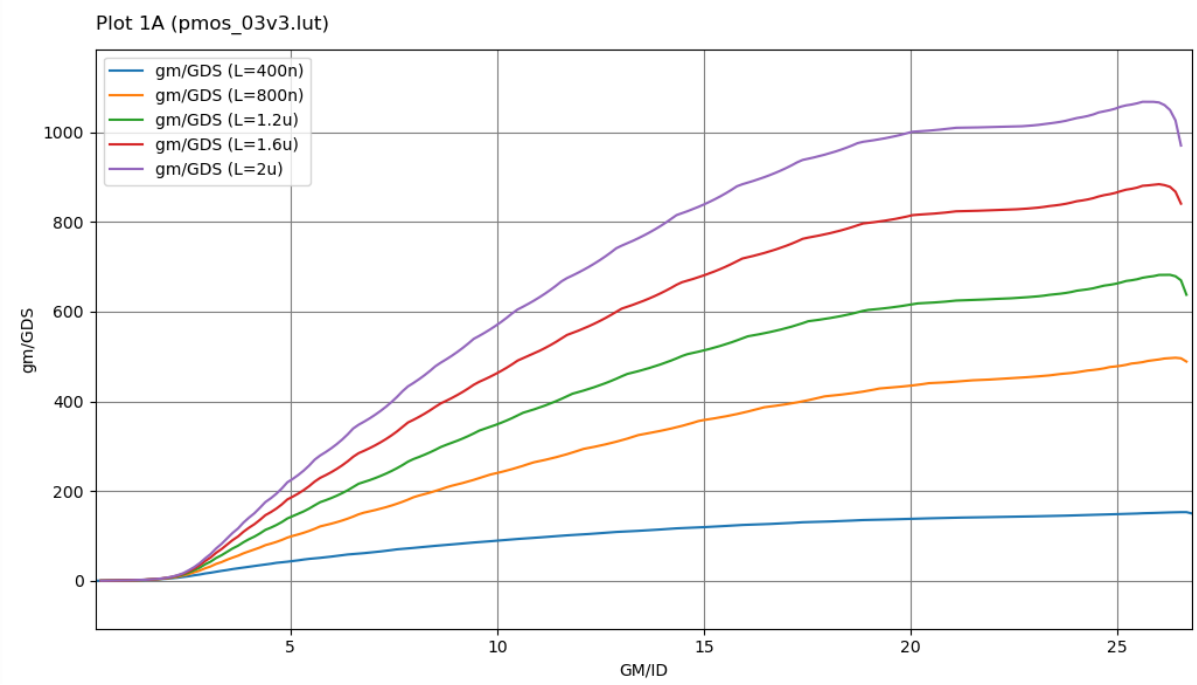


Figure 9:intrinsic gain

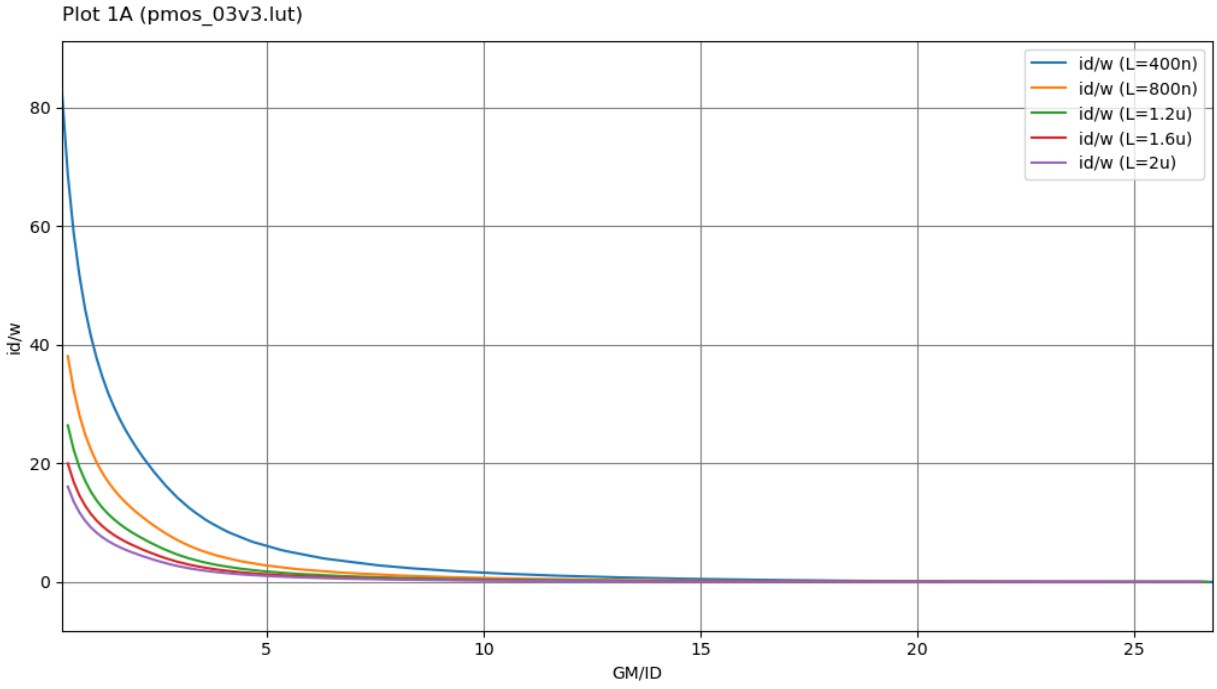


Figure 10:ID/W

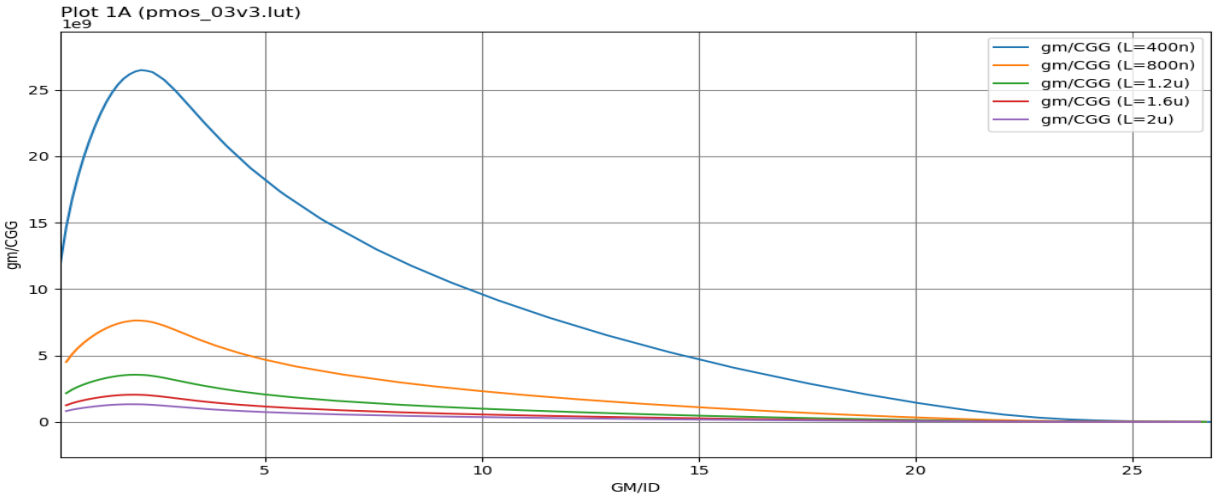


Figure 12:GM/CGG

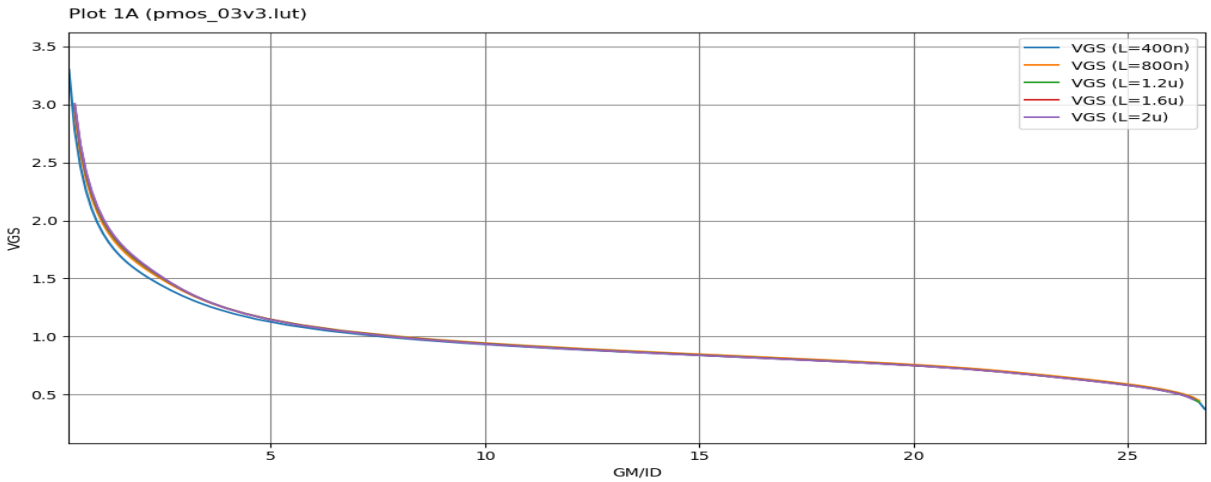


Figure 11:VGS

NMOS:

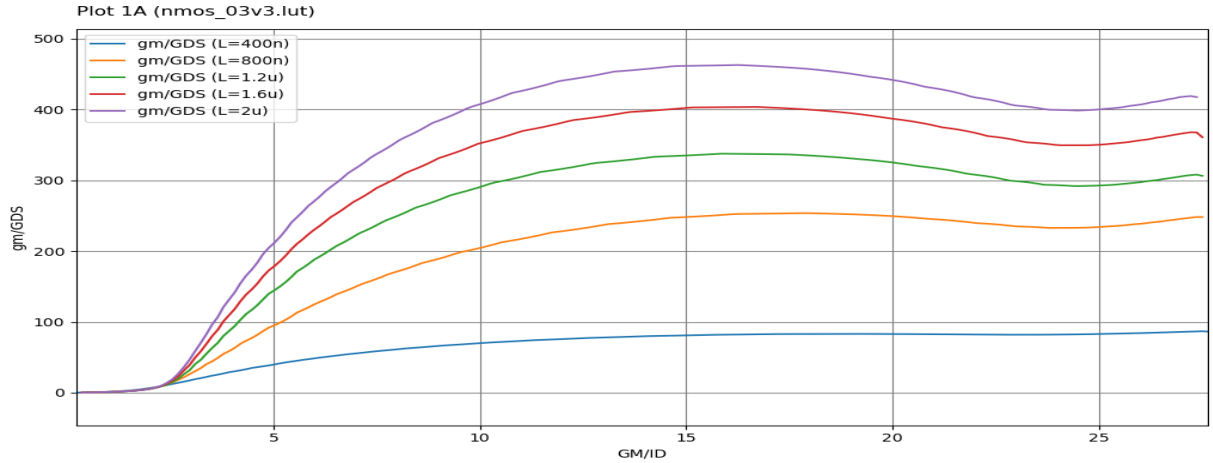


Figure 13: intrinsic gain

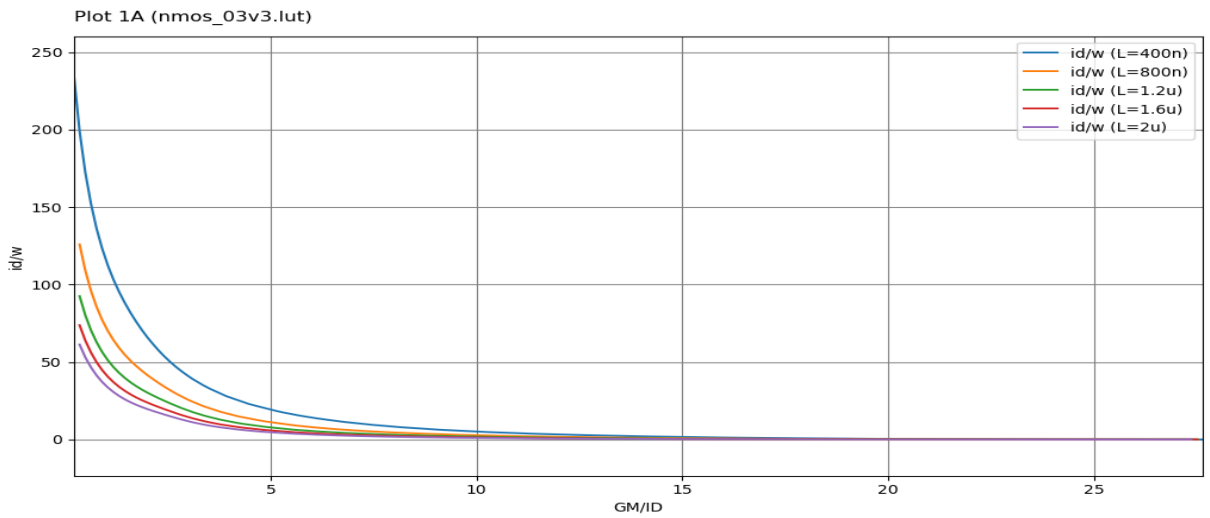


Figure 16:id/w

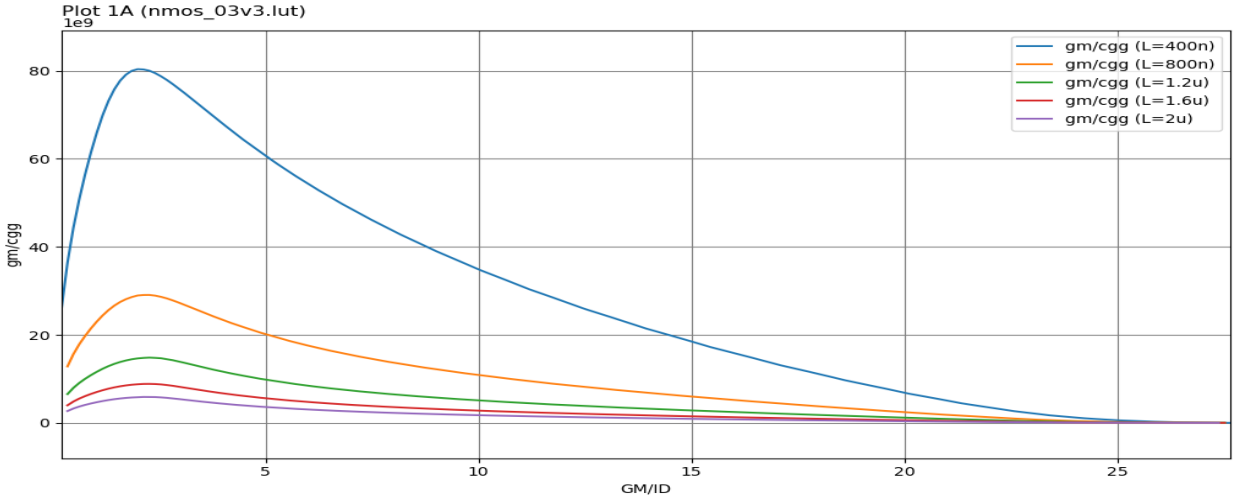


Figure 15:GM/CGG

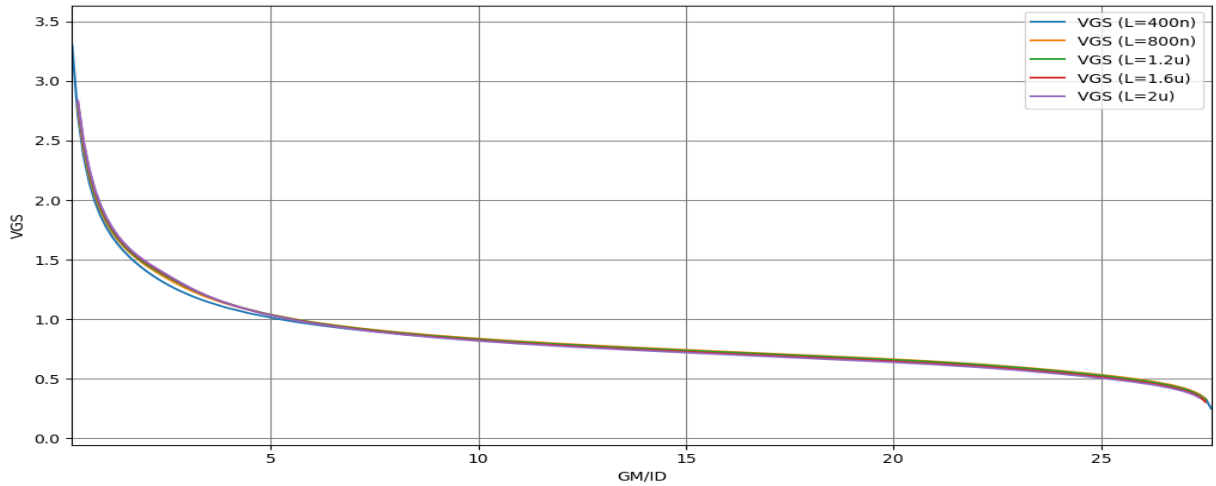


Figure 14:VGS

Part 2: OTA Design

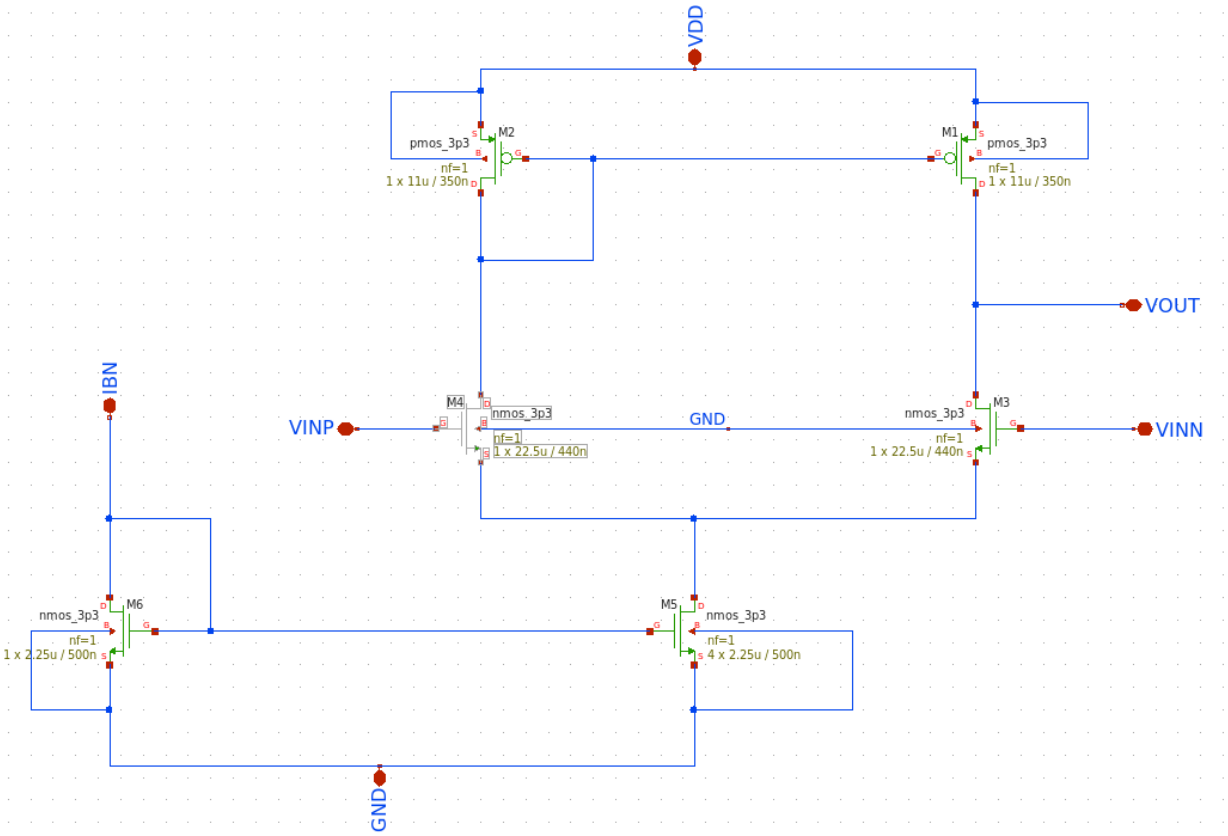


Figure 17:SCHEMATIC

- To maximize input common-mode range near VDD, an NMOS input pair was selected because NMOS transistors naturally allow operation closer to the positive supply rail than PMOS transistors

Design for input pair (NMOS):

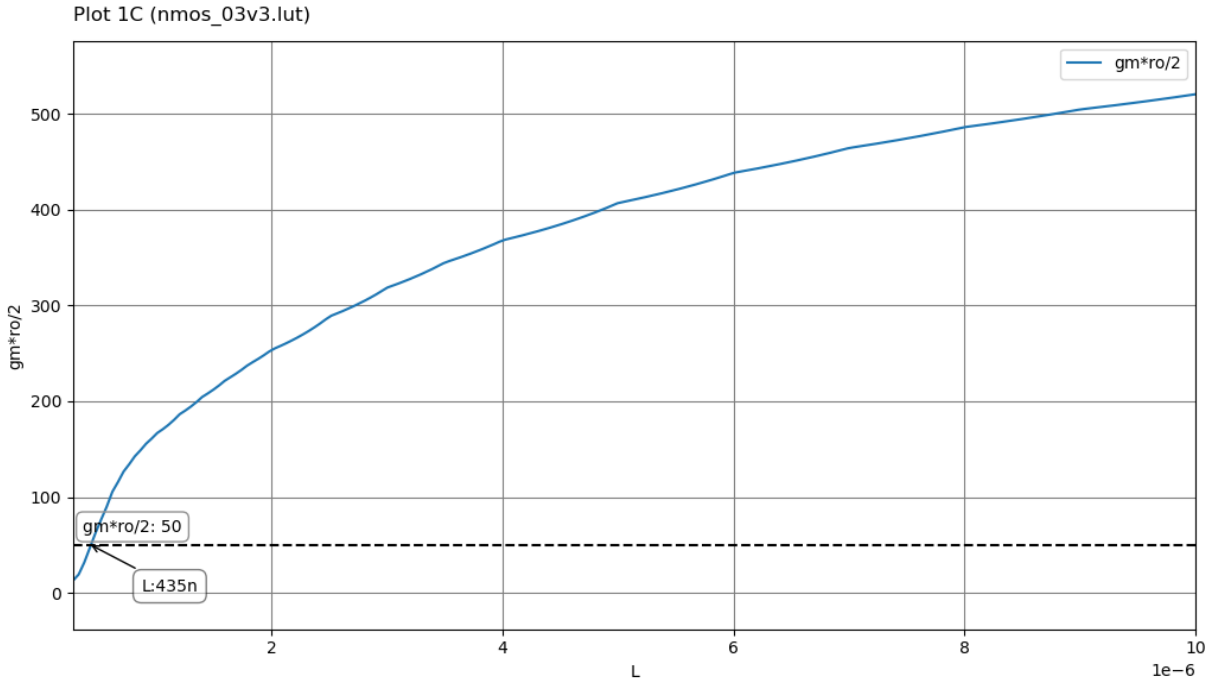
$|A_V| = gm_n \times (r_{on}//r_{op})$ assume $r_{on} = r_{op}$ → $|A_V| = 0.5 \times gm_n \times r_{on} >= 50$

GBW $= \frac{gm}{2\pi \times C_L} >= 10M$ → $gm >= 2\pi \times C_L \times 10M = 0.000314$

Assume current id=20u → $\frac{gm}{id} >= 5\pi >= 15.7$

And for some margin I will take $\frac{gm}{id} = 17$

Assuming vds on M4 and M2 =0.7 and on M5(tail) =0.4 to reduce body effect



I will choose L = 440n [M4, M3]

And from ADT I will get W

	Name	TT-27.0
4	W	22.51u
5	VGS	828.3m
6	VDS	700m
7	VSB	400m
8	gm/ID	16.85
9	Vstar	118.7m
10	fT	1.94G
11	gm/gds	104.3
12	VA	6.187

16	gm	337u
17	gmb	90.81u
18	gds	3.232u
19	ro	309.4k
20	Ron	35k
21	VTH	819.8m
22	VDSAT	92.63m
23	cgg	27.65f
24	cdd	15.76f

AS shown: W=22.5u [M4, M3]

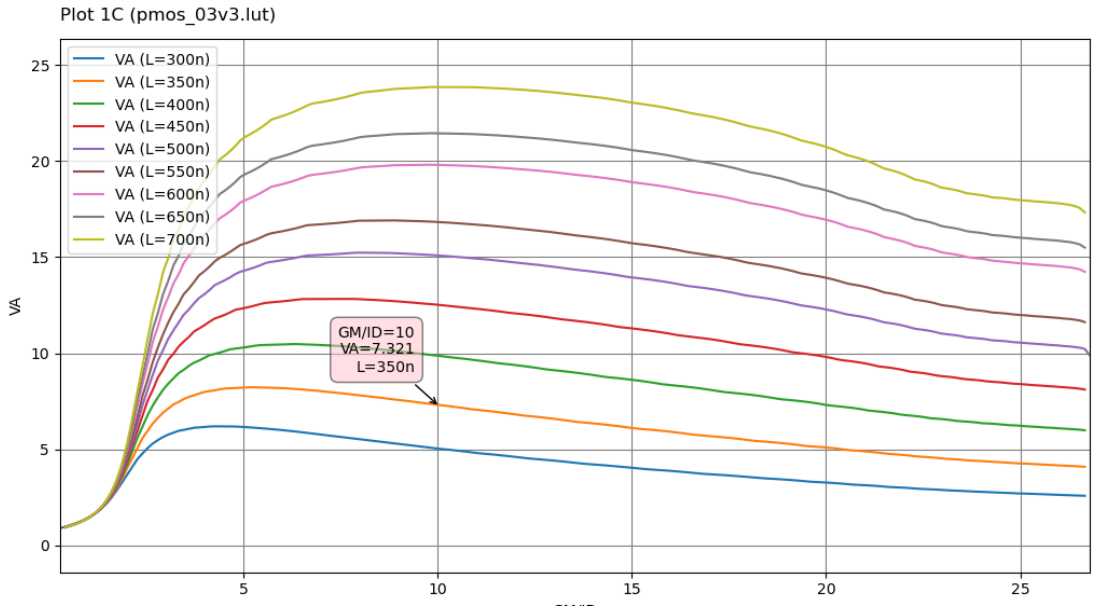
Vthn=0.8198 V

Design for load (PMOS):

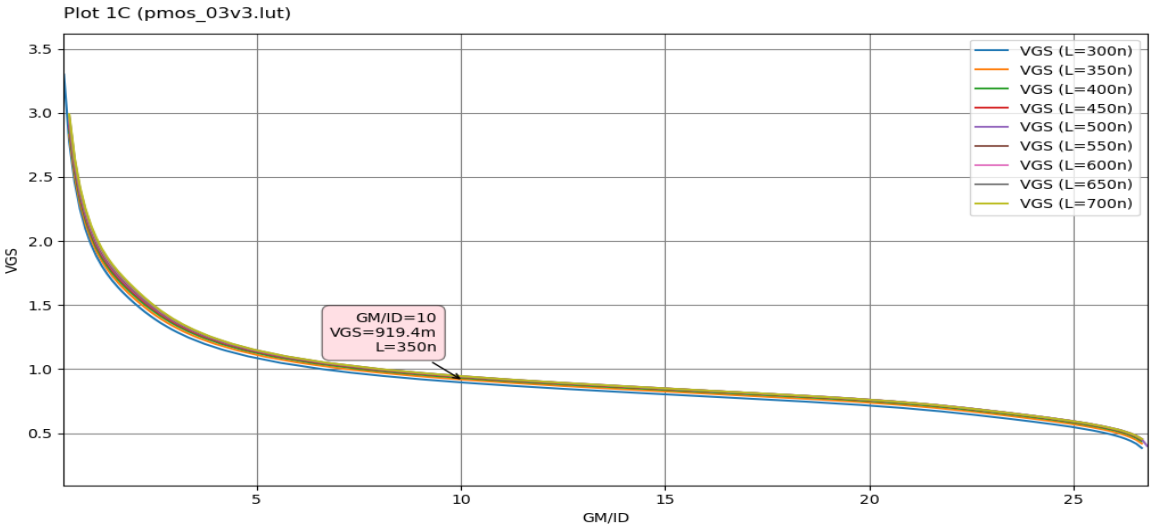
VICMmax < VDD – VSG +VTHn VSG<=1.1198 Assume $r_{op} = r_{on}$

$0.5 \times gm_n \times r_{op} >= 50$ $r_{op} = \frac{V_A}{I_D} >= \frac{50 \times 2}{gm_n}$ $V_A >= 5.93$

And assume gm/id=10



AS shown to satisfy $V_A >= 5.93$ I will take L =350n



Chosen L satisfy VSG<=1.1198

After putting values we got in SA we will find

	Name	TT-27.0
4	W	10.88u
5	VGS	920.5m
6	VDS	700m
7	VSB	0
8	gm/ID	9.912
9	Vstar	201.8m
10	fT	2.013G
11	gm/gds	72.67
12	VA	7.331

	Name	TT-27.0
13	ID/W	1.838
14	gm/W	18.22
15	AREA	3.808p
16	gm	198.2u
17	gmb	77.1u
18	gds	2.728u
19	ro	366.6k
20	Ron	35k
21	VTH	765.4m

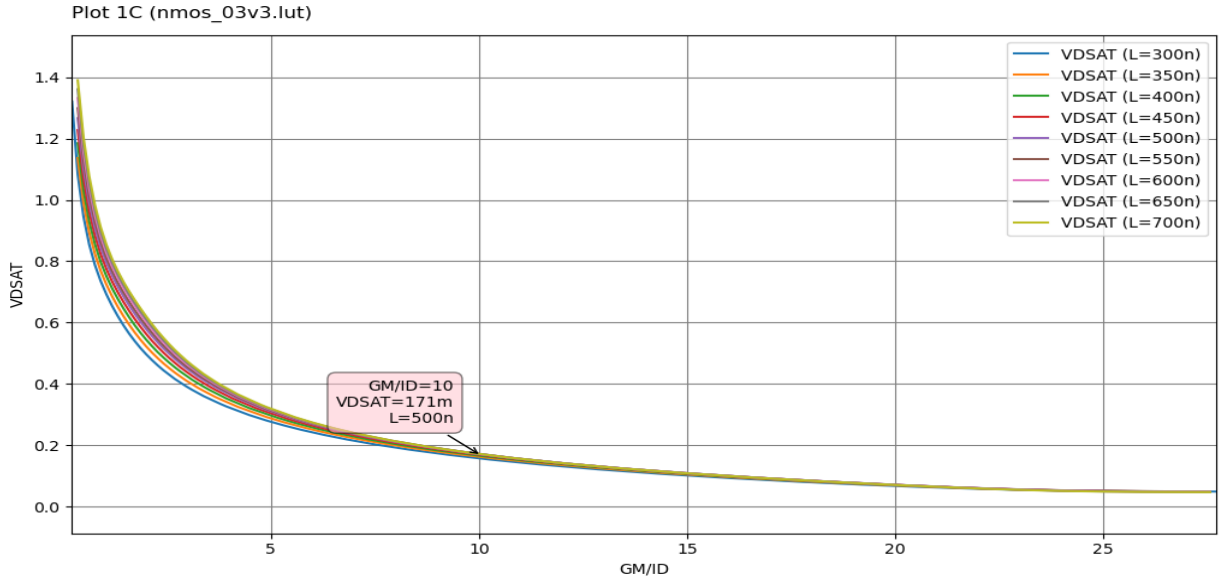
I choose W=11u

Design for the tail current source (NMOS):

VICMmin <= VGSn+VDsat → VDsat <= VICMmin- VGSn

VDsat <= 1-0.8283 → VDsat <=0.1717

Assume gm/id =10



I will choose L = 500n

From SA :

	Name	TT-27.0
13	ID/W	4.287
14	gm/W	42.58
15	AREA	4.665p
16	gm	397.3u
17	gmb	142.4u
18	gds	3.335u
19	ro	299.8k
20	Ron	17.5k
21	VTH	710m

	Name	TT-27.0
3	L	500n
4	W	9.33u
5	VGS	846.4m
6	VDS	700m
7	VSB	0
8	gm/ID	9.932
9	Vstar	201.4m
10	fT	4.048G
11	gm/gds	119.1

I WILL Choose W=9u

Parameter	Input pair **M3,M4**	Load **M2 ,M1**	tail current source **M5**	tail current source **M6**
W	22.5u	11u	9u	2.25u
L	440n	350n	500n	500n
GM	340uS	200uS	400uS	400uS
ID	20uA	20uA	40uA	10uA
GM/ID	17	10	10	10
V*	117.29 mV	193.5 mV	202.93 mV	203.834 mV
VDsat	91 mV	171.9 mV	175.5 mV	175.9 mV
Vov	8.112 mV	145.9 mV	142 mV	142 mV

After that I made new schematic because problem with X schem so you will find

M1, M2 input pair

M4, M6 LOAD

M3, M5 tail current source

Part 3: Open-Loop OTA Simulation

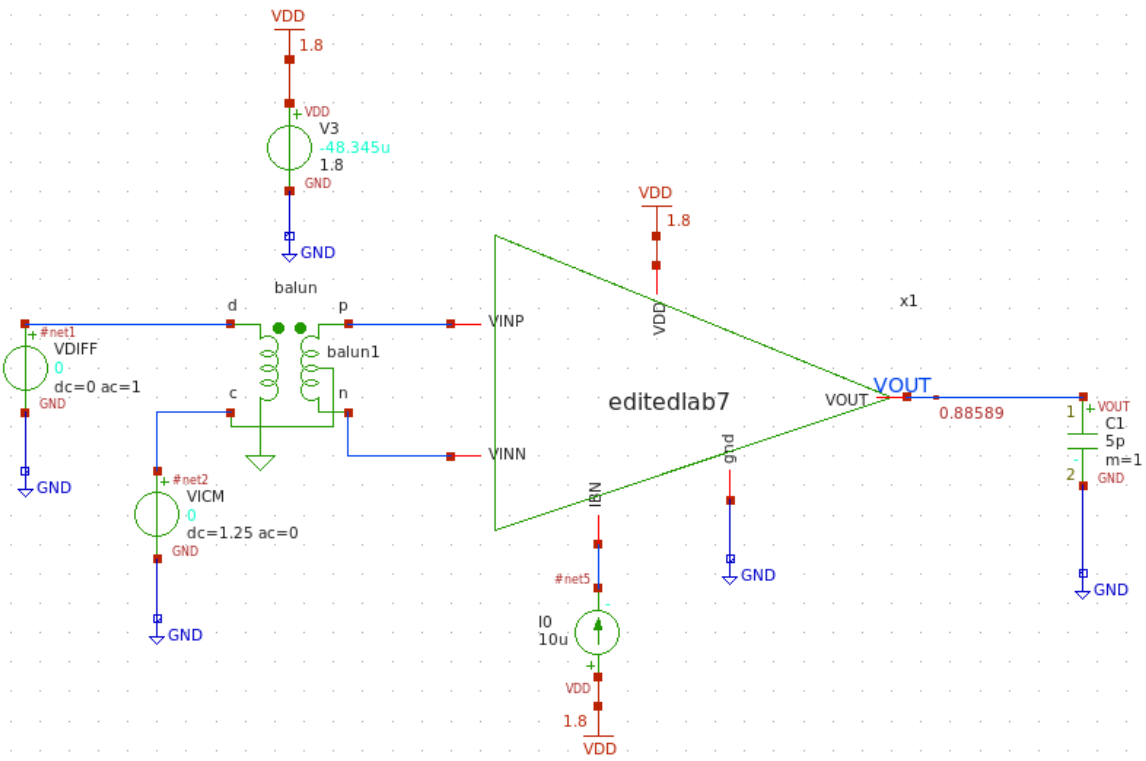
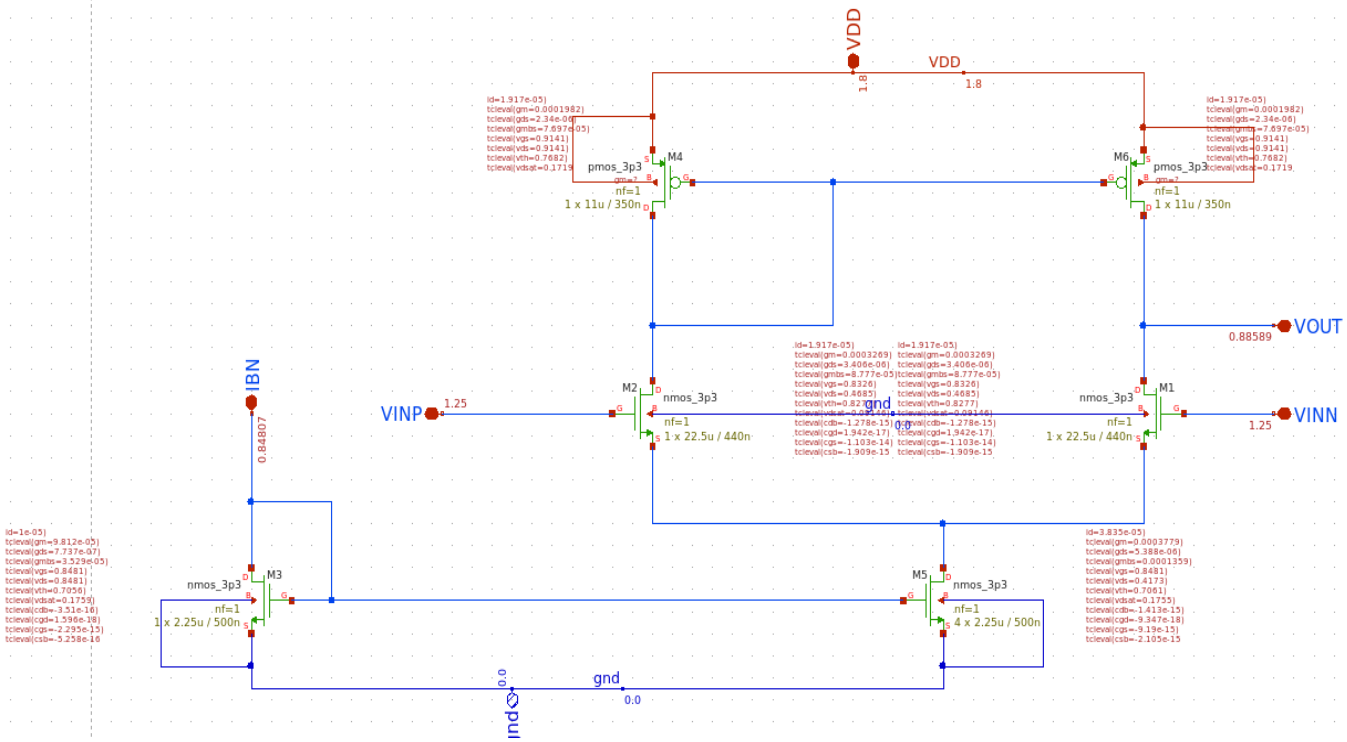


Figure 18:symbol

1) Schematic of the OTA with DC node voltages clearly annotated.



values from interactive:

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm6.m0           m.x1.xm4.m0           m.x1.xm3.m0
     model           pmos_3p3.12           pmos_3p3.12            nmos_3p3.8
        id           1.91726e-05           1.91726e-05                 1e-05
        gm           0.000198166           0.000198166           9.81192e-05
       gds           2.33988e-06           2.33988e-06           7.73674e-07
       vgs              0.914109              0.914109              0.848062
       vth              0.768215              0.768215              0.705603
       vds              0.914107              0.914107              0.848056
     vdsat              0.171919              0.171919              0.175871

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm5.m0           m.x1.xm2.m0           m.x1.xm1.m0
     model            nmos_3p3.8           nmos_3p3.12           nmos_3p3.12
        id           3.83452e-05           1.91726e-05           1.91726e-05
        gm           0.000377915           0.000326933           0.000326933
       gds           5.38805e-06           3.40636e-06           3.40636e-06
       vgs              0.848062              0.832643              0.832643
       vth              0.706113              0.827703              0.827703
       vds              0.417345              0.468531              0.468531
     vdsat              0.175497             0.0914581             0.0914581
```

Is the current (and gm) in the input pair **exactly** equal?

Yes — the currents (and therefore **gm**) in the input pair are exactly equal, since there's no mismatch. the two transistors in the input pair have the same VGS,VDS, and identical W/L

What is DC voltage at VOUT? Why?

0.88589, there's no mismatch and VOUT= 1.8-vgsp=1.8-0.914109 =0.88589

2)Diff small signal ccs:

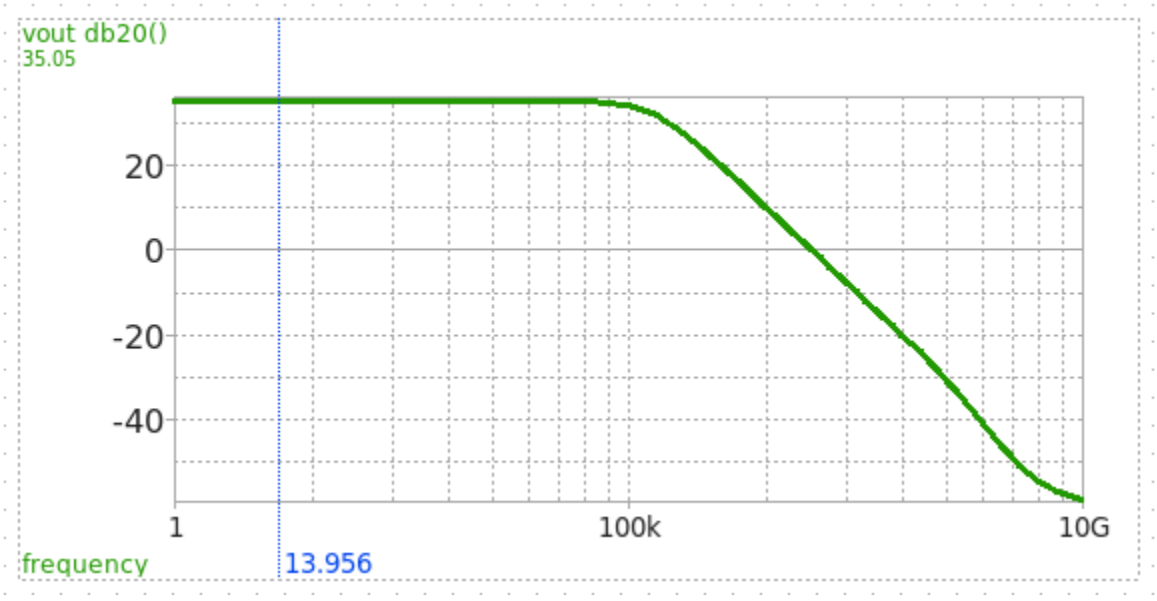


Figure 19:DIFF GAIN VS FREQ (IN db)

From simulation:

```
gain                =  5.656023e+01 at=  1.000000e+00
bw                  =  1.807540e+05
GBW = 1.02235E+07
```

Hand analysis:

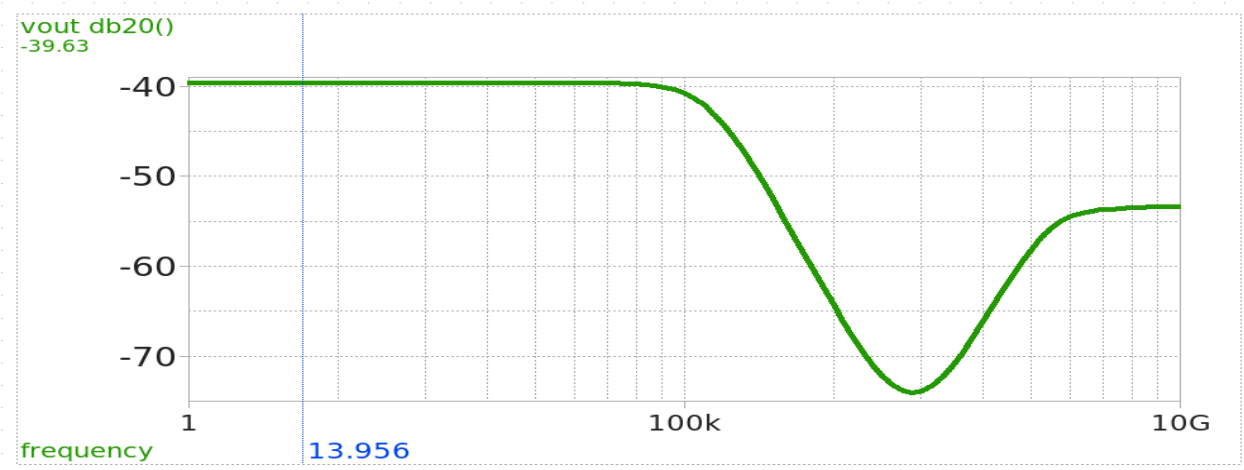
$|A_{Vdiff}| = gm_n \times (r_{on}//r_{op}) = 56.89 = 35.1$ db

$BW = \frac{1}{2\pi \times C_L \times (r_{on}//r_{op})} = 182.909\ KHZ$

$GBW = \frac{gm}{2\pi \times C_L} = 10.4\ MHZ > 10MHZ$

	GAIN	BW	GBW
FROM SIMULATION	35.05 db	180.754 KHZ	10.22 MHZ
FROM HAND ANALYSIS	35.1 db	182.909 *KHZ*	10.4 *MHZ*

3)CM small signal ccs:



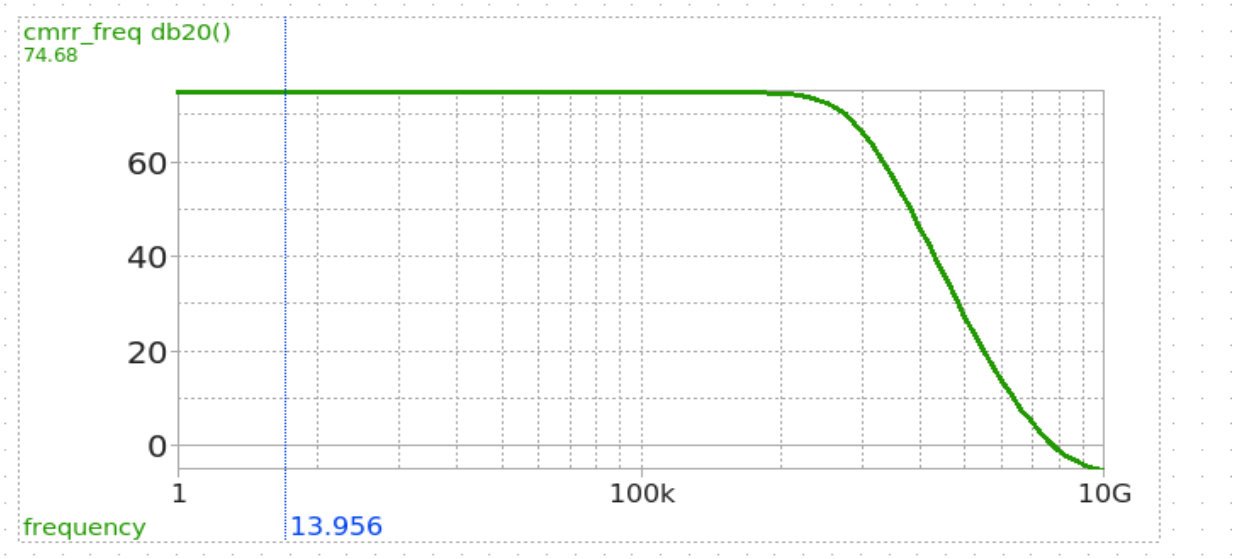

```
cmgain                =   1.043745e-02 at=   1.000000e+00
```

HAND analysis:

$$|A_{Vcm}| = \frac{1}{2 \times g_{mp} \times r_{o\ tail}} = 0.01359 = -37.33\ dB$$

	simulation	Hand analysis
$\lvert A_{Vcm} \rvert$	**-39.63 db**	**-37.33 db**

4)CMRR:



Hand analysis:

CMRR (db)= AVD(db)-AVCM(db) =72.43 db

	simulation	Hand analysis
CMRR	**74.68 db**	**72.43 db**

5)Diff large signal ccs:

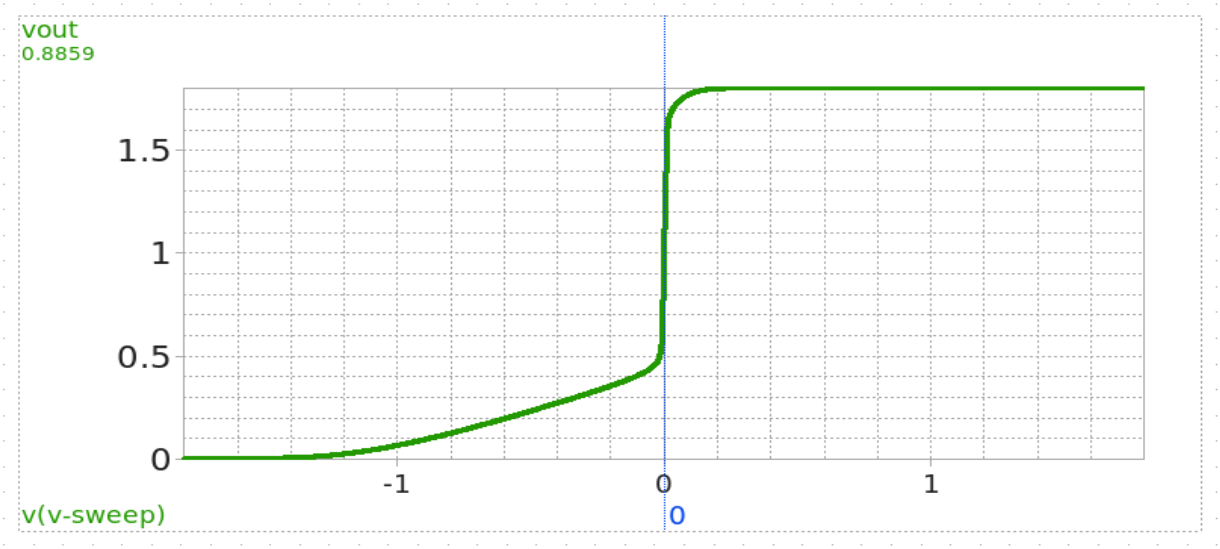
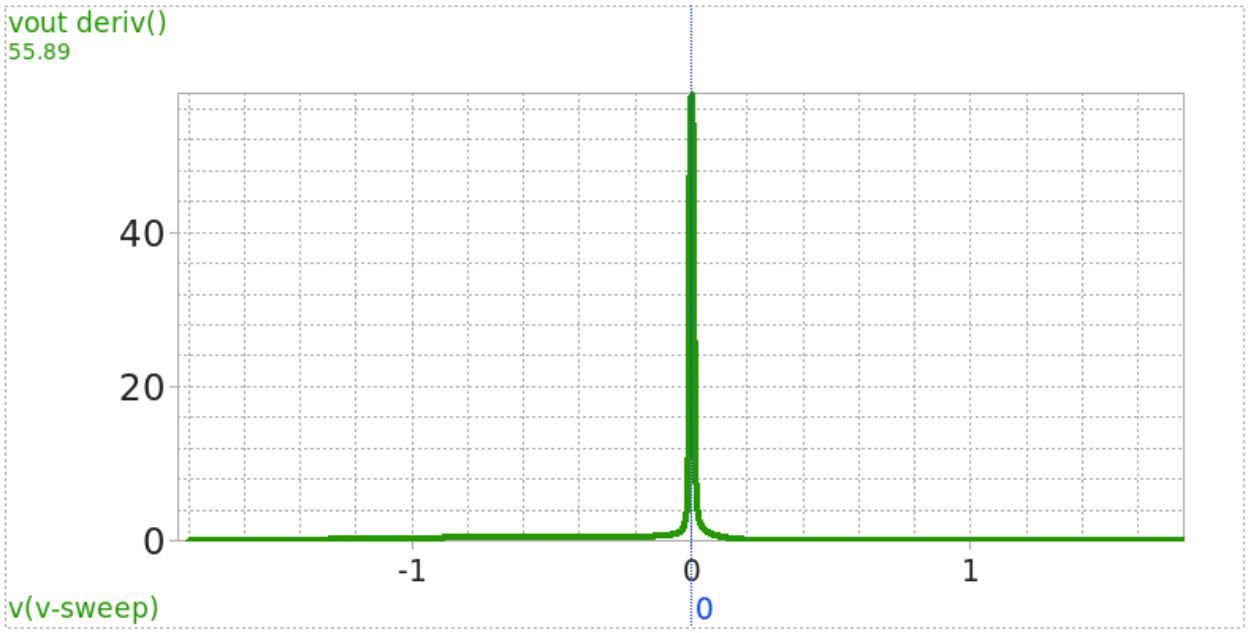


Figure 20: VOUT VS VID

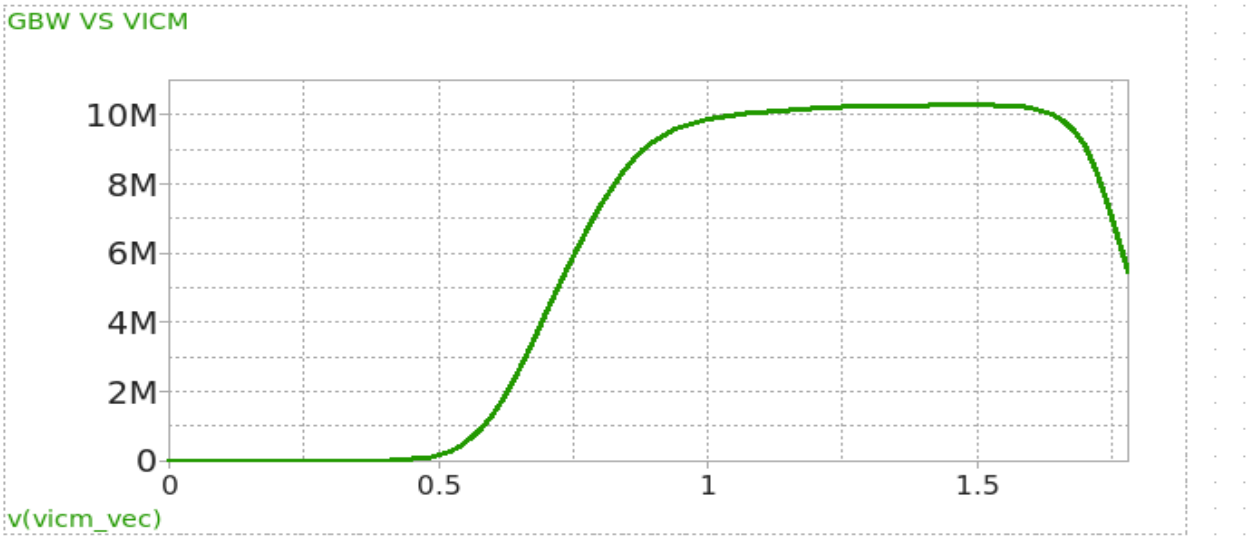
At VID=0, Vout=0.8859 V because:

The diode-connected PMOS load sets Vout=VDD−VGS,p with VDD=1.8Vand VGS,p≈0.9141V, the output settles to 0.8859V (DC bias point). Confirms no systematic offset (balanced input pair and current mirror) and VID = 0, the output simply settles to the OTA's internal bias (diode/mirror node) voltage set by the bias network and device sizing



Peak = 55.89 V which almost = Avd

6) CM large signal ccs (GBW vs VICM):

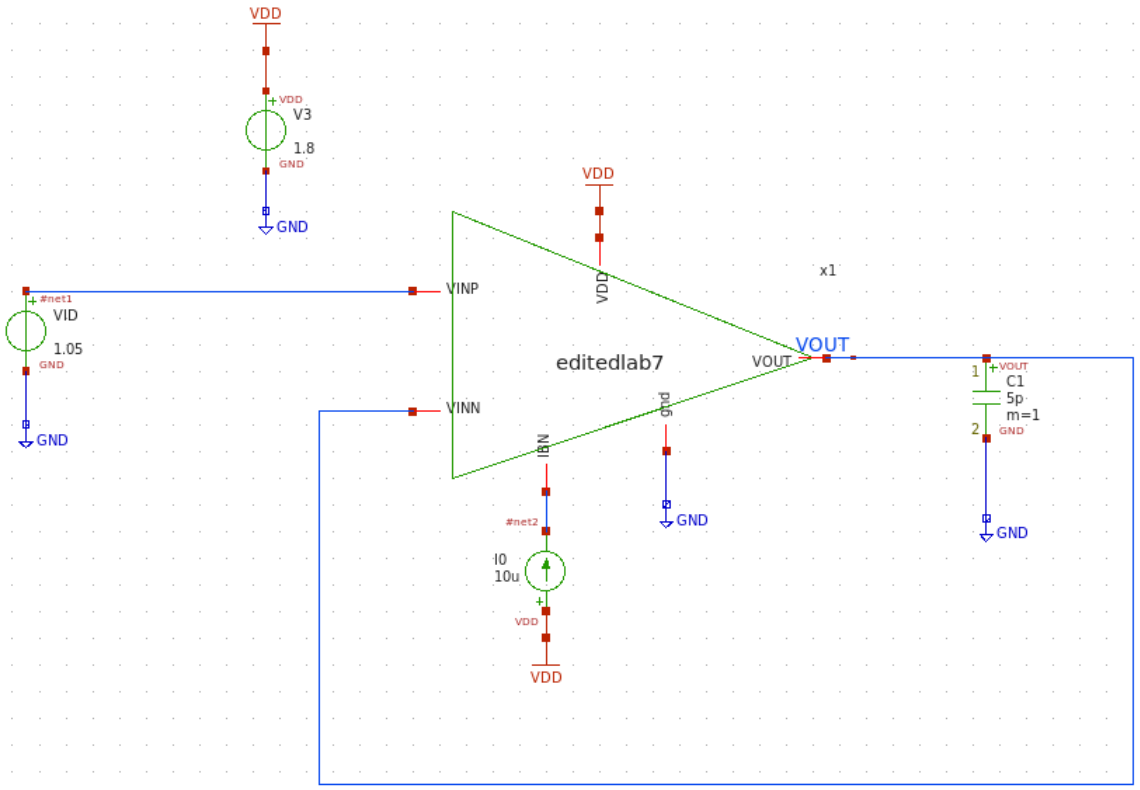


Values from interaction :

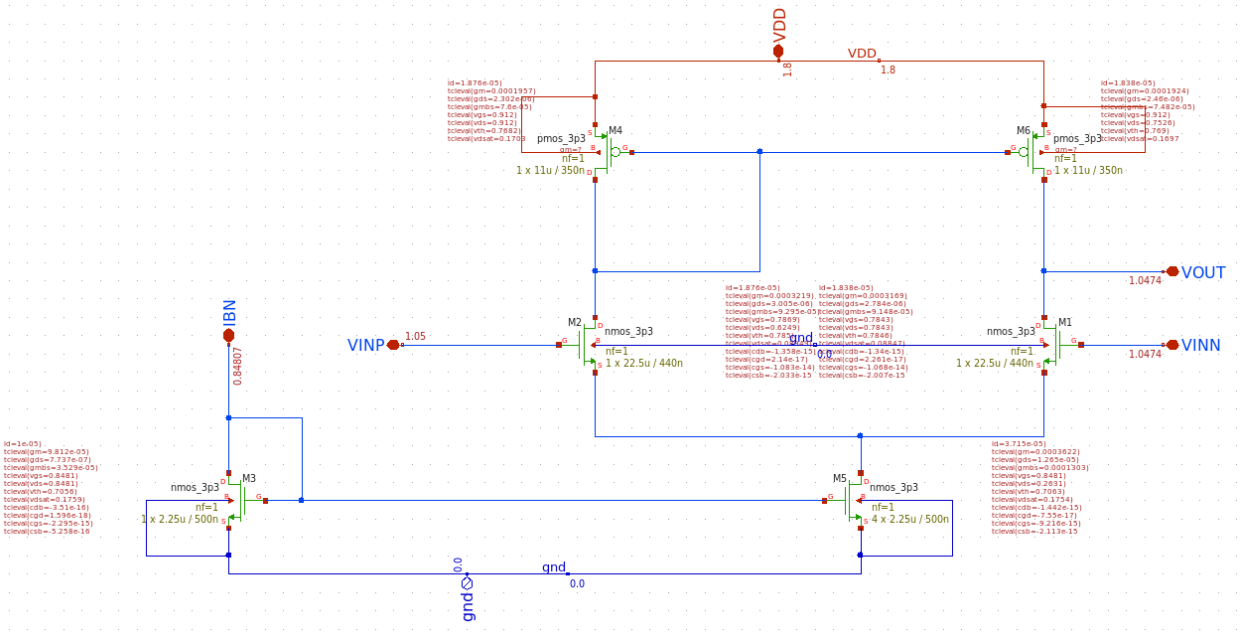
```
gain                =  1.293584e+00 at=  1.000000e+00
bw                  =  4.240433e+06
max_gbw             =  1.031222e+07 at=  2.511886e+07
min_vincm           =  9.044883e-01
max_vincm           =  1.692378e+00
min_vincm = 9.044883e-01
max_vincm = 1.692378e+00
cmir = 7.878897e-01
```

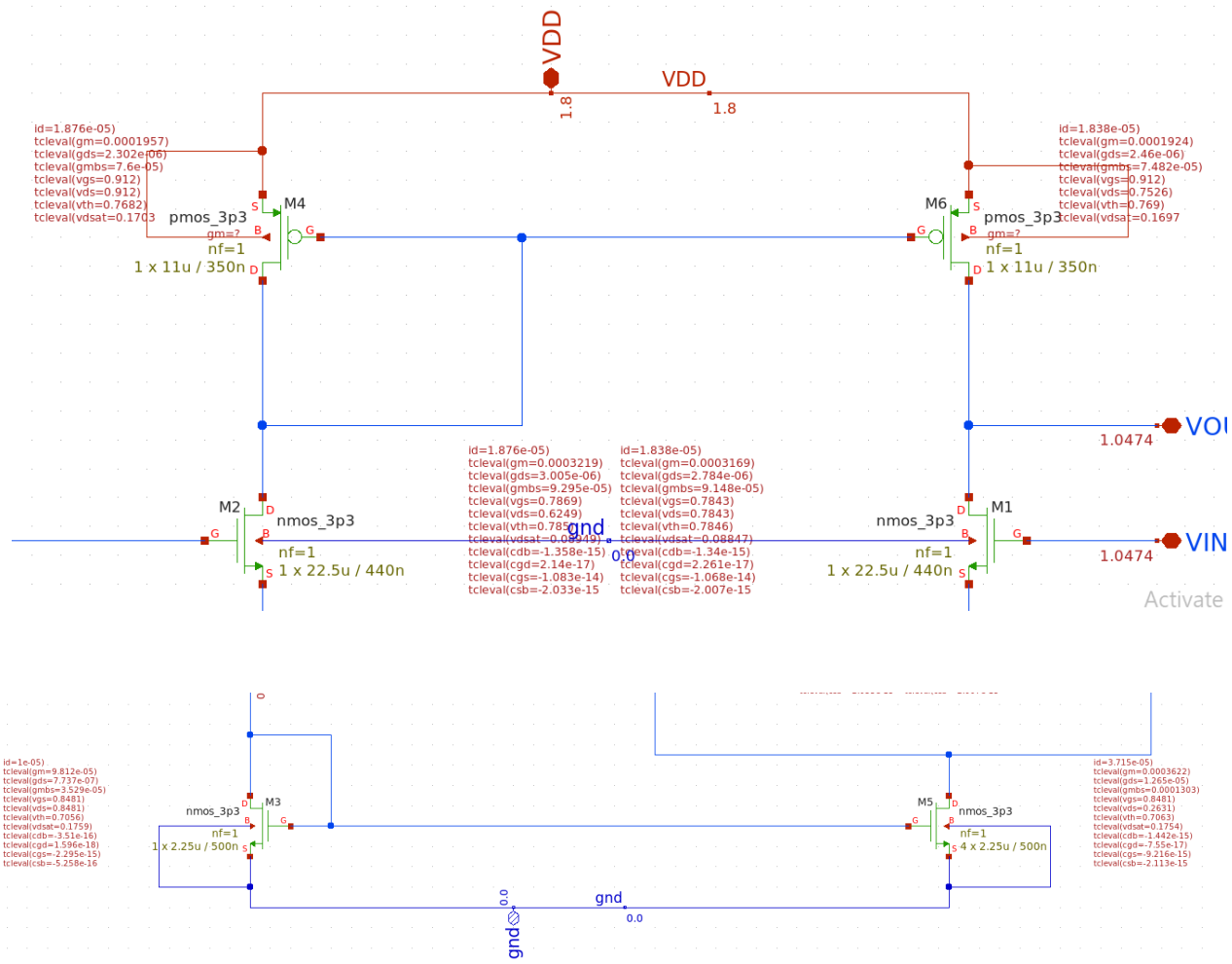
0.904 < VICM < 1.69 Which achieves our specs in the first

PART 4: Closed-Loop OTA Simulation:



1) Schematic of the OTA with DC OP point clearly annotated in unity gain buffer configuration





values from interactive :

device	m.x1.xm6.m0	m.x1.xm4.m0	m.x1.xm3.m0
model	pmos_3p3.12	pmos_3p3.12	nmos_3p3.8
id	1.83831e-05	1.87619e-05	1e-05
gm	0.000192435	0.000195683	9.81192e-05
gds	2.46028e-06	2.3015e-06	7.73674e-07
gmbs	7.48246e-05	7.59959e-05	3.52911e-05
vgs	0.912048	0.912048	0.848062
vth	0.769037	0.768225	0.705603
vds	0.752622	0.912046	0.848056

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm5.m0	m.x1.xm2.m0	m.x1.xm1.m0
model	nmos_3p3.8	nmos_3p3.12	nmos_3p3.12
id	3.71451e-05	1.87619e-05	1.83831e-05
gm	0.000362193	0.000321936	0.000316894
gds	1.2655e-05	3.00486e-06	2.78364e-06
gmbs	0.000130348	9.29508e-05	9.14755e-05
vgs	0.848062	0.786906	0.78428
vth	0.706296	0.785008	0.78455
vds	0.263082	0.624855	0.784279

Is the current (and gm) in the input pair exactly equal[1]? Why?

No — in closed-loop operation, a small differential input voltage is required due to the OTA's finite gain, which creates an effective mismatch between the two input transistors. This mismatch causes their drain currents — and therefore their gm — to be slightly different.

Calculate the mismatch in I_D and gm.

The mismatch in input pair M1,M2 and after getting values from interactive will be :

1. Input Pair (M1 vs M2)

Transconductance (gm)

- $gm_{\text{M1}} = 316.894\,\mu S$
- $gm_{\text{M2}} = 321.936\,\mu S$
- $gm_{\text{no mismatch}} = \text{Average}(326.933, 326.933) = 326.933\,\mu S$

$$\text{gm Mismatch} = \frac{316.894 - 321.936}{326.933} \times 100 = \boxed{-1.54\%}$$

Current (ID)

- $ID_{\text{M1}} = 18.3831\,\mu A$
- $ID_{\text{M2}} = 18.7619\,\mu A$
- $ID_{\text{no mismatch}} = \text{Average}(19.1726, 19.1726) = 19.1726\,\mu A$

$$\text{ID Mismatch} = \frac{18.3831 - 18.7619}{19.1726} \times 100 = \boxed{-1.98\%}$$

2. Current Mirror Load (M4 vs M6)

Transconductance (gm)

- $gm_{\text{M4}} = 195.683\,\mu S$
- $gm_{\text{M6}} = 192.435\,\mu S$
- $gm_{\text{no mismatch}} = \text{Average}(198.166, 198.166) = 198.166\,\mu S$

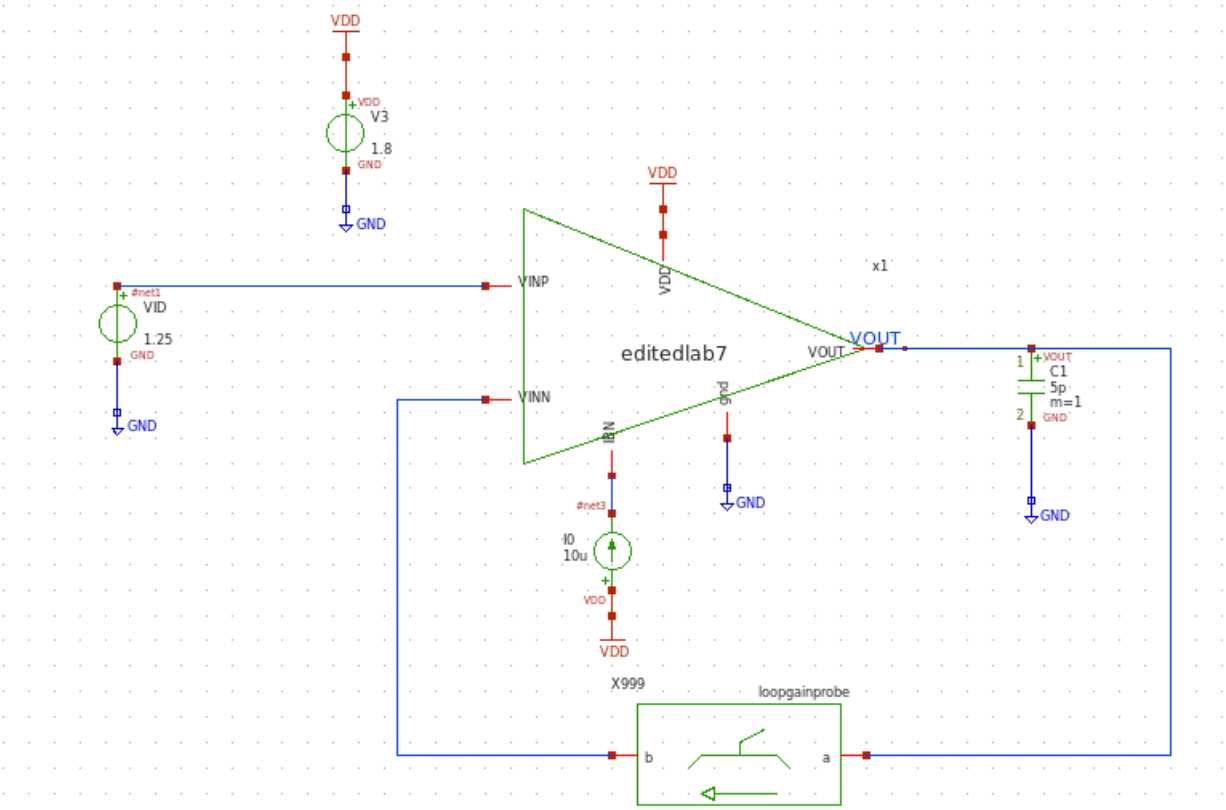
$$\text{gm Mismatch} = \frac{195.683 - 192.435}{198.166} \times 100 = \boxed{1.64\%}$$

Current (ID)

- $ID_{\text{M4}} = 18.7619\,\mu A$
- $ID_{\text{M6}} = 18.3831\,\mu A$
- $ID_{\text{no mismatch}} = \text{Average}(19.1726, 19.1726) = 19.1726\,\mu A$

$$\text{ID Mismatch} = \frac{18.7619 - 18.3831}{19.1726} \times 100 = \boxed{1.98\%}$$

2)Loop gain



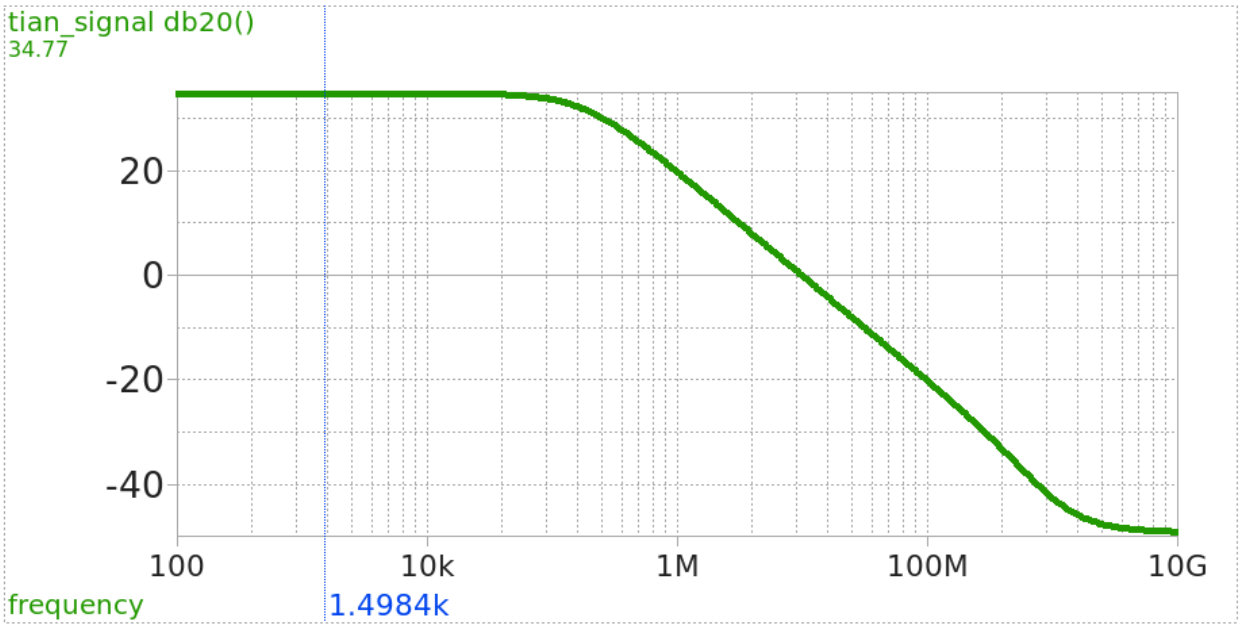


Figure 21:GAIN VS FREQ (in db)

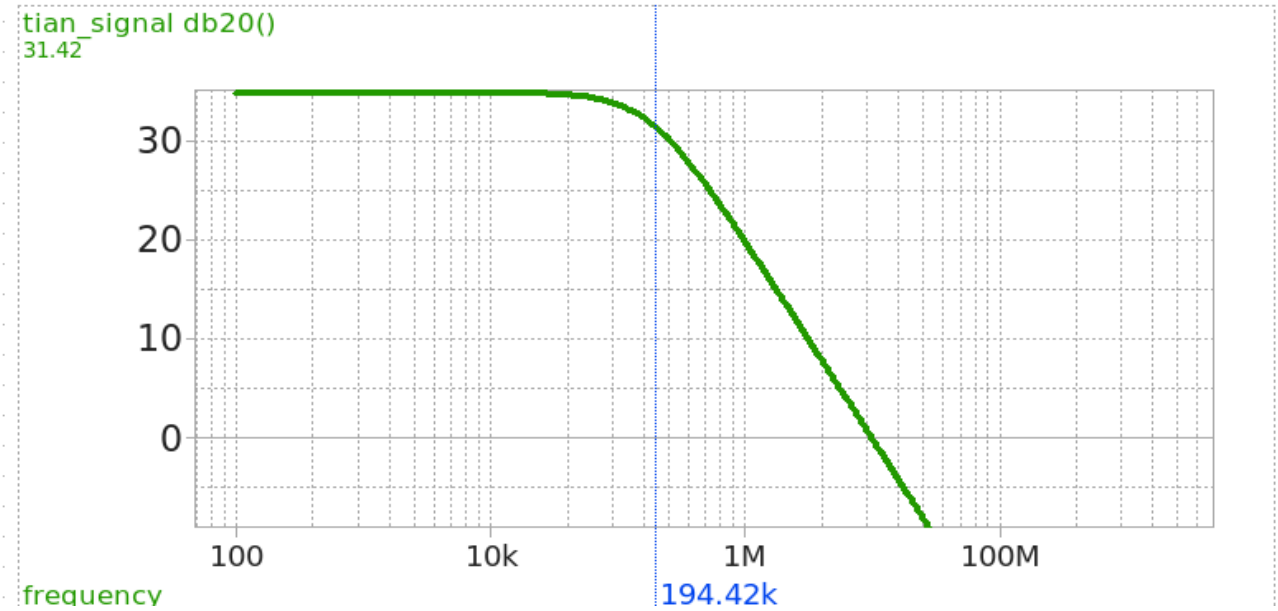


Figure 22:gain (-3db) vs freq

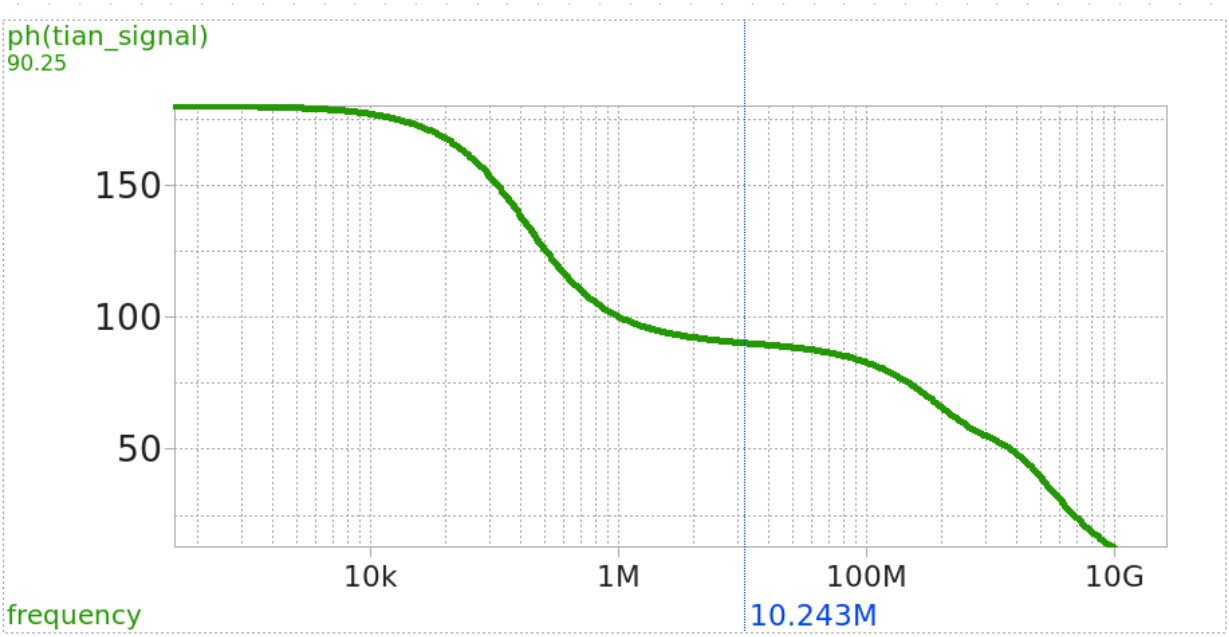


Figure 23:phase vs freq

From interactive :

```
gain_crossover_freq =   9.881904e+06
phaseatzerogain     =   9.031480e+01
pm = 8.968520e+01
```

(For closed loop):

From simulation

$|A_V| = \frac{A_{open\ loop}}{1+LG} = \frac{56.56}{1+54.76} = 1.01$

BW = $BW_{open\ loop} \times (1 + LG) = 194.42\ K \times (1 + 54.76) = 10.84\ MHZ$

GBW = 10.95 MHZ

Hand analysis:

$|A_V| = \frac{A_{open\ loop}}{1+LG} = \frac{56.89}{1+56.89} = 0.98$

BW = $BW_{open\ loop} \times (1 + LG) = 194.42\ K \times (1 + 56.89) = 10.588\ MHZ$

GBW = 10.378 MHZ

	GAIN	BW	GBW	GAIN	BW	GBW
	CLOSED LOOP			OPEN LOOP		
FROM SIMULATION	1.01	10.84 MHZ	10.95 MHZ	56.56	194.42 KHZ	10.22 MHZ
FROM HAND ANALYSIS	0.98	10.588 MHZ	10.378 MHZ	56.89	182.909 KHZ	10.4 MHZ

Comment

With = 1, the loop gain is equal to the open-loop gain. According to feedback theory, closing the loop reduces the closed loop gain by a factor of 1+LG while increasing the bandwidth by the same factor. This trade-off keeps the gain–bandwidth product nearly constant. Since β = 1, the measured loop gain and bandwidth changes directly match the open-loop values, confirming that the GBW remains essentially the same in both cases.

	Specs	Achieved specs	
Open loop DC voltage gain	>= 34dB	35.05 dB	✓
CMRR @ DC[1]	>= 74dB	74.68 dB	✓
Phase margin	>= 70^{o}	90.31 ^{o}	✓
CM input range – low	<= 1V	0.904 V	✓
CM input range – high	>=1.5V	1.69 V	✓
GBW	>= 10MHz	10.22 MHZ	✓