Analog IC Design – (Xschem ,Ngspice,ADT)
Lab 02
Common Source Amplifier

PART 1: Sizing Chart:

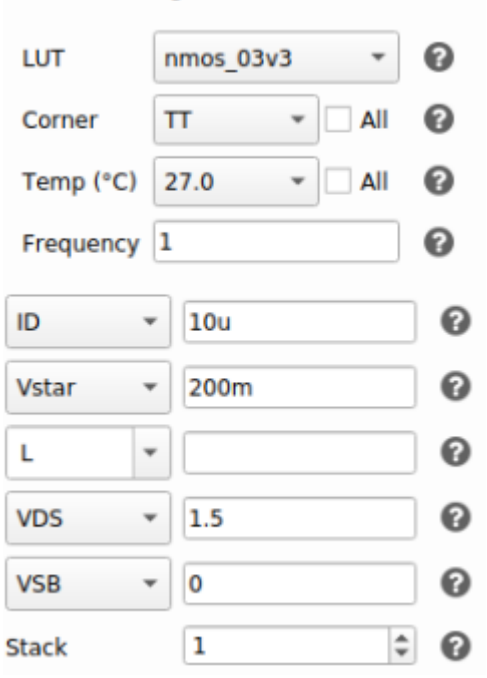
spec	Value
DC Gain	-10
Supply	$2.5V$
Current consumption	$10\ \mu A$

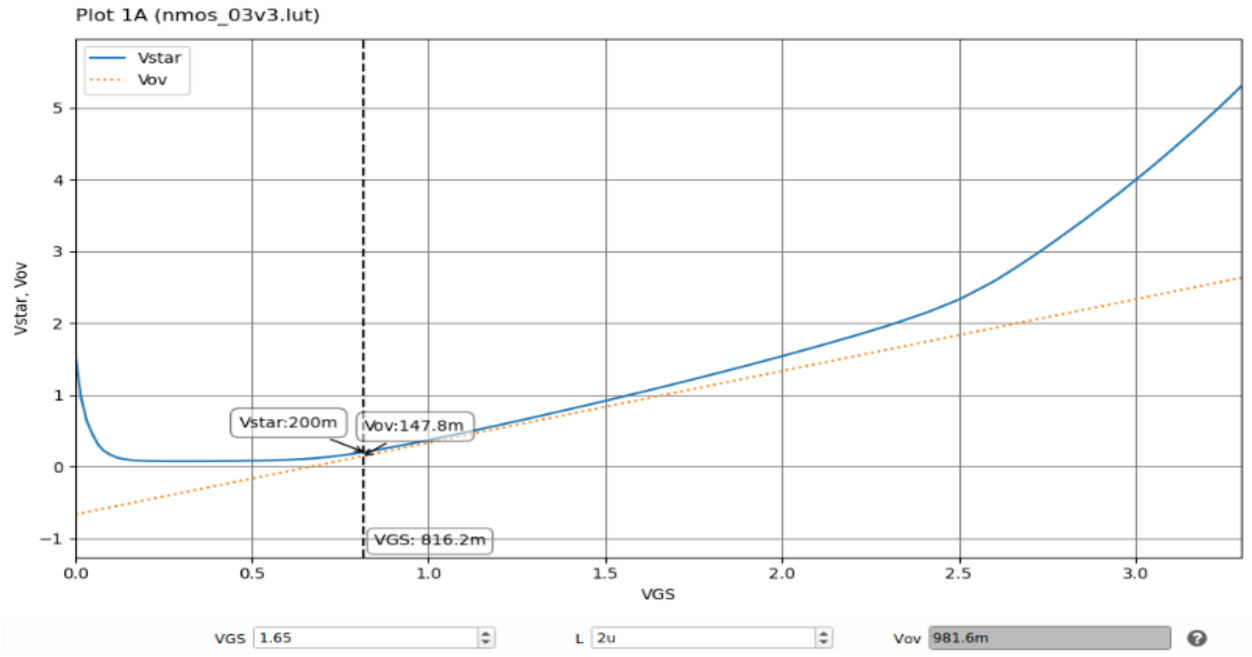
$$R_D = \frac{V_{RD}}{I_D} = 100\ K\Omega \quad , \quad V^* = 200Mv$$

From ADT:

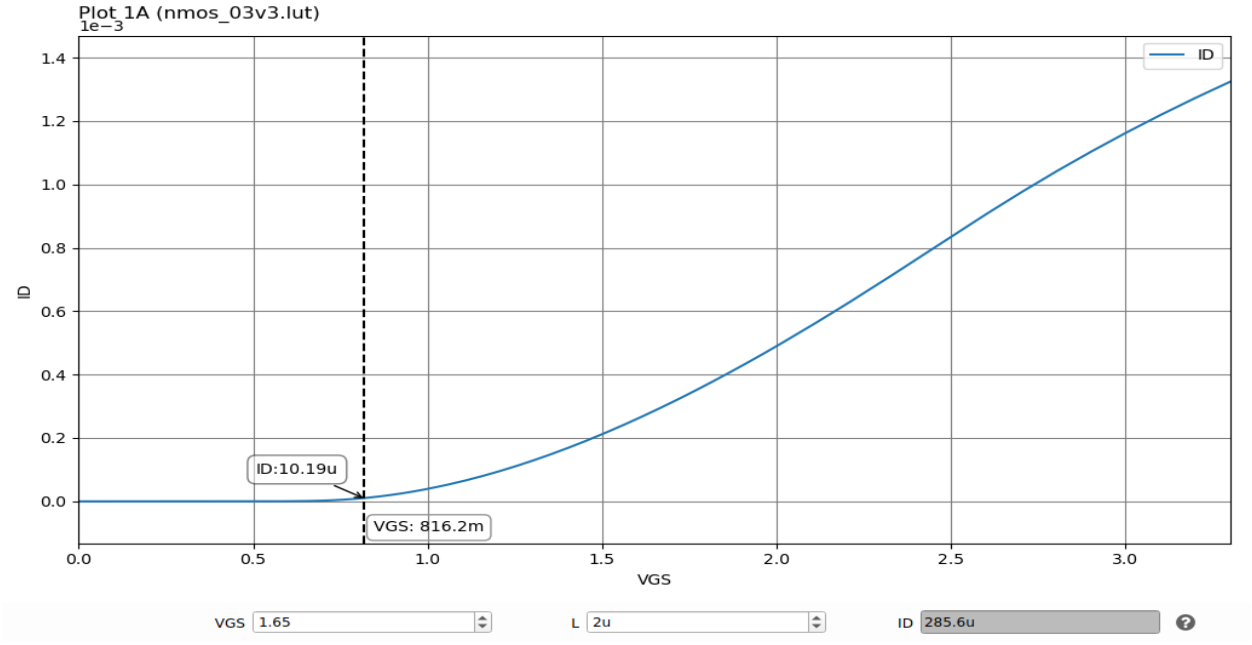
	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	2u
4	W	9.76u
5	VGS	818.1m
6	VDS	1.5
7	VSB	0
8	gm/ID	9.917
9	Vstar	201.7m
10	fT	282MEG
11	gm/gds	561.2

	Name	TT-27.0
12	VA	56.59
13	ID/W	1.025
14	gm/W	10.16
15	AREA	19.52p
16	gm	99.17u
17	gmb	38.82u
18	gds	176.7n
19	ro	5.659MEG
20	Ron	150k
21	VTH	668.4m
22	VDSAT	158.5m

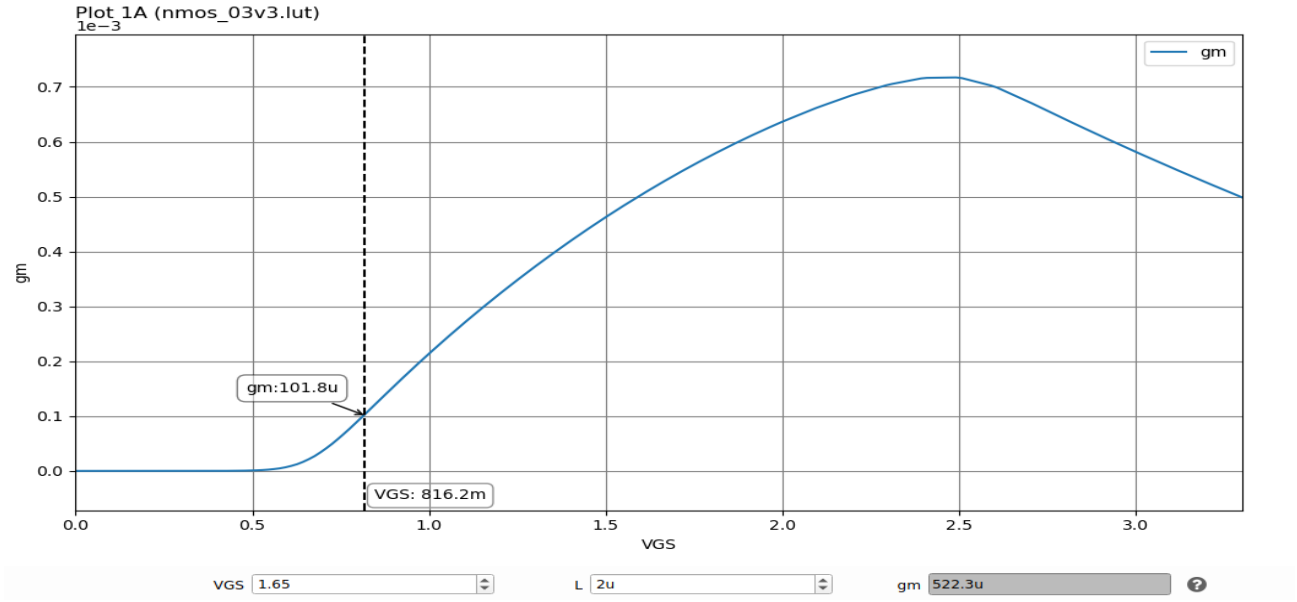




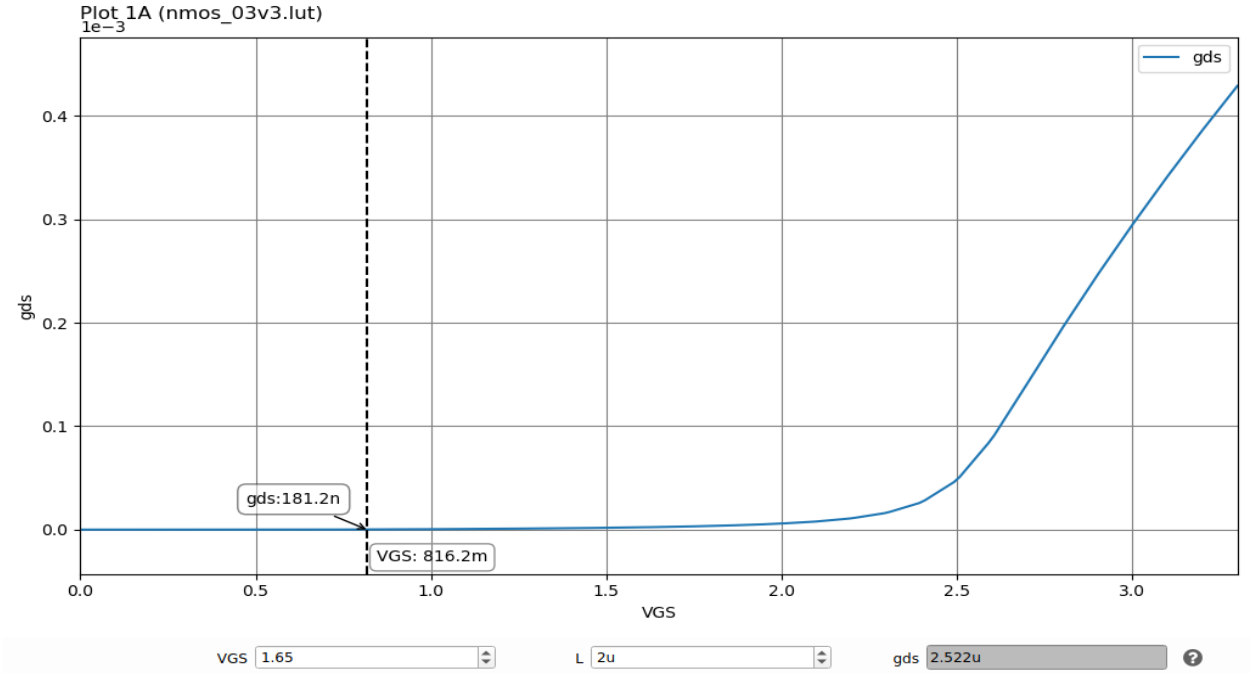
Vov and V VS Vgs*



Id VS Vgs



gm VS Vgs



gds VS Vgs

From graphs the required value will be:

1-

V*	**200**mV
IDx	**10.19 u**
R_D	**100** KΩ
V_{ovQ}	147.8 mV
V_{GSQ}	816.2 mV
g_{mx}	101.8 uS
g_{dsx}	181.2 nS
Vth	**668.4 mV**

2-

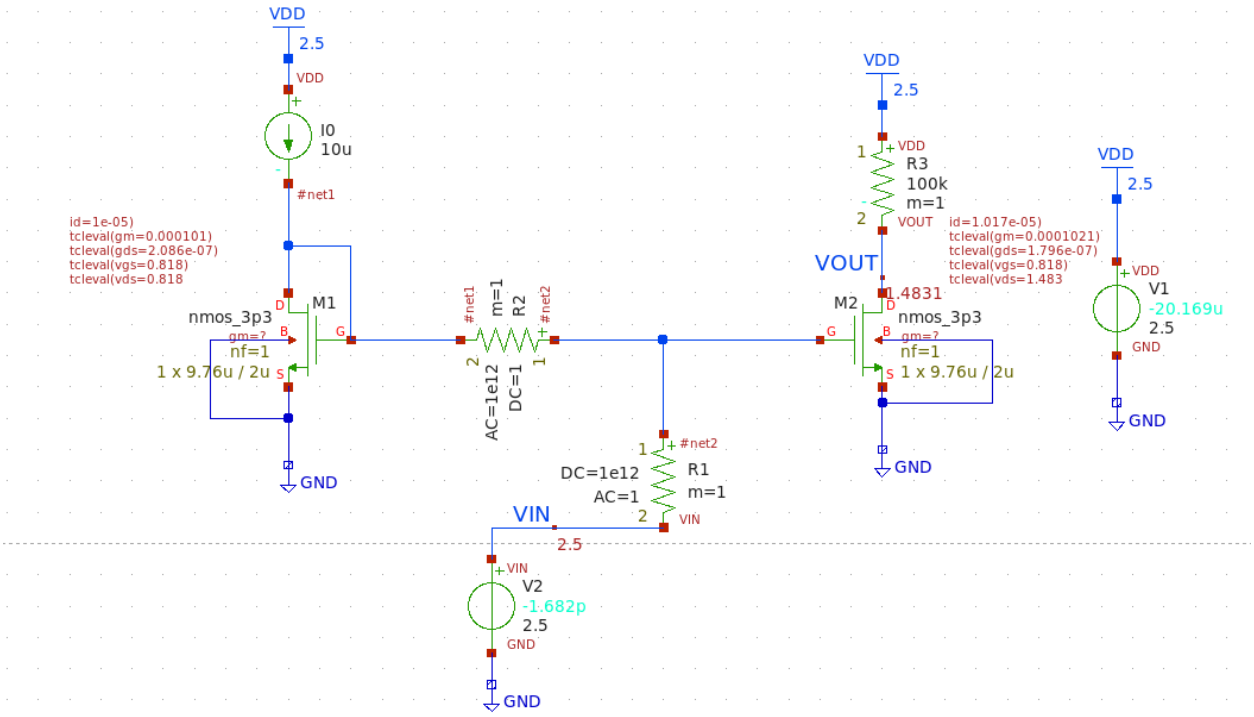
W	Id
10 μm	10.2μA
9.76 μm	10 μA

3-. Compare the results from ADT to the values you calculated in a table.

parameter	ADT	Cross multiplication
Id	10 uA	10.19μA
W	9.76 um	**10** μm
V_{GS}	818.1mV	816.2 mV
g_m	99.17 uS	101.8 uS
g_{ds}	176.7 nS	181.2 nS
r_o	5.659 MΩ	5.519 MΩ
$gain\ with\ ro$	-9.745	-9.9988
$gain\ without\ ro$	-9.917	-10.18

PART 2: CS Amplifier:

1.op Analysis



Schematic

DC OP:

	Values from simulation	Values from part 1
id	10.17 μA	10.19 μA
gm	102.1 μS	101.8 uS
gds	179.6 nS	181.2 nS
ro	5.568 MΩ	5.519 MΩ

Comparison of r_o and RD:

In this case and from shown table, the output resistance r_o is much larger than the drain resistance RD. Since $r_o \gg RD$, its effect on the overall gain is minimal. Therefore, ignoring r_o in the simulation is a valid approximation and does not introduce significant error.

However, if we were to use a minimum-length channel (L = Lmin), the short-channel effects become more pronounced, and r_o decreases significantly. As a result, ignoring r_o in that case could lead to noticeable error in gain calculations. So, the error would not remain the same when using minimum-length devices.

Analytical Calculation of Gain:

| Intrinsic gain| =gm*ro= 568.49 – – – – – – – – – | analytic gain| =gm*Rd=10.21

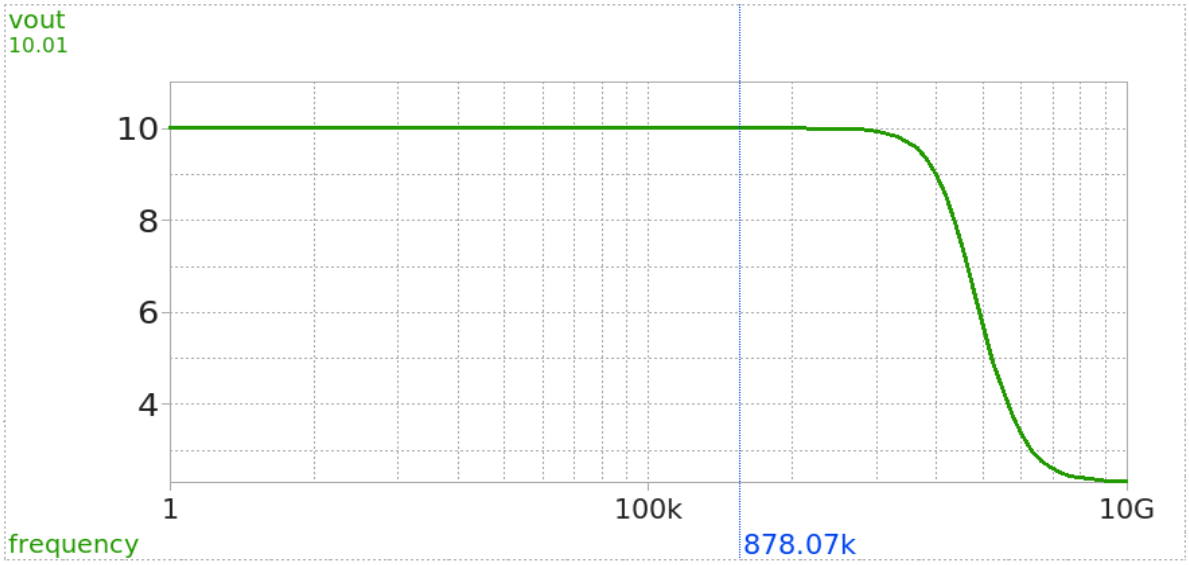
After calculating the analytical gain, we find that it is **much smaller than the intrinsic gain** of the transistor.

This means the relationship is:

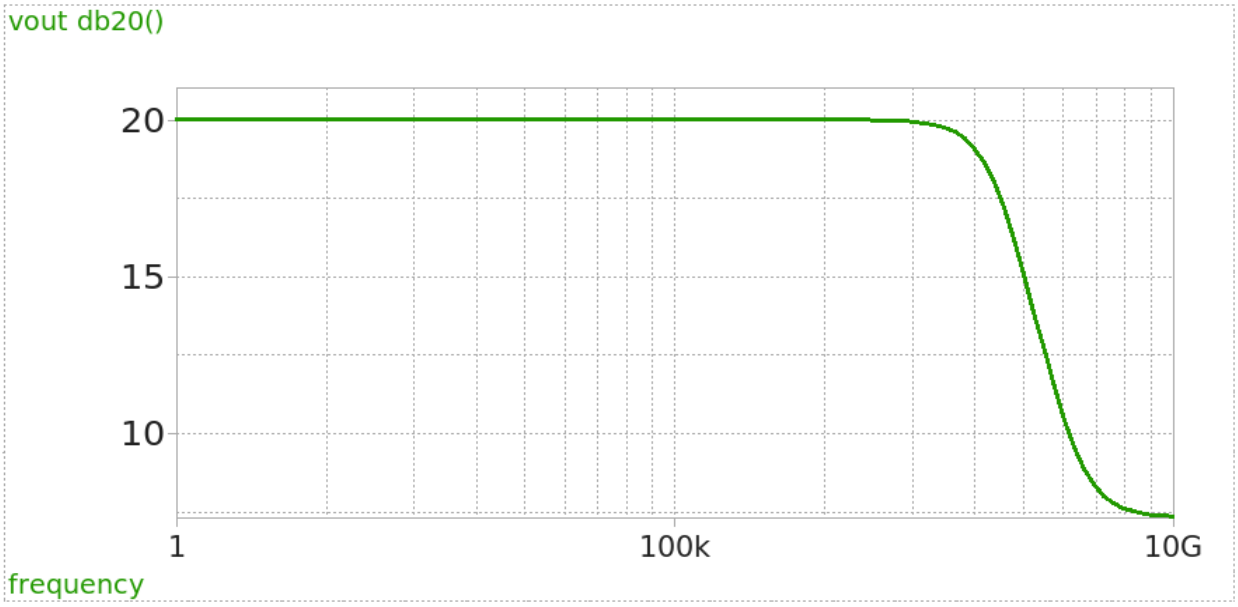
Analytical Gain ≪ Intrinsic Gain

The intrinsic gain ($g_m \cdot r_o$) represents the maximum theoretical gain of the device, while the analytical gain is limited by external circuit components such as the drain resistance (RD).

Ac simulation:



VOUT VS freq

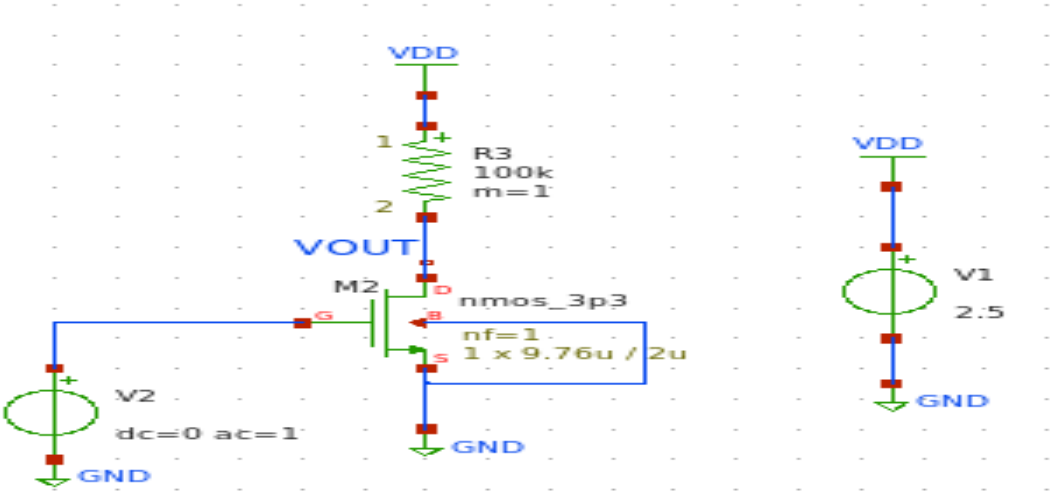


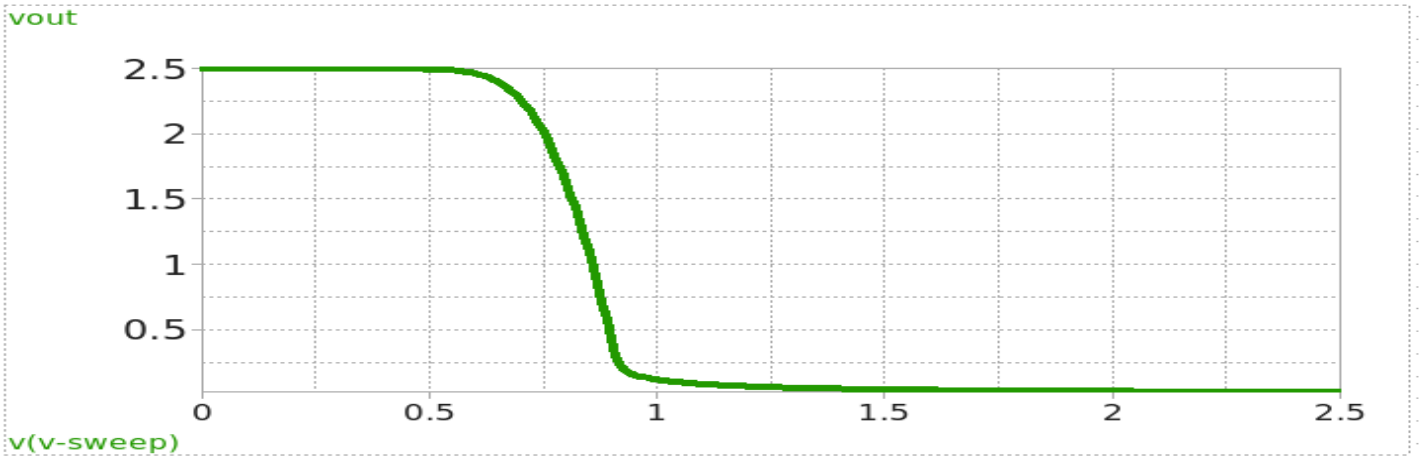
vout in db VS freq

Magnitude of fc gain $=10.01 \approx 10$ V

Our design specification requires a minimum DC gain of approximately 12 V. The obtained result is very close to this target, meaning the design meets the specified gain requirement within acceptable margin and approximately satisfy our specs

Gain non-linearity(Large Signal Operation DC Sweep):





Vout vs Vin

VOUT vs. VIN Report and Linearity:

The relationship between **VOUT and VIN is non-linear** because **VOUT changes significantly at different values of VGS**. As the MOSFET moves through the cutoff, triode, and saturation regions, its behavior changes, causing the output voltage to vary in a non-linear manner with respect to the input voltage

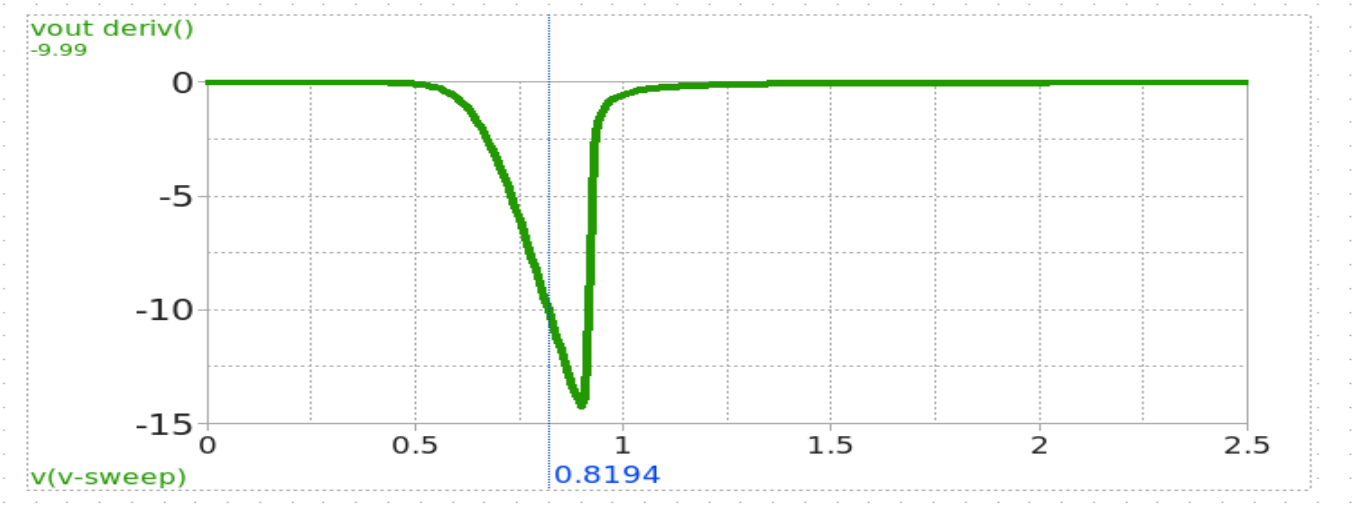


Figure 14: derivative of VOUT

Is the gain linear (independent of the input)? Why?

The gain is **nonlinear**, but at small input voltages (VIN), the gain is approximately linear, though it still depends on VIN to some extent. As the input increases, the transistor transitions through different operating regions, causing the gain to vary and show nonlinear dependence on the input

Gain non-linearity(Transient Analysis)

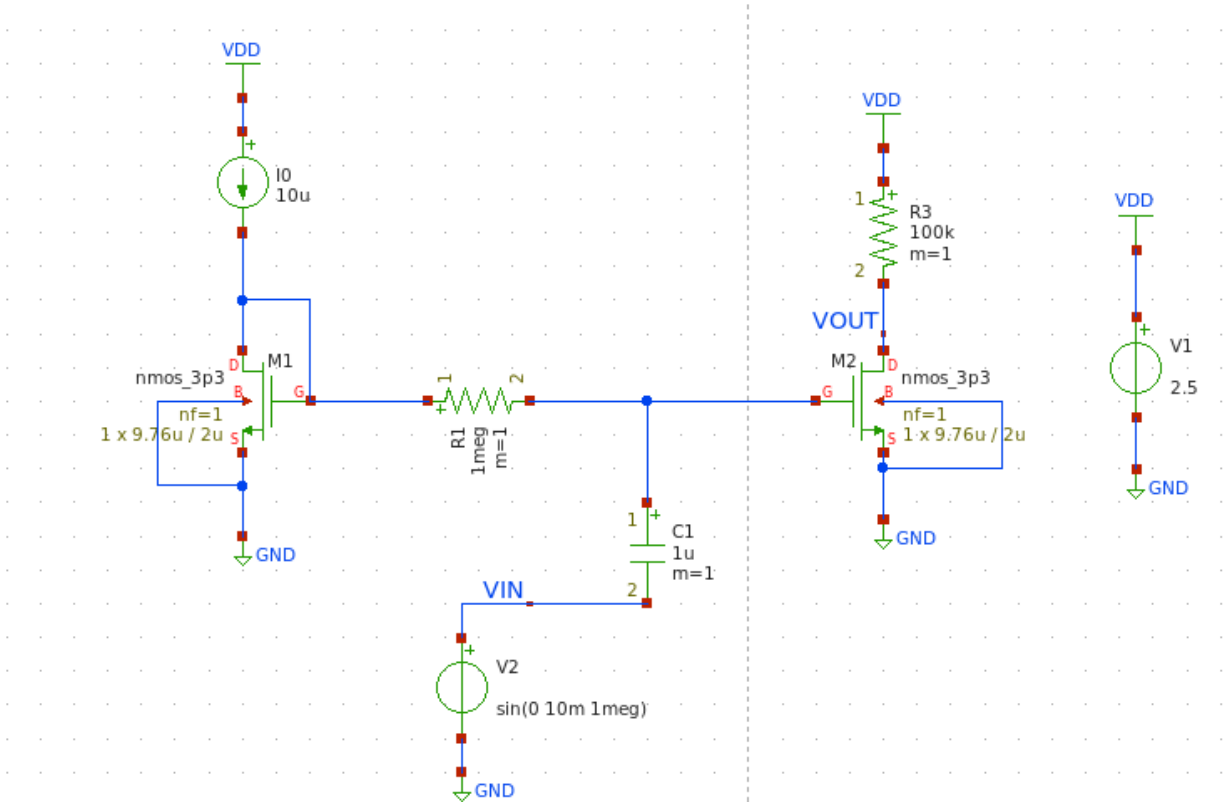
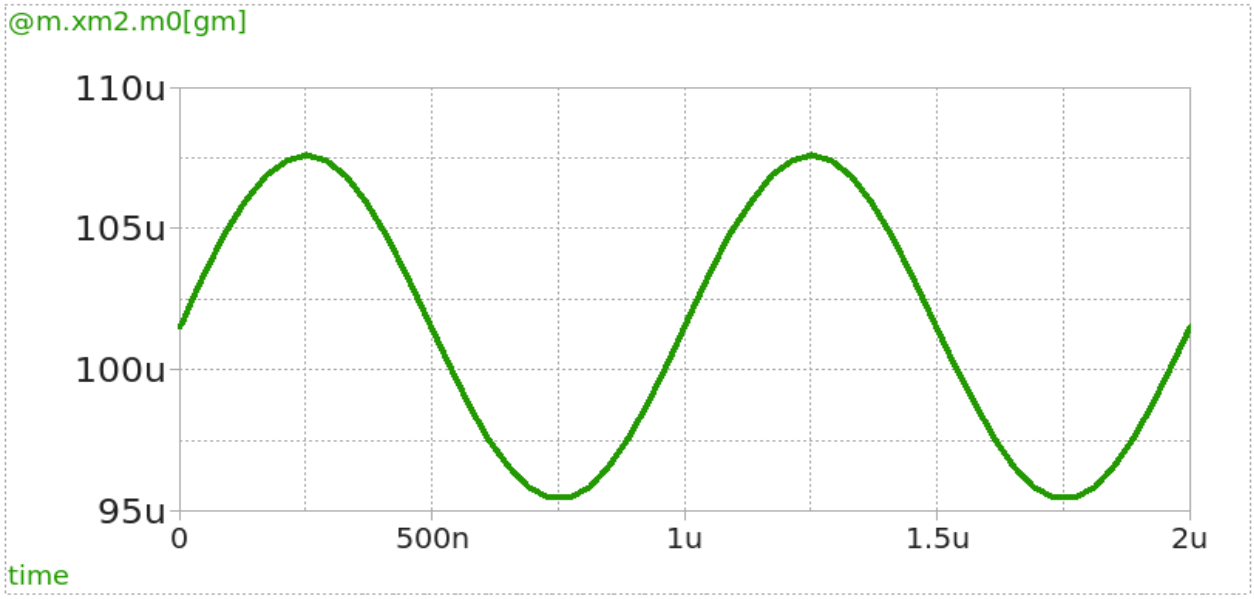
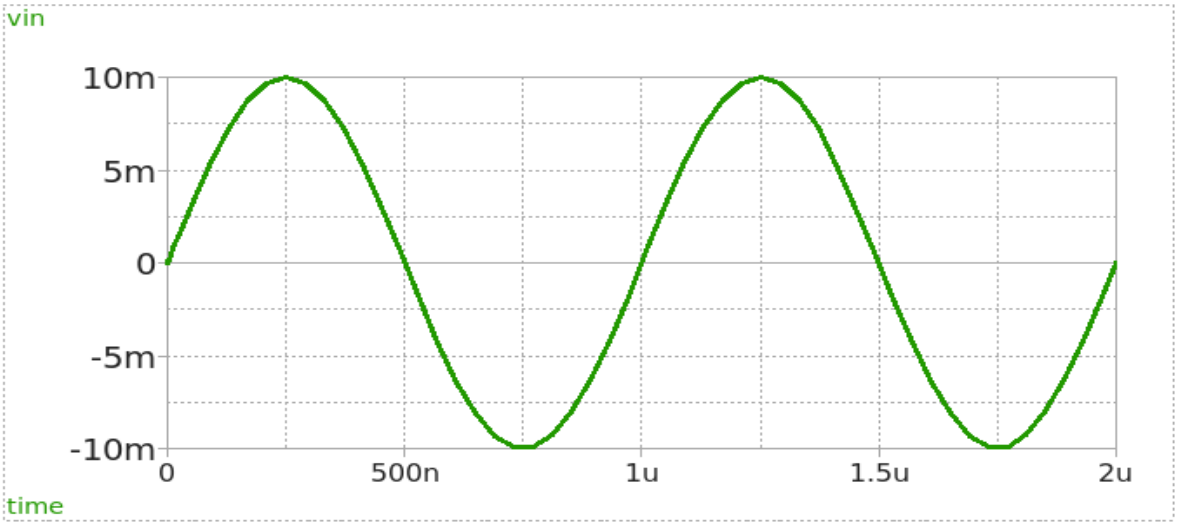


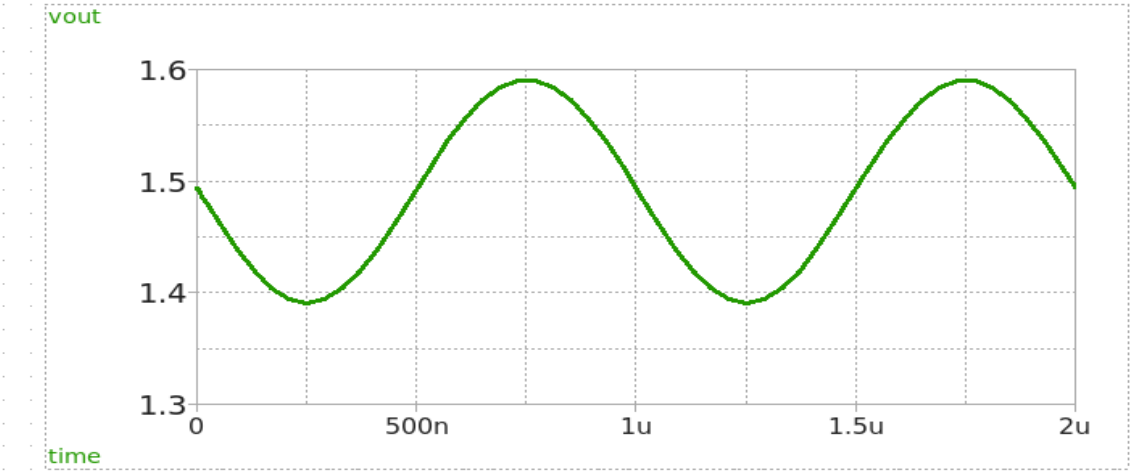
Figure 1: schematic



gm vesus time



VIN versus TIME



VOUT versus TIME

Does gm vary with the input signal?

Based on the time and width (W) data provided, we can infer that gm likely does vary with the input signal since the width values change over time

What does that mean?

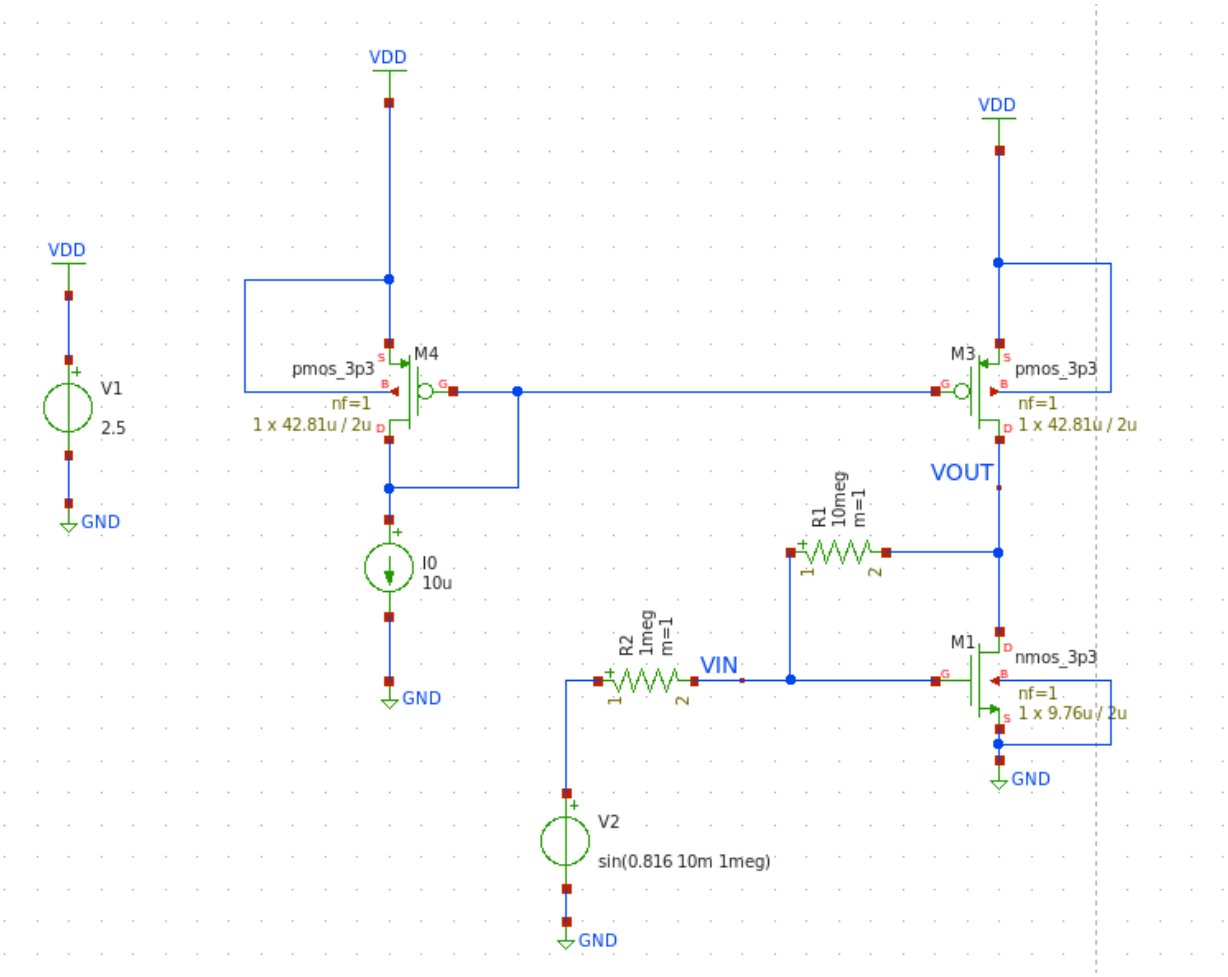
The variation in gm with the input signal indicates that the amplifier's transconductance is signal-dependent. This suggests the amplifier is operating in a non-linear region for at least part of the input signal range, as gm would remain constant in a perfectly linear operation.

Is this amplifier linear?

The amplifier appears to be non-linear based on:

- The variation in gm confirms non-linear behavior

5. Gain Linearization (Negative Feedback)



Schematic

$$R_{in} = \frac{R_f}{A_V} = 1M\Omega$$

From ADT find the sizing of the PMOS device.;

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	2u
4	W	42.81u
5	VGS	936.8m
6	VDS	1
7	VSB	0
8	gm/ID	9.9
9	Vstar	202m

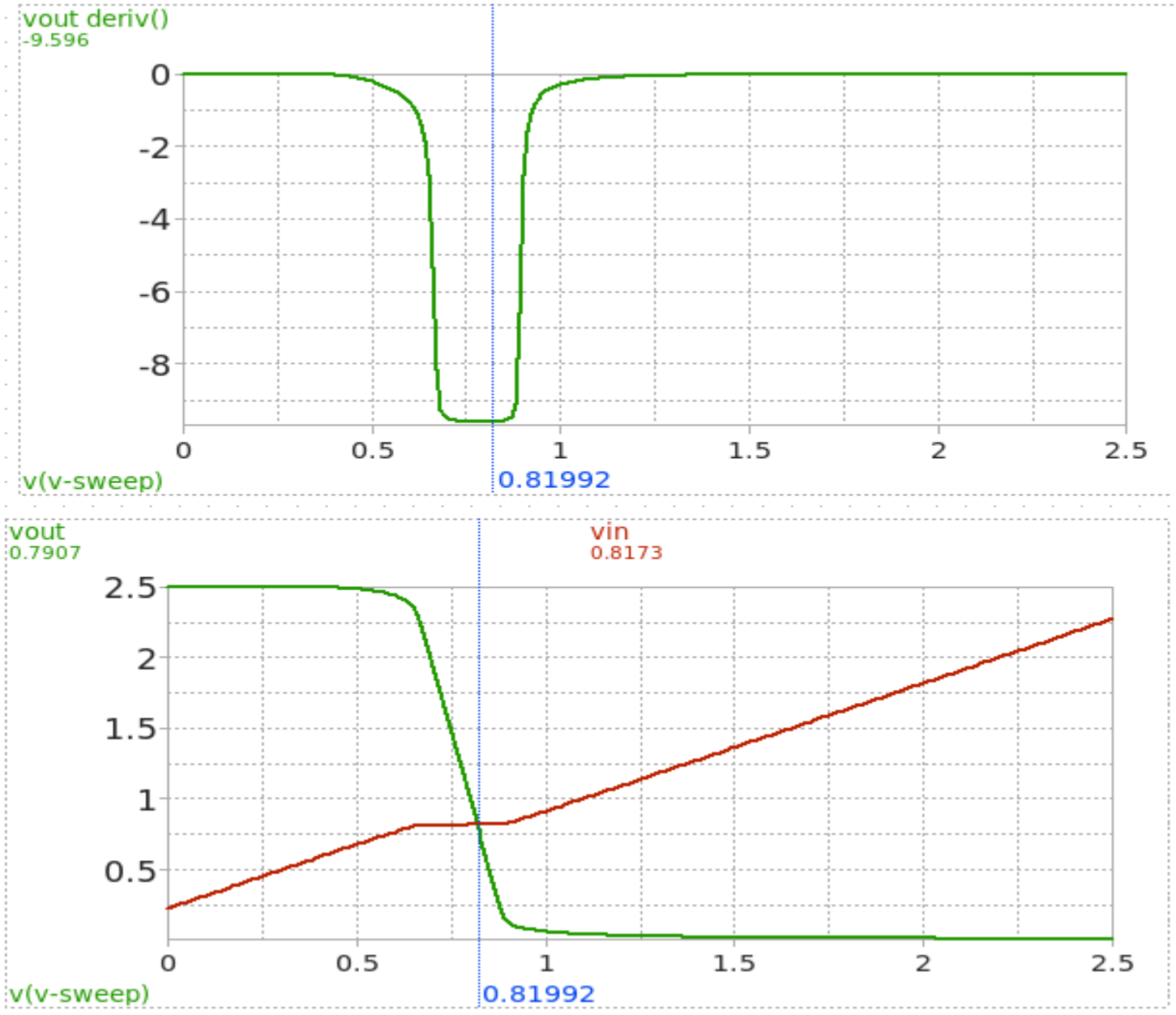
Y-Expr gm/ID*fT

Plot

Results:

	Name	TT-27.0
9	Vstar	202m
10	fT	57.65MEG
11	gm/gds	877.3
12	VA	88.61
13	ID/W	233.6m
14	gm/W	2.313
15	AREA	85.62p
16	gm	99u
17	gmb	48.02u

Y-Expr gm/ID*fT



VIN &VOUT&deriv VOUT VS Vsig

Is VOUT vs. VSIG Linear in the Operating Range? Why?

VIN and VOUT cross at VSIG ≈ 0.82mV, matching VGS of M1 at the bias point.

At this point, no current flows through the feedback resistor (RF) → No voltage drop → VOUT = VIN.This ensures the closed-loop gain is determined purely by resistor ratios (Rf/Rin).

Is the gain linear (independent of the input) in the operating range of the amplifier? Why?

- Yes Since VIN ≈ VOUT ≈ 813mV, there is no voltage drop across resistors (RF, Rin) → behaves like a virtual short.
- No current flows into the MOSFET gate → VSIG directly controls VOUT with a fixed gain (Rf/Rin).
- No gm dependence → Linear relationship.

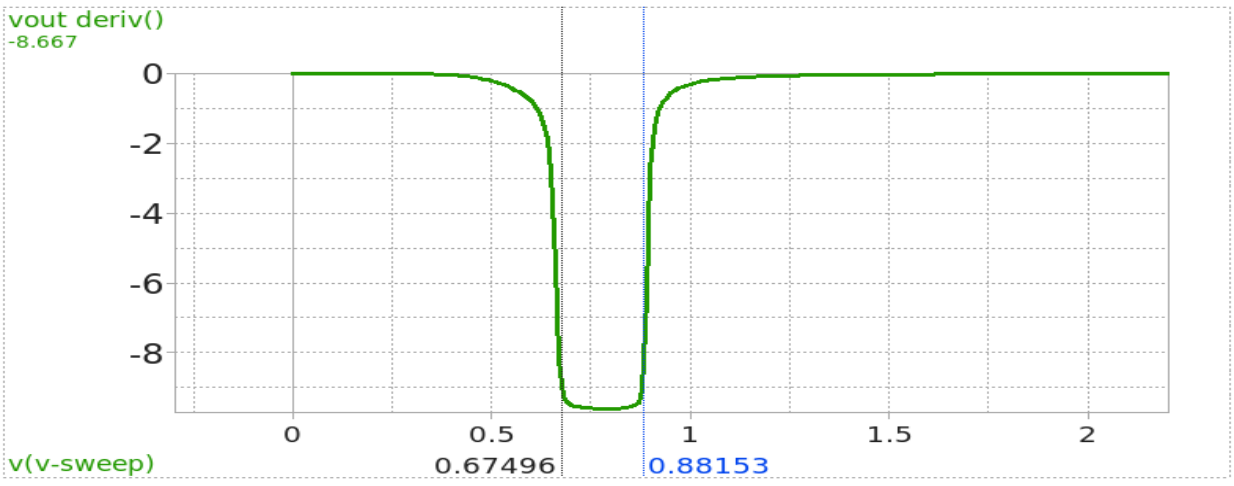
VIN is almost constant in the operating range of the amplifier. What is its value? Why?

VIN ≈ VGS ≈ 812mV (DC bias).

- No current flows through RF or Rin → No voltage drop → VIN = VSIG (DC).
- The MOSFET gate draws zero DC current → VIN remains pinned at VGSQ.

Analytically calculate the DC input range over which the gain is linear. Compare your analysis with the simulation result.

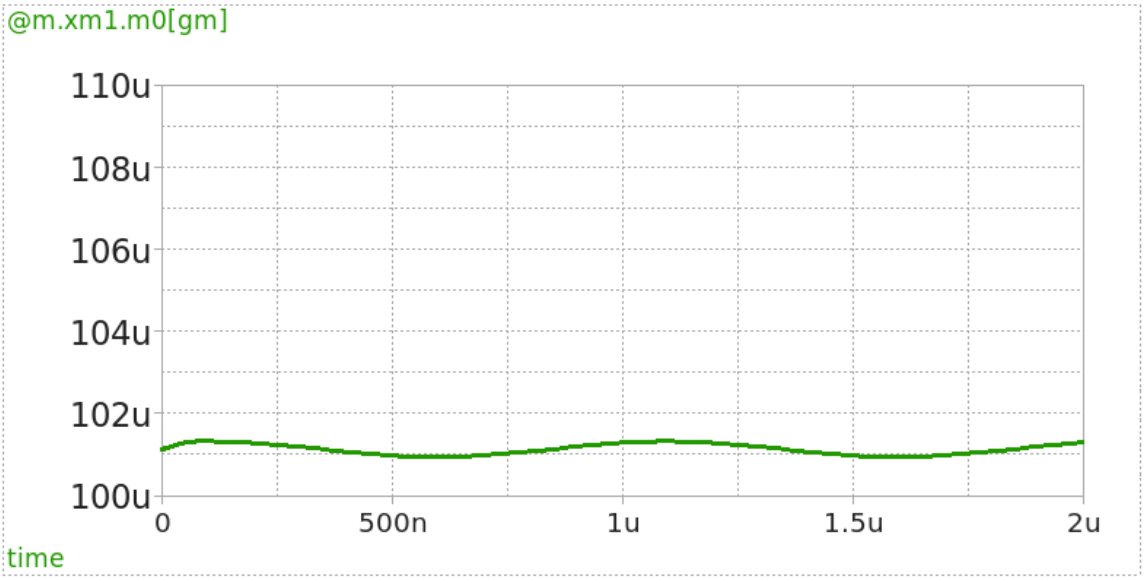
→ by the gain ≈ $\frac{V_{DD}-2V^*}{|A_v|}$ = 210 mv



from simulation:

→ it approximately = 206 mv

gm vs time :



1. Feedback Amplifier (Current Plot)

gm Range: 95µ–110µ (variation ≈ 15µ)

Stability:

gm stays relatively stable over time.

Small fluctuations (≈5–10µ) due to feedback correction.

Feedback forces VIN ≈ VOUT, stabilizing the operating point.

Closed-loop gain (Rf/Rin) dominates, reducing gm dependence.

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2. Resistive-Loaded Open-Loop Amplifier (Previous Plot)

gm Range: 100µ–110µ (variation ≈ 10µ)

Instability:

Larger peak-to-peak variation (≈10µ) despite smaller range.

No feedback → gm directly tracks input signal (more sensitive to VGS changes).

Gain depends on gm·RD, making it input-dependent.

No mechanism to suppress gm variations.