# Analog IC Design (Xschem, Ngspice, ADT) Lab 01

LPF Simulation and MOSFET Characteristics

## PART 1: Low Pass Filter Simulation (LPF):

### 1. Transient Analysis

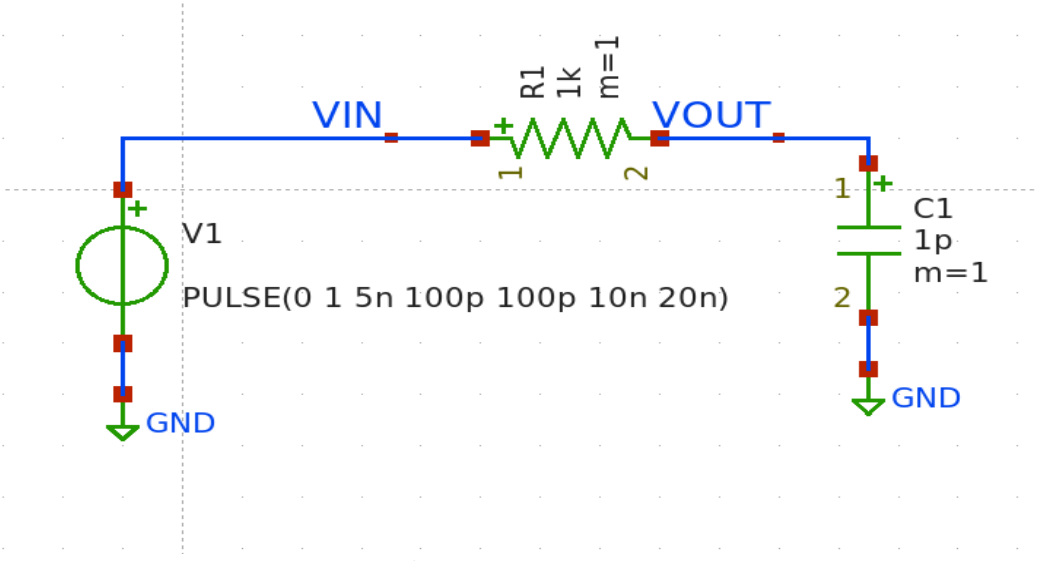
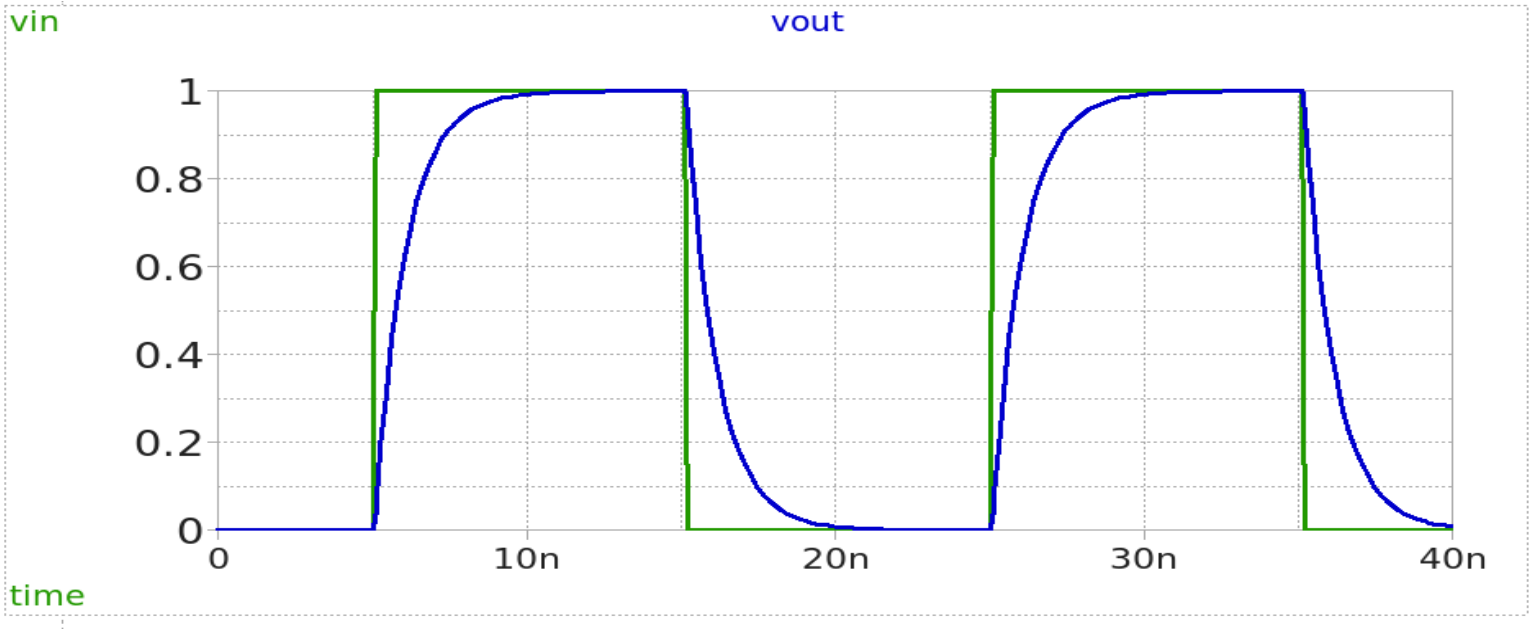



*Figure 1:SCHEMATIC*

**Transient analysis results for two periods:**



**rise and fall time (10% to 90%) :**

```
t_rise                =  2.194799e-09 targ=  7.350398e-09 trig=  5.155599e-09
t_fall                =  2.190539e-09 targ=  1.744592e-08 trig=  1.525538e-08
```

## Export the results to an output text file:

```
1 const.r_val = 1.000000e+03
2 tran1.t_rise = 2.194799e-09
3 tran1.t_fall = 2.190539e-09
```

### Compare simulation with analytical results:

Given that the filter uses R = 1 k Ω and C = 1 pF,

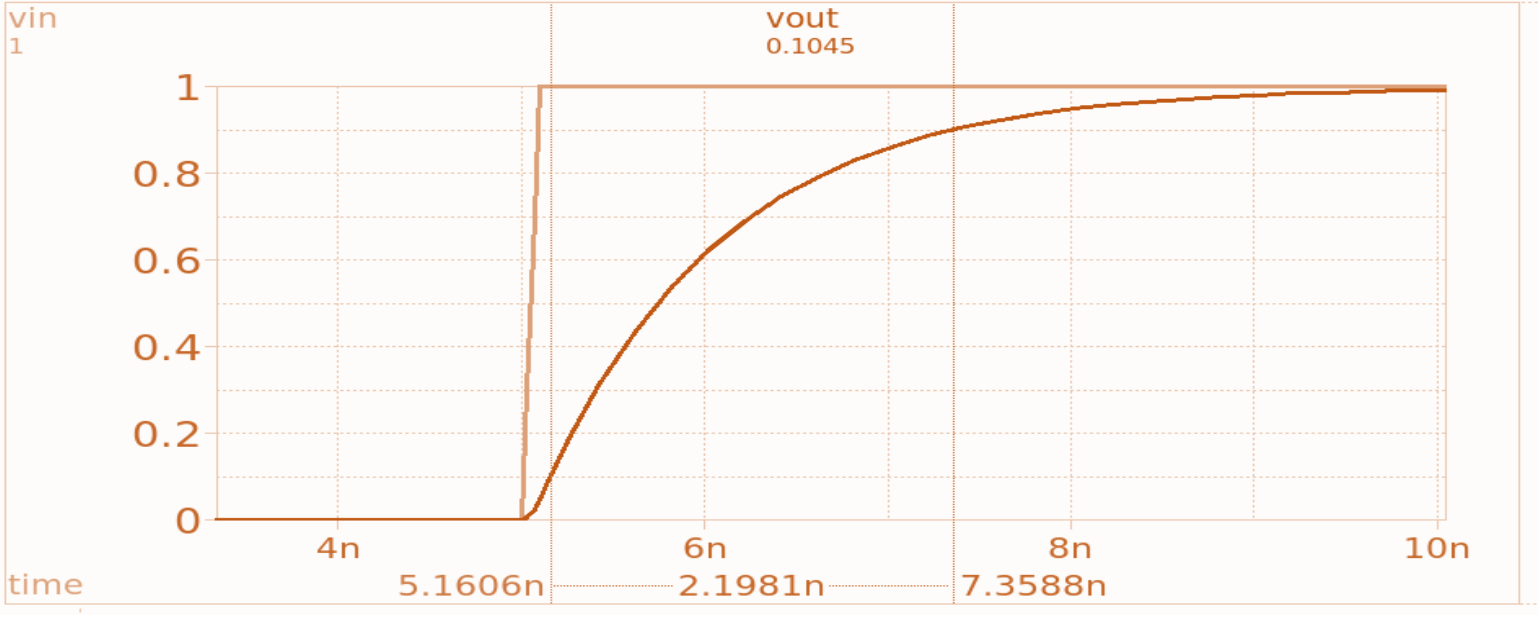
the time constant is: $\tau = RC = 1k\Omega \times 1\ pF = 1ns$ ⟶ $T_{rise} \approx 2.2 \times \tau = 2.2 \times 1ns = 2.2ns$

| | Simulation Results | Hand Analysis |
|---|---|---|
| T_Rise | 2.194799 ns | 2.2 ns |
| T_Fall | 2.190539 ns | 2.2 ns |

comment

The simulated output showed a rise time and fall time close to **2.2 ns**, which confirms that the filter responds as expected and matches the theoretical behavior of a first-order low-pass filter

**we can also from graph calc t_fall and t_rise using difference between two cursers as shown in the next photo at R=1K:**



**parametric sweep for $R = 1{:}\ 1{:}\ 5k\Omega$:**

**AT R=1K**

```
t_rise               =  2.194799e-09 targ=  7.350398e-09 trig=  5.155599e-09
t_fall               =  2.190539e-09 targ=  1.744592e-08 trig=  1.525538e-08
```

**AT R=2K**

```
t_rise               =  4.392096e-09 targ=  9.652757e-09 trig=  5.260660e-09
t_fall               =  4.392619e-09 targ=  1.974099e-08 trig=  1.534837e-08
```

**AT R=3K**

```
t_rise               =  6.589698e-09 targ=  1.195651e-08 trig=  5.366814e-09
t_fall               =  6.590324e-09 targ=  2.195146e-08 trig=  1.536114e-08
```

**AT R=4K**

```
t_rise               =  8.787352e-09 targ=  1.425855e-08 trig=  5.471196e-09
t_fall               =  8.787581e-09 targ=  2.402509e-08 trig=  1.523751e-08
```

**AT R=5K**

```
Error: measure  t_rise  trig(TARG) : out of interval
 meas tran t_rise trig v(vout) val=0.1 rise=1 targ v(vout) val=0.9 rise=1 failed
!


Error: measure  t_fall  trig(TRIG) : out of interval
 meas tran t_fall trig v(vout) val=0.9 fall=1 targ v(vout) val=0.1 fall=1 failed
!
```

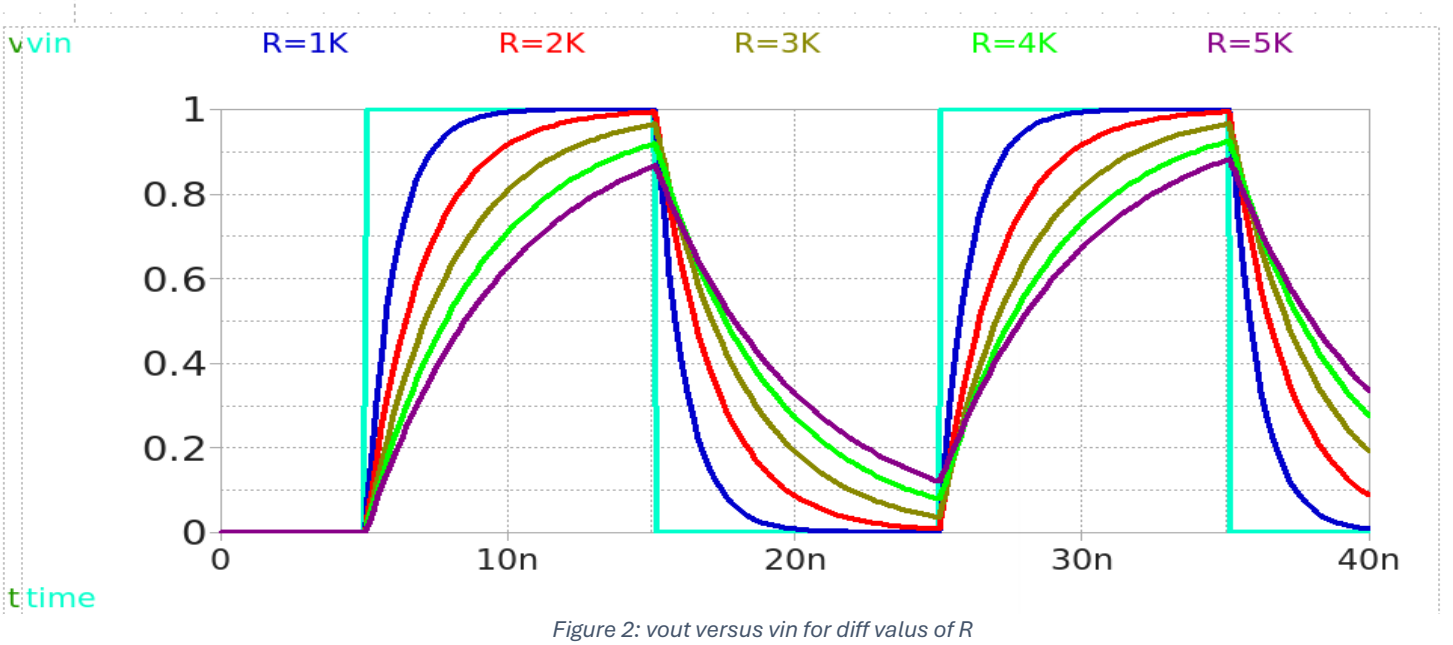



*Figure 2: vout versus vin for diff valus of R*

## ***Comment on the Results:***

The parametric sweep (R = 1–5 kΩ, C = 1 pF) confirmed that higher resistances increase the RC time constant, slowing the output waveform's rise/fall times. At R = 5 kΩ, the output failed to reach 10%/90% thresholds within the simulation window, causing an out-of-range error.

## Export the results to an output text file:

```
const.r_val = 1.000000e+03
tran1.t_rise = 2.194799e-09
tran1.t_fall = 2.190539e-09
const.r_val = 2.000000e+03
tran2.t_rise = 4.392096e-09
tran2.t_fall = 4.392619e-09
const.r_val = 3.000000e+03
tran3.t_rise = 6.589698e-09
tran3.t_fall = 6.590324e-09
const.r_val = 4.000000e+03
tran4.t_rise = 8.787352e-09
tran4.t_fall = 8.787581e-09
```

Code I used:

s1

```
.control
save all
let R_val = 1000
let R_stop = 5000
let R_step = 1000
while R_val le R_stop
alter R1 R_val
tran 200p 40n
meas tran t_rise TRIG v(vout) VAL=0.1 RISE=1 TARG v(vout) VAL=0.9 RISE=1
meas tran t_fall TRIG v(vout) VAL=0.9 fall=1 TARG v(vout) VAL=0.1 fall=1
print R_val t_rise t_fall >> tran_result.txt
write rc_ckt.raw
set appendwrite
let R_val = R_val + R_step
end
.endc
```

## 2. AC Analysis

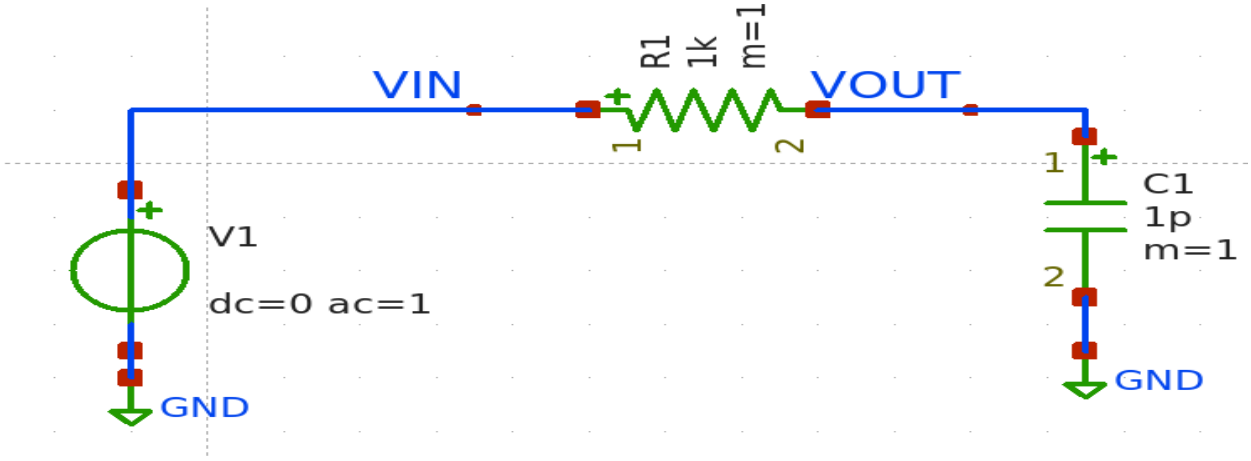



*Figure 3:Schematic*

bode plot &phase:

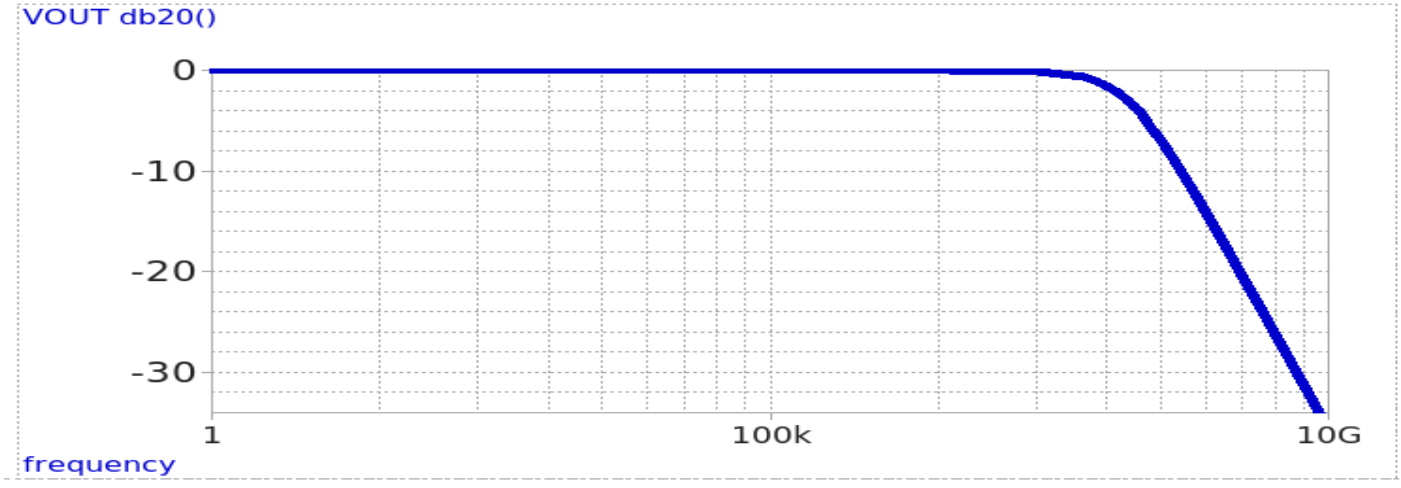



*Figure 4:vout in db*

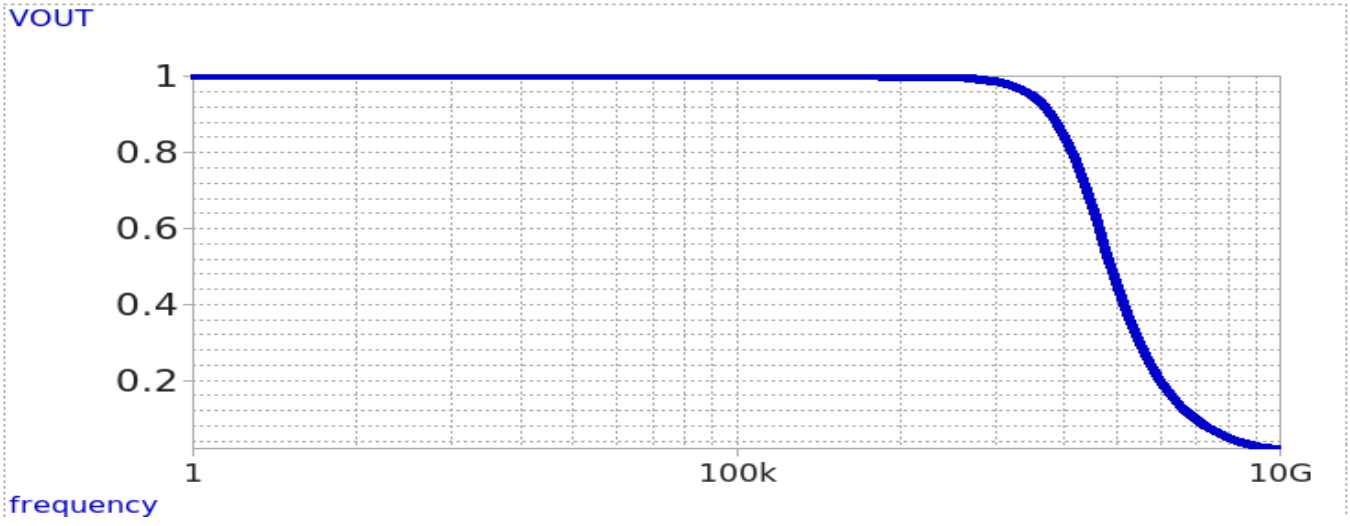



*Figure 5: vout in linear scale*

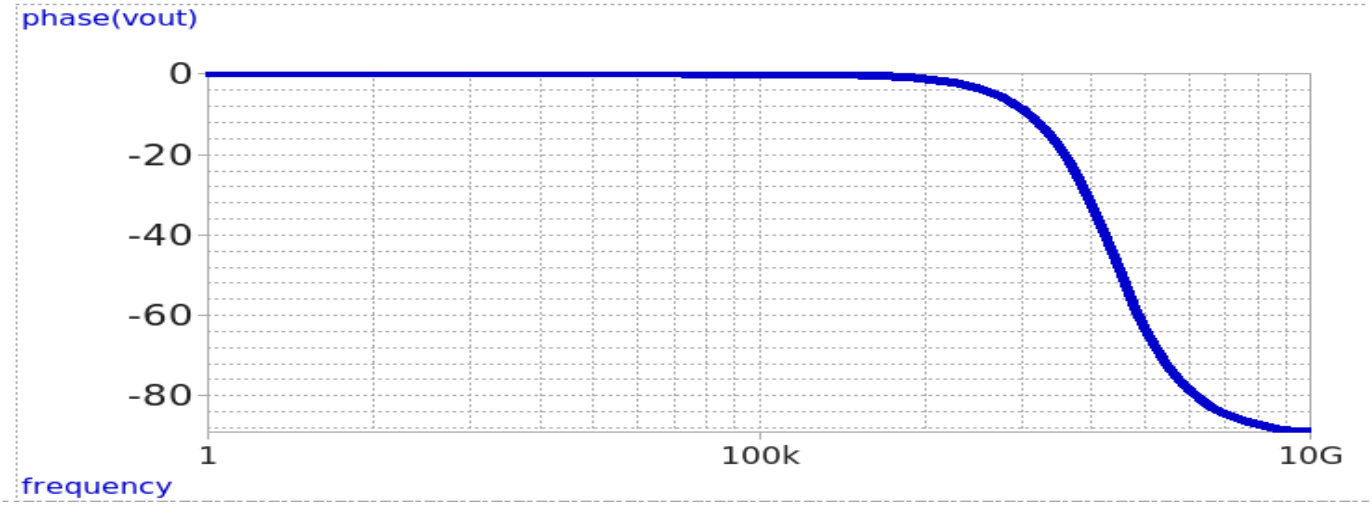



*Figure 6: phase*

**DC gain and 3dB bandwidth:**

```
max_gain              =  1.000000e+00 at=  1.584893e+00
bw                    =  1.592554e+08
```

## Export the results to an output text file

```
1 const.r_val = 1.000000e+03
2 ac1.max_gain = 1.000000e+00
3 ac1.bw = 1.592554e+08
```

## Compare simulation with analytical results:

**Hand analysis**: τ= RC = 1kΩ×1pF =1ns ⟶ $F_C = \frac{1}{2\pi\tau} = 159.155$ MHZ

| | Simulation Results | Hand Analysis |
|---|---|---|
| Bandwidth | 159.255MHz | 159.155 MHz |

## parametric sweep for $R = 1,10,100,1000k\Omega$

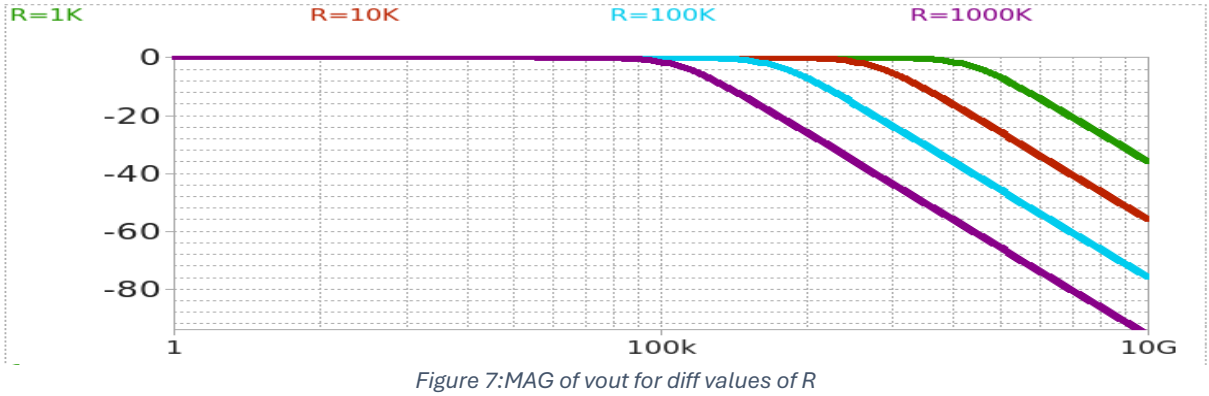



*Figure 7:MAG of vout for diff values of R*

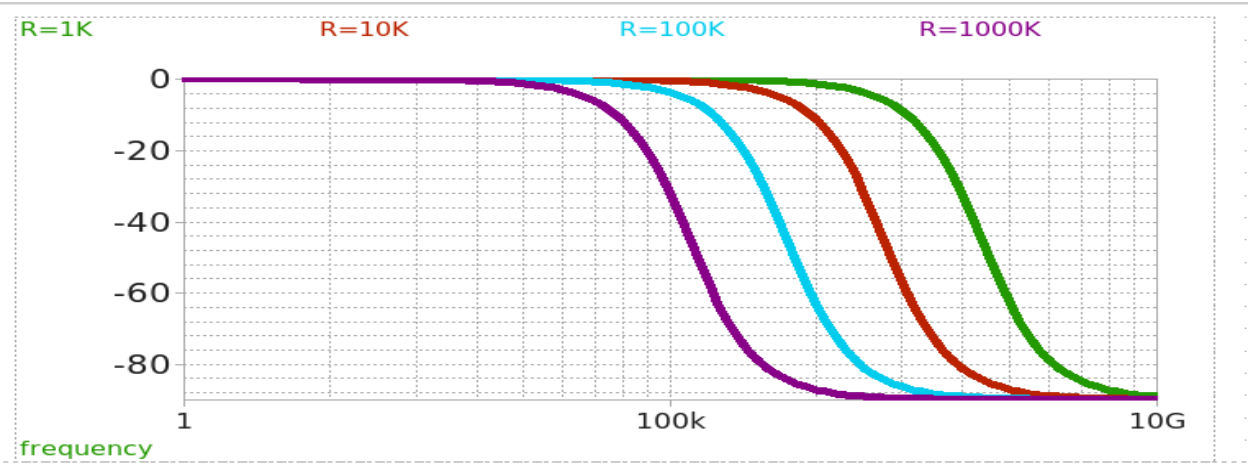



*Figure 8:phase of vout for diff values of R*

***CODE USED IN THIS PART:***

s1

```
.control
save all
let R_val = 1k
let R_stop = 1meg
let R_mult = 10
while R_val le R_stop
alter R1 R_val
ac dec 10 1 10g
meas ac MAX_GAIN MAX vmag(vout) FROM=1 TO=10G
meas ac BW WHEN vmag(vout)=0.707 FALL=1
print R_val MAX_GAIN BW >> ac_result.txt
write rc_ckt_2.raw
set appendwrite
let R_val = R_val * R_mult
end
.endc
```

***export text file :***

```
const.r_val = 1.000000e+03
ac1.max_gain = 1.000000e+00
ac1.bw = 1.592554e+08
const.r_val = 1.000000e+04
ac2.max_gain = 1.000000e+00
ac2.bw = 1.592554e+07
const.r_val = 1.000000e+05
ac3.max_gain = 1.000000e+00
ac3.bw = 1.592554e+06
const.r_val = 1.000000e+06
ac4.max_gain = 1.000000e+00
ac4.bw = 1.592554e+05
```

## ***Comment on the Results:***

As the resistor value increased from 1 kΩ to 1 MΩ, the bandwidth steadily decreased. This behavior is expected, as higher resistance slows the filter's response, reducing its ability to pass higher frequencies where $F_C = \frac{1}{2\pi RC}$

# Part 2: MOSFET Characteristics

## SCHEMATIC:

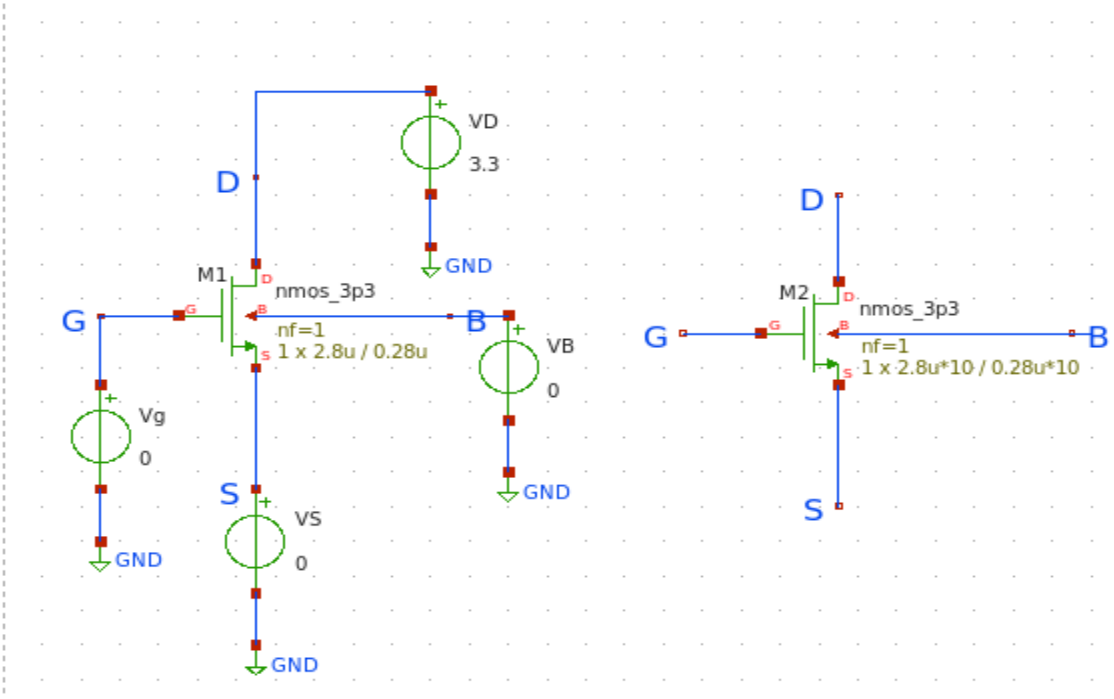



*Figure 9:NMOS*

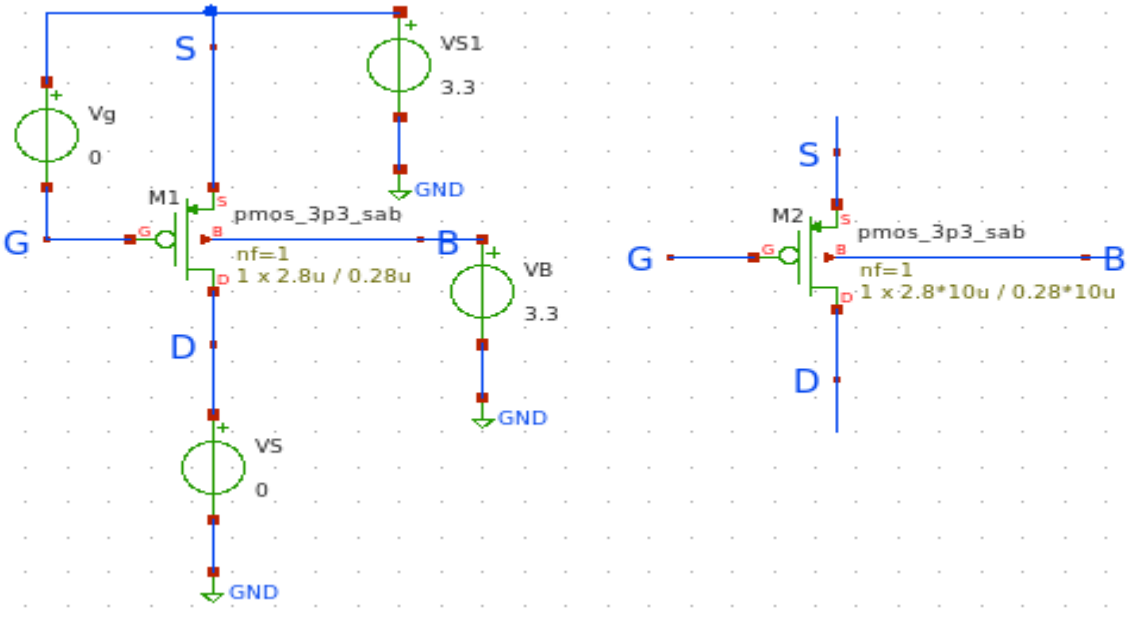
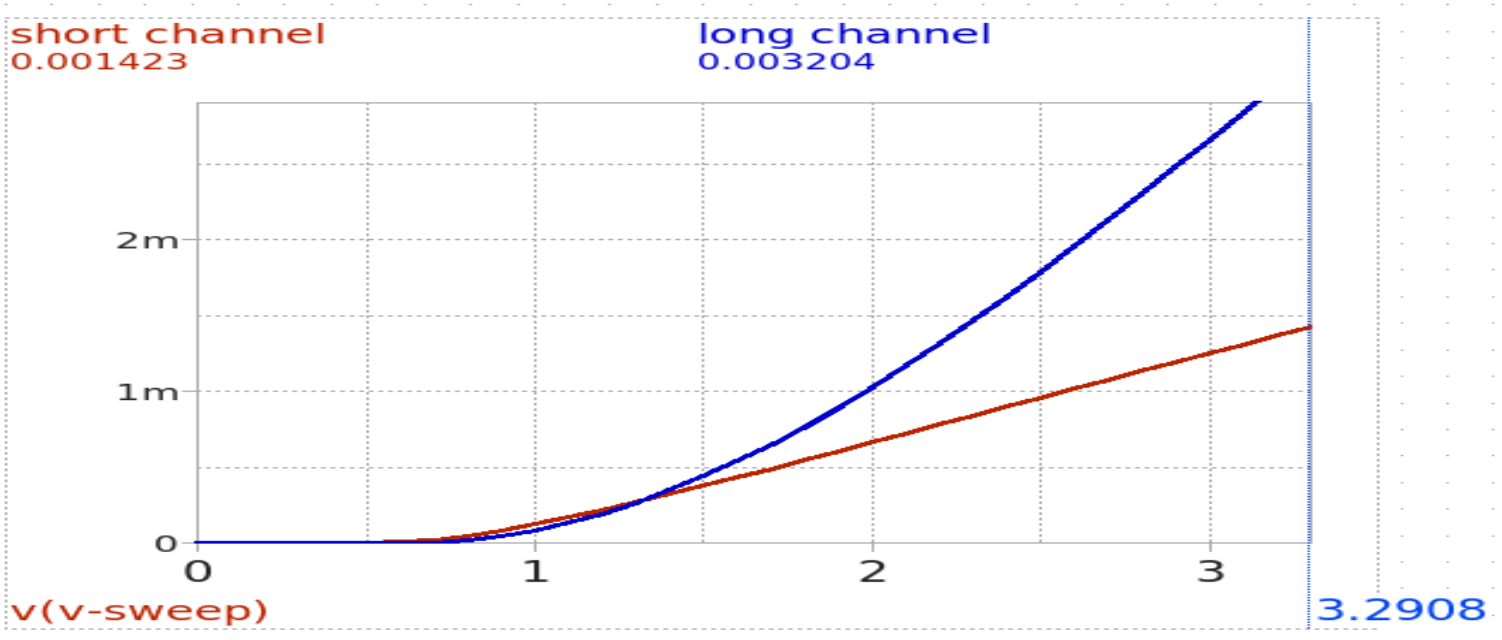


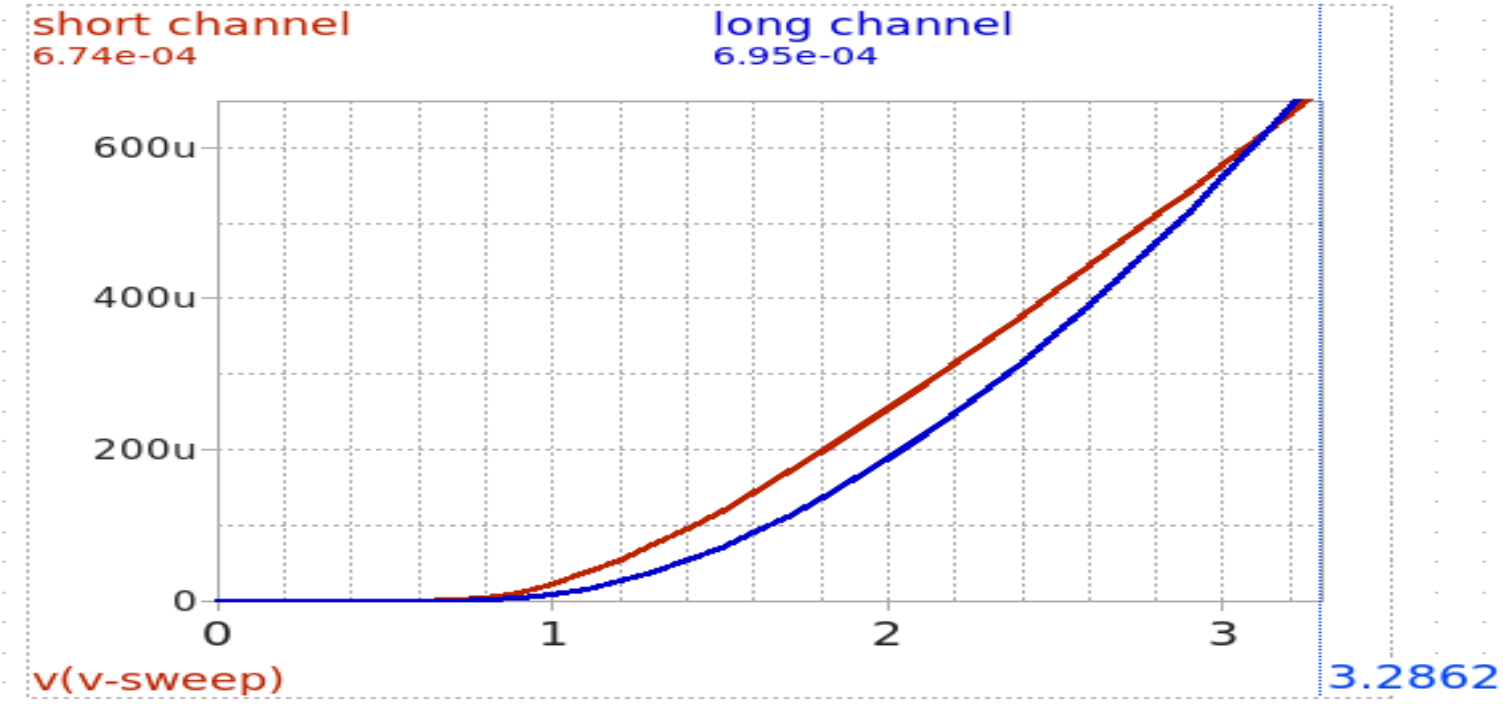

*Figure 10:PMOS*

## 1. ID vs VGS

- NMOS short channel and long channel overlaid




- PMOS short channel and long channel overlaid



***Comment on the differences between short channel and long channel:***

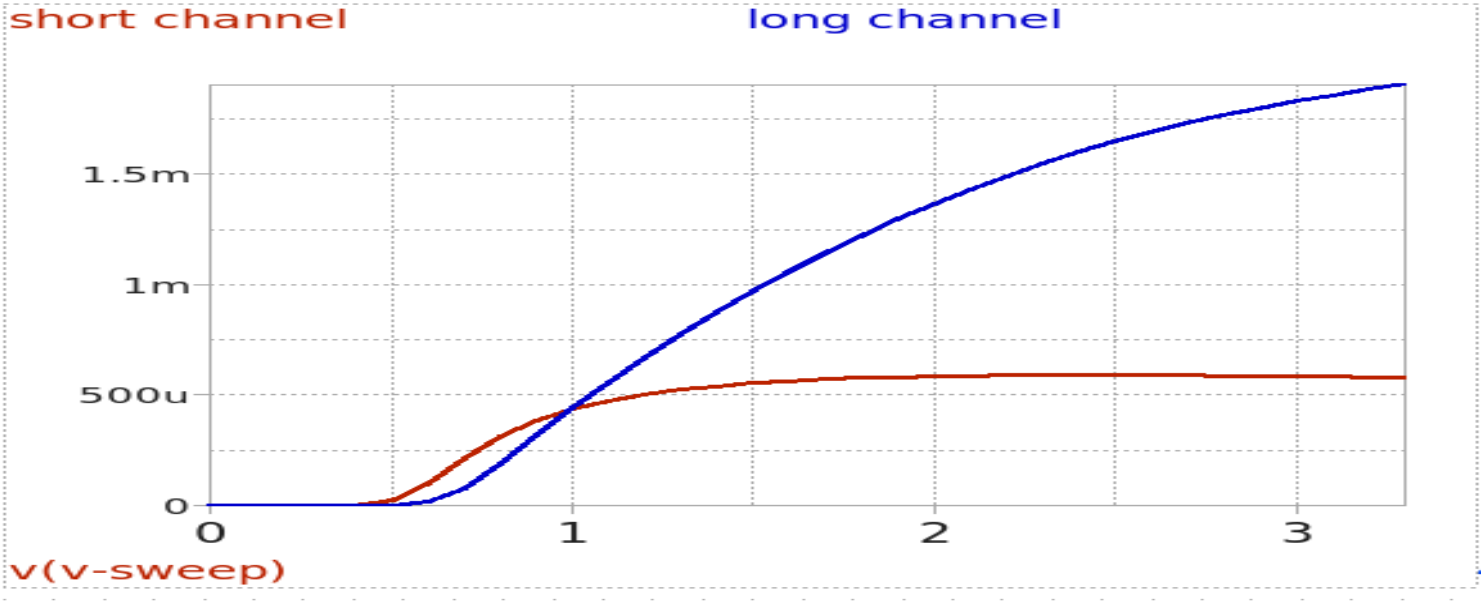
- Long-channel MOSFETs exhibit higher drain current compared to short-channel devices when using the same W/L ratio. This is due to reduced short-channel effects and more ideal carrier transport in long-channel devices.
- In the saturation region, long-channel devices follow the ideal quadratic $I_D \propto$(VGS−Vth)^2 behavior. In contrast, short-channel devices show a more linear $I_D$ response due to velocity saturation and other short-channel effects.
- Ratio of currents of NMOS $\frac{I_{Long}}{I_{Short}} = \frac{0.003204}{0.001423} = 2.25$

***Comment on the differences between NMOS and PMOS:***

- NMOS is more affected by short-channel effects, such as velocity saturation and threshold voltage variation, making it more sensitive to scaling than PMOS.
- NMOS has higher current than PMOS due to the higher electron mobility compared to hole mobility.
- Ratio of currents of SHORT channel $\frac{I_{Nmos}}{I_{Pmos}} = \frac{0.001423}{0.000674} = 2.11$
- Ratio of currents of long channel $\frac{I_{Nmos}}{I_{Pmos}} = \frac{0.003204}{0.000695} = 4.61$

## 2. $g_m$ vs VGS :

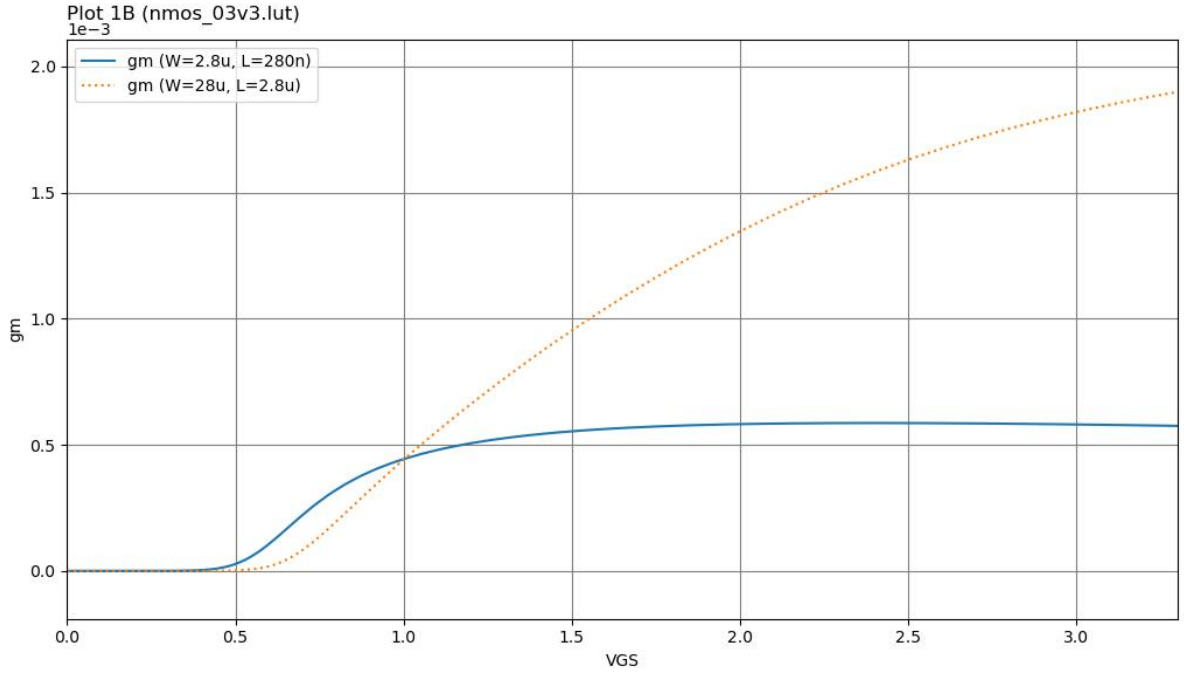
- NMOS short channel AND long channel overlaid:



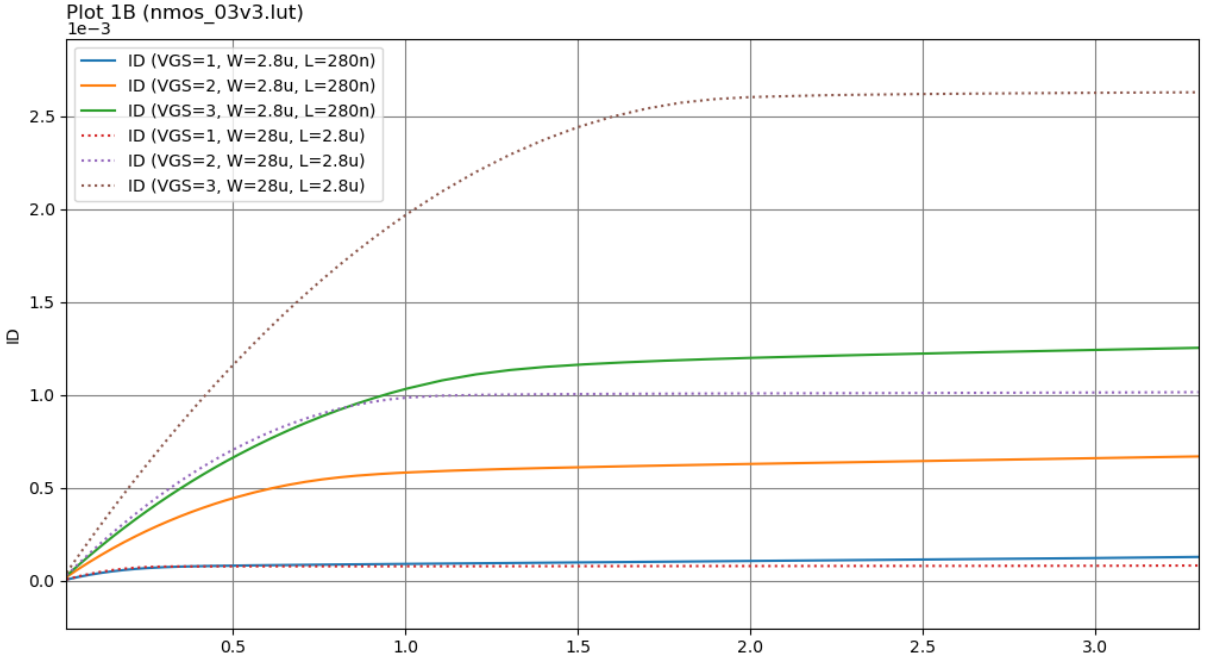

***Comment on the Differences Between Short-Channel and Long-Channel Devices:***

- Short-channel devices do not exhibit a purely quadratic increase in $g_m$, as carrier velocity saturates under high electric fields, leading to early saturation of transconductance.
- In contrast, long-channel devices show a more gradual and extended increase in $g_m$, following the classical quadratic dependence of MOSFETs in the saturation region.
- For short-channel devices, $g_m$ saturates earlier, limiting their gain and linearity.
- Long-channel devices maintain increasing $g_m$ over a wider range of $V_{GS}$ offering better analog performance and linearity.

## $g_m$ vs VGS (using ADT)




## 3. ID vs VDS (use ADT) : Plot the results overlaid



*Comment on the differences between short channel and long channel results:*

- *The long-channel NMOS transistor exhibits a higher current.*
  • *This occurs because of short-channel effects, such as velocity saturation, decrease the carriers' effective mobility, which in turn limits the current.*
  • *The long-channel device's current behavior closely follows the classic quadratic MOSFET current model.*
- *On the other hand The short-channel NMOS transistor shows a steeper slope in the saturation region.*
  *This happens because the stronger electric field near the drain in short-channel devices effectively shortens the channel length, causing the drain current (ID) to continue increasing even after the device enters saturation.*