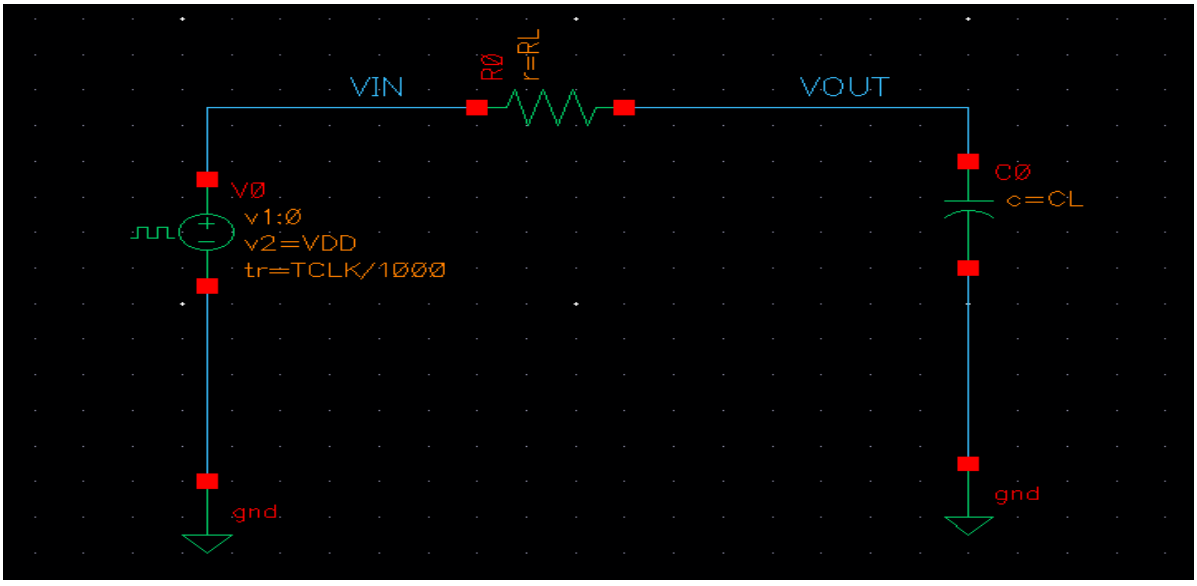
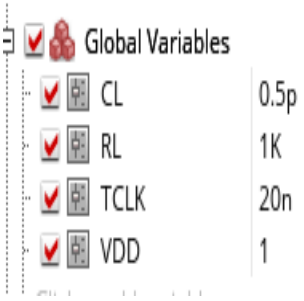
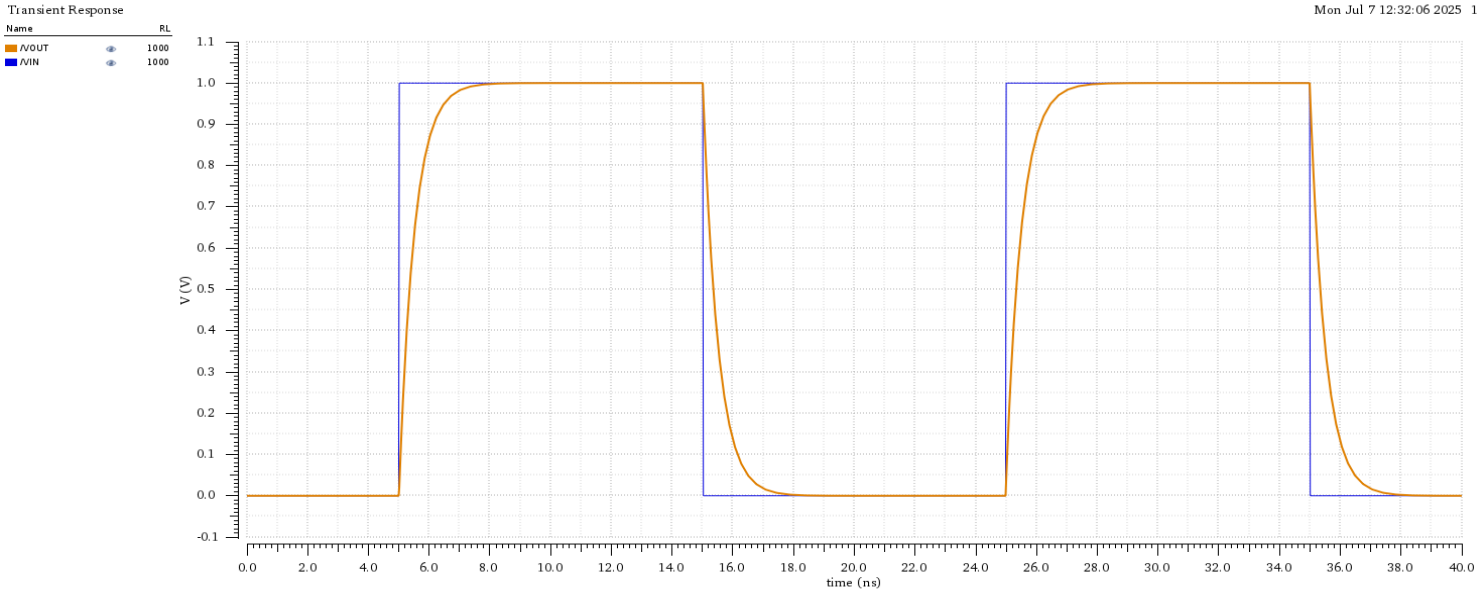
Analog IC Design – Cadence Tools
Lab 01
LPF Simulation and MOSFET Characteristics

PART 1: Low Pass Filter Simulation (LPF):

1. Transient Analysis







Transient analysis results for two periods :

rise and fall time (10% to 90%) using Cadence calculator expressions:

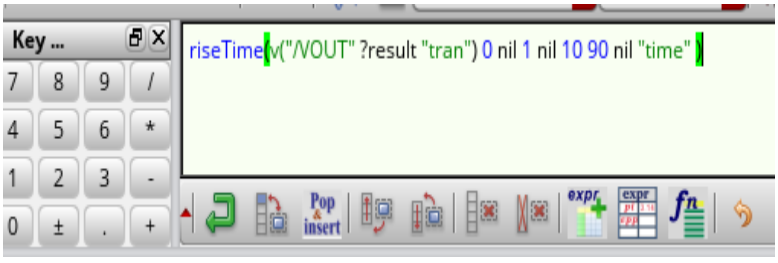


Figure 3:expression for "rise time"

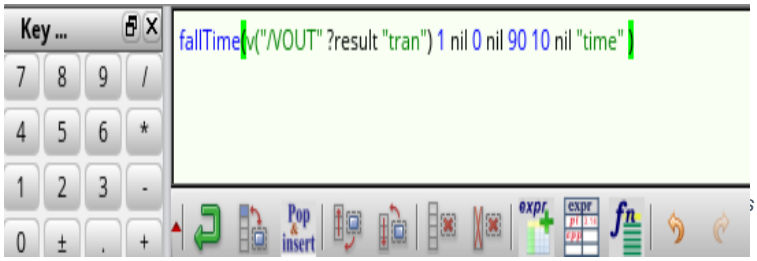


Figure 4: expression for "fall time"

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_LABS:lpf_tb:1	/VOUT				
ITI_LABS:lpf_tb:1	/VIN				
ITI_LABS:lpf_tb:1	/V0/PLUS				
ITI_LABS:lpf_tb:1	T_RISE	1.1n			
ITI_LABS:lpf_tb:1	T_FALL	1.1n			

Figure 4: Values of "rise time" &"fall time"

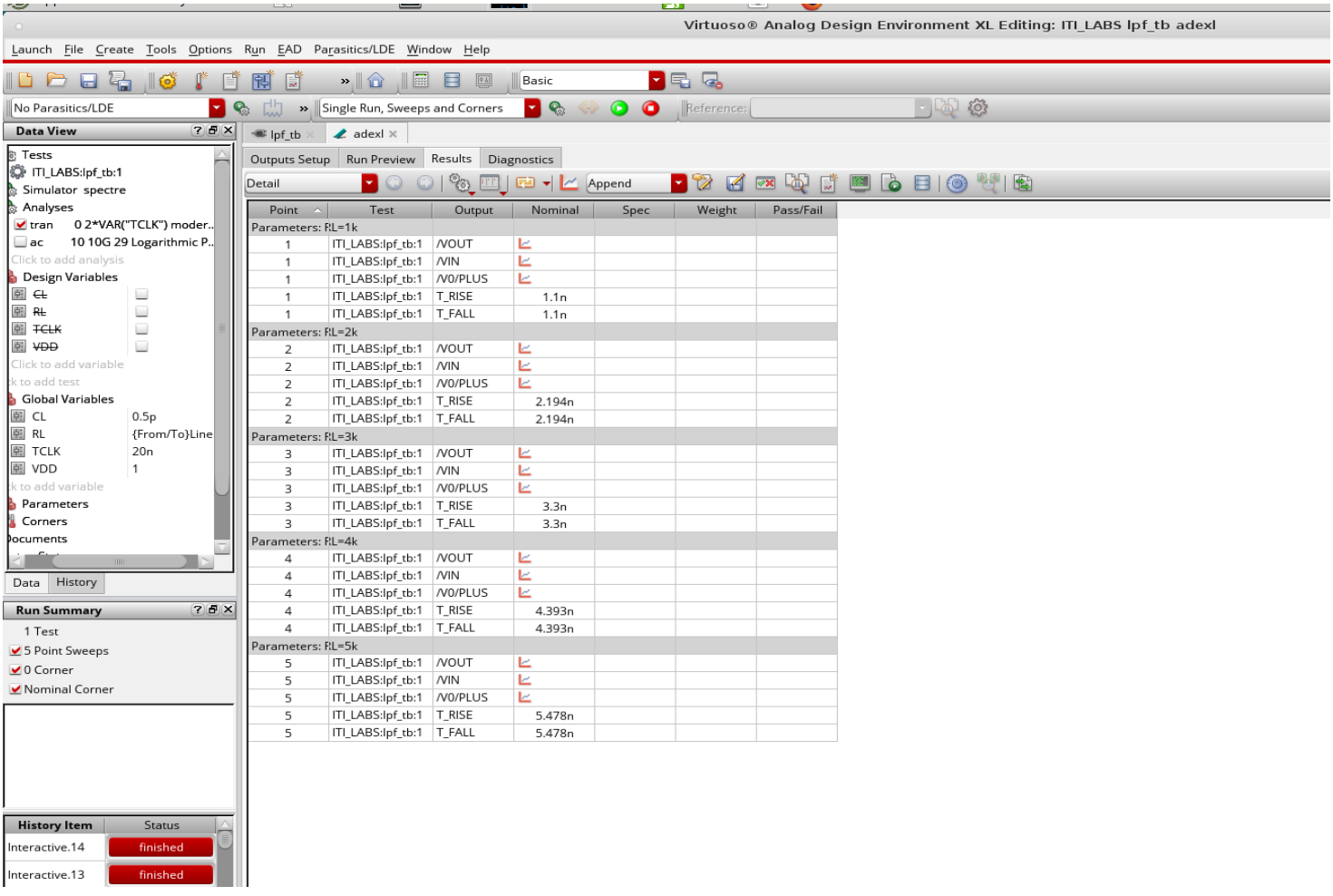
Compare simulation with analytical results:

Given that the filter uses R = 1 k Ω and C = 0.5 pF, the time constant is:
$\tau = RC = 1k\Omega \times 0.5pF = 0.5ns$ ⟶ $T_{rise} \approx 2.2 \times \tau = 2.2 \times 0.5ns = 1.1ns$

	Simulation Results	Hand Analysis
T_Rise	1.1 ns	1.1 ns

The simulated output showed a rise time and fall time close to **1.1 ns**, which confirms that the filter responds as expected and matches the theoretical behavior of a first-order low-pass filter

parametric sweep for $R = 1{:}\ 1{:}\ 5k\Omega$:

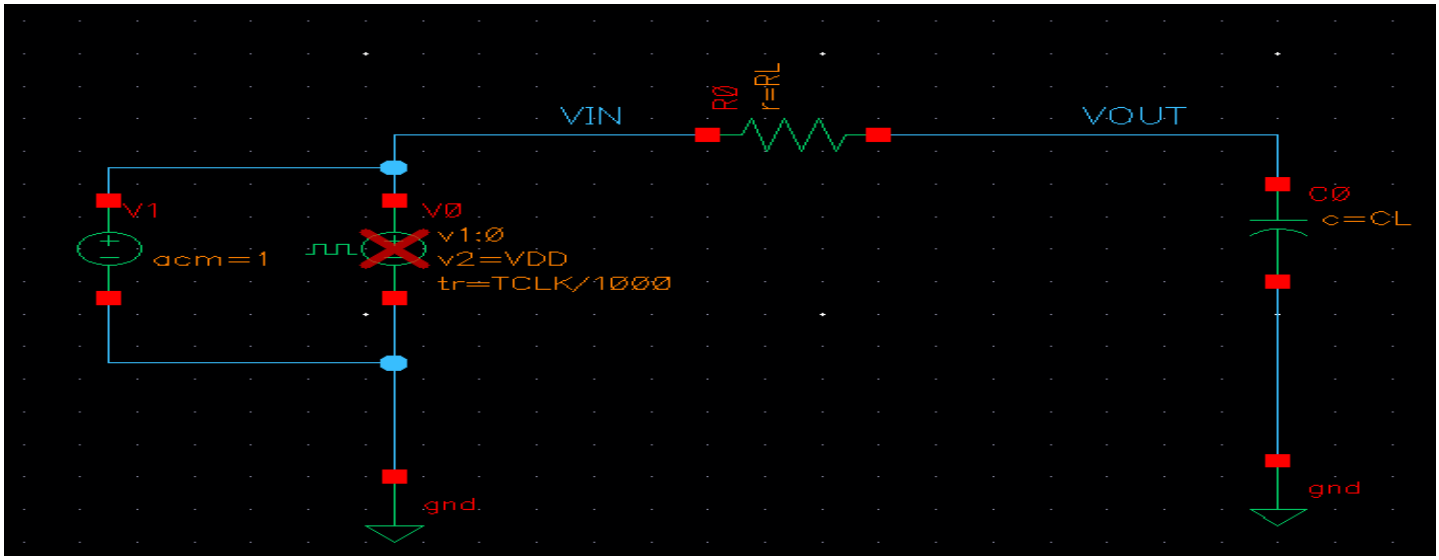


Comment on the Results:

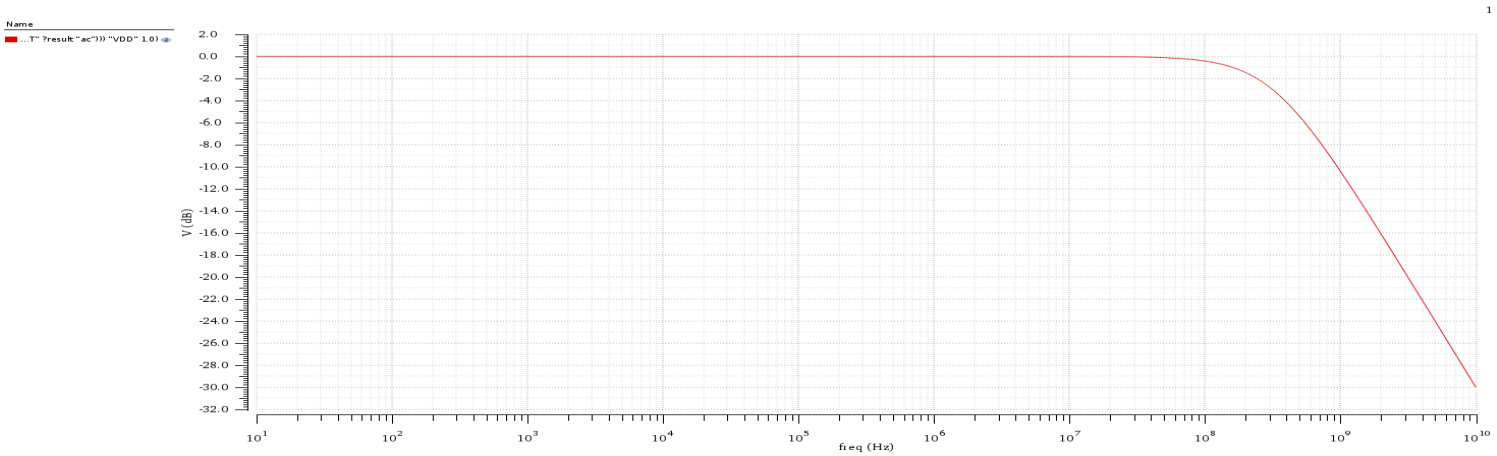
A parametric sweep was performed by varying the resistor value from **1 kΩ to 5 kΩ**, while keeping the capacitor constant at **0.5 pF**. As expected, the output waveform became increasingly slower with higher resistance. This is because the time constant τ=RC increases linearly with R. Consequently, the rise and fall times of the output waveform increased, and the filter took longer to respond to changes in the input. This behavior confirms the direct proportionality between R and the filter's time constant, as predicted analytically.

The rise and fall time expressions did not give errors during the parametric sweep because the output signal always had valid transitions between 10% and 90% levels, regardless of the resistor value. Cadence applies the expressions to each sweep case separately, so the measurements remain valid across all simulations.

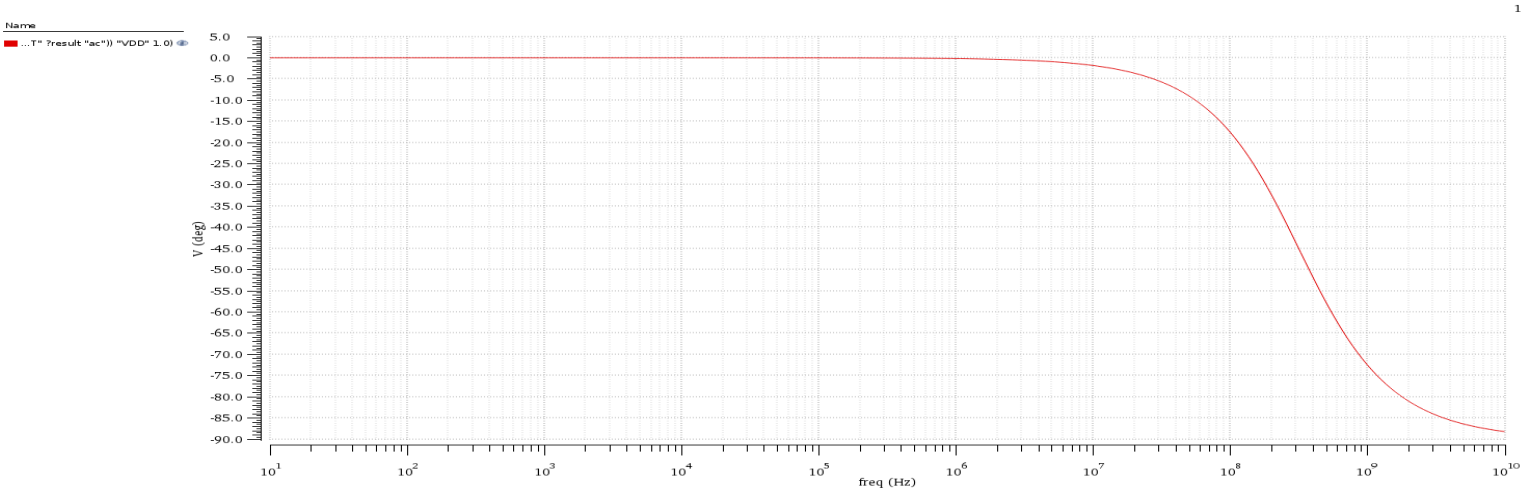
2. AC Analysis



Bode Plot (Mag in db):



Phase:




```
phase(v("/VOUT" ?result "ac"))
```

```
dB20(mag(v("/VOUT" ?result "ac")))
```

DC gain and 3dB bandwidth:

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_LABS:lpf_tb:1	/VOUT				
ITI_LABS:lpf_tb:1	/VIN				
ITI_LABS:lpf_tb:1	dB20(mag(v("/VOUT" ?result ...				
ITI_LABS:lpf_tb:1	Ao	1			
ITI_LABS:lpf_tb:1	Bandwidth	317.7M			

```
bandwidth(mag(v("/VOUT" ?result "ac")) 3 "low" )
```

```
ymax(mag(v("/VOUT" ?result "ac")))
```

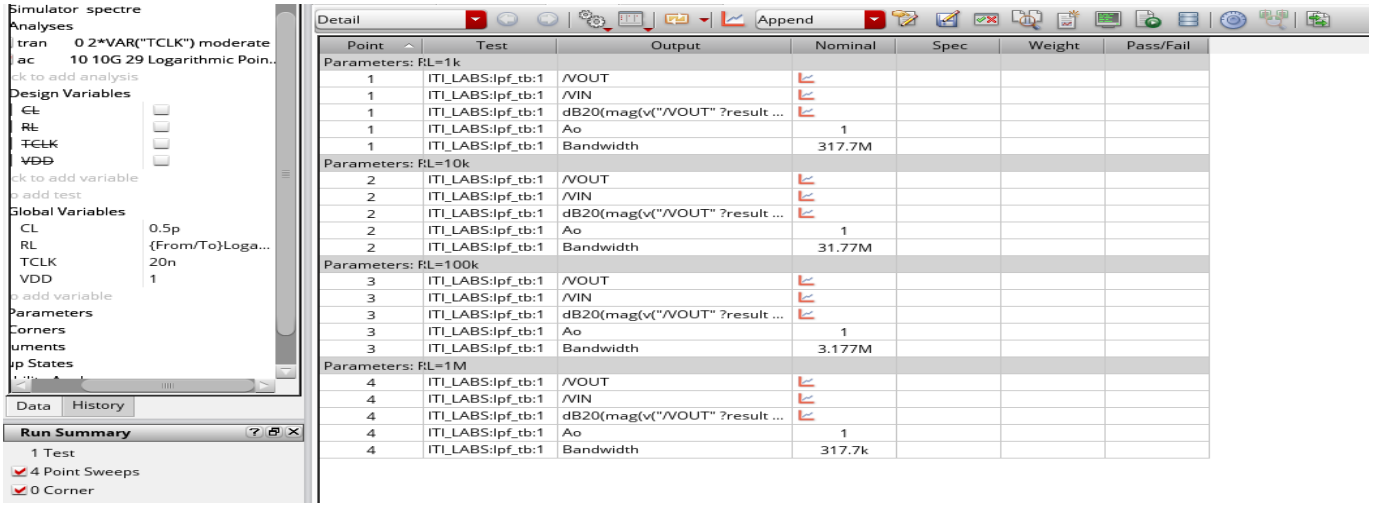
```
dB20(mag(v("/VOUT" ?result "ac")))
```

Compare simulation with analytical results:

Hand analysis: τ= RC = 1kΩ×0.5pF =0.5ns ⟶ $F_C = \frac{1}{2\pi\tau} = 318.34$ MHZ

	Simulation Results	Hand Analysis
Bandwidth	317.7 MHz	318.34 MHz

parametric sweep for $R = 1,10,100,1000k\Omega$



Comment on the Results:

As the resistor value increased from 1 kΩ to 1 MΩ, the bandwidth steadily decreased. This behavior is expected, as higher resistance slows the filter's response, reducing its ability to pass higher frequencies where $F_C = \frac{1}{2\pi RC}$

Part 2: MOSFET Characteristics

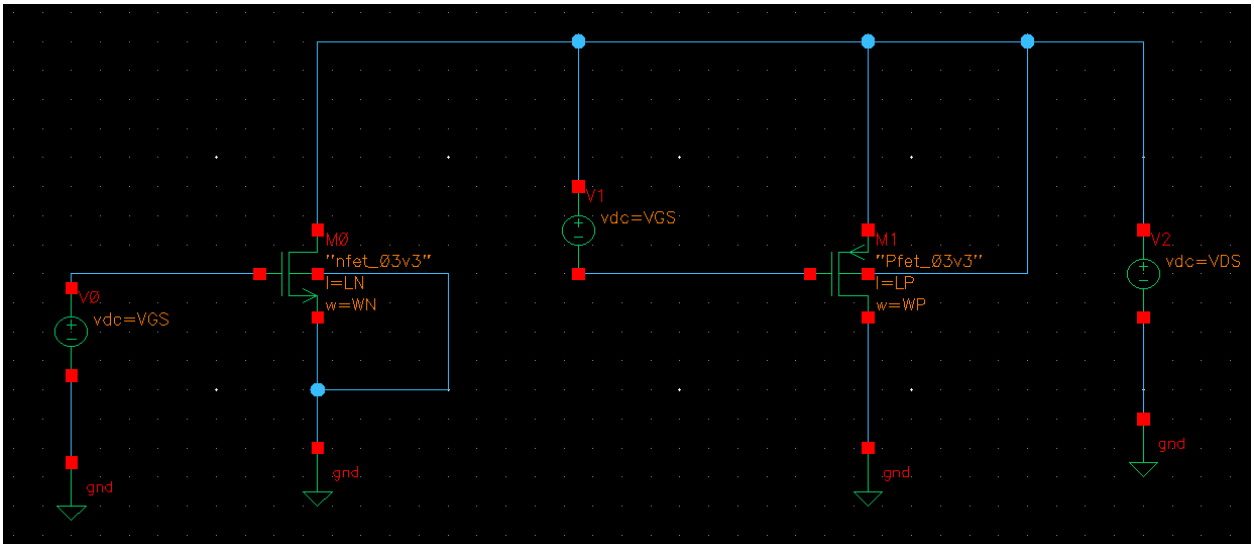
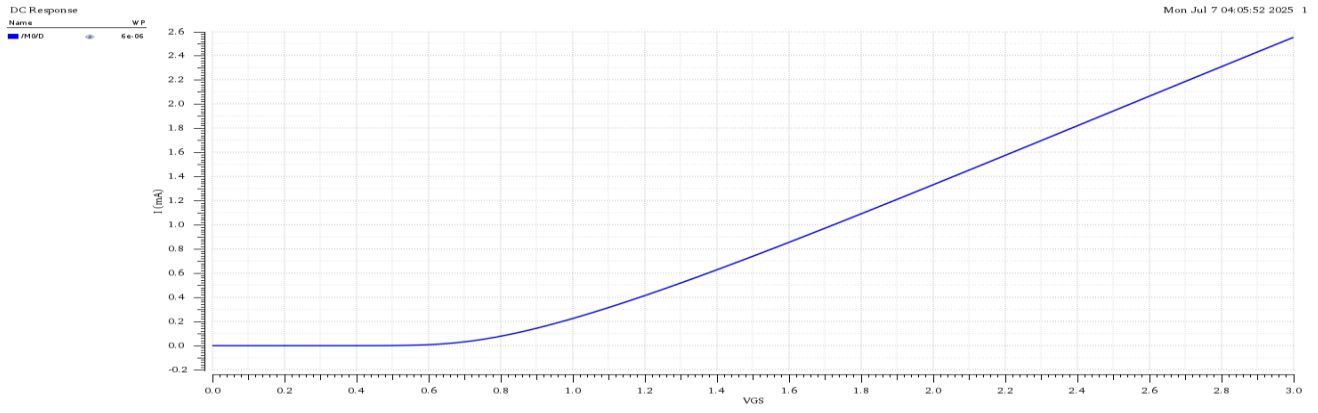


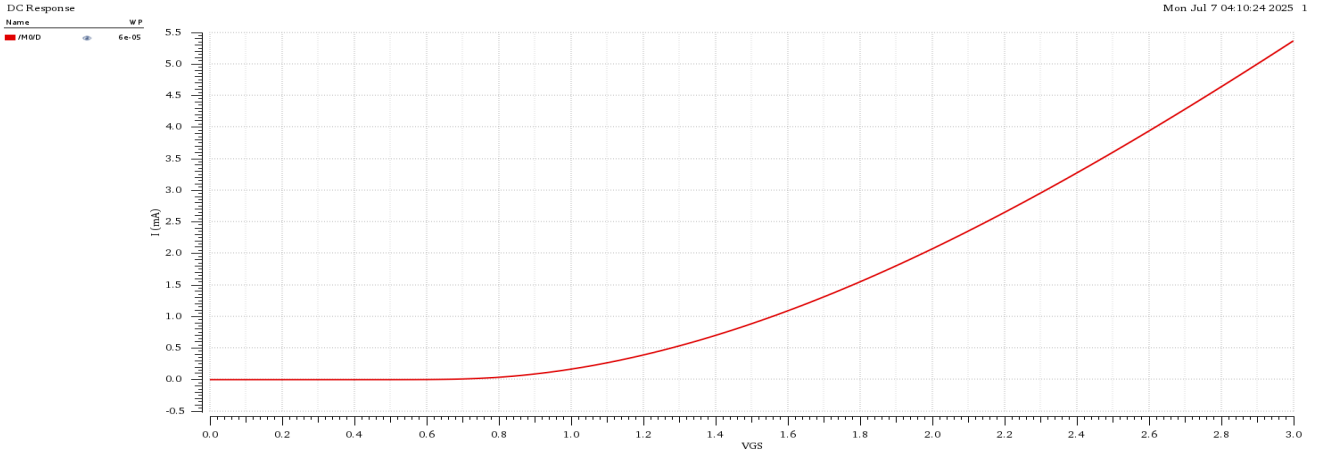
Figure 5:schematic

1. ID vs VGS

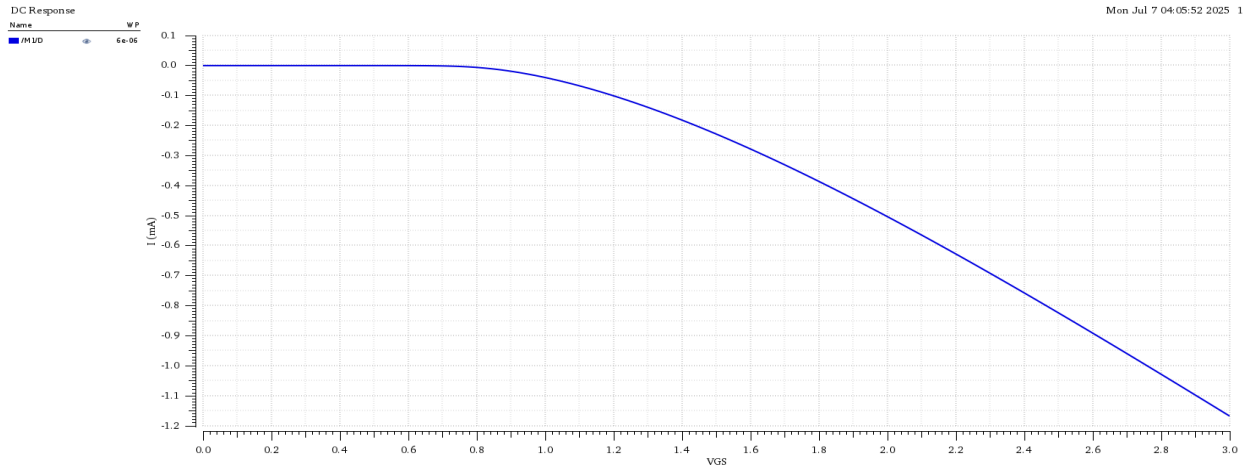
- NMOS short channel:



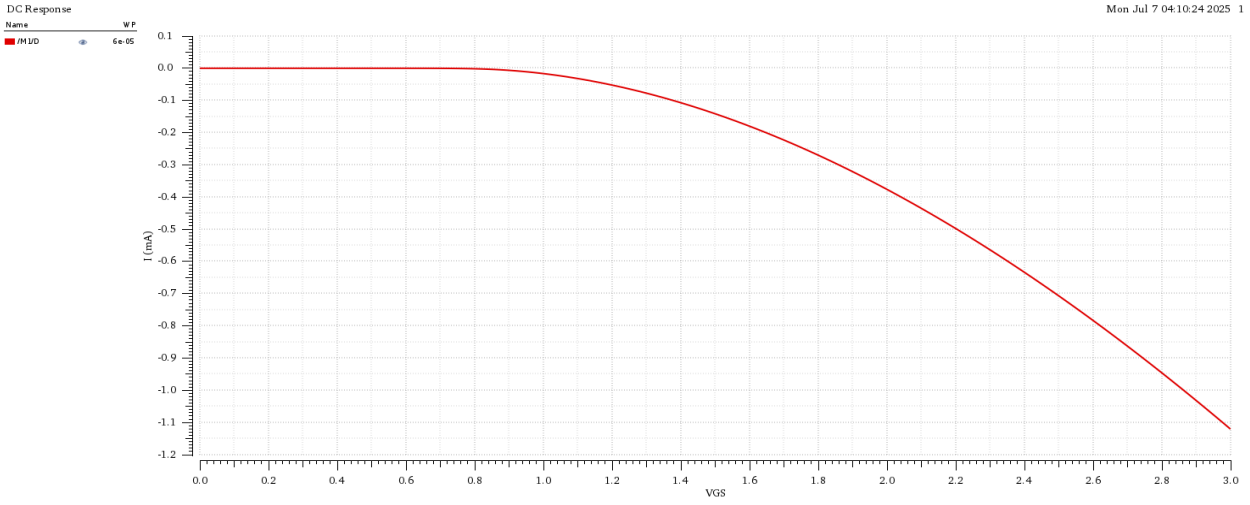
- NMOS long channel:



- PMOS short channel:



- PMOS long channel:



Comment on the differences between short channel and long channel:

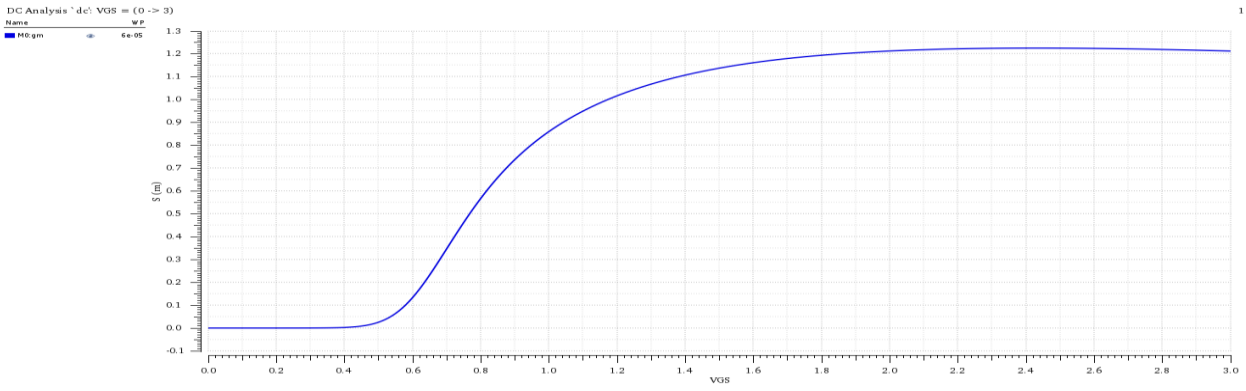
- Long-channel MOSFETs exhibit higher drain current compared to short-channel devices when using the same W/L ratio. This is due to reduced short-channel effects and more ideal carrier transport in long-channel devices.
- In the saturation region, long-channel devices follow the ideal quadratic $I_D \propto$(VGS−Vth)^2 behavior. In contrast, short-channel devices show a more linear I_D response due to velocity saturation and other short-channel effects.
- Ratio of currents of NMOS $\frac{I_{Long}}{I_{Short}} = \frac{5.361}{2.553} = 2.1$ (from table for current on cadence)

Comment on the differences between NMOS and PMOS:

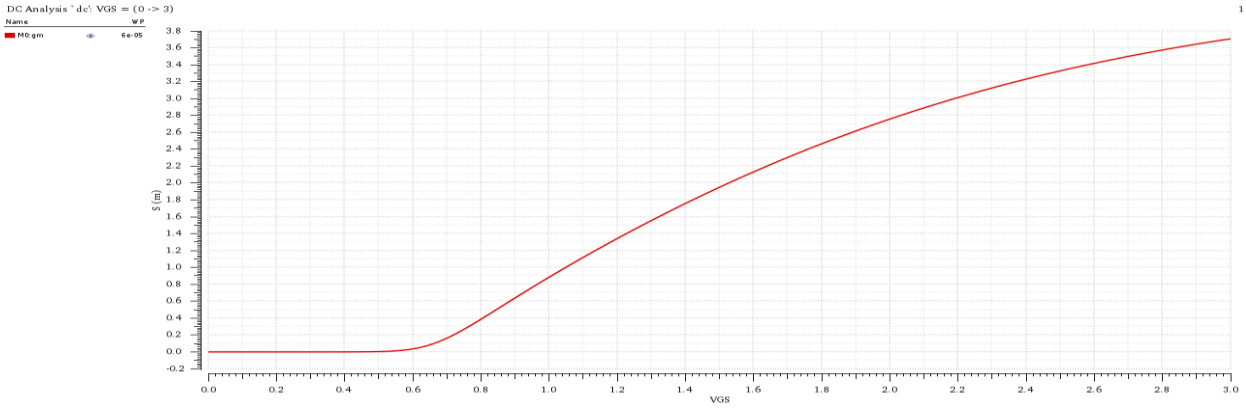
- NMOS is more affected by short-channel effects, such as velocity saturation and threshold voltage variation, making it more sensitive to scaling than PMOS.
- NMOS has higher current than PMOS due to the higher electron mobility compared to hole mobility.
- Ratio of currents of long channel $\frac{I_{Nmos}}{I_{Pmos}} = \frac{5.361}{1.119} = 4.8$ (from table for current on cadence)

2. g_m vs VGS :

- NMOS short channel:



- NMOS long channel:

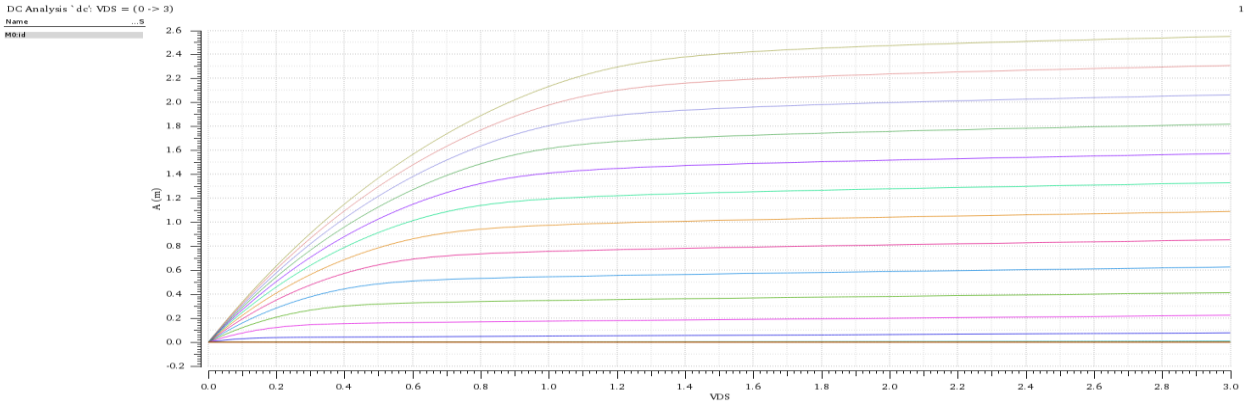


Comment on the Differences Between Short-Channel and Long-Channel Devices:

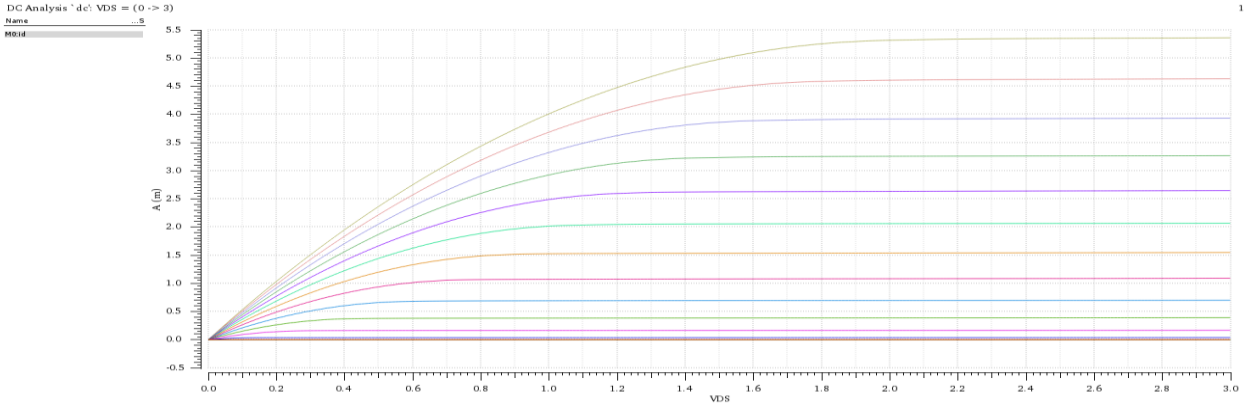
- Short-channel devices do not exhibit a purely quadratic increase in g_m, as carrier velocity saturates under high electric fields, leading to early saturation of transconductance.
- In contrast, long-channel devices show a more gradual and extended increase in g_m, following the classical quadratic dependence of MOSFETs in the saturation region.
- For short-channel devices, g_m saturates earlier, limiting their gain and linearity.
- Long-channel devices maintain increasing $g_m$over a wider range of V_{GS}offering better analog performance and linearity.

3. ID vs VDS

- NMOS short channel:



- NMOS long channel:



Comment on the differences between short channel and long channel results:

- *The long-channel NMOS transistor exhibits a higher current.*
  • This occurs because of short-channel effects, such as velocity saturation, decrease the carriers' effective mobility, which in turn limits the current.
  • The long-channel device's current behavior closely follows the classic quadratic MOSFET current model.
- *On the other hand The short-channel NMOS transistor shows a steeper slope in the saturation region.*
  This happens because the stronger electric field near the drain in short-channel devices effectively shortens the channel length, causing the drain current (ID) to continue increasing even after the device enters saturation.