Analog IC Design – Xschem and Master Micro Tools Lab
06
Differential Amplifier

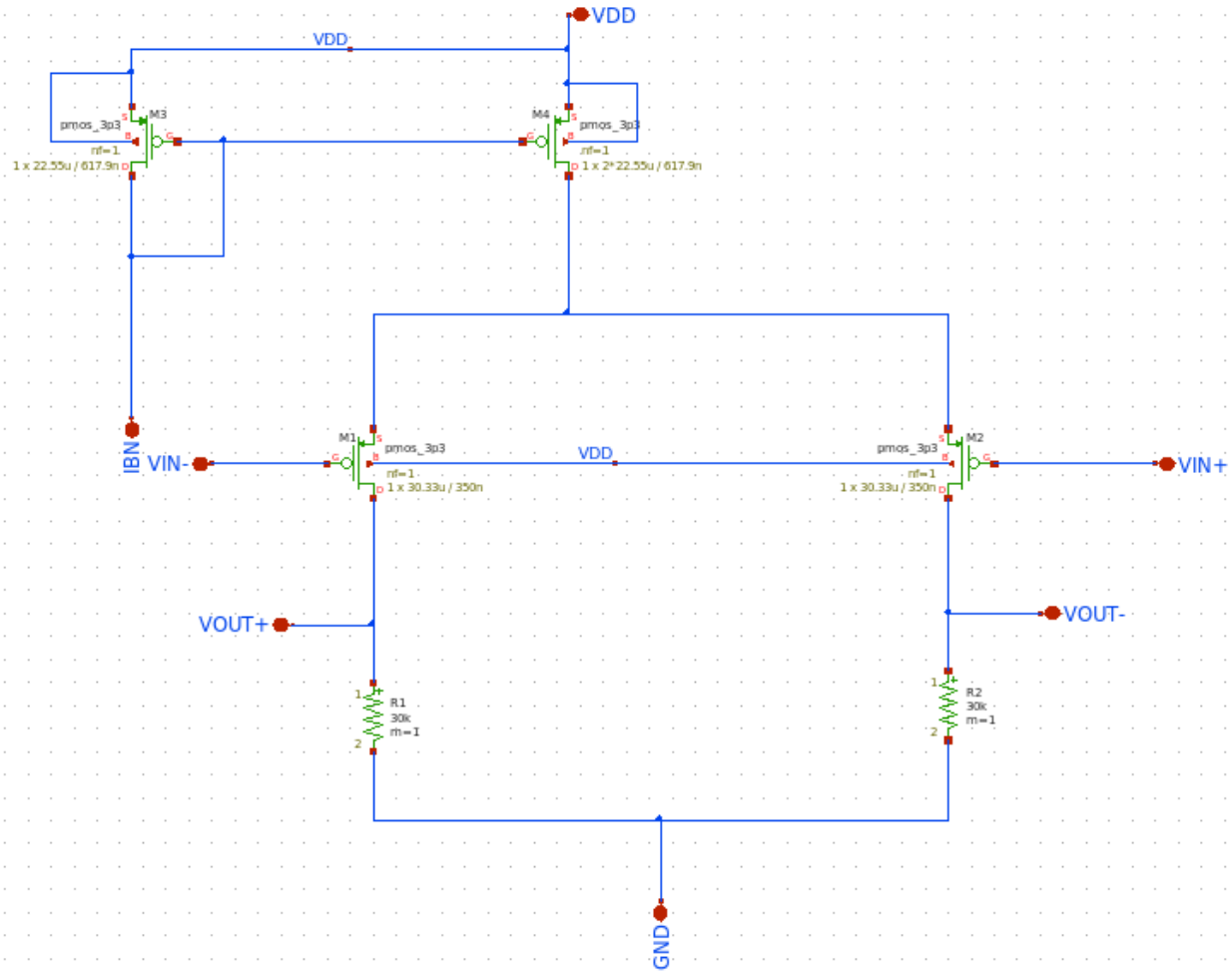
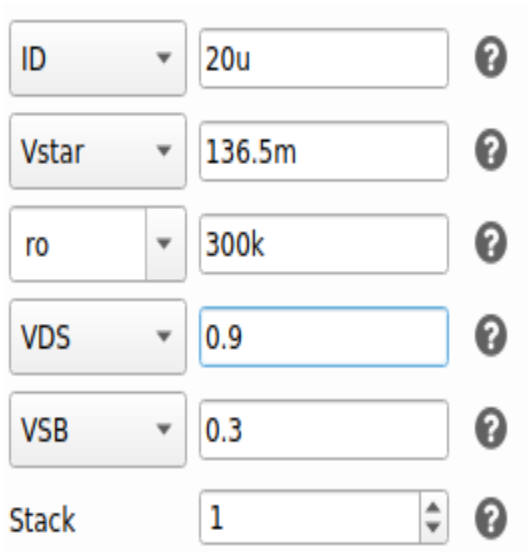


Figure :schematic

- RD = $\frac{\text{VOUT}}{\text{ID}} = \frac{\text{VDD}}{3*\text{ID}} = \frac{1.8}{3\times20\times10\text{e-}06} = 30\ \text{K}\Omega$

- V* = $\frac{1.82V_{RD}}{|A_V|}$ = 136.5 mV

SIZING OF M1, M2



	Name	TT-27.0
1	ID	20u
2	IG	N/A
3	L	350n
4	W	30.33u
5	VGS	940.4m
6	VDS	900m
7	VSB	300m
8	gm/ID	14.28
9	Vstar	140.1m

calculating the required CM input level

- v_{icm} (required) = VDD-VDS4-VGS2=0.56 V

SIZING OF M3, M4

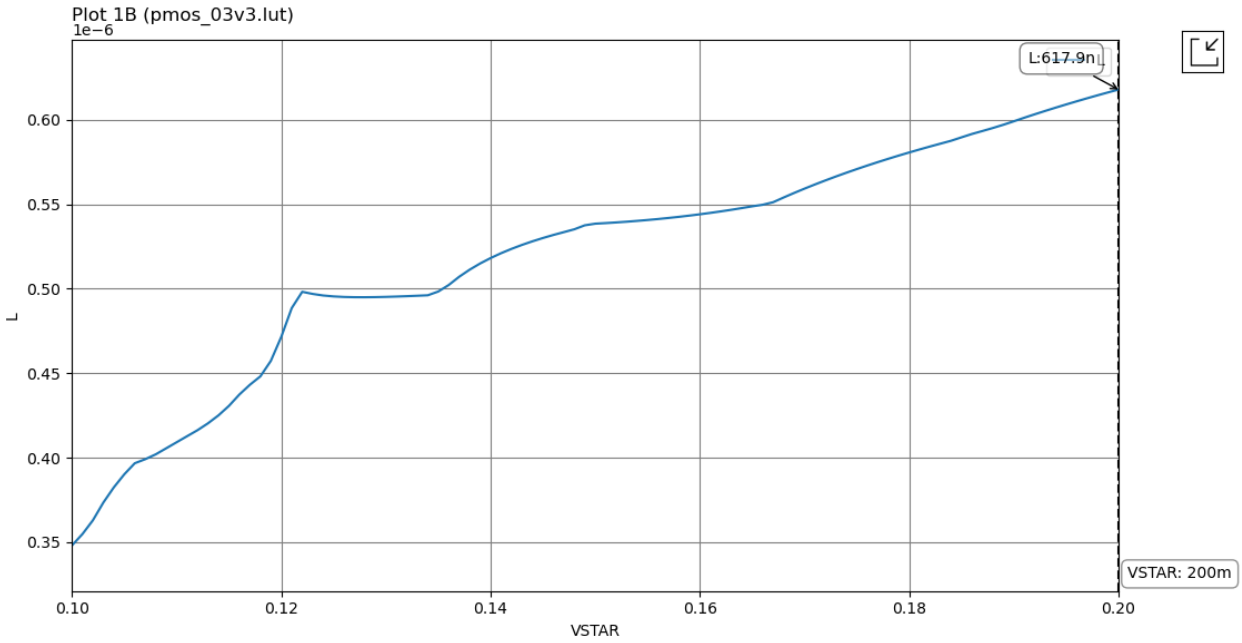


*Figure 1: L VS V**

- L3=L4=617.9 n

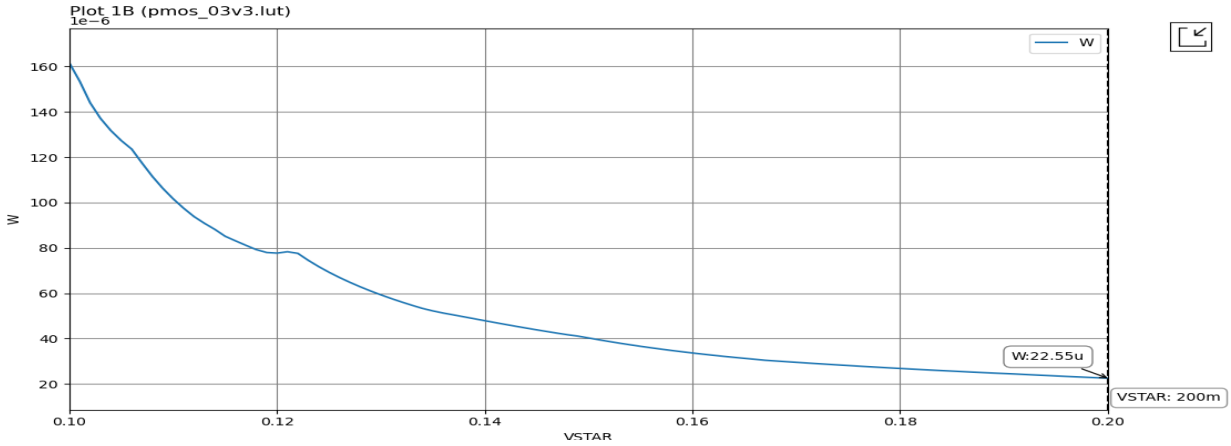


*Figure 2: W VS V**

w4=2×w3=45.1u

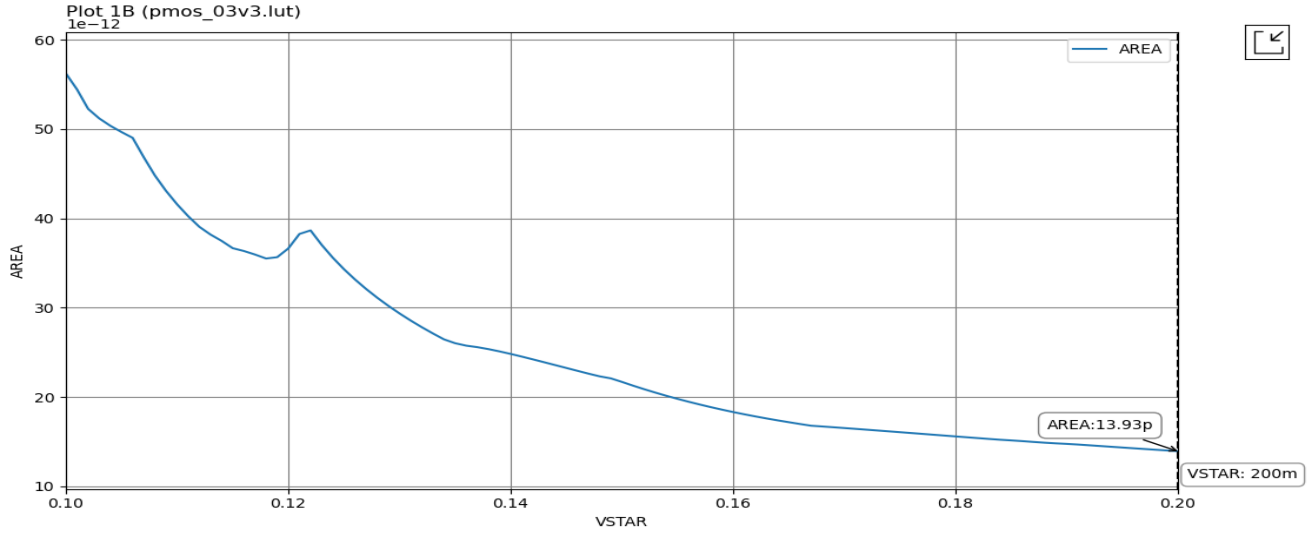


*Figure 3: area VS V**

from ADT VDSat= 165.3 mV

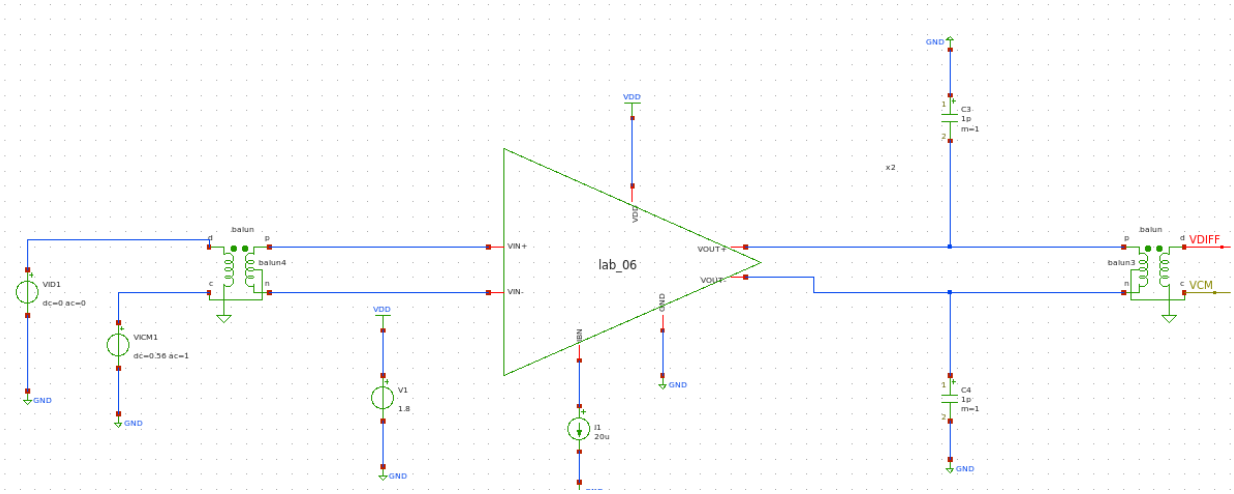
v_{icm} (MIN)= VOUT-VTH1 = 0.6-0.87= -0.27 V

v_{icm} (MAX) = VDD-VDSat4-VGS2 =1.8-0.94-165.3=0.6947 V

So

$$-0.27 < v_{icm} < 0.6947$$

Part 2: Differential Amplifier Simulation:



1)OP simulation:

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm4.m0           m.x1.xm3.m0           m.x1.xm2.m0
     model           pmos_3p3.13           pmos_3p3.13           pmos_3p3.12
        id           3.84807e-05                  2e-05           1.92404e-05
        gm           0.000393227          0.000205061          0.000283025
       gds           4.92826e-06          7.70177e-07          3.08792e-06
       vgs              0.942092             0.942092             0.939237
       vth              0.790303              0.79015             0.874307
       vds               0.30076             0.942091             0.922024
     vdsat              0.161631             0.161741             0.118024

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm1.m0
     model           pmos_3p3.12
        id           1.92404e-05
        gm           0.000283025
       gds           3.08792e-06
       vgs              0.939237
       vth              0.874307
       vds              0.922026
     vdsat              0.118024
```

Figure 4: dc op from simulation

All transistors [M0,M1,M2,M3] Work in saturation, because vds>vdsat

2)Diff small signal ccs:

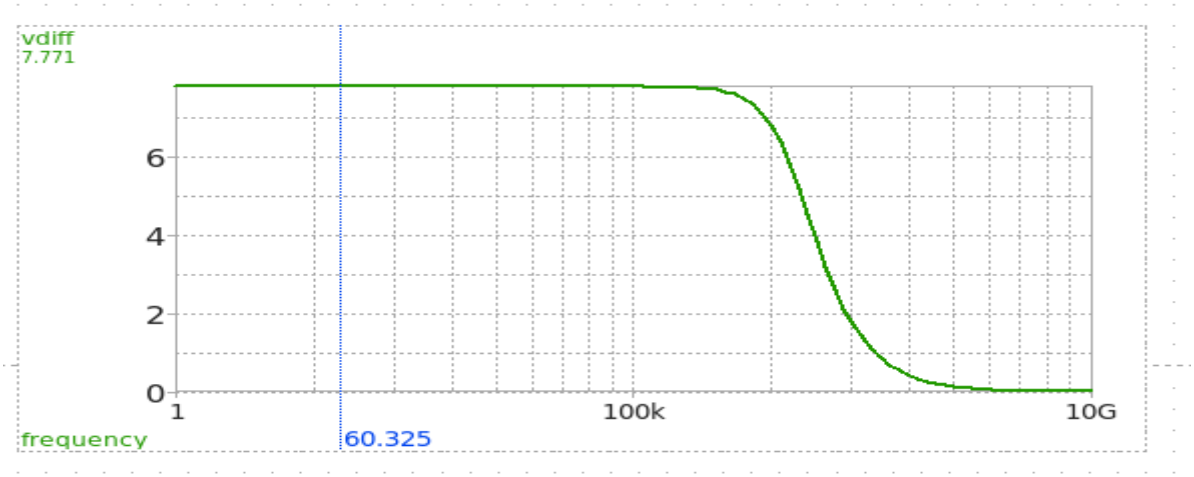


Figure 5:vdiff vs freq (linear scale)

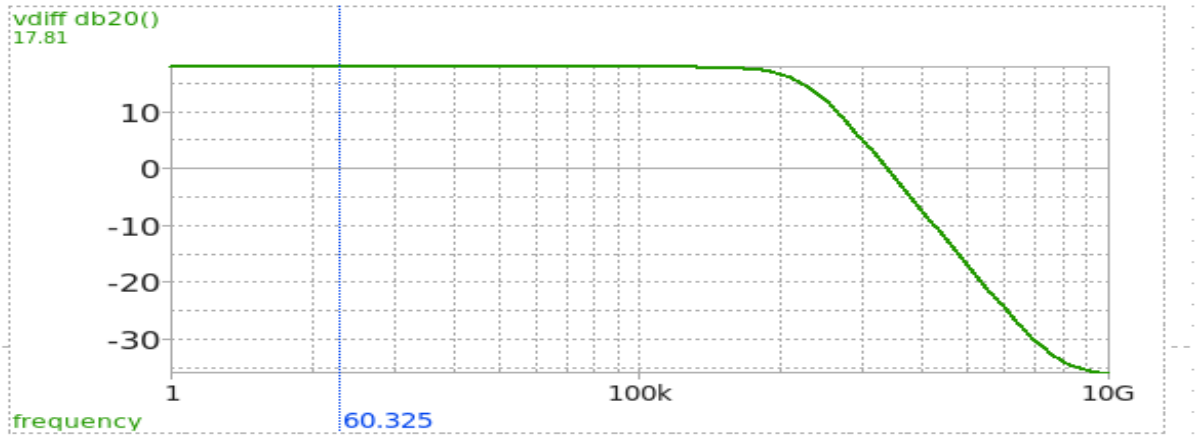


Figure 6: vdiff vs freq (in db)

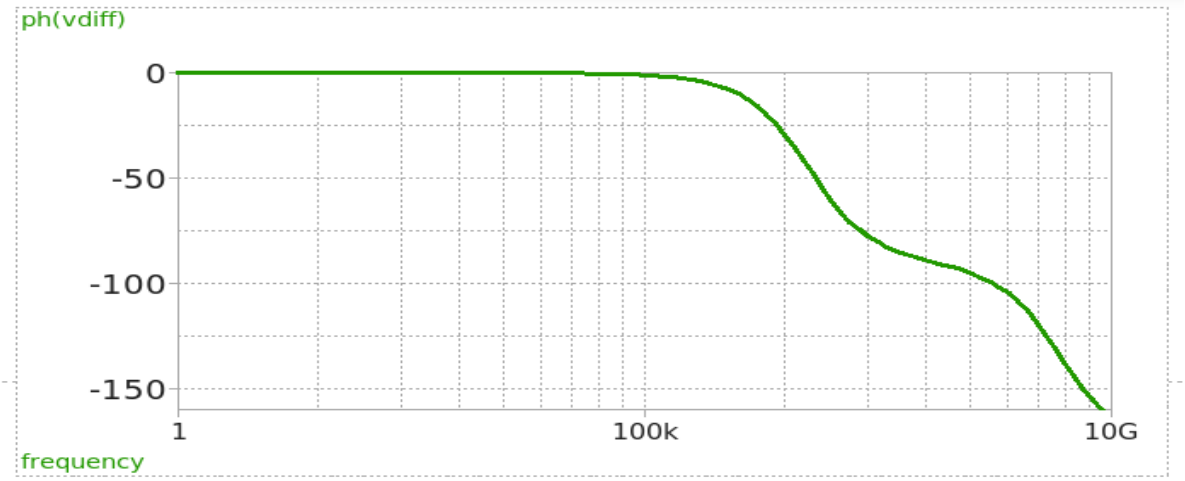


Figure 7: phase(vdiff) vs freq

Simulation:

```
gain_max            =  7.770751e+00 at=  1.000000e+00
bw                  =  5.676726e+06
```

Hand analysis:

Gain = gian of CS = gm (RD//$\frac{1}{g_{ds2}}$) = 7.77087 BW= $\frac{1}{2\pi\times(RD//\frac{1}{g_{ds2}})\times Cl}$ = 5.7966 MHZ

- Compare the DC diff gain and BW with hand analysis in a table.

	GAIN	BW
FROM SIMULATION	7.77	5.78 MHZ
FROM HAND ANALYSIS	7.77	5.79 MHZ

3) CM small signal ccs:

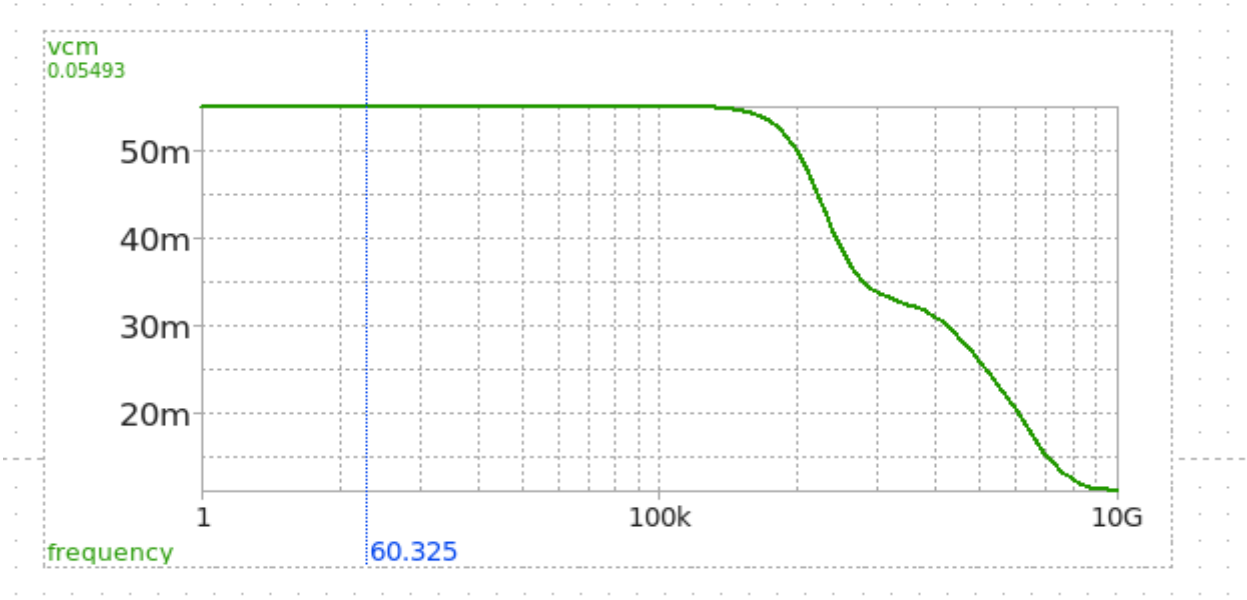


Figure 8: VCM VS freq (linear scale)

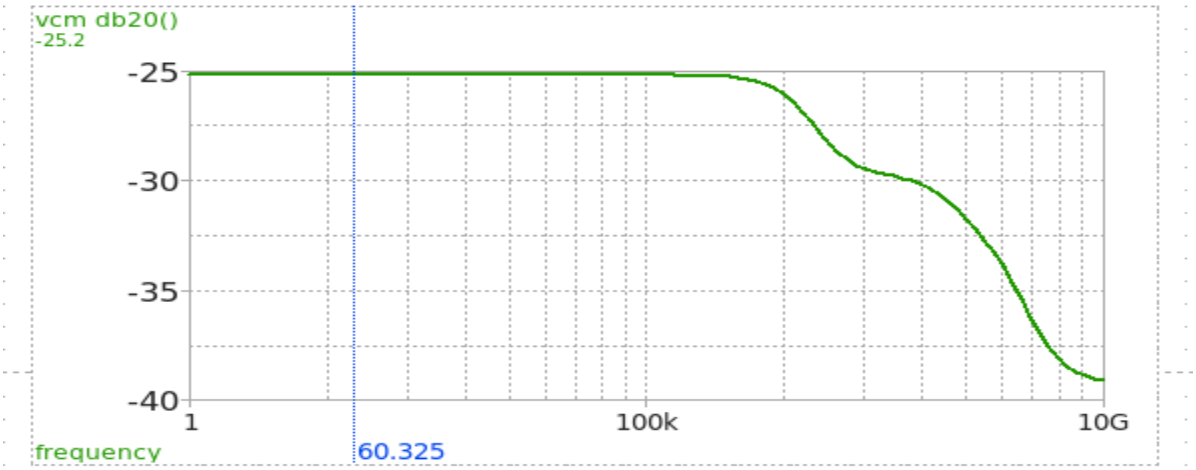


Figure 10: VCM VS ferq (in db)

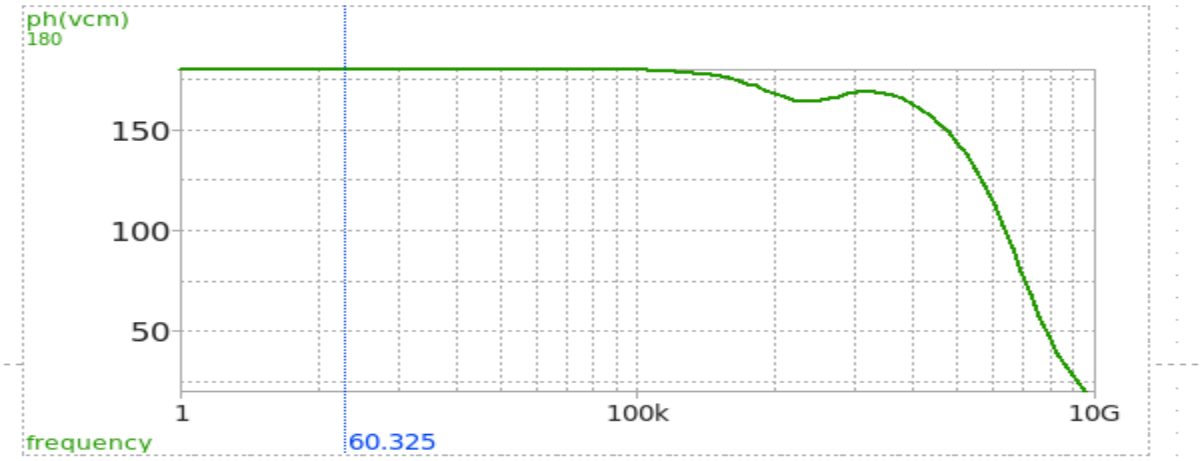


Figure 9: phase (VCM) VS freq

Simulation:

```
cmgain                =  5.493339e-02 at=  1.000000e+00
```

Hand analysis:

Gain = gain of cs degenerated = $\frac{gm_2 \times RD}{1+_{2\times gm_2}\frac{1}{gds_4}} = 7.33*10\text{^}-2$

Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?

	GAIN
FROM SIMULATION	0.0549
FROM HAND ANALYSIS	0.0733

Yes, the DC Common-Mode Gain (Avcm) is less than 1.This is by design, because the tail current source provides degenrated high impedance that rejects common-mode signals .

Justify the variation of Avcm vs frequency.

Avcm decreases with frequency.

At high frequency: gain drops due to CL loading and parasitic effects

Plot Avd/Avcm in dB

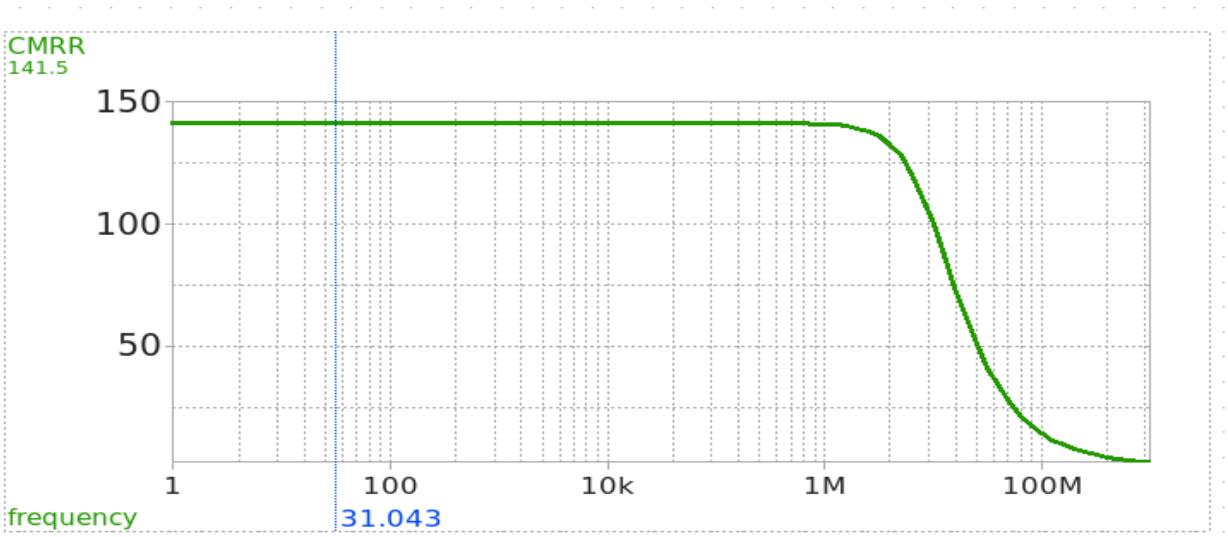


Figure 11: CMRR (linear scale)

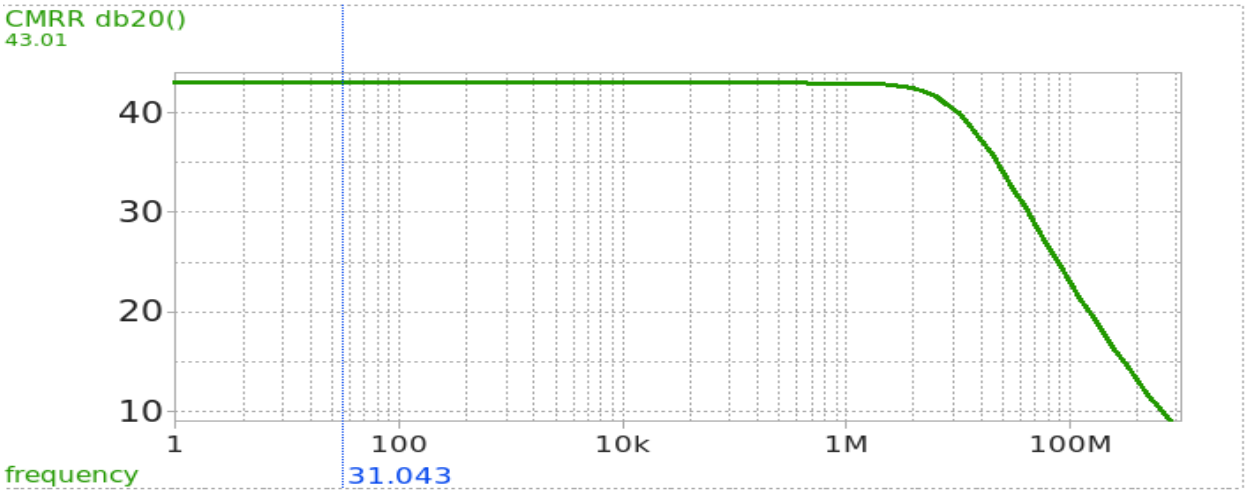


Figure 12: CMRR (IN db)

AS showm from simulation: CMRR = 43.01 db

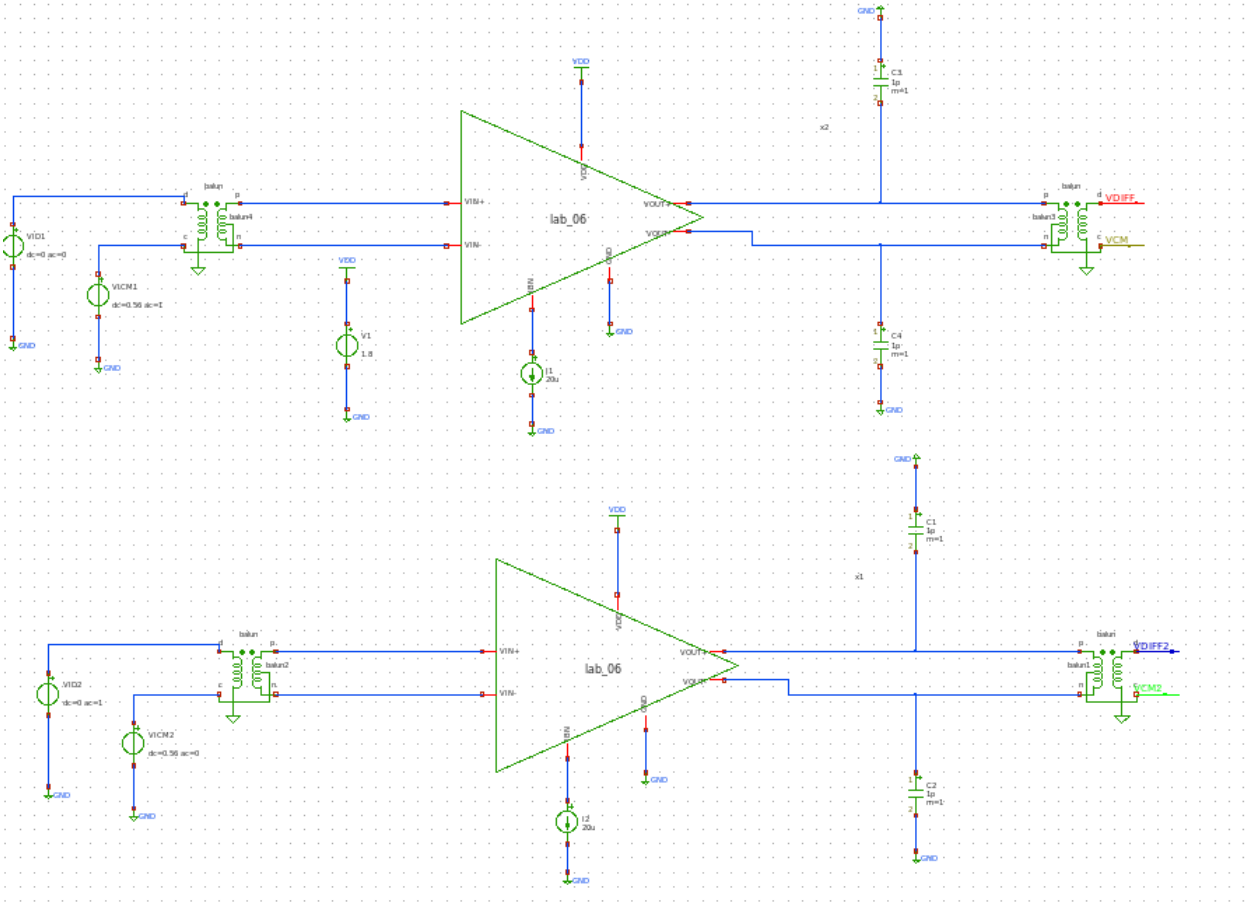
Hand analysis: CMRR = $\frac{A_{diff}}{A_{cm}} = \frac{7.771}{0.5493} = 106 = 40.51db$

	CMRR
FROM SIMULATION	43.01 db
FROM HAND ANALYSIS	40.51 db

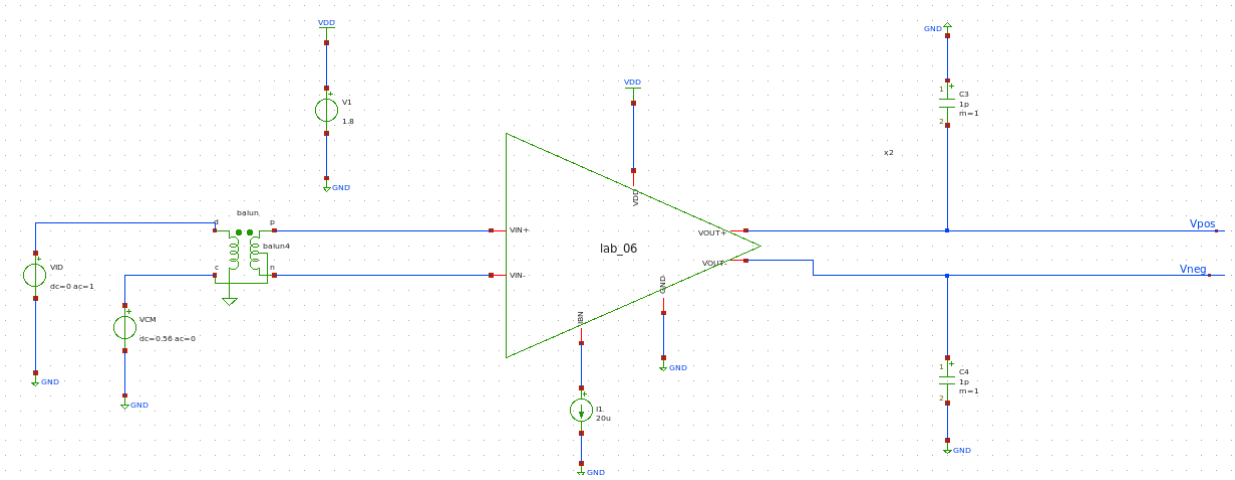
Justify the variation of Avd/Avcm with frequency.

At low frequency, CMRR (Avd/Avcm) is high, because the tail current source provides high impedance (RSS), effectively rejecting common-mode signals.

At high frequency, CMRR decreases because the parasitic capacitance (Cp) at the tail node bypasses RSS, reducing the impedance



4) Diff large signal ccs:



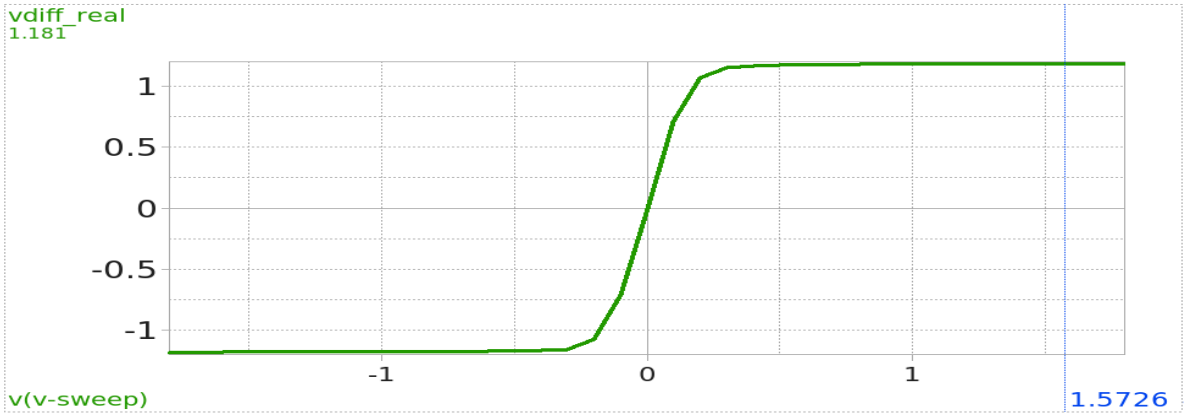


Figure 14:(VODIFF vs VIDIFF) extreme +ve value

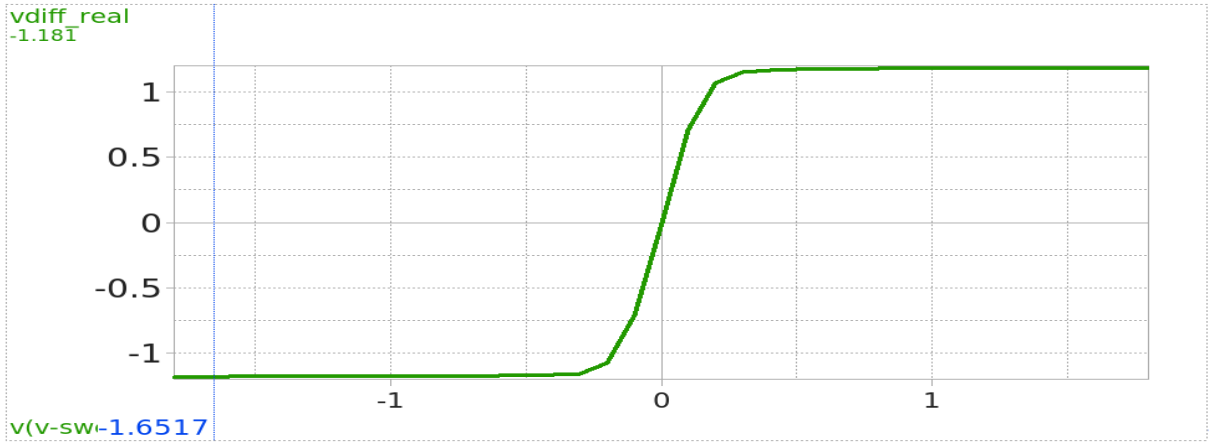


Figure 13:(VODIFF vs VIDIFF) extreme -ve value

Hand analysis

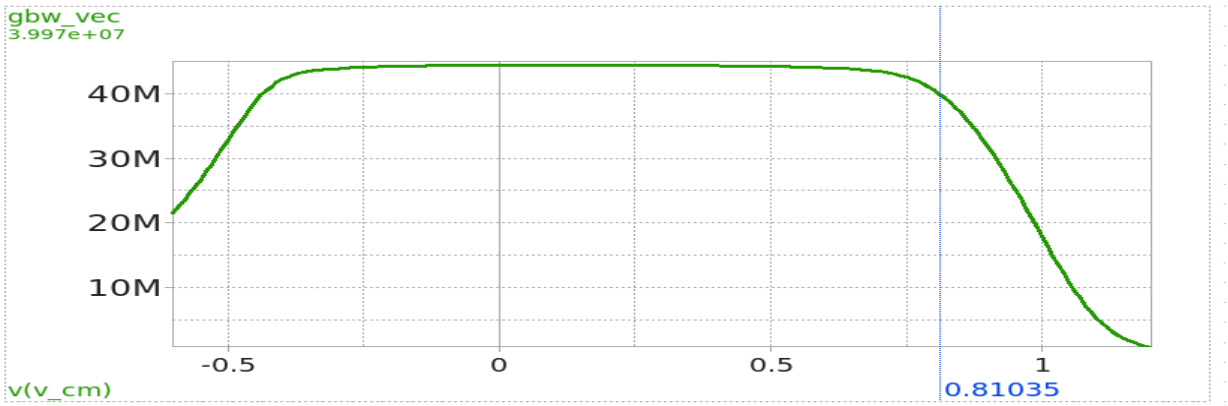
VODIFF (extreme +ve value) = - VODIFF (extreme -ve value) = ISS ×RD = 1.2V

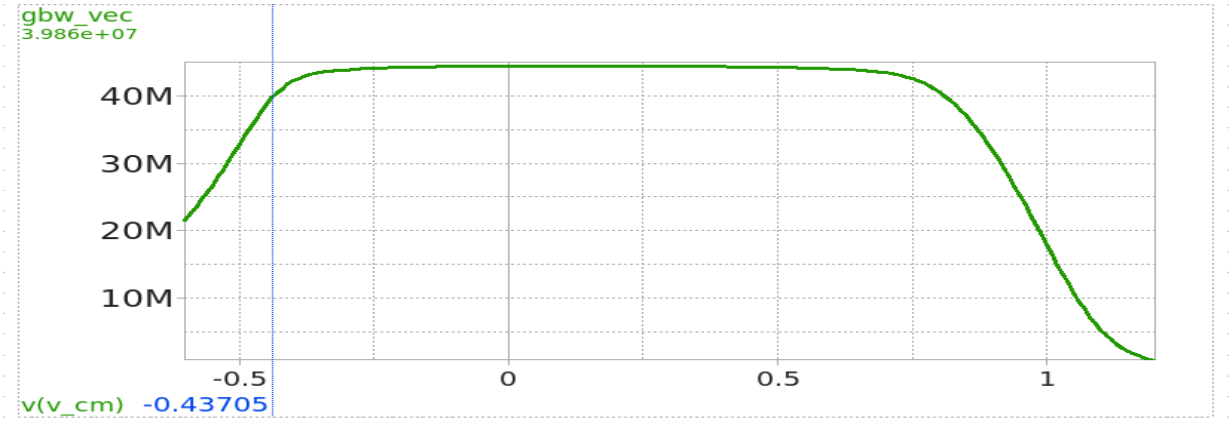
	VODIFF (extreme +ve value)	VODIFF (extreme -ve value)
FROM SIMULATION	1.181	-1.181
FROM HAND ANALYSIS	1.2	-1.2

5) CM large signal ccs (GBW vs Vicm):

GBW_vex_max = 44.43 M

GBW VS VCM within 90% OF MAX GAIN






```
vcm_min = -4.30000e-01
vcm_max = 8.100000e-01
```

	VCM_MIN	VCM_MAX
FROM SIMULATION	-0.43 V	0.81 V
FROM HAND ANALYSIS	-0.27 V	0.6947 V