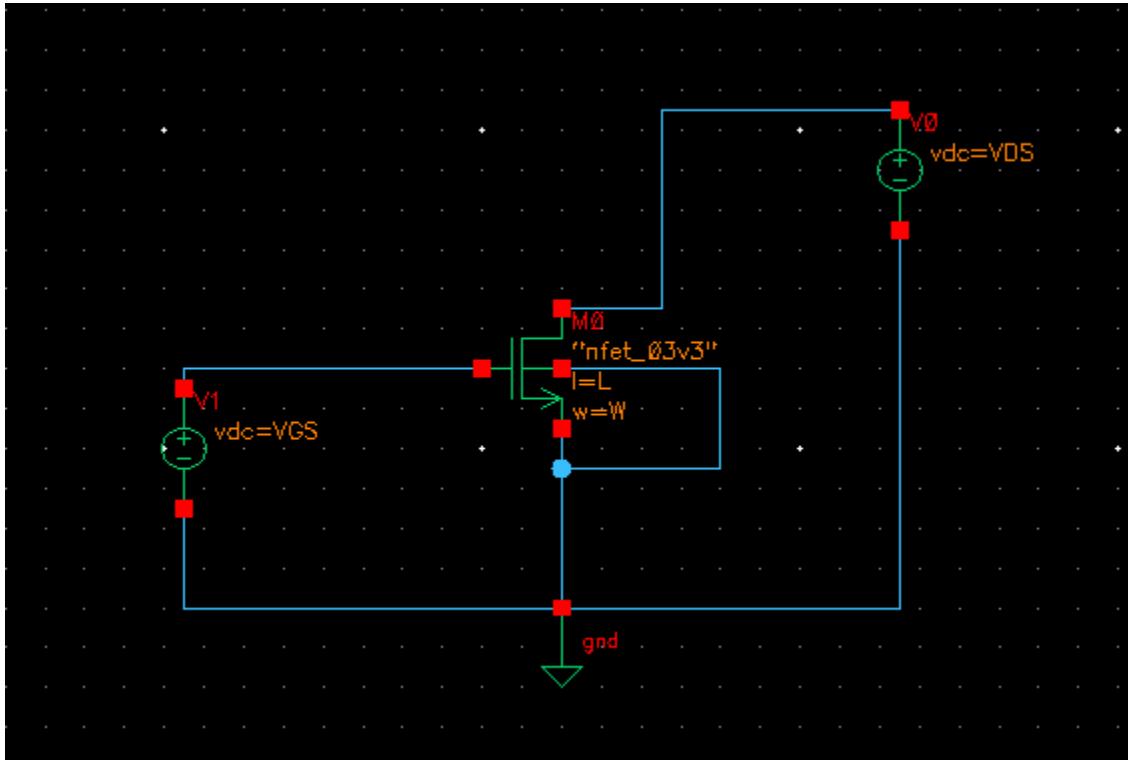


# Analog IC Design – Cadence Tools

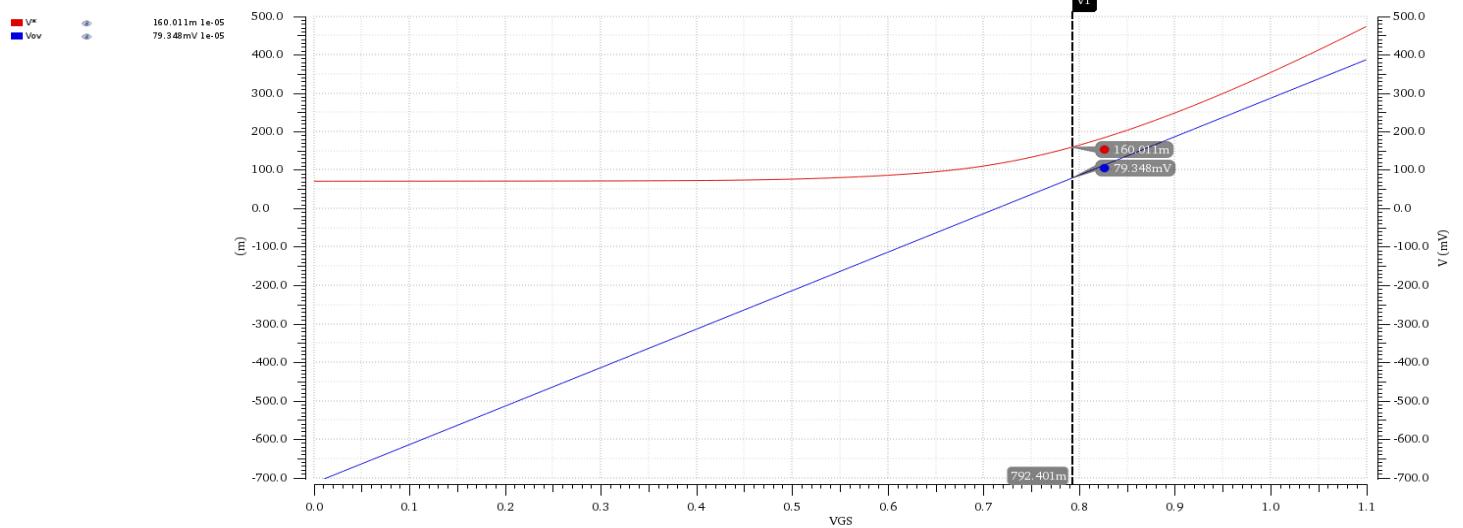
## Lab 03

### Cascode Amplifier

#### Part 1: Sizing Chart:

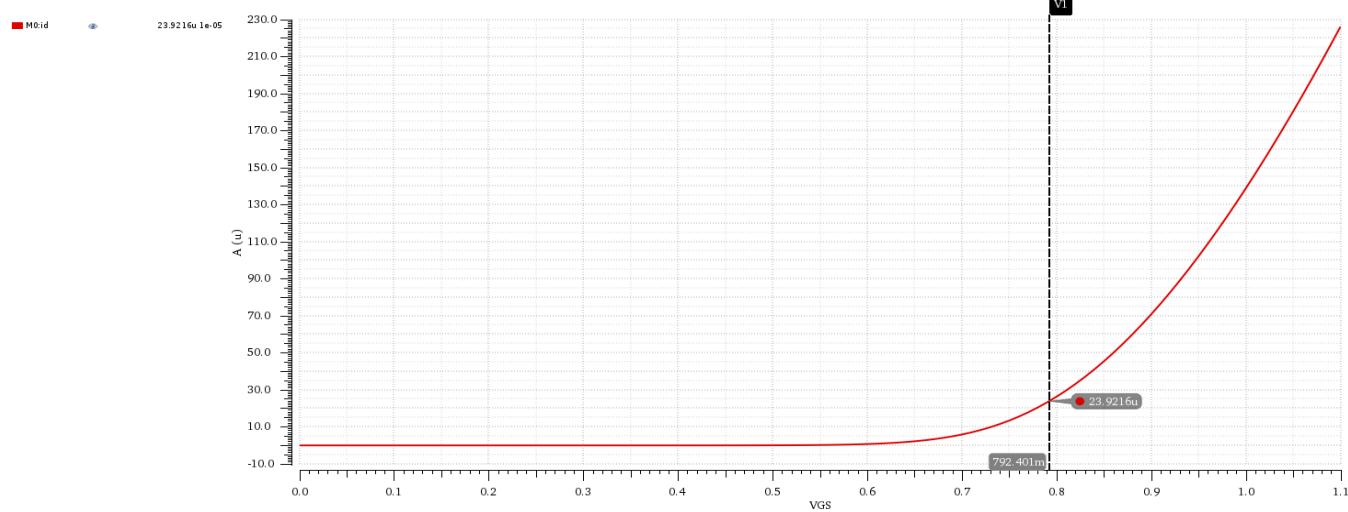


spec	0.18um CMOS
L	0.5um
V*	160mV
Supply	1.8VA
Current consumption	10 $\mu$ A

Figure 1: $V^*$  and  $V_{ov}$  VS  $V_{gs}$ 

DC Analysis `dc': VGS = (0 -&gt; 1.1)

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Figure 2: $I_D$  VS  $V_{gs}$

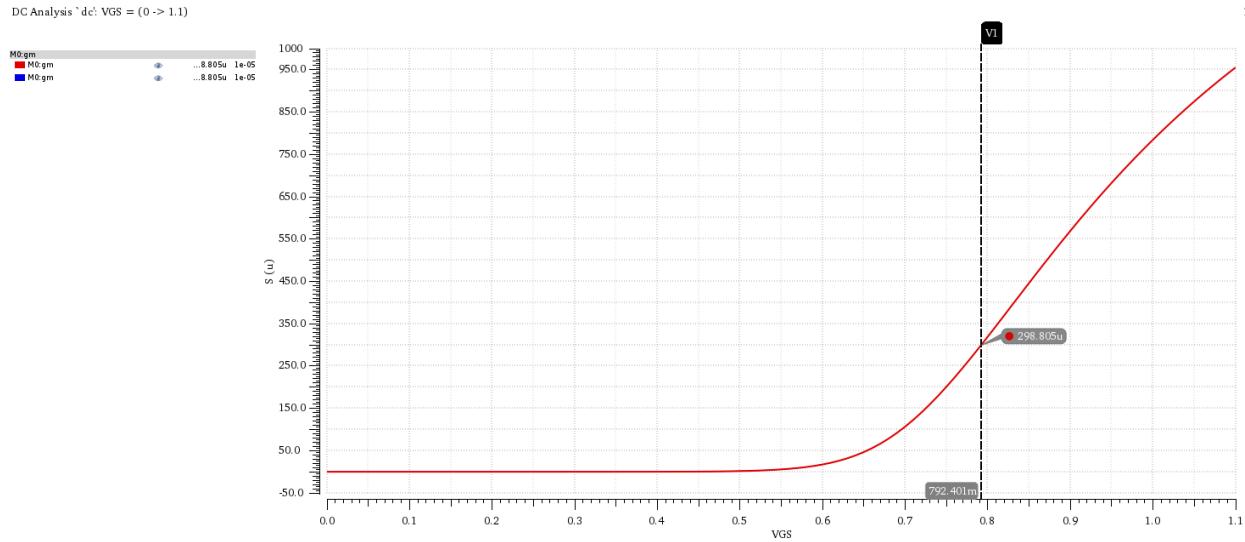


Figure 3: gm VS Vgs

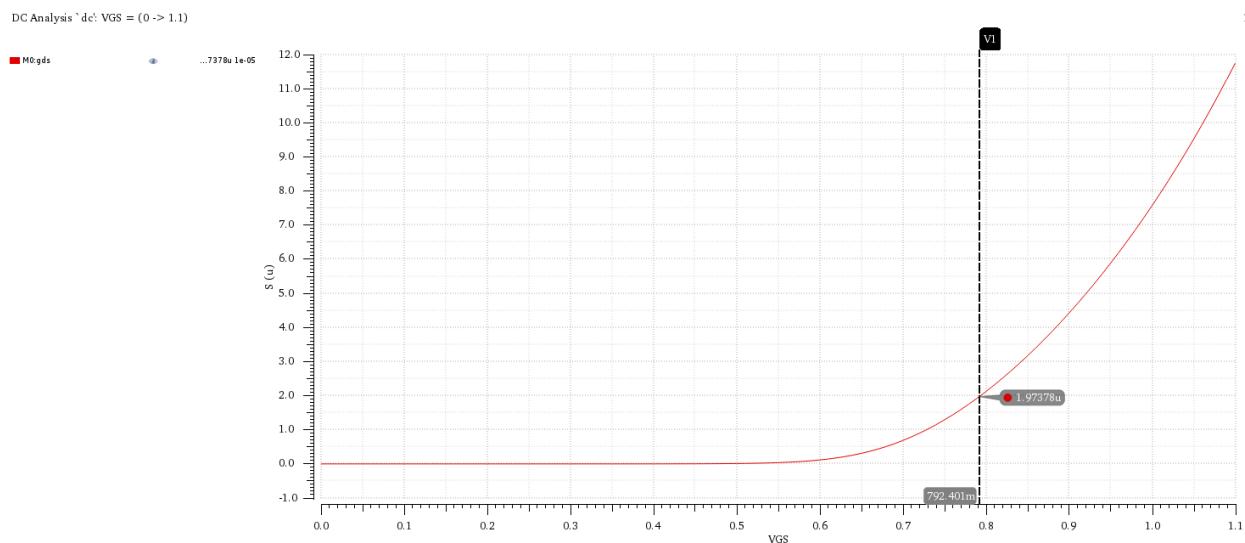


Figure 4:gds VS Vgs

**1-**

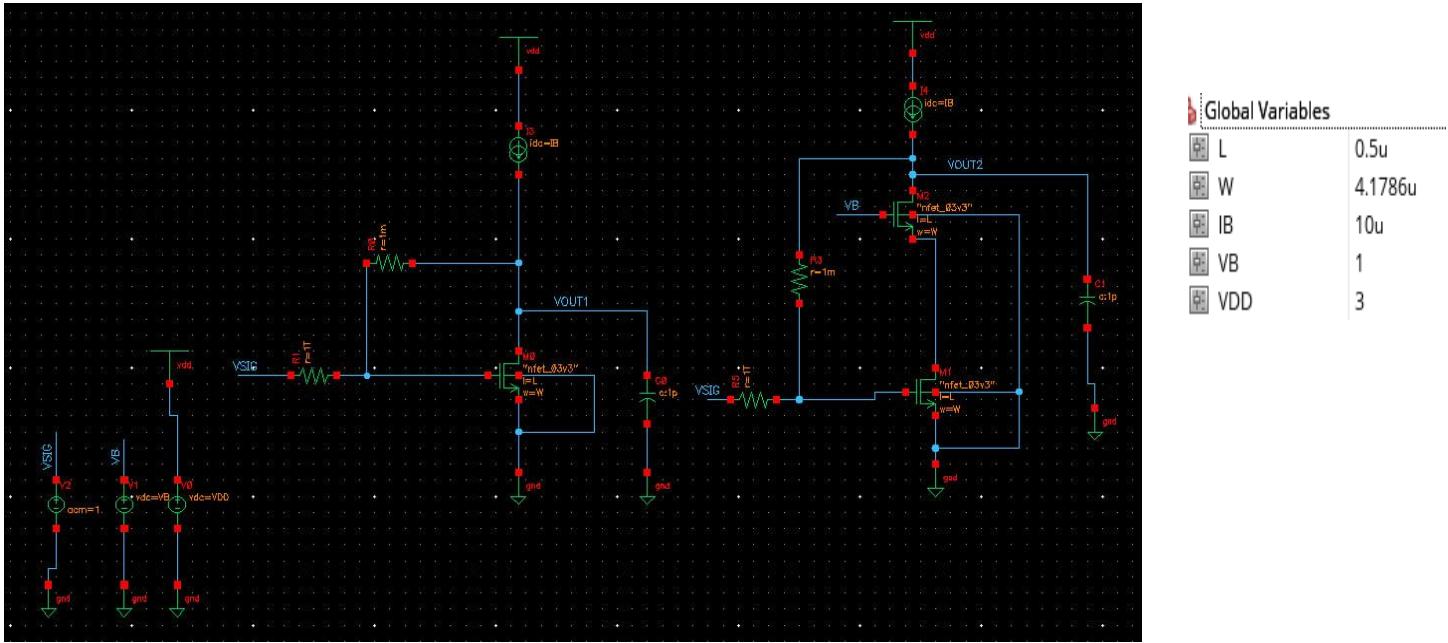
$V^*$	160 mV
$V_{ovQ}$	<b>79.348</b> mV
$V_{GSQ}$	<b>792.401</b> mV
$I_{Dx}$	<b>23.9316</b> $\mu A$
$g_{mx}$	<b>298.805</b> $\mu S$
$g_{dsx}$	1.79378 $\mu S$

**2-**

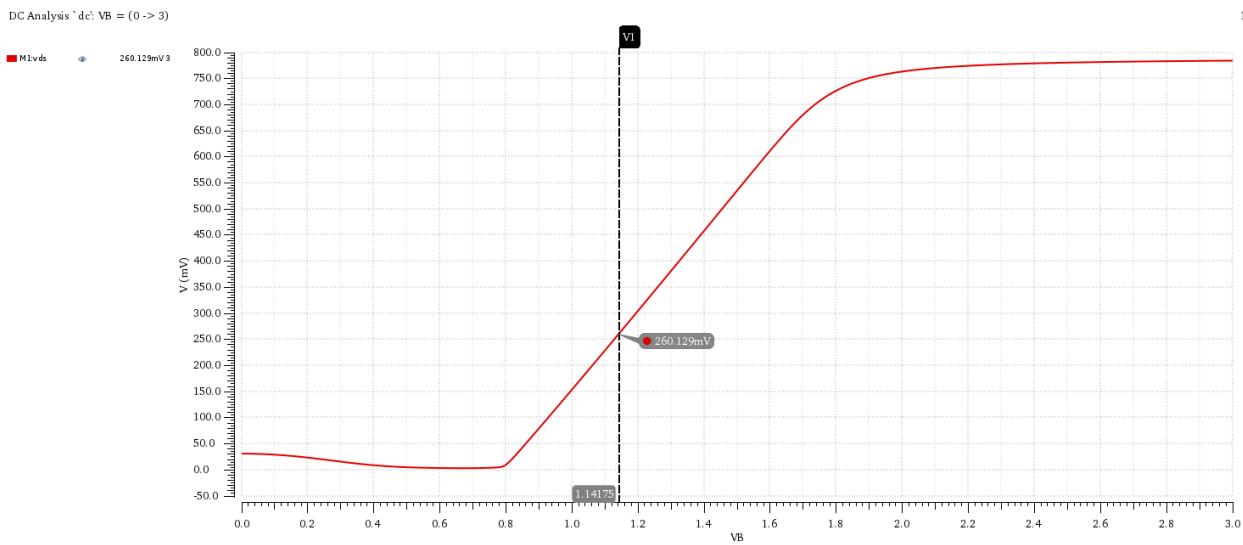
W	Id
<b>10</b> $\mu m$	<b>23.9316</b> $\mu A$
<b>4.1786</b> $\mu m$	<b>10</b> $\mu A$
$g_m$	0.1249 mS
$g_{ds}$	0.7495 $\mu S$
$r_o$	1.3341 M $\Omega$

## PART 2: Cascode for Gain :

## 1. OP Analysis :



*Figure 5:schematic*



*Figure 6:VB VS VDS*

AS SHOWN VB from graph = 1.14175 V

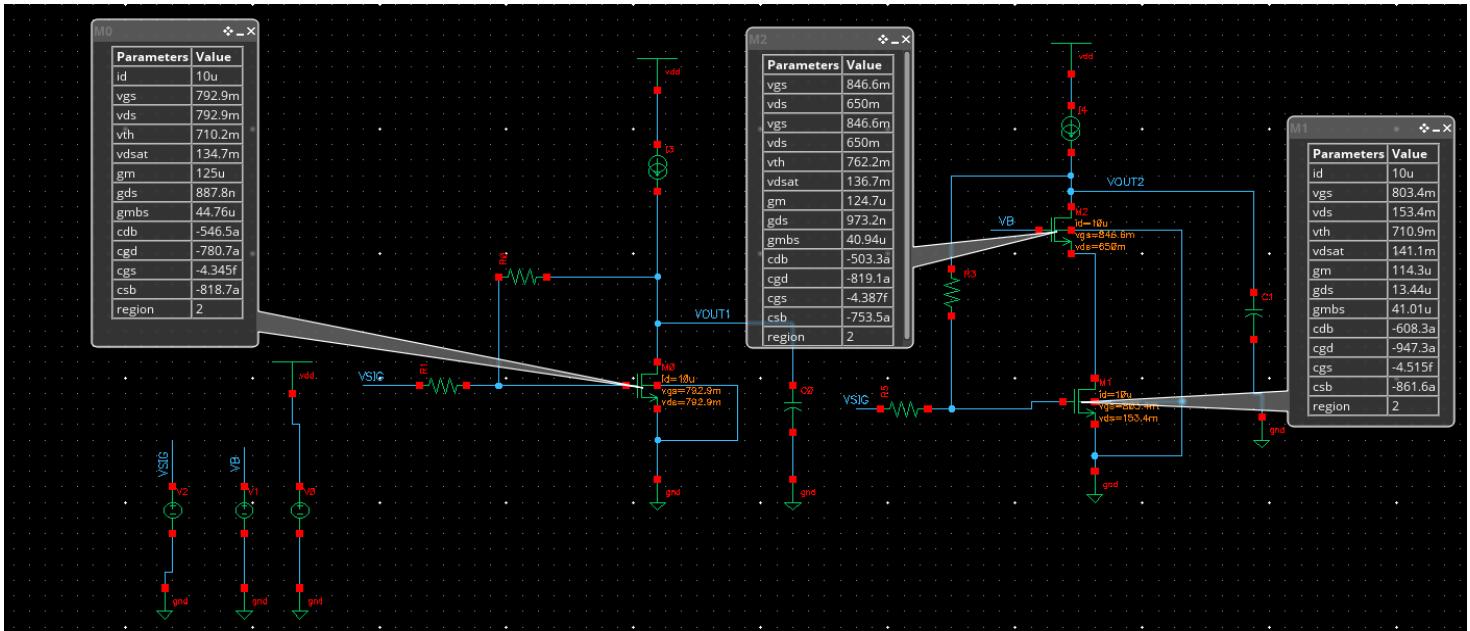


Figure 7: schematic with annotation

As we see all transistors work in **region (2)** “saturation region”

**Do all transistors have the same vth? Why?**

**Transistors have not the same Vth** The threshold voltage (Vth) of a transistor can vary due to several factors, even among transistors of the same type. Here are the key reasons for the observed differences in Vth in your data:

### 1. Process Variations

Manufacturing Tolerances: During fabrication, slight variations in doping concentrations, oxide thickness, or channel length/width can occur, leading to differences in Vth.

Random Dopant Fluctuations (RDF): Random distribution of dopant atoms in the channel can cause localized variations in Vth.

### 2- Body Effect (Substrate Bias)

The threshold voltage depends on the voltage between the source and the substrate (VSB). If the substrate bias varies, Vth will also change

### 3-Drain-Induced Barrier Lowering (DIBL)

At higher drain-to-source voltages (VDS), the electric field from the drain can lower the potential barrier in the channel, effectively reducing Vth. This is more pronounced in short-channel devices.

What is the relation ( $\ll$ ,  $<$ ,  $=$ ,  $>$ ,  $\gg$ ) between gm and gds?

gm $\gg$ gds

What is the relation ( $\ll$ ,  $<$ ,  $=$ ,  $>$ ,  $\gg$ ) between gm and gmb?

gm $>$ gmb

What is the relation ( $\ll$ ,  $<$ ,  $=$ ,  $>$ ,  $\gg$ ) between cgs and cgd?

cgs $>$ cgd

What is the relation ( $\ll$ ,  $<$ ,  $=$ ,  $>$ ,  $\gg$ ) between csb and cdb?

Csb $>$ cdb

#### The dc gain, BW, UFG and GBW of both circuits from simulation

Test	Output	Nominal	Spec	Weight	Pass/Fail
LAST_LAB:last:1	VOUT1_DB				
LAST_LAB:last:1	GAIN DB 1	42.97			
LAST_LAB:last:1	GAIN MAG 1	140.8			
LAST_LAB:last:1	BW1	140.8k			
LAST_LAB:last:1	GBW 1	19.88M			
LAST_LAB:last:1	UFG1	19.84M			
LAST_LAB:last:1	VOUT2 DB	<input type="text"/>			
LAST_LAB:last:1	GAIN DB 2	77.15			
LAST_LAB:last:1	GAIN MAG	7.205k			
LAST_LAB:last:1	BW2	2.655k			
LAST_LAB:last:1	GBW2	19.18M			
LAST_LAB:last:1	UFG2	19.27M			

Figure 8: table of requirements

Bode plot :

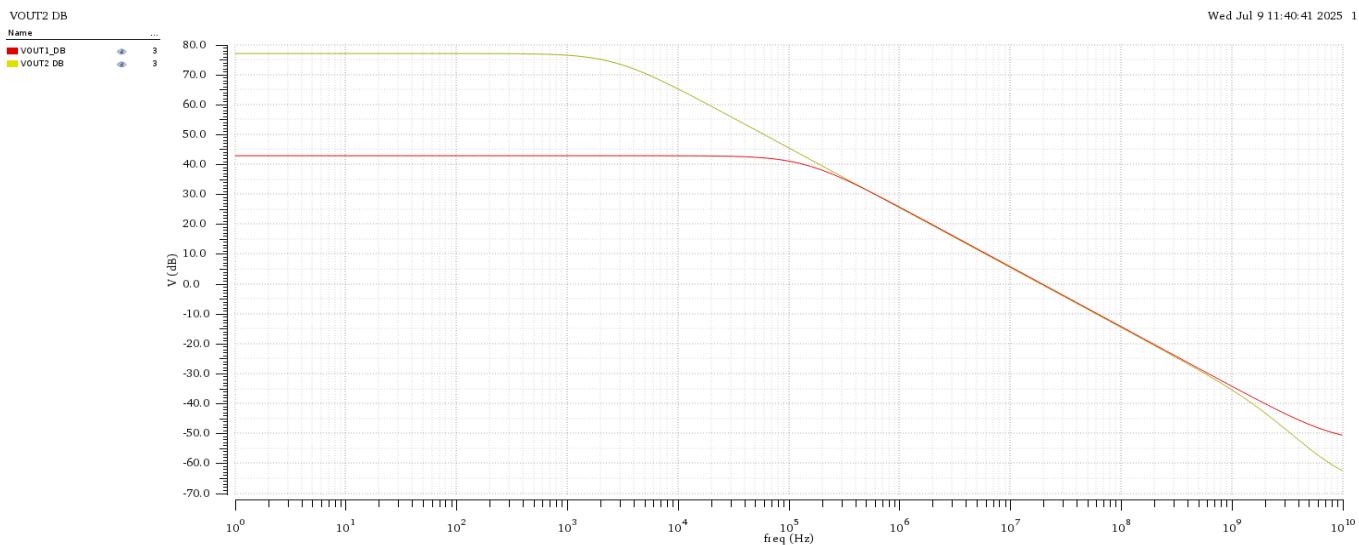


Figure 9:vout1db\_vout2db VS freq

### Hand analysis:

In a common source amplifier , dc gain (mag) given by :

$$A_V = gm \times r_o = gm \times \frac{1}{gds} = 140.797$$

But In a cascode amplifier , dc gain (mag) given by:

$$A_V = gm \times R_{out} = -gm_1 \times r_{o2}(gm_2 + gmb_2)r_{o1} \approx 7.45 K$$

	CS	Cascode
DC gain hand analysis	140.797	7.45 K
DC gain from simulation	140.8	7.205 K

### COMMENT

The **cascode amplifier** provides **much higher DC gain** than a common-source (CS) stage because it **boosts the output resistance**.

CS Amplifier: Gain is limited by  $r_{o1}r_{o1}$  (drain-source resistance of single transistor).

Cascode Amplifier: Adds a second transistor to multiply  $r_{o1}r_{o1}$ , dramatically increasing output resistance and gain.