Analog IC Design
Lab 11 (Mini Project 02)
Fully-Differential Folded Cascode OTA

Part 1: gm/ID Design Charts

1) For L = 0.28u

PMOS:

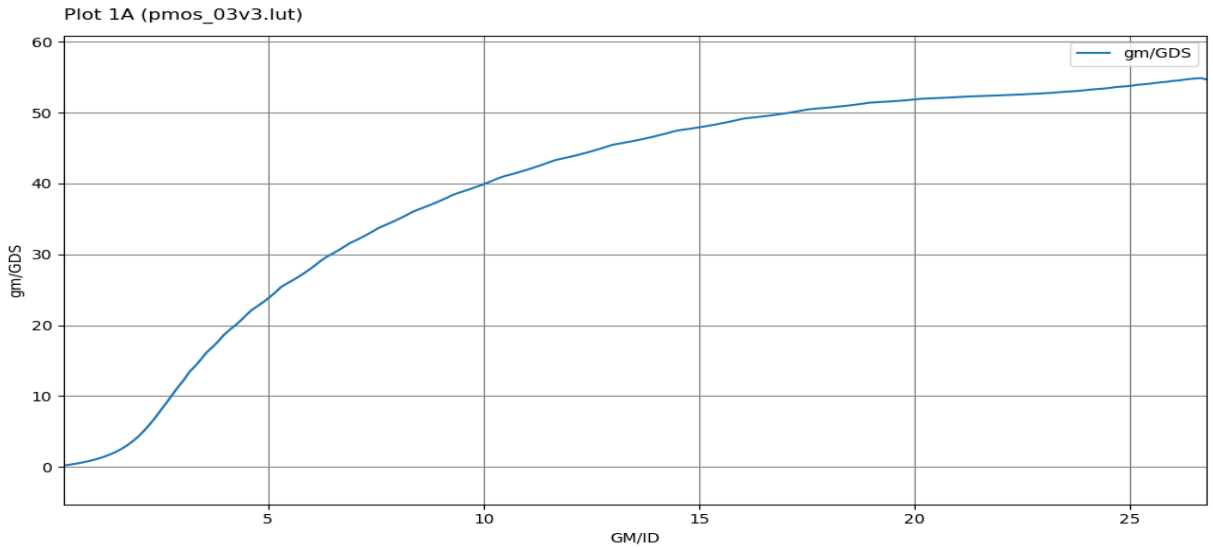


Figure 1: intrinsic gain

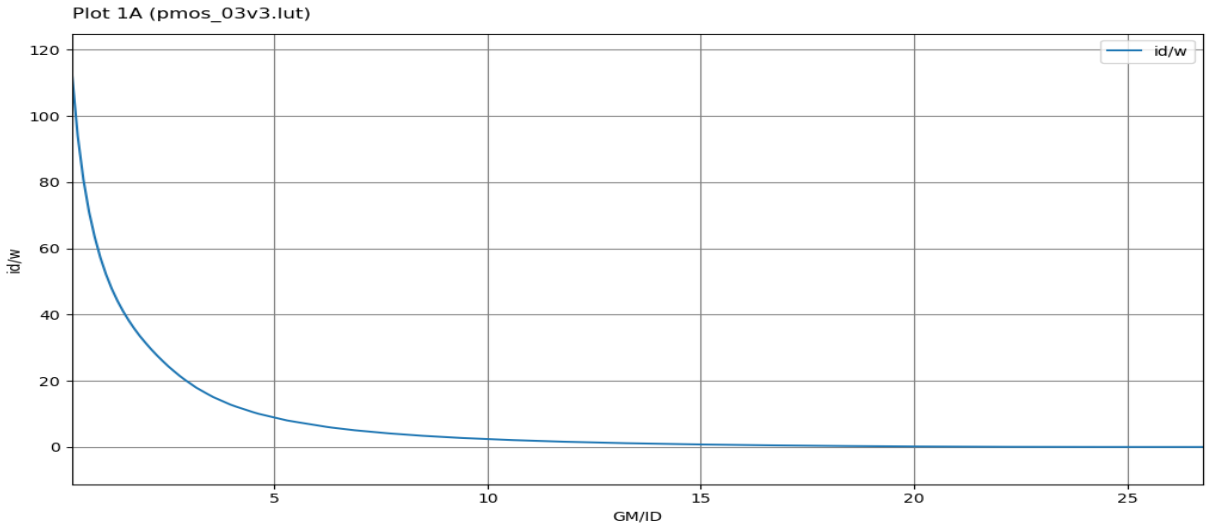


Figure 2: ID/W

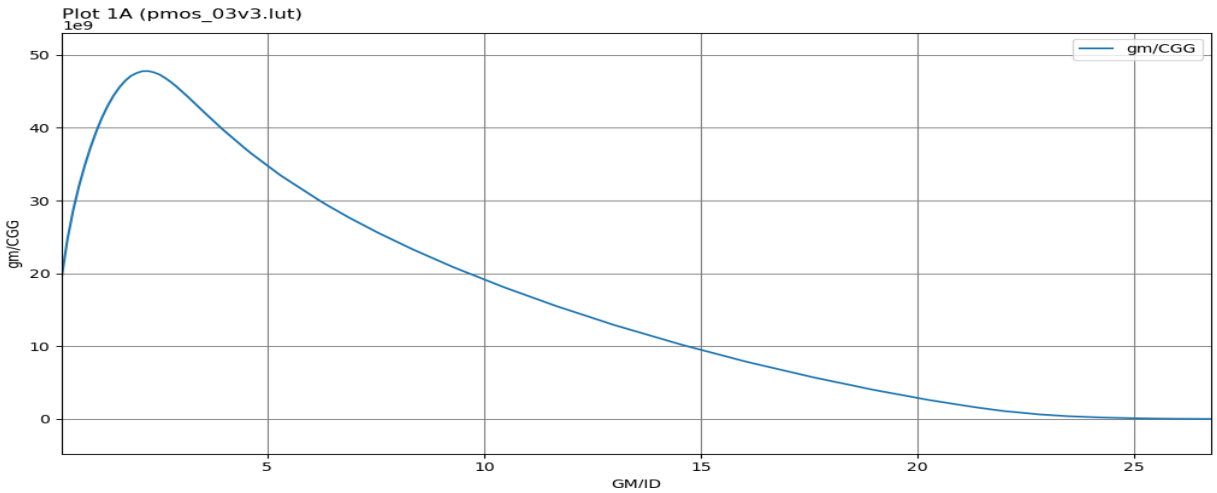


Figure 5:GM/CGG

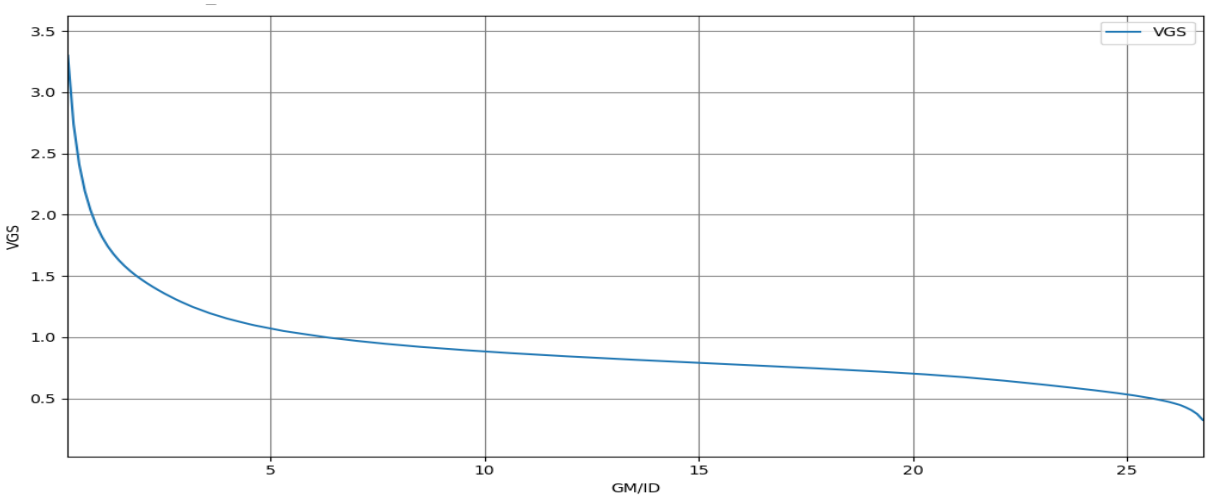


Figure 4:VGS

NMOS

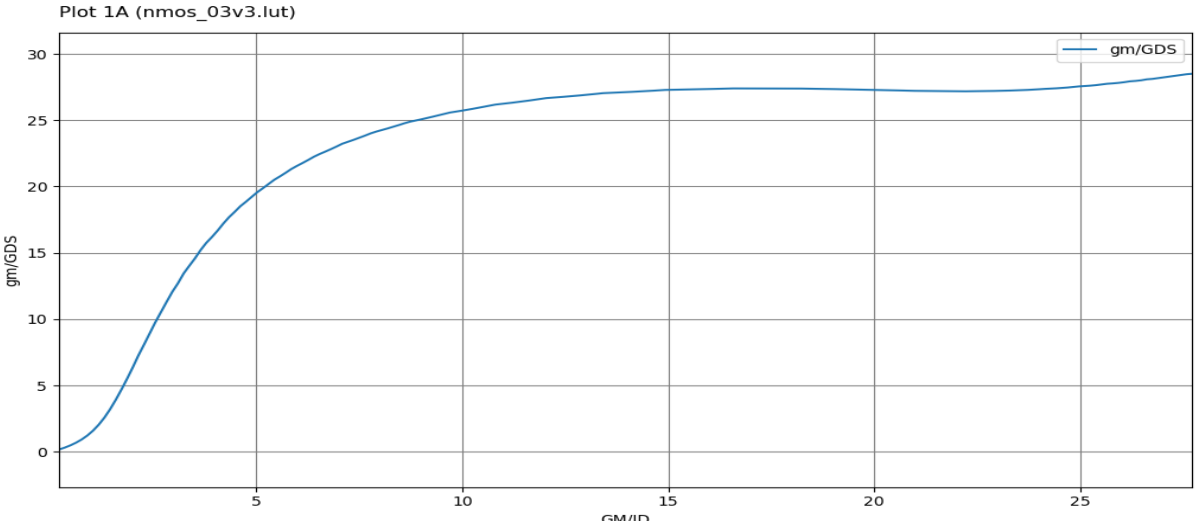


Figure 3: intrinsic gain

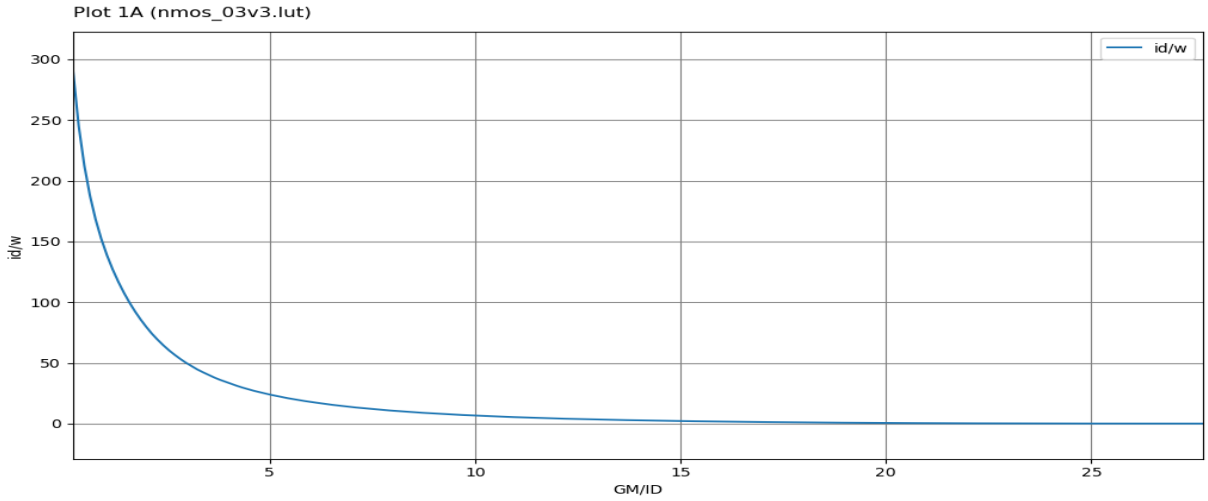


Figure 8:ID/W

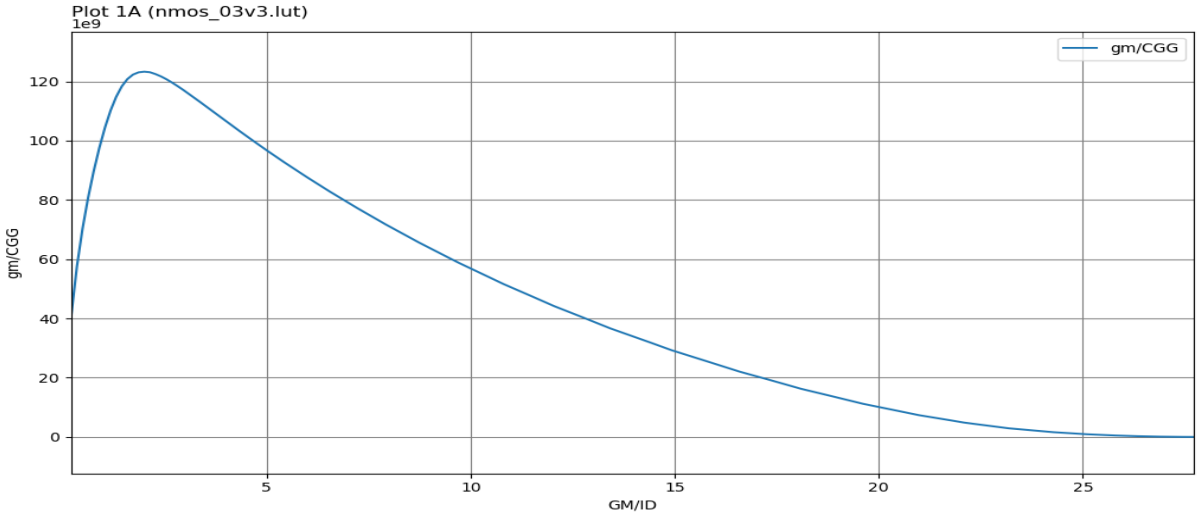


Figure 7:GM/CGG

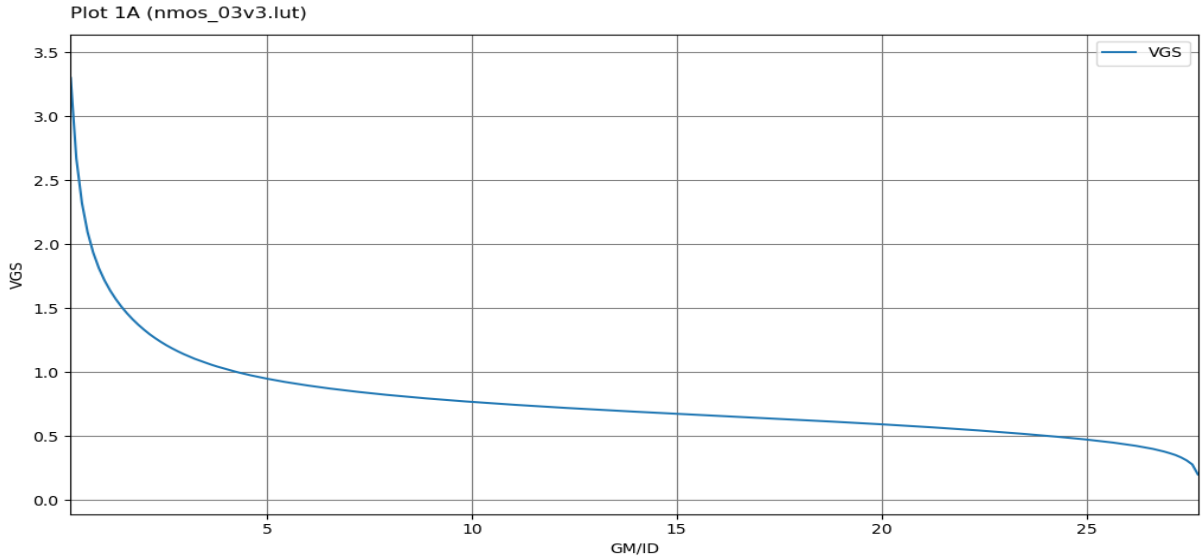


Figure 6:VGS

For L=0.4u:0.4u:2u

PMOS:

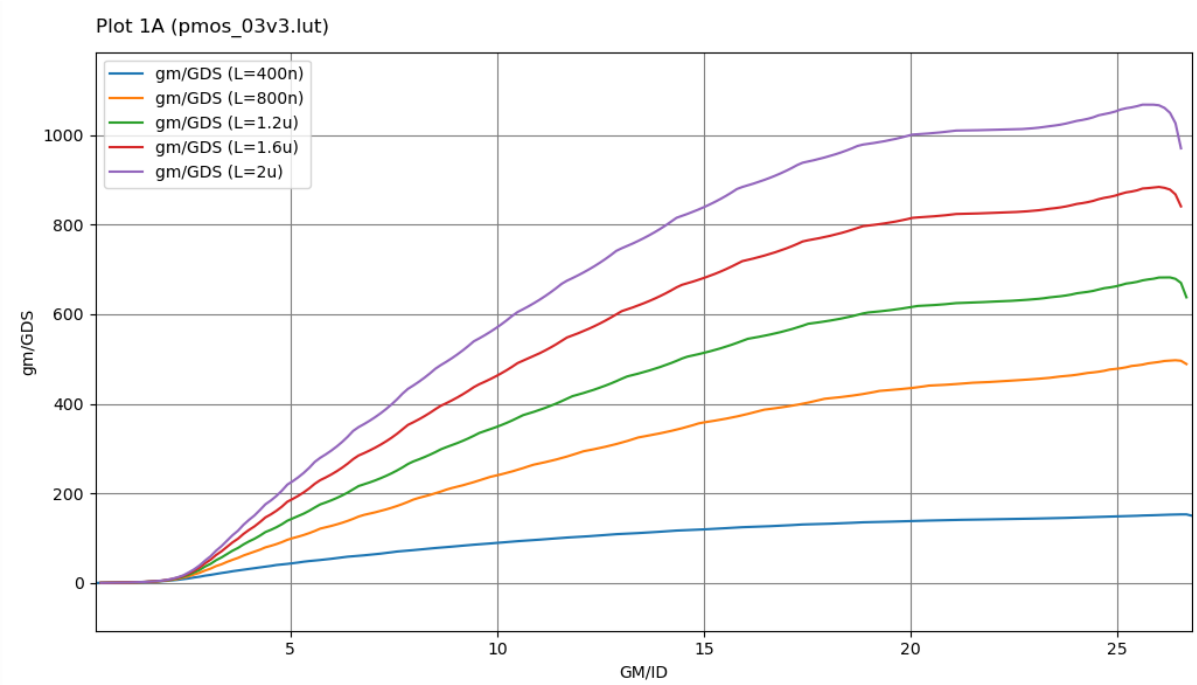


Figure 9:intrinsic gain

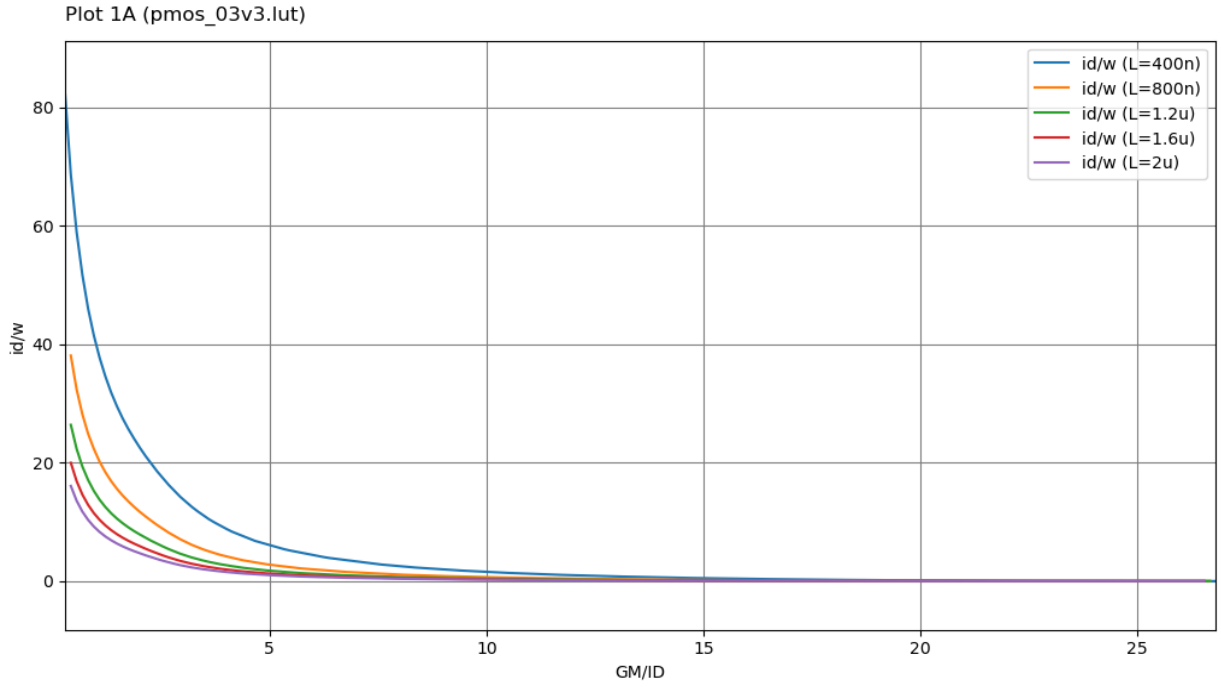


Figure 10:ID/W

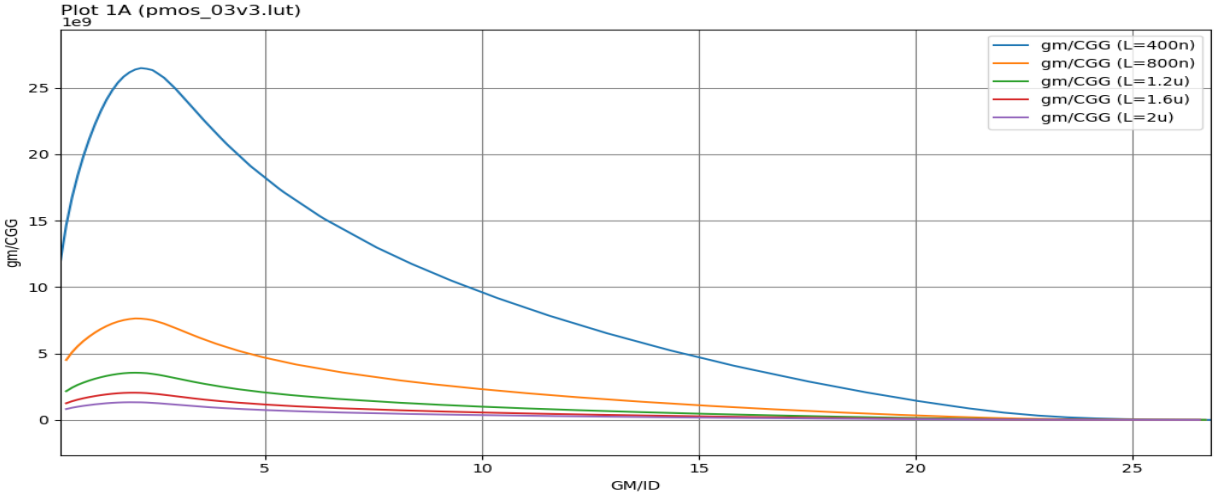


Figure 12:GM/CGG

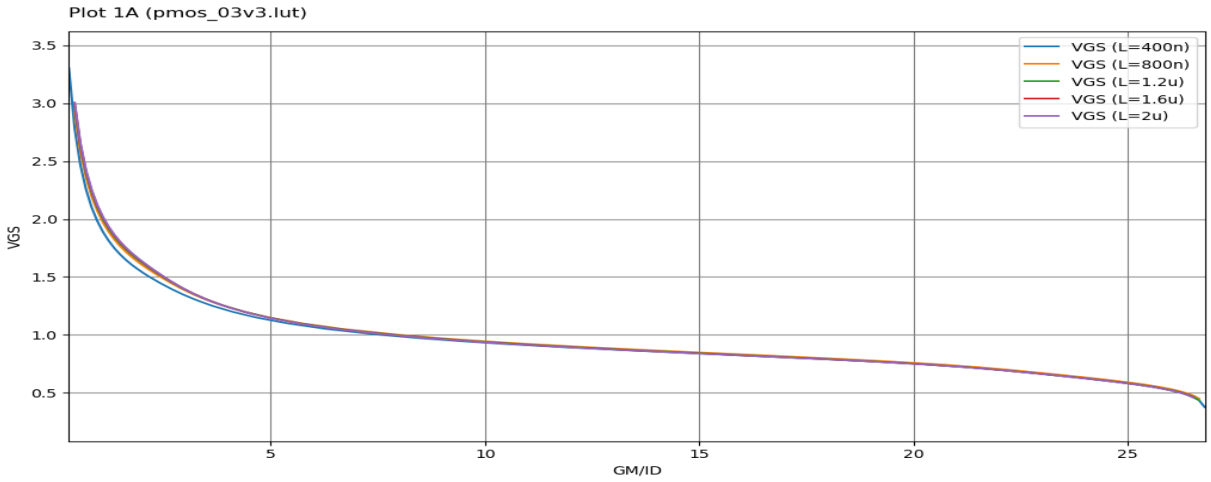


Figure 11:VGS

NMOS:

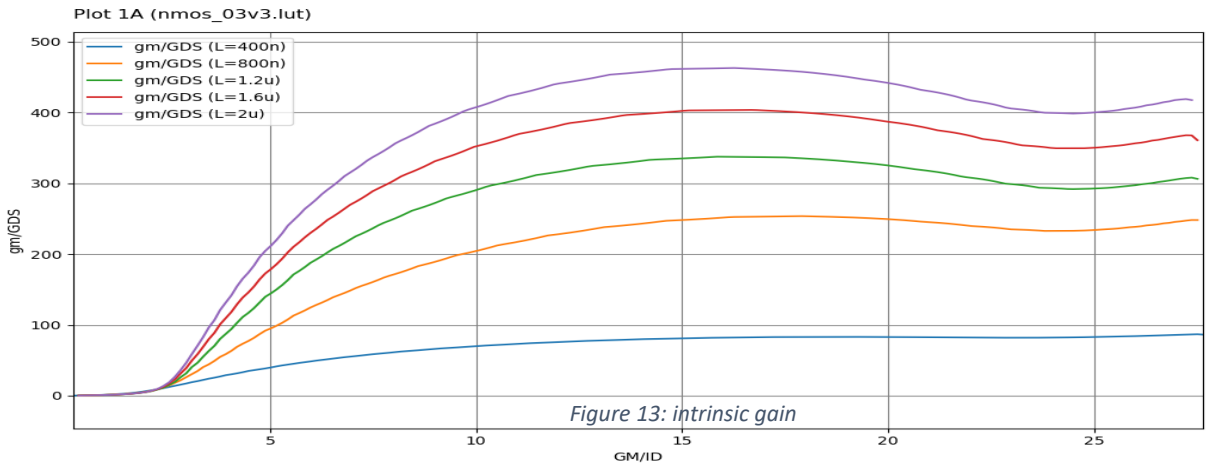


Figure 13: intrinsic gain

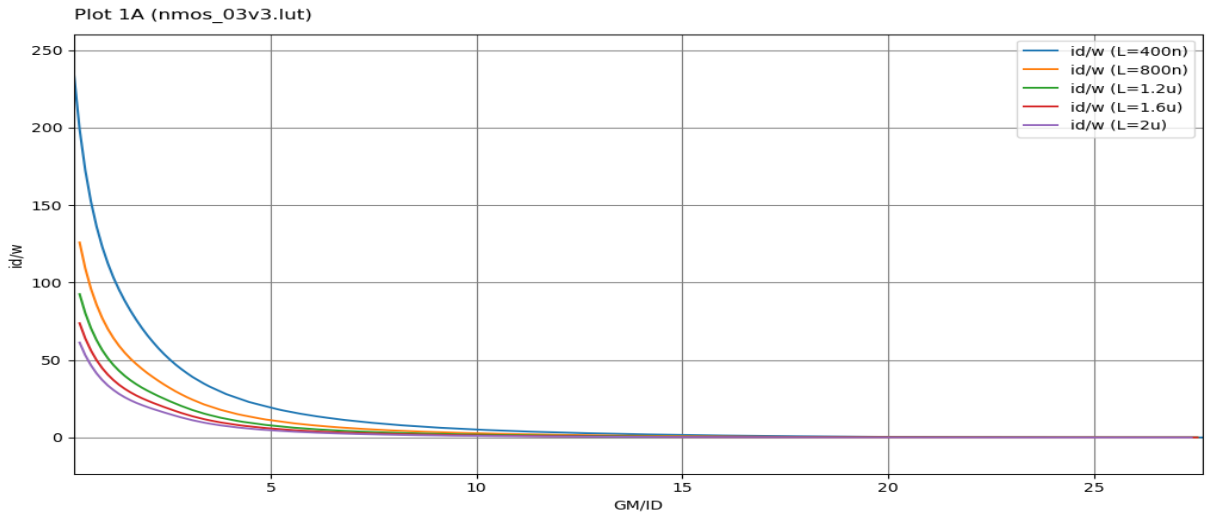


Figure 16:id/w

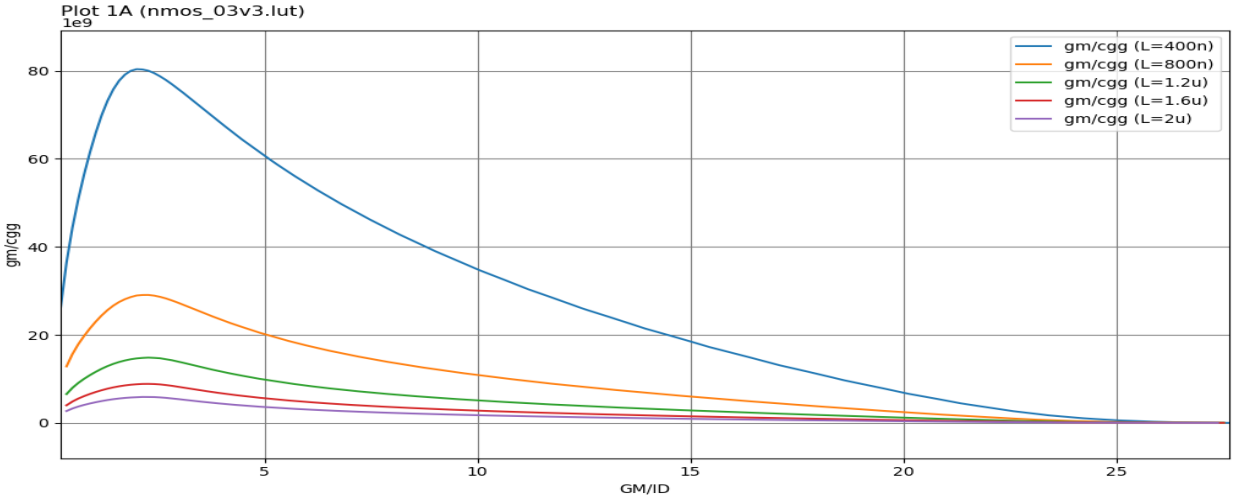


Figure 15:GM/CGG

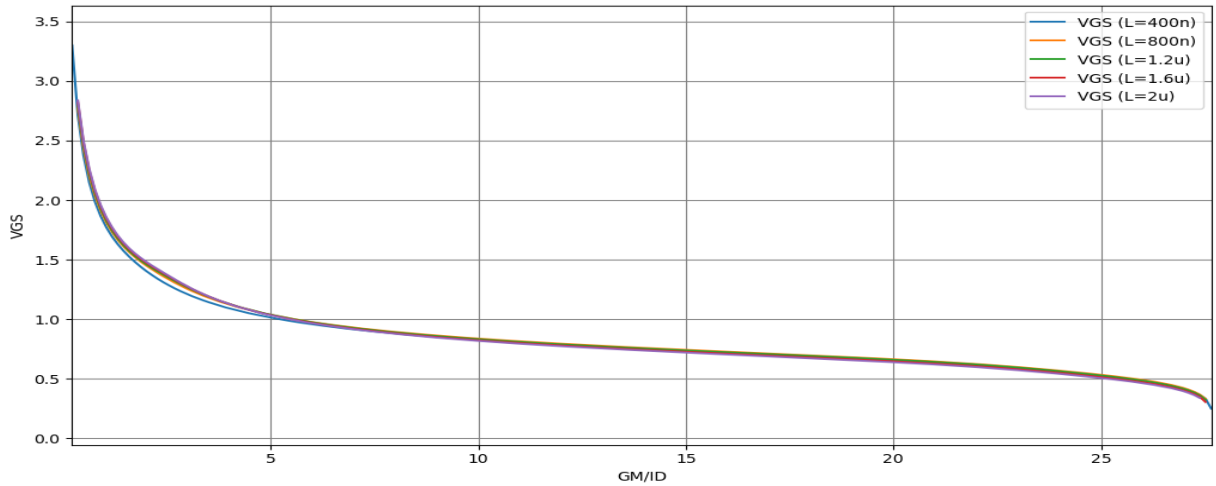


Figure 14:VGS

PART 2: OTA Design

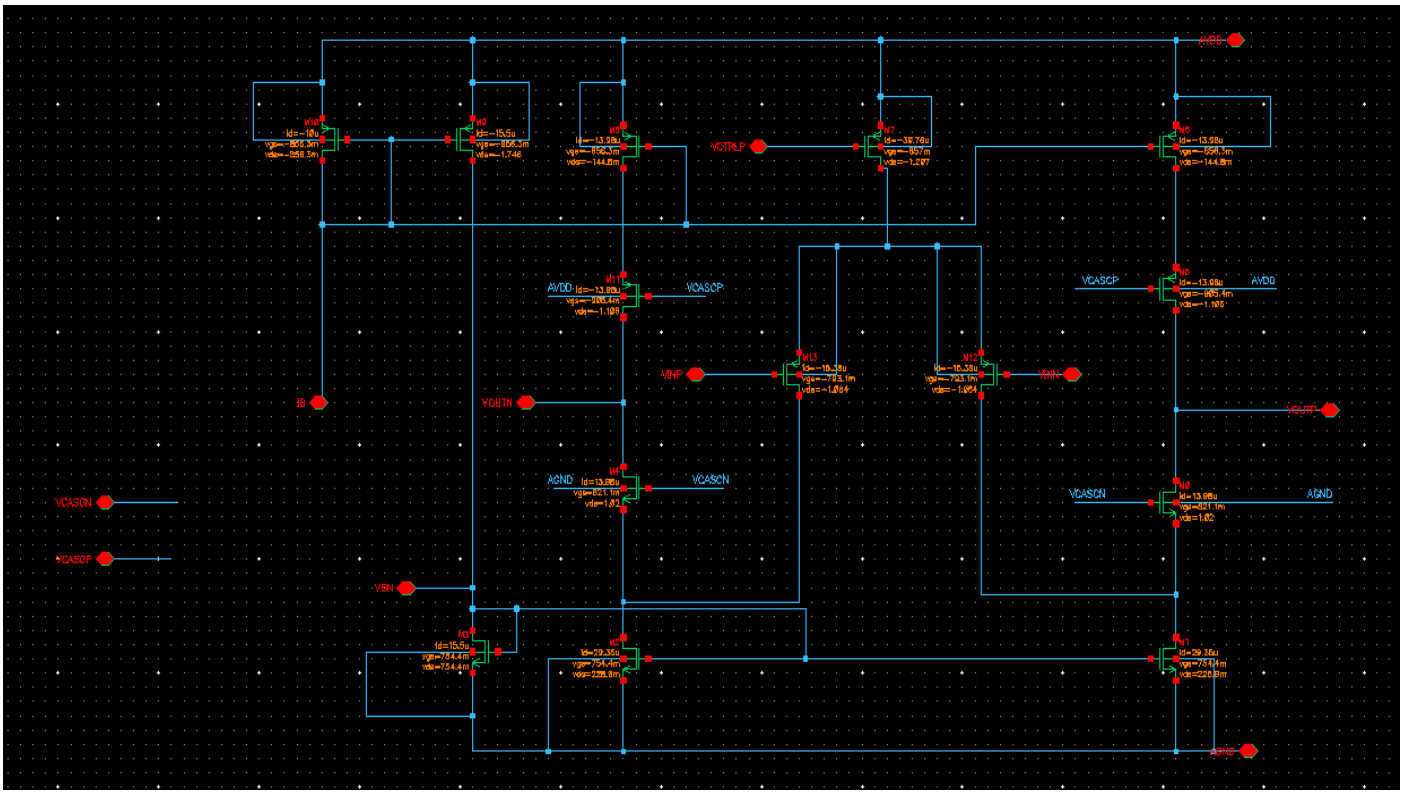


Figure 17:schematic

Design for input pair (PMOS):

Loop gain = 1000 , Trise= 100n

$C_{in} = 2 \times C_f \longrightarrow \frac{1}{\beta} = \frac{C_f}{C_{in}+C_f} = 3 \longrightarrow A_{OL} = 3000 = 69.54dB$

$GBW_{CL} = \frac{1}{\beta} \times \frac{4.6}{2\pi \times Trise} = \frac{gm}{2\pi \times Trise} = 22MHZ \longrightarrow$ gm= 207uS

$GBW_{CL(without\ loading)} = \frac{gm}{2\pi \times C_L}$ =66 MHZ

I will take margin for gm =240uS

I will assume gm/id=16 ⟶ id=15 uA

I took small L = 300n , W= 26.28u

	Name	TT-27.0
3	L	300n
4	W	26.28u
5	VGS	783.5m
6	VDS	1.25
7	VSB	0
8	gm/ID	15.73
9	Vstar	127.1m
10	fT	1.201G
11	gm/gds	70.15

Figure 18: values from SA

Design for cascode (PMOS&NMOS):

Id = 15u , assume gm/id=15, L=500n (same assumption for NMOS & PMOS)

NMOS

	Name	TT-27.0
3	L	500n
4	W	11.23u
5	VGS	752m
6	VDS	625m
7	VSB	0
8	gm/ID	14.92
9	Vstar	134.1m
10	fT	2.199G
11	gm/gds	133.3

PMOS

	Name	TT-27.0
3	L	500n
4	W	39.89u
5	VGS	848.8m
6	VDS	625m
7	VSB	0
8	gm/ID	14.94
9	Vstar	133.8m
10	fT	484.7MEG
11	gm/gds	195.5

Design for current mirror (PMOS&NMOS):

Id = 15u , assume gm/id=10, L=600n (same assumption for NMOS & PMOS)

. A large gm will not help the gain but will increase the offset and noise.

NMOS

	Name	TT-27.0
3	L	500n
4	W	11.23u
5	VGS	752m
6	VDS	625m
7	VSB	0
8	gm/ID	14.92
9	Vstar	134.1m
10	fT	2.199G
11	gm/gds	133.3

PMOS

	Name	TT-27.0
3	L	500n
4	W	39.89u
5	VGS	848.8m
6	VDS	625m
7	VSB	0
8	gm/ID	14.94
9	Vstar	133.8m
10	fT	484.7MEG
11	gm/gds	195.5

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

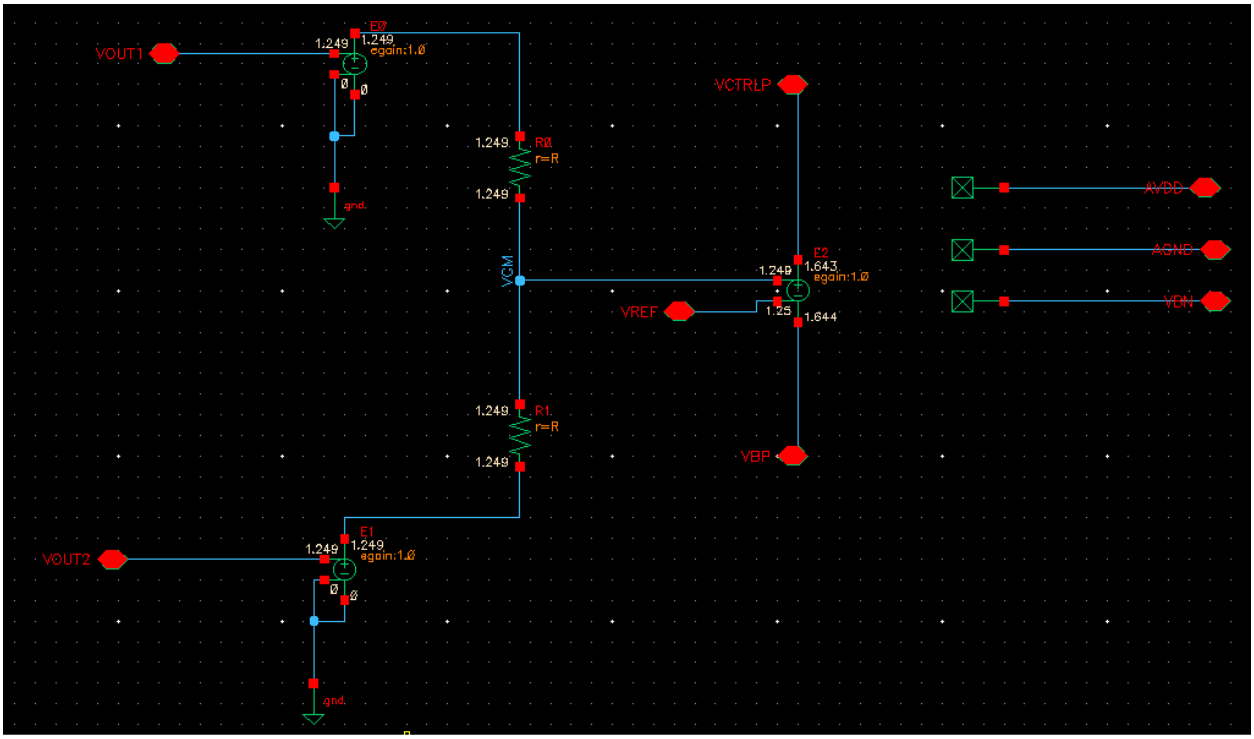


Figure 19:(Behavioral CMFB

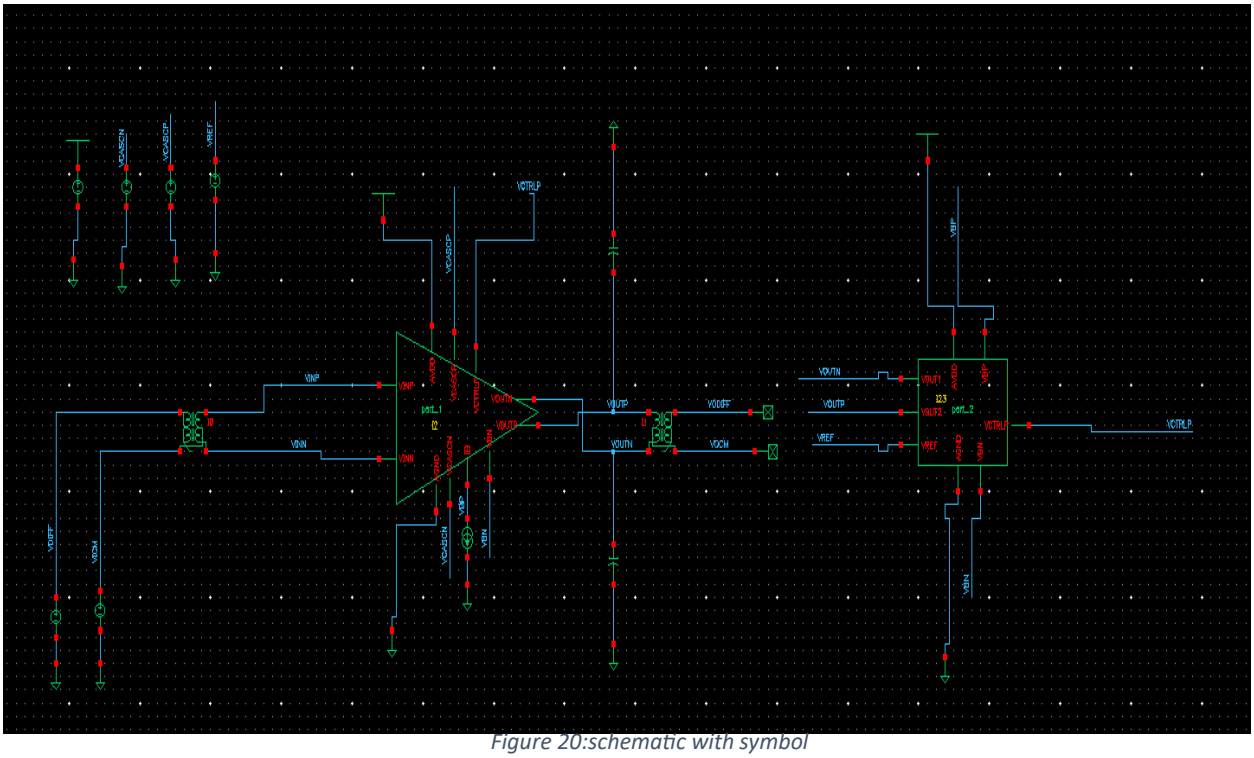


Figure 20:schematic with symbol

1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.

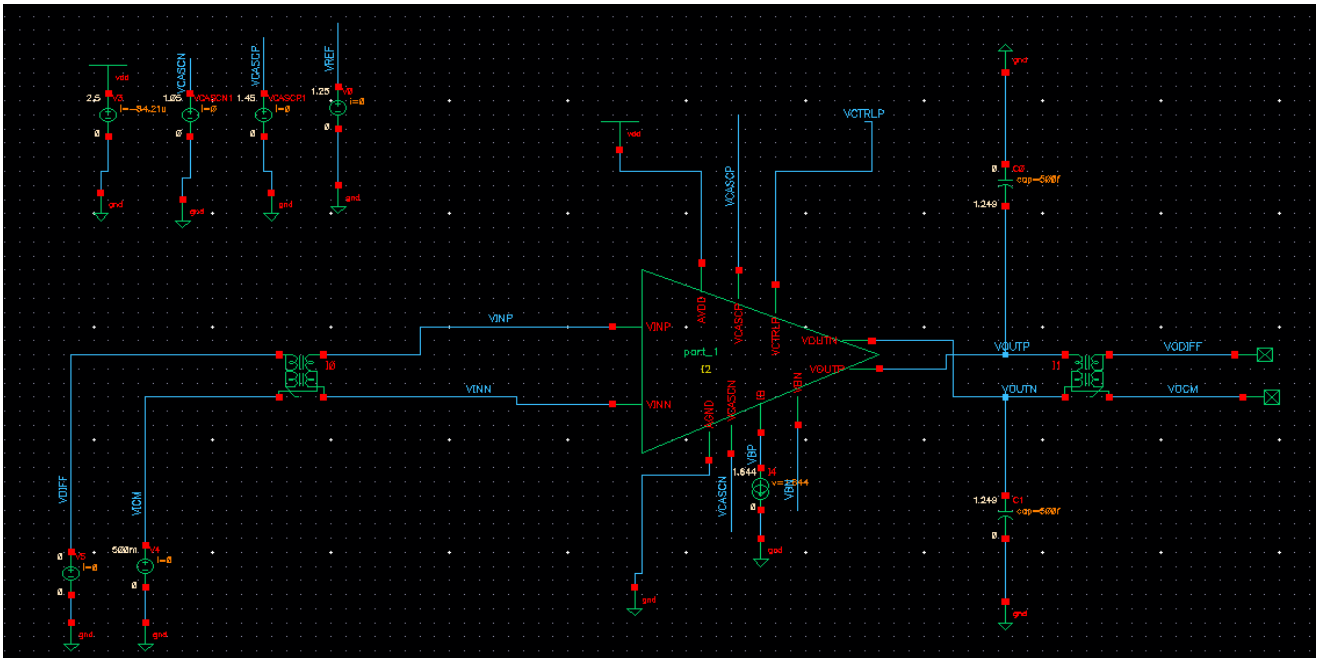


Figure 21:SCHEMATIC WITH DC VOLTAGES ANNOTATED

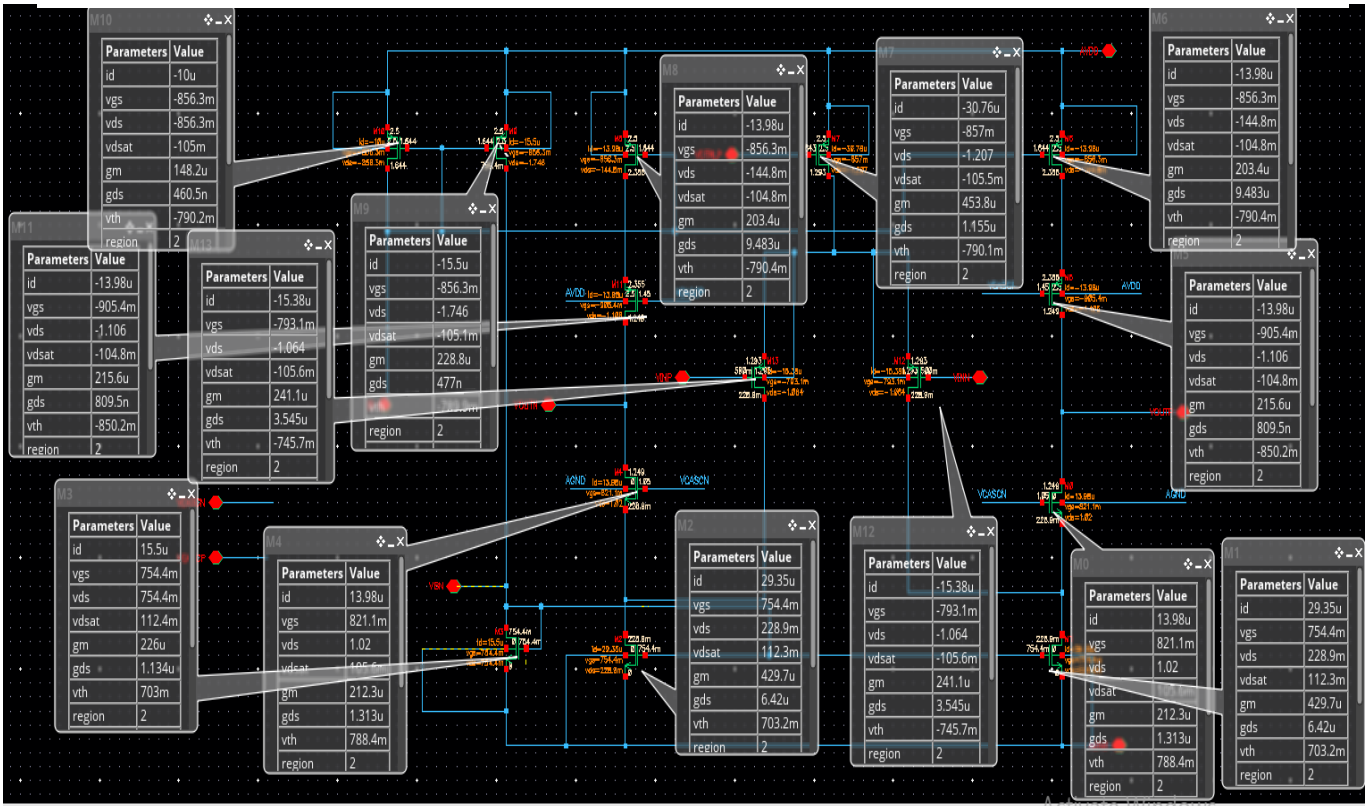


Figure 22:SCHEMATIC OTA ANNOTATED AS REQUIED

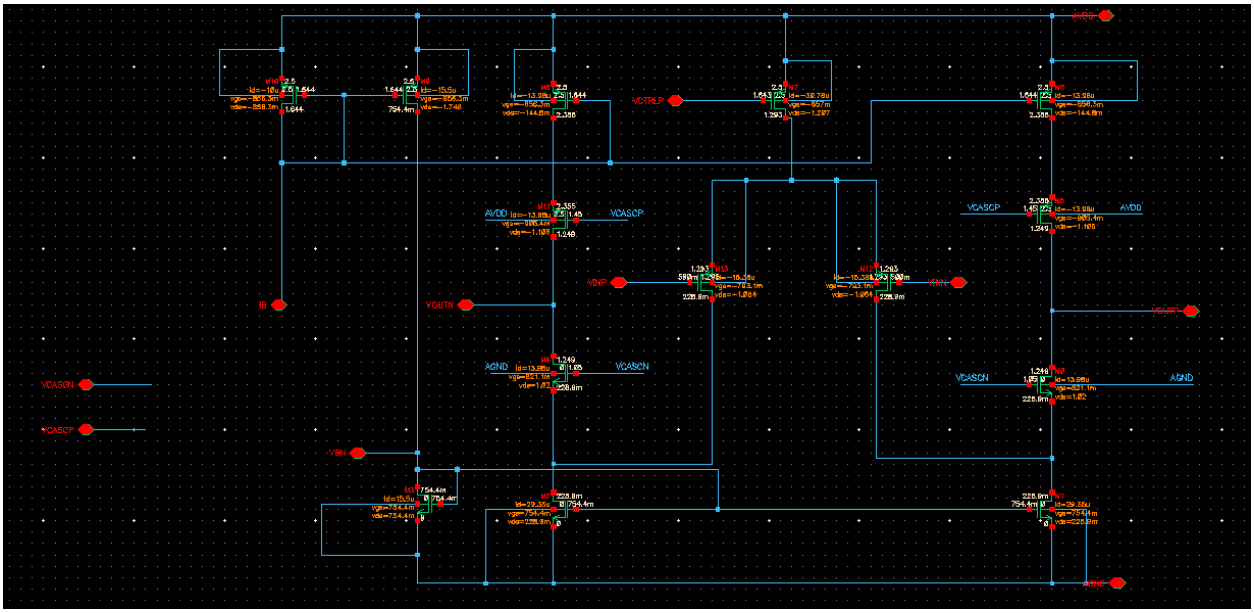


Figure 23:SCHEMATIC with DC node voltages

Vref $\approx \frac{VDD}{2} = 1.25V$

VCASCN ≈ VGSN + V*=1.09V

VCASCP ≈ VDD - |VGSP| - V*=1.4498V

What is the CM level at the OTA output?

- VOUT=1.249≈ Vref

What are the differential input and output voltages of the error amplifier? What is the relation between them?

DIFF INPUT= 1 m

DIFF OUTPUT = 1 m

RELATION=$\frac{\text{DIFF OUTPUT}}{\text{DIFF INPUT}} = \frac{1.644-1.643}{1.25-1.249} = 1 = gain\ of\ VCVS$

2)Diff small signal ccs:

Plot diff gain (magnitude in dB and phase) vs frequency

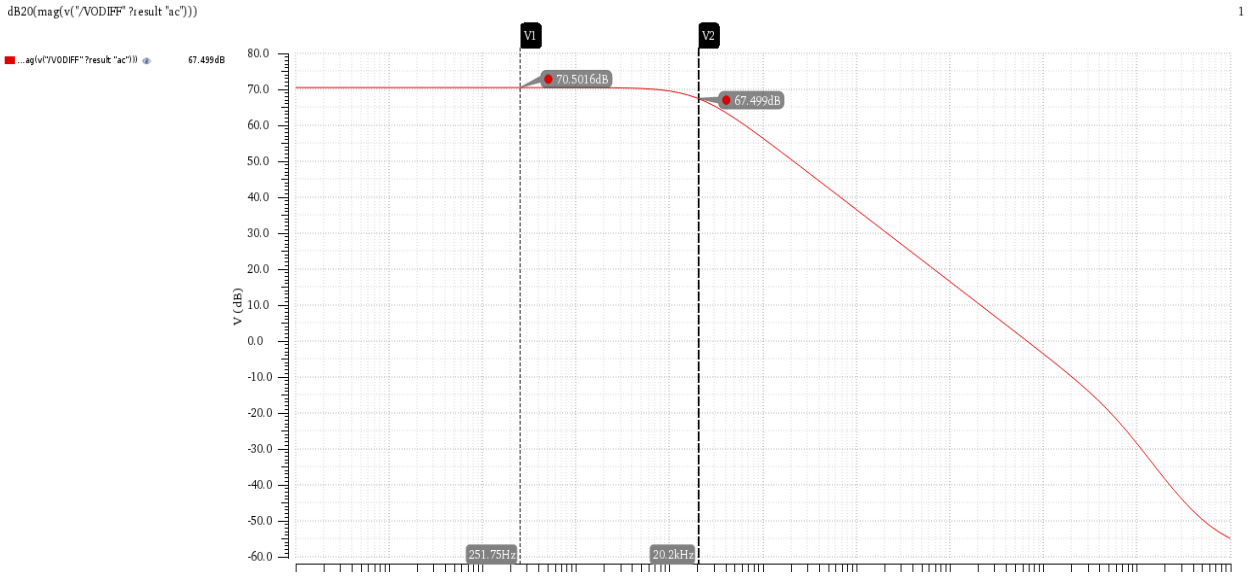


Figure 25: VODIFF VS FREQ (in dB)

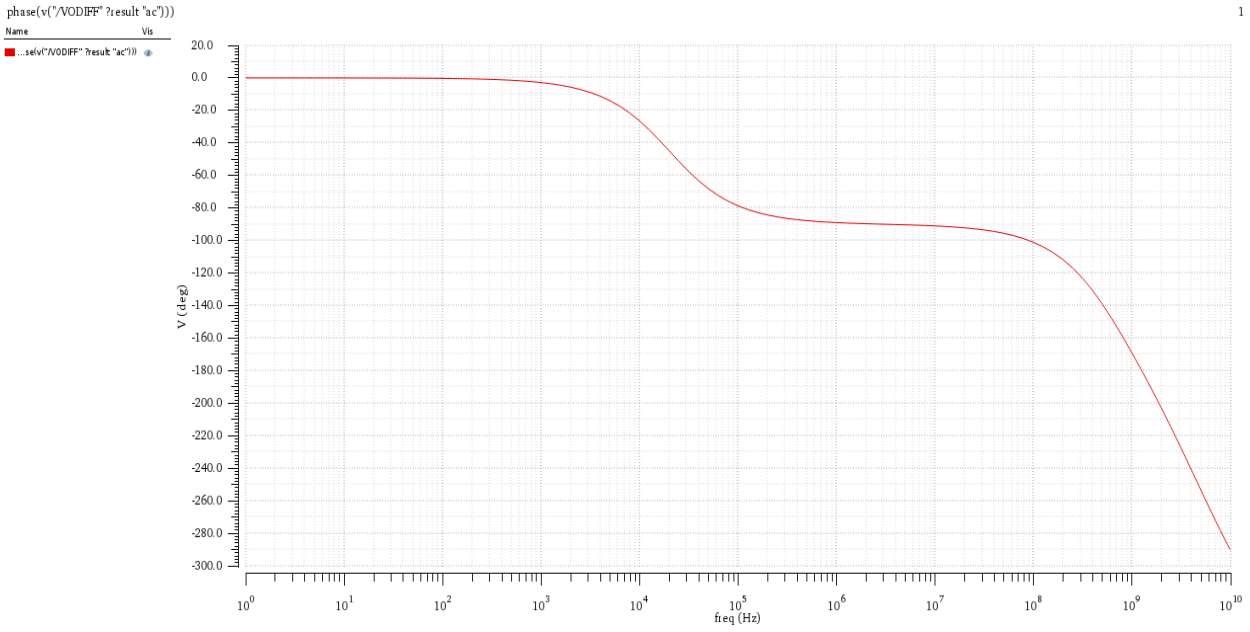


Figure 24:VODIFF VS FREQ (PHASE)

Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

FROM SIMULATION:

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_mini_project:part_3:1	A0	3.351k			
lab11_mini_project:part_3:1	A0_dB	70.5			
lab11_mini_project:part_3:1	BW	20.2k			
lab11_mini_project:part_3:1	UGF	68.2M			
lab11_mini_project:part_3:1	GBW	67.85M			
lab11_mini_project:part_3:1	PM	82.6			

HAND ANALYSIS:

$R_{OUT} = r_{04}(1 + gm_4 r_{02}) // r_{011}(1 + gm_{11} r_{08})$= 13.88 MΩ

$|A_V| = gm_{13(input\ pair)} \times R_{OUT}$ =3346.47=70.49dB

BW = $\frac{1}{2\pi \times R_{OUT} \times C_{OUT}}$ =20.29 KHZ

GBW=$\frac{gm(input\ pair)}{2\pi \times C_{OUT}}$ =66.887 MHZ nearly= UGF

PM= 180-$tan^{-1}\left(\frac{wu}{dominant\ pole}\right) - tan^{-1}\left(\frac{wu}{non-dominant\ pole}\right) = 83.4$

The non-dominant pole frequency was extrapolated from the Bode magnitude plot. It was taken as the frequency at which the gain roll-off deviated from the initial -20 dB/decade slope, indicating the presence of a second pole

non-dominant pole≈ 600MHZ

	GAIN	BW	UGF	GBW	PM
From simulation	70.5 dB	20.2 KHZ	68.2 MHZ	67.85 MHZ	82.6˚
From hand analysis	70.49 dB	20.29 *KHZ*	66.887MHZ	66.887MHZ	83.4˚

PART 4: Open-Loop OTA Simulation (Actual CMFB)

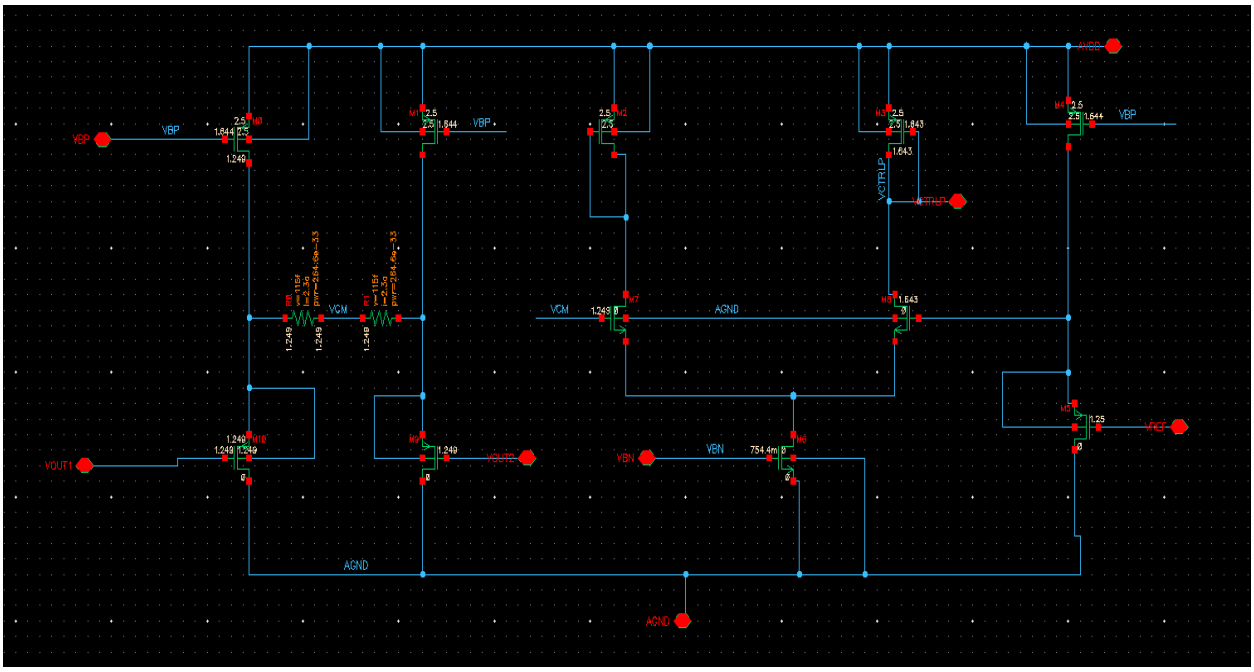


Figure 26:schematic

1)

Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated

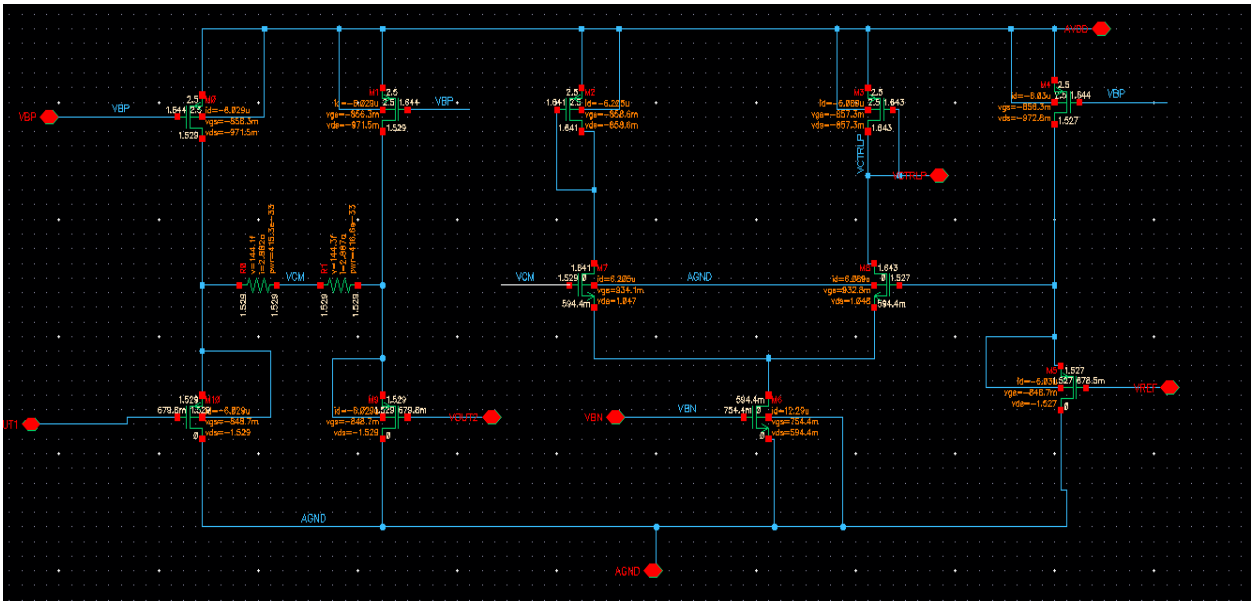


Figure 27:CMFB annotated

VREF to maximize output swing = 678.5 mV

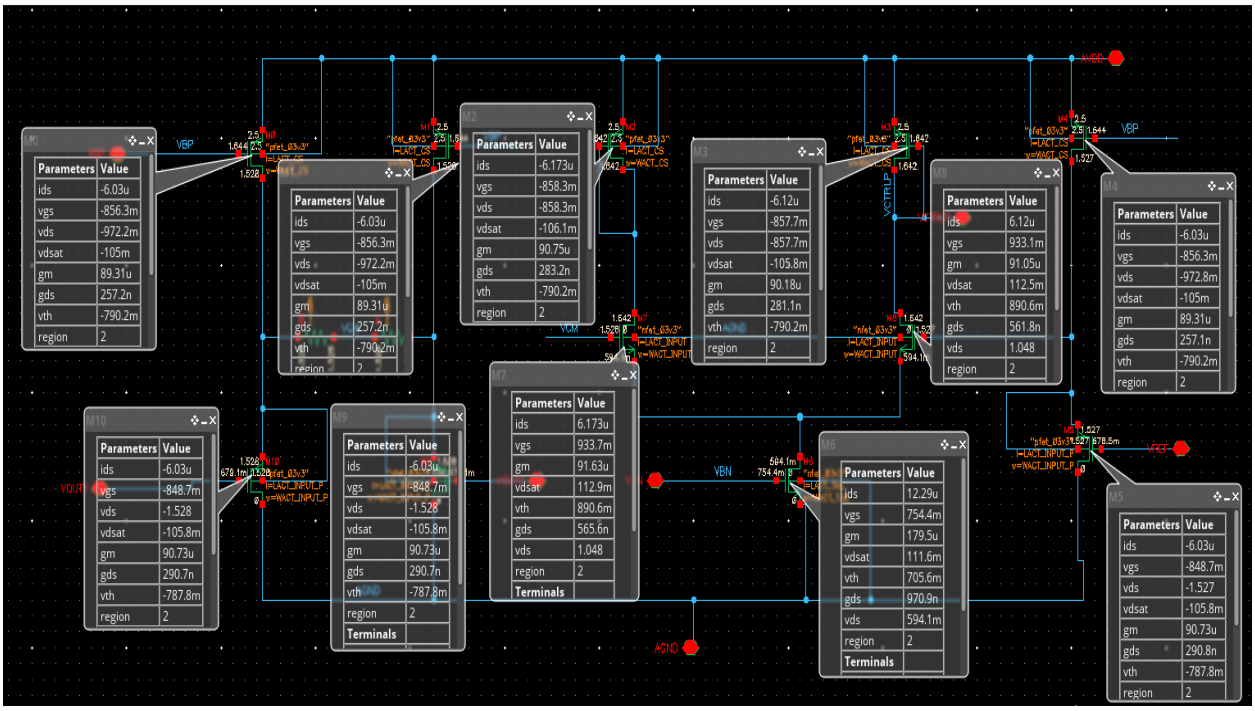
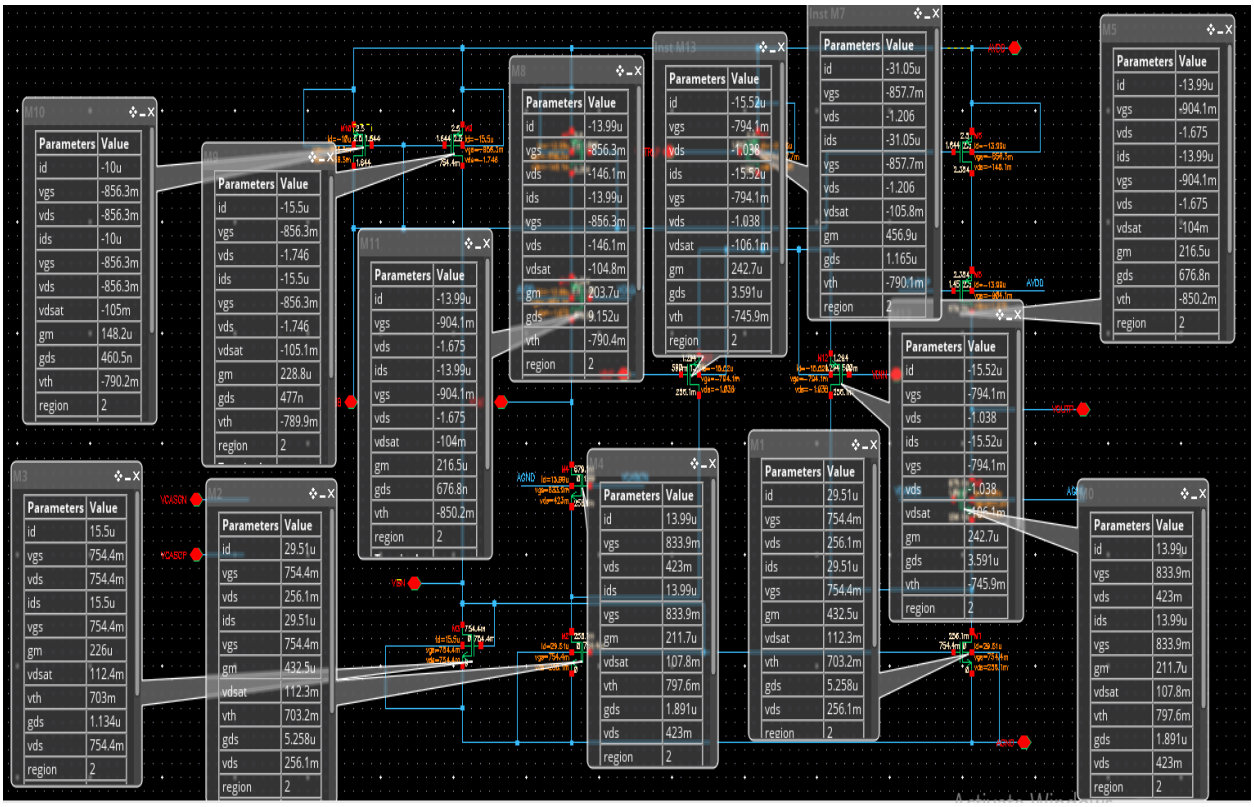


Figure 28:ACTUAL CMFB



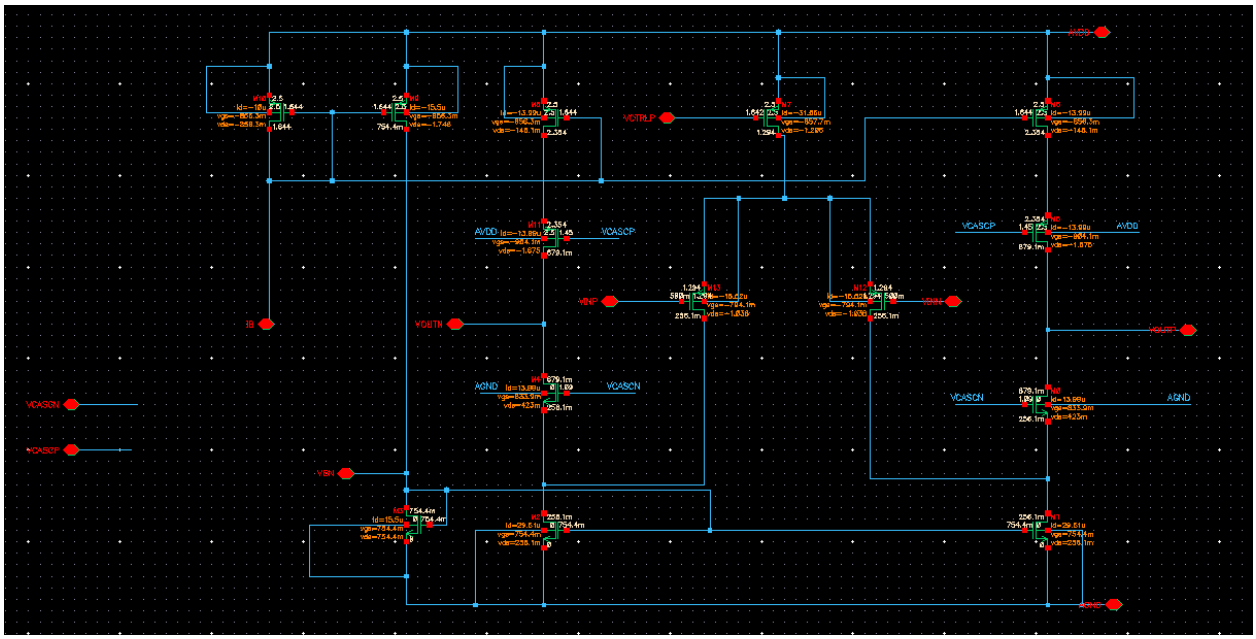
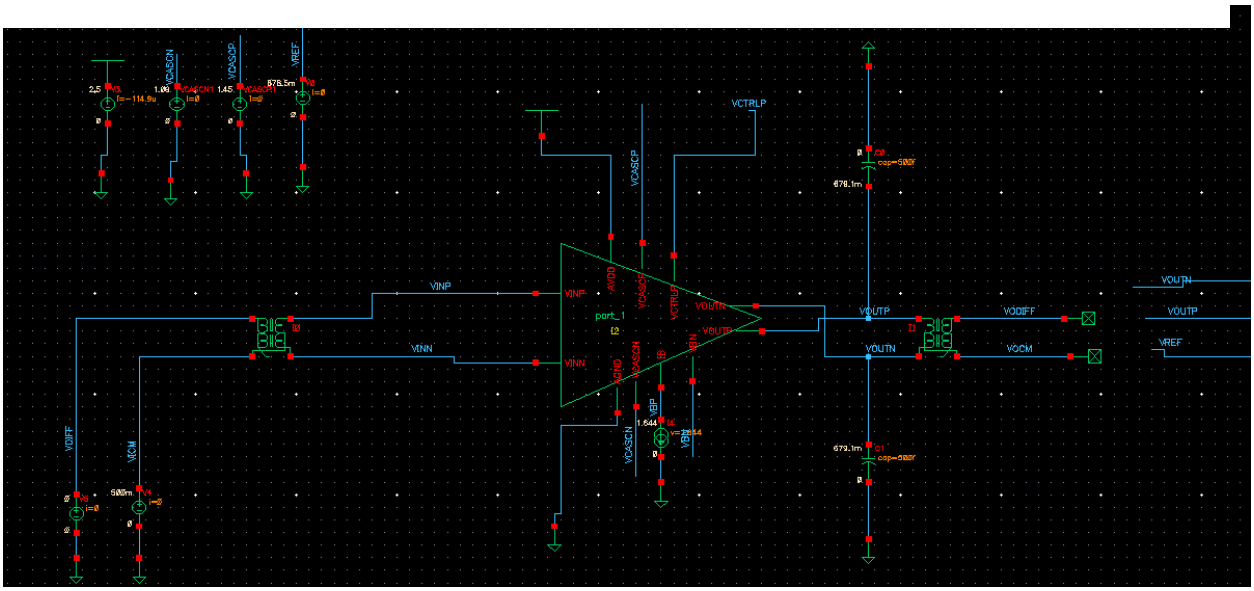


Figure 29:OTA voltage node annotated



What is the CM level at the OTA output? Why?

- The measured output common-mode voltage is 679.1 mV. This value is nearly equal to the applied VREF voltage because the common-mode feedback (CMFB) circuit is functioning correctly. The CMFB loop uses negative feedback to continuously compare the average output voltage to VREF and adjust the OTA's bias current to minimize any error, forcing VOCM to converge to the value of VREF.

What are the differential input and output voltages of the error amplifier? What is the relation between them?

DIFF INPUT=1.3m

DIFF OUTPUT=1.3m

$RELATION = \frac{\text{DIFF OUTPUT}}{\text{DIFF INPUT}}$=gain of error AMP= 1

2) Diff small signal ccs:

Plot diff gain (magnitude in dB and phase) vs frequency.

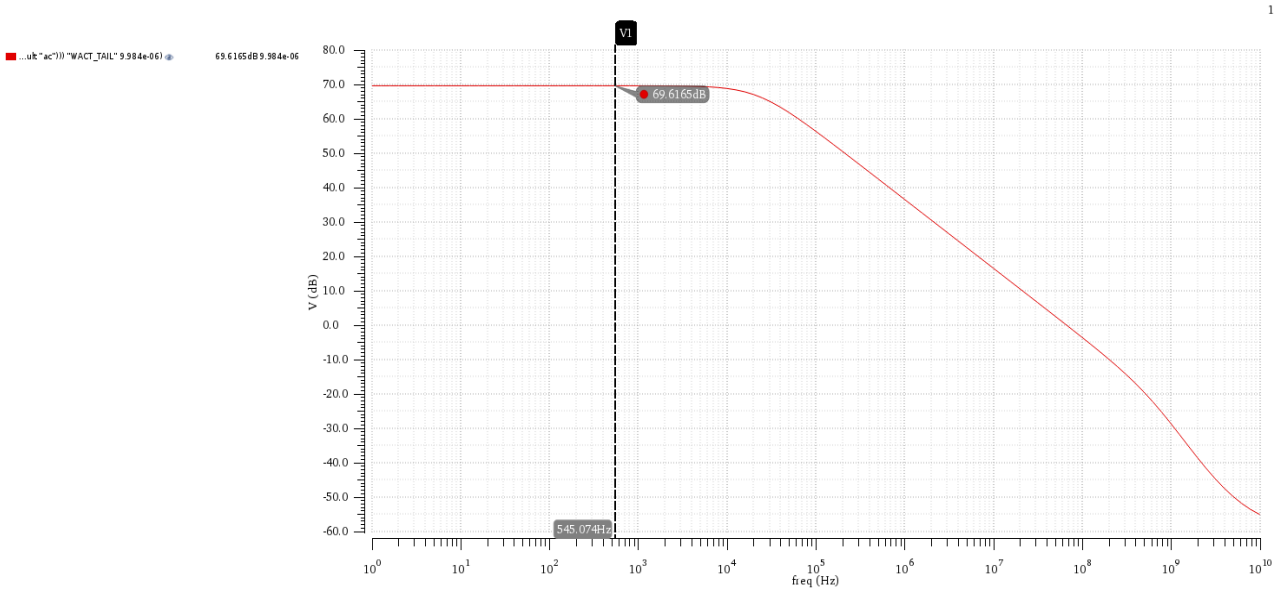


Figure 30: VODIFF VS FREQ (in dB)

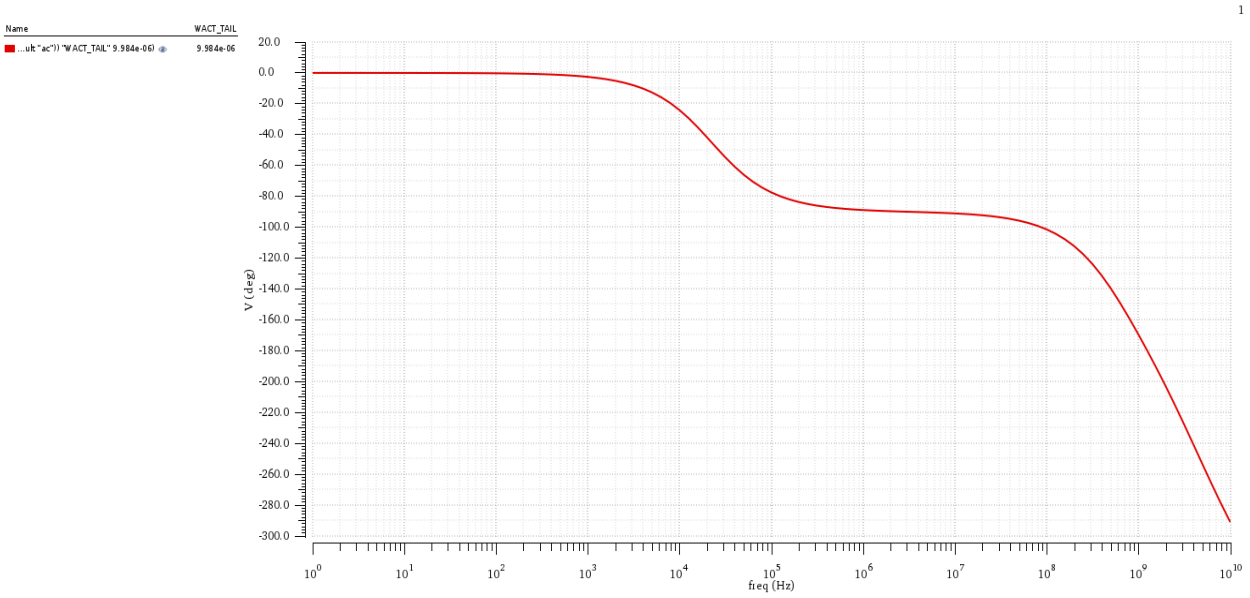


Figure 31:VODIFF VS FREQ (PHASE)

Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

FROM SIMULATION:

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_mini_project:part_3:1	A0	3.027k			
lab11_mini_project:part_3:1	A0_dB	69.62			
lab11_mini_project:part_3:1	BW	22.39k			
lab11_mini_project:part_3:1	UGF	68.07M			
lab11_mini_project:part_3:1	GBW	67.93M			
lab11_mini_project:part_3:1	PM	82.38			

HAND ANALYSIS:

$gm_{13(input\ pair)} = 242.7uS$

$R_{OUT} = r_{04}(1 + gm_4 r_{02})//r_{011}(1 + gm_{11} r_{08})$= 12.54 MΩ

$|A_V|$=$gm_{13(input\ pair)} \times R_{OUT}$ =3043.458=69.66dB

BW = $\frac{1}{2\pi \times R_{OUT} \times C_{OUT}}$ =22.26 KHZ

GBW=$\frac{gm(input\ pair)}{2\pi \times C_{OUT}}$ =67.766 MHZ nearly= UGF

	GAIN	BW	UGF	GBW
From simulation	69.62 dB	22.39 KHZ	68.07 MHZ	67.93 MHZ
From hand analysis	69.66 dB	22.26 KHZ	67.766 MHZ	67.766 MHZ

PART 5: Closed Loop Simulation (AC and STB Analysis)

1) Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop /configuration.

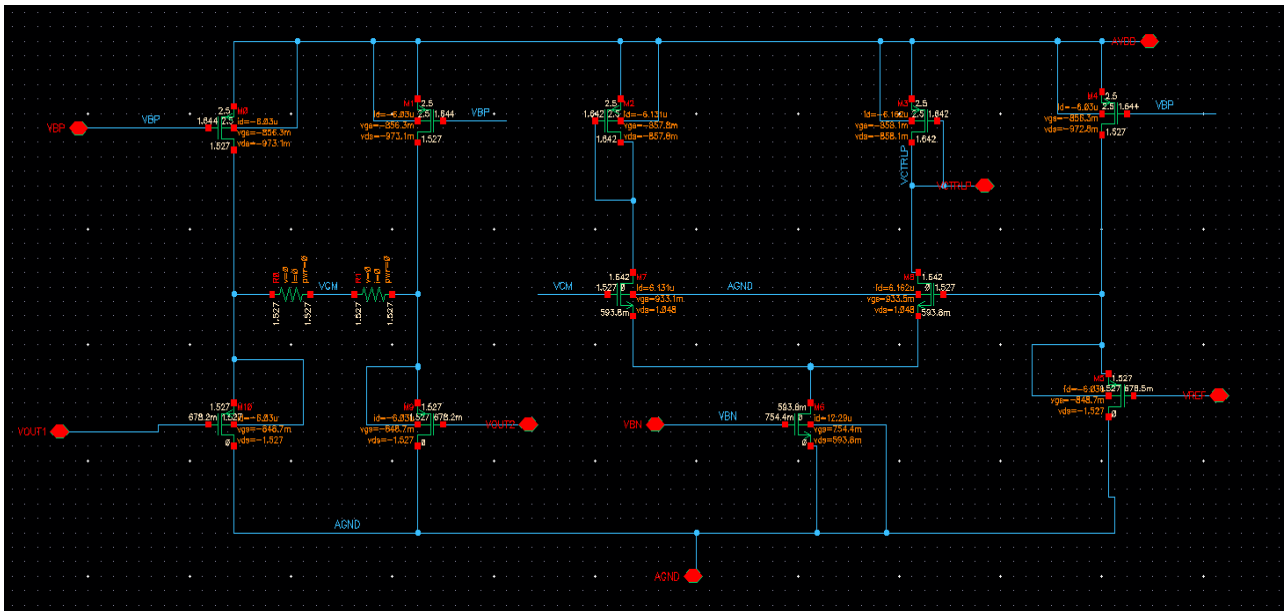
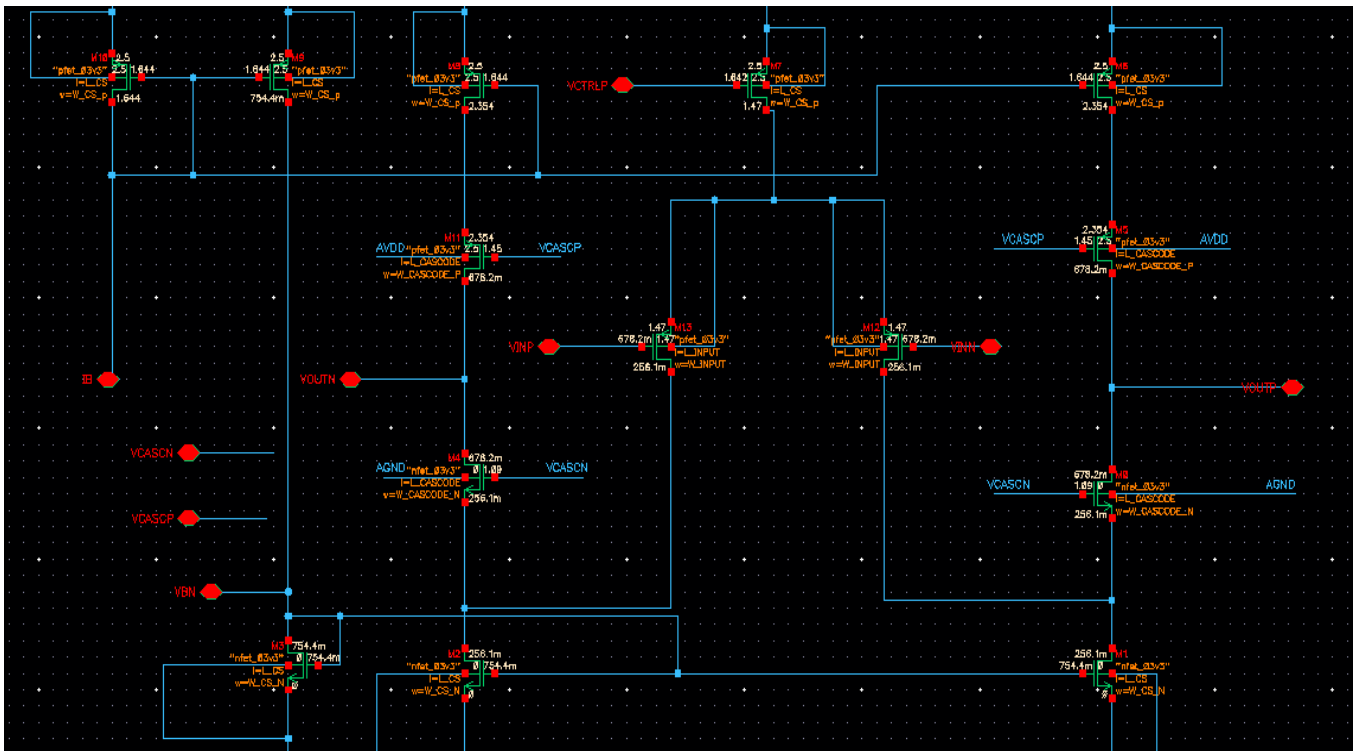


Figure 32: Actual CMFB annotated



What is the CM level at the OTA output? Why?

What is the CM level at the OTA input? Why?

- The common-mode level at both the OTA output and input is 678.2 mV, equal to VREF. The output level is set directly by the CMFB circuit. The input level is forced to the same potential through the DC feedback resistors (Rf), which provide a negative feedback path for the common mode signal The input capacitors (Cin) block any external DC signal, demonstrating that VIN, CM = VOUT,CM due to negative feedback

2) Differential closed-loop response:

Plot VODIFF vs frequency

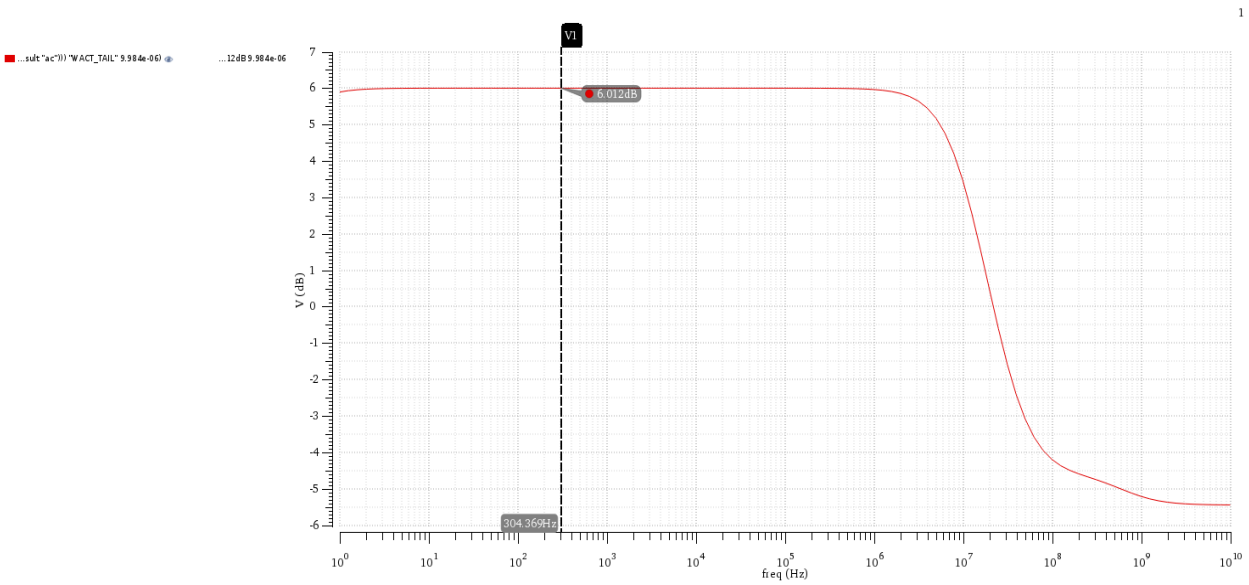


Figure 33: OTA annotated

Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_mini_project:part_3:1	A0	1.998			
lab11_mini_project:part_3:1	A0_dB	6.012			
lab11_mini_project:part_3:1	BW	11.69M			
lab11_mini_project:part_3:1	UGF	22.34M			
lab11_mini_project:part_3:1	GBW	23.13M			
lab11_mini_project:part_3:1	PM	82.86			

3) Differential and CMFB loops stability (STB analysis):

Plot loop gain in dB and phase vs frequency for the two simulations overlaid.

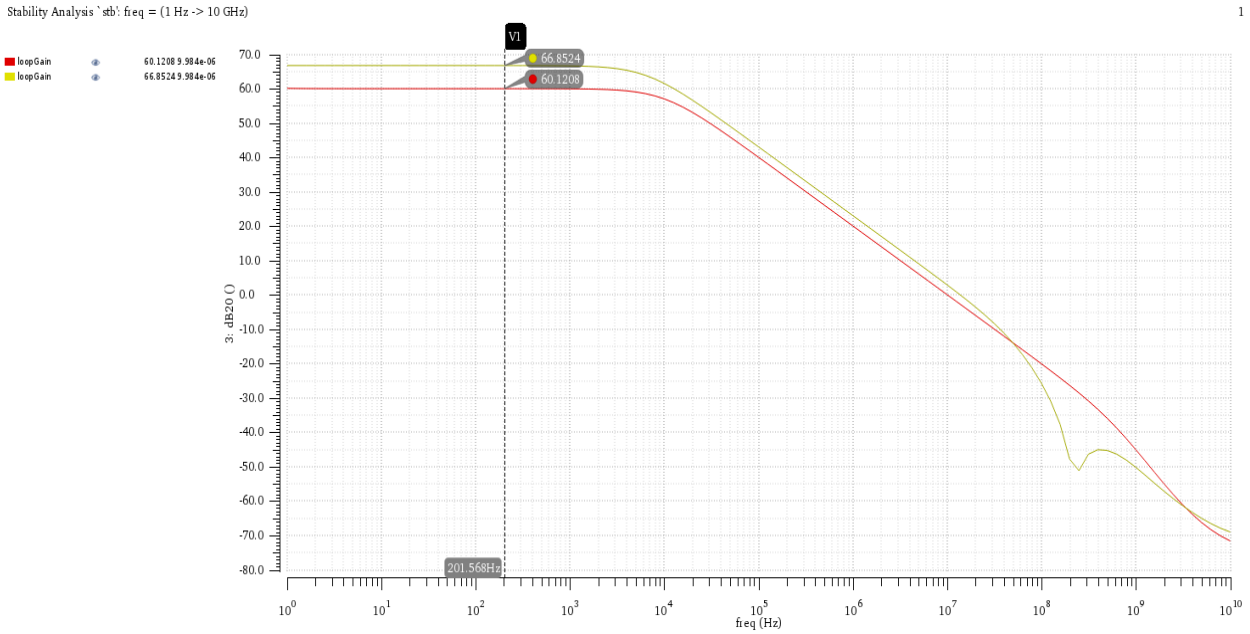


Figure 34: Loop gain vs freq (in dB)

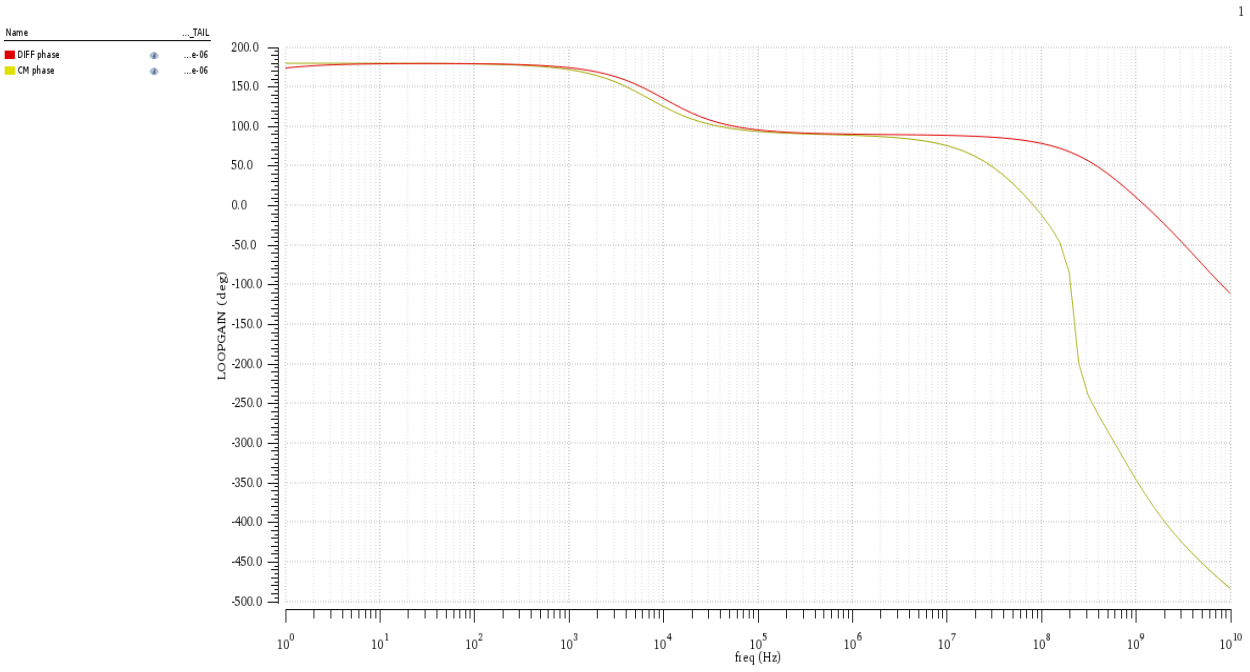


Figure 35: PHASE VS FREQ

Compare GBW and PM of diff and CM loops. Comment.

	WACT_TAIL	gainBwP...stb")))	getData...) (Deg)
1	9.984E-6	10.00E6	88.93

Figure 37: GBW and PM of diff loop

	WACT_TAIL	gainBwP...stb")))	getData...) (Deg)
1	9.984E-6	14.47E6	70.68

Figure 36:GBW and PM of CM loop

Comment:

The CMFB loop is intentionally designed to be faster (higher GBW) than the differential loop to ensure rapid rejection of common-mode disturbances. However, its longer signal path—passing through additional stages like the sensing network and error amplifier—introduces more non-dominant poles and excess phase shift, resulting in a lower phase margin (PM). Despite this trade-off, the CMFB loop remains stable with adequate

Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment

	GAIN	GBW
Loop Gain(diff)	60.1208 dB =1014	10 MHZ
Open loop	69.62 dB =3027	67.93 MHZ

COMMENT

The loop gain decreased to 1/3 of the open-loop gain due to the feedback factor β = 1/3, since the loop gain LG = β · A_OL. The total output capacitance increased because of loading capacitors, which reduced the bandwidth and thus decreased the GBW.

PART 6: Closed Loop Simulation (Transient Analysis)

1) Differential and CMFB loops stability (transient analysis) + CL settling time: Differential input pulse

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same

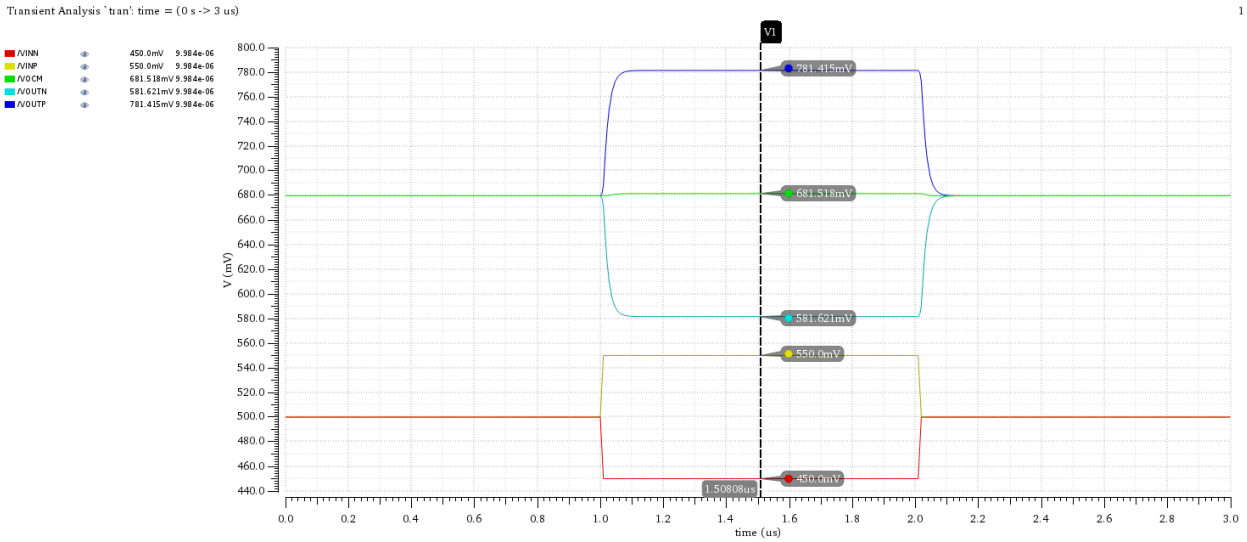


figure.

Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

- No, there is no differential or common-mode ringing observed in the transient response. Both loops are stable with adequate phase margin the differential loop has a high PM of 88.9°, and the CMFB loop has a robust PM of 70.7°

Calculate the 1% settling time and compare it to the required specification

	Expression	Value
1	riseTime(VT("/...	78.86E-9

Figure 39:value of trise

```
riseTime(VT("/VODIFF") 0 t 1.6u t 0 99 nil "time" )
```

Figure 38: expression i used

Which achieved our spec , If not achieved we can increase ROUT of OTA by increasing L and that will increase gain and GBW

We can also calc it from grapgh by calculating ymax and multiply it by 0.99 and make cursor at this point and second at rise of output

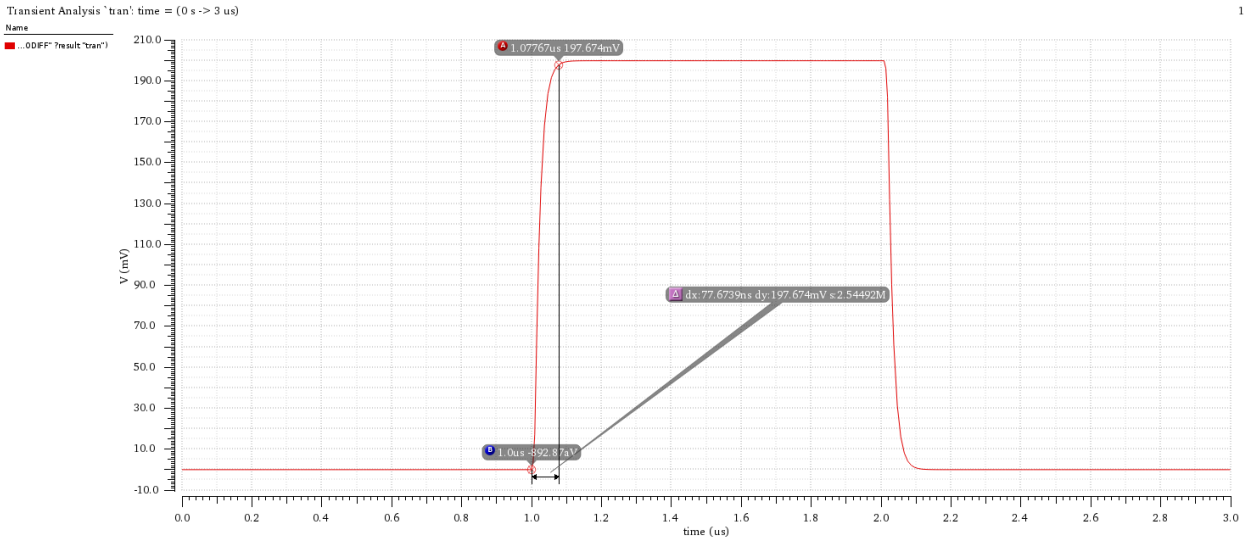
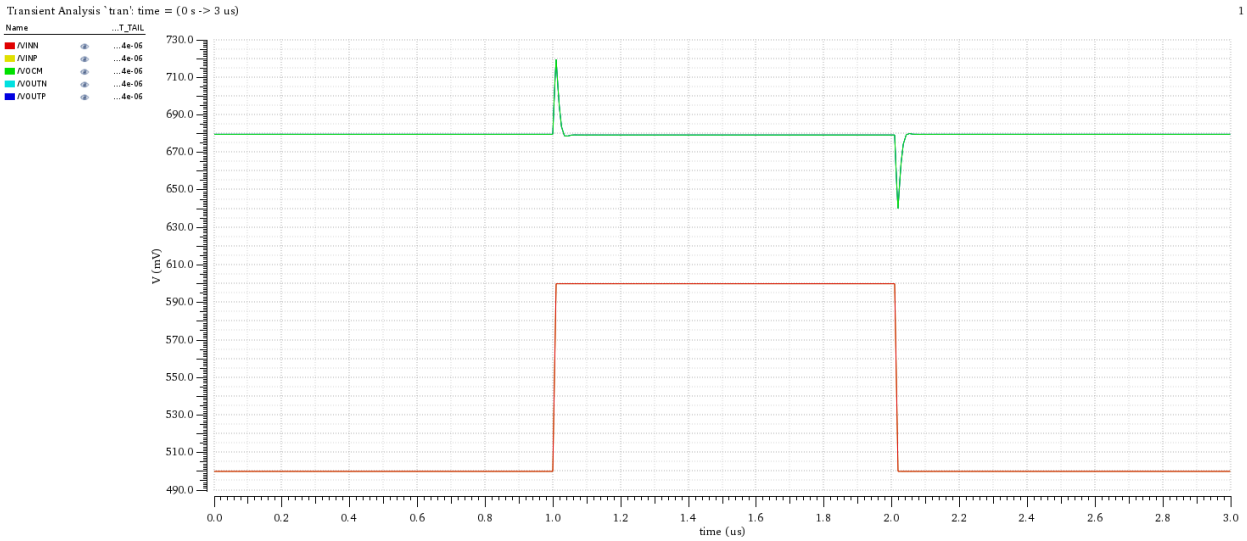


Figure 40:vodiff vs time

	WACT_TAIL	ymax(v(...tran"))
1	9.984E-6	199.8E-3

2) Differential and CMFB loops stability (transient analysis): CM input pulse

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



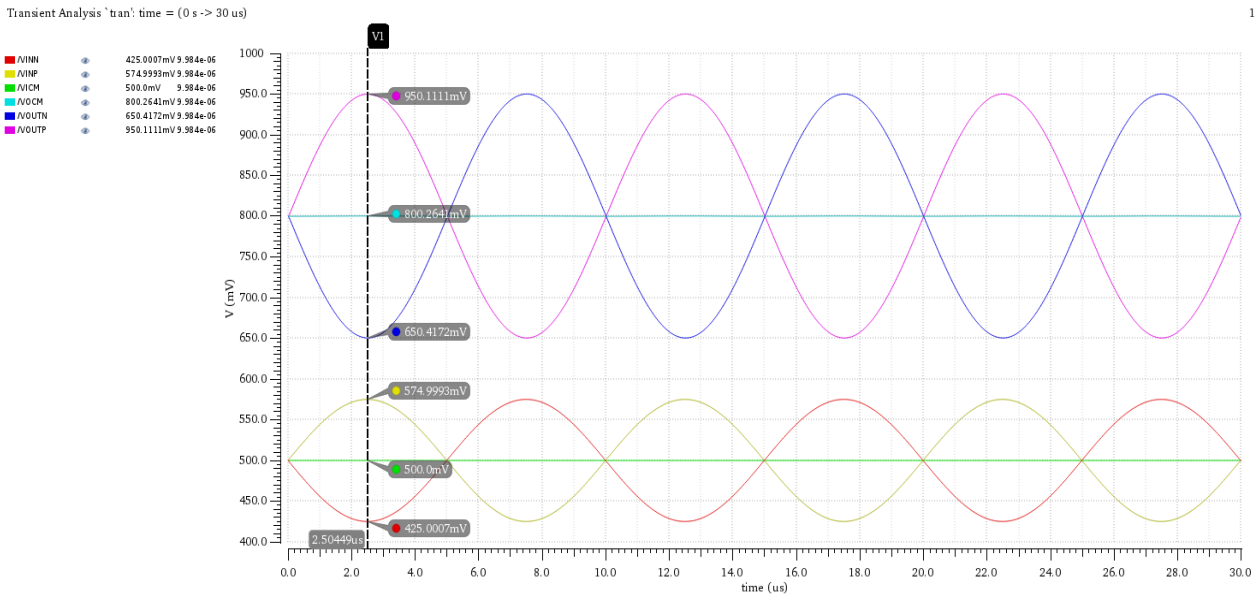
Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

- No, there is no differential or common-mode ringing observed in the transient response. Both loops are stable with adequate phase margin the differential loop has a high PM of 88.9°, and the CMFB loop has a robust PM of 70.7°

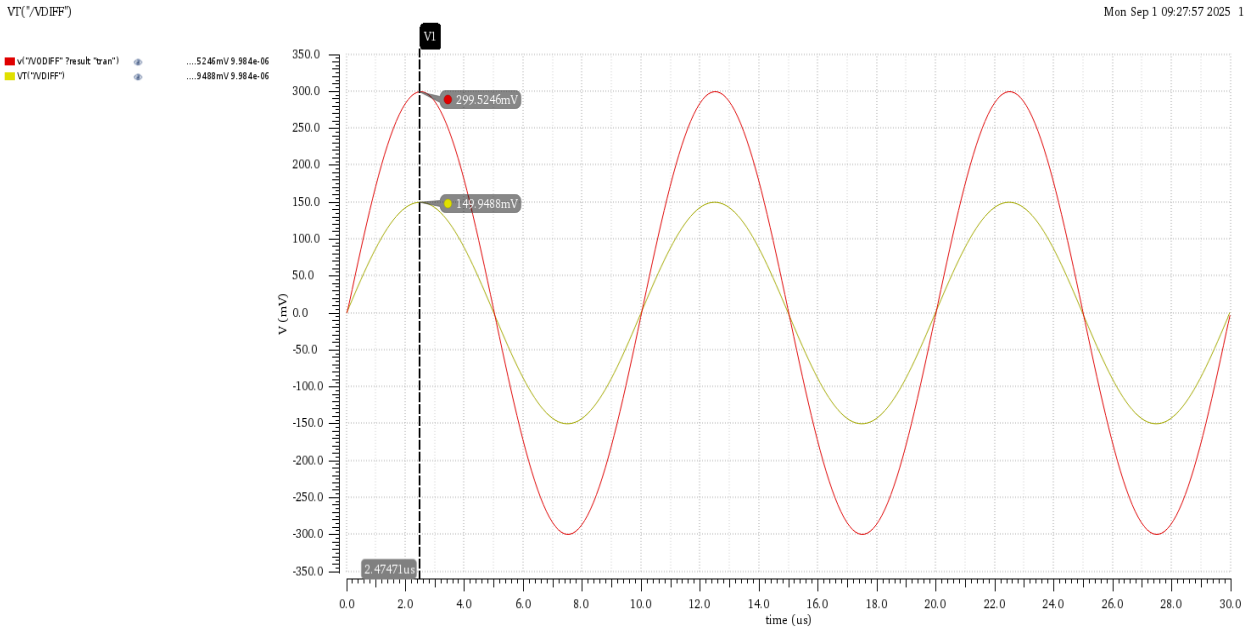
3) Output swing:

I have increased VREF a little to avoid overlapping between curves

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



Calculate the diff input and output peak-to-peak swings and the closed loop gain.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_mini_project:part_3:1	DIFF OUTPUT P_P	599.3m			
lab11_mini_project:part_3:1	DIFF INPUT P_P	300m			

Figure 41: diff input & output peak to peak

	Expression	Value
1	ymax(value(v("...	1.998

Figure 42:Closed loop gain

Part7(Optional): vcascn & vcascb implementation

NOTE: I will repeat this part again with magic battery as we got in lab 3

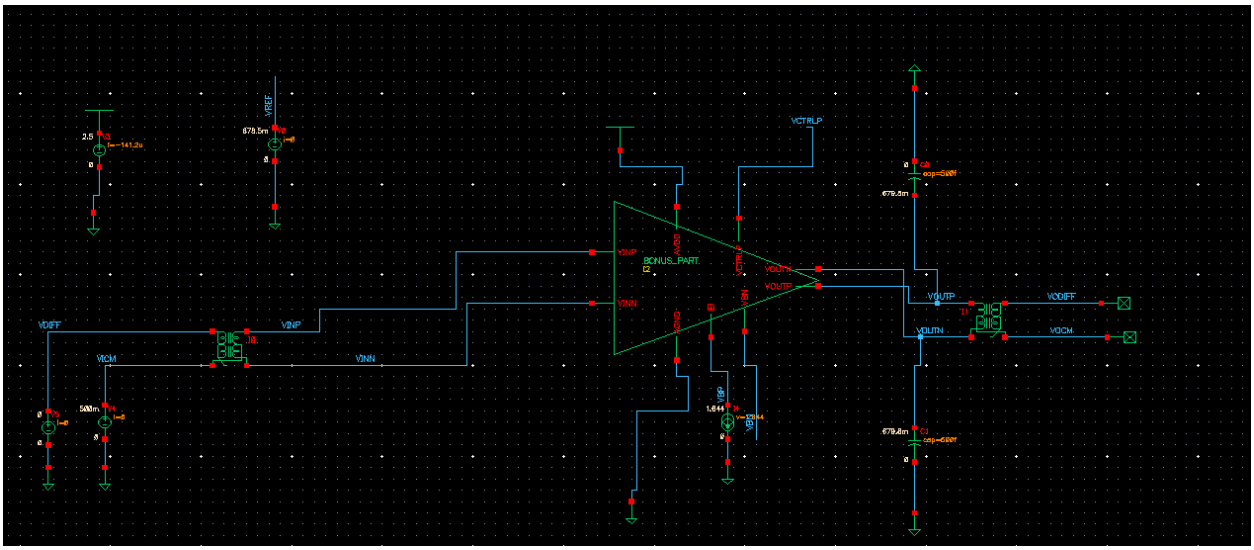


Figure 43:schematic

I have removed vcascn & vcascb sources because we will do battery with transistors instead of them

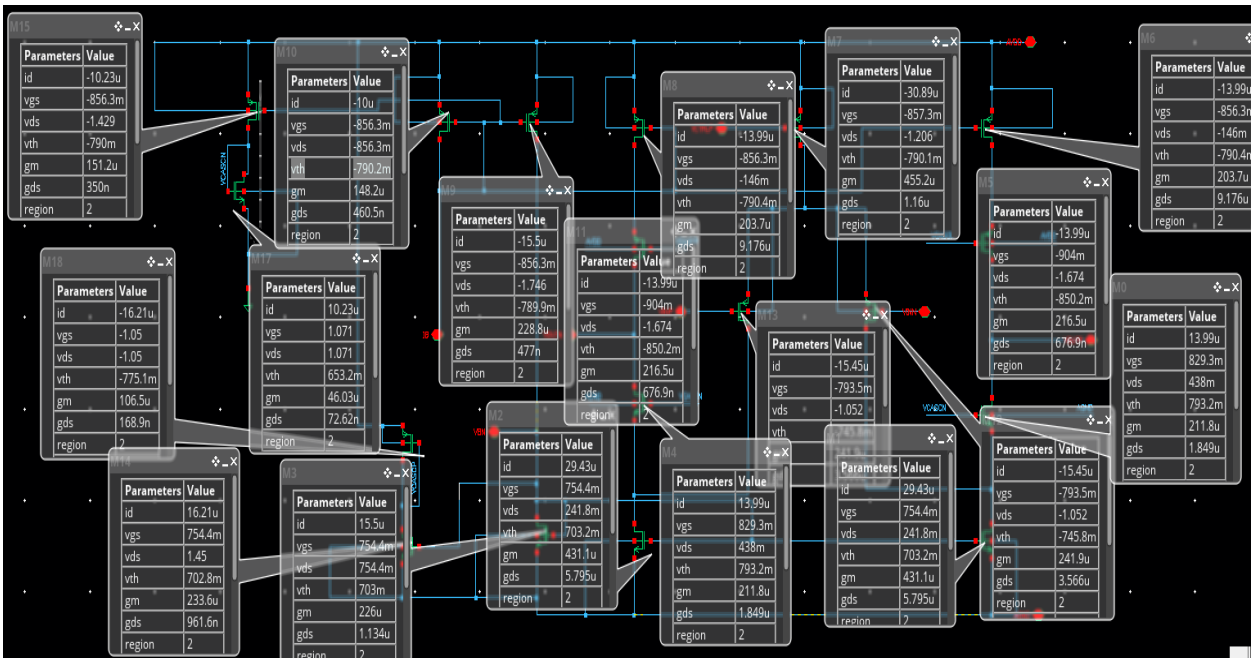


Figure 44: OTA op annotated

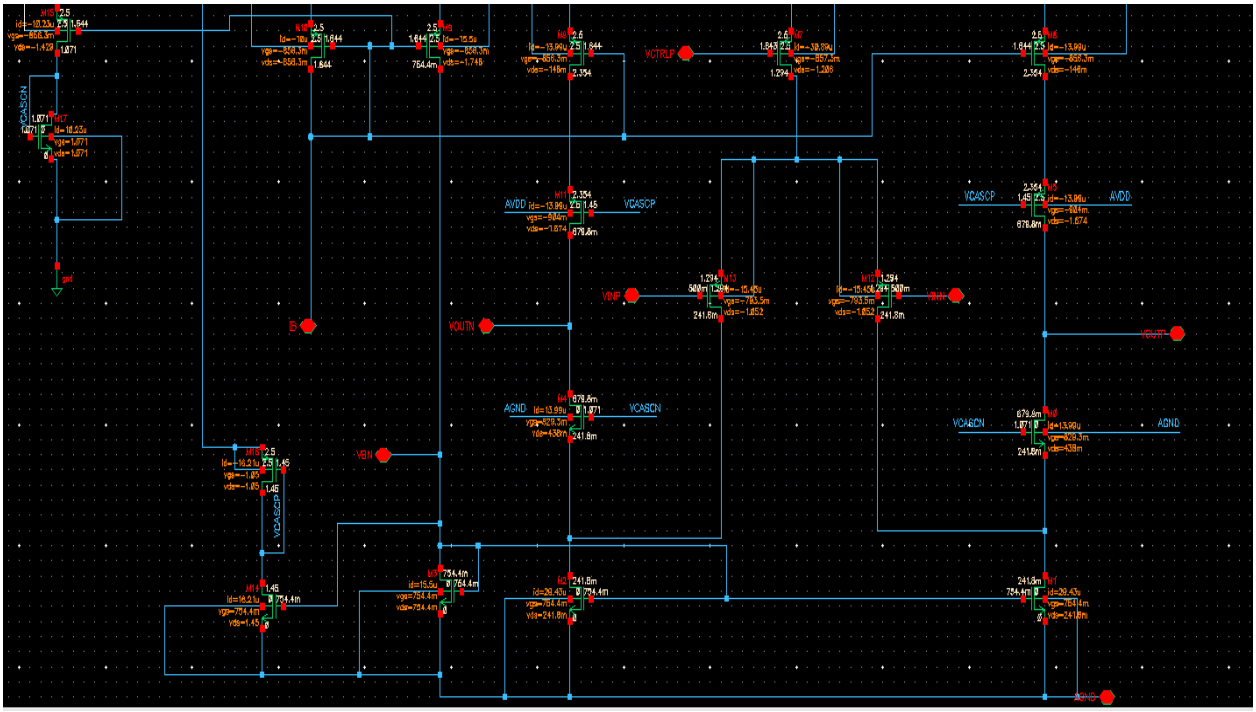


Figure 45: ota dc nodes annotated

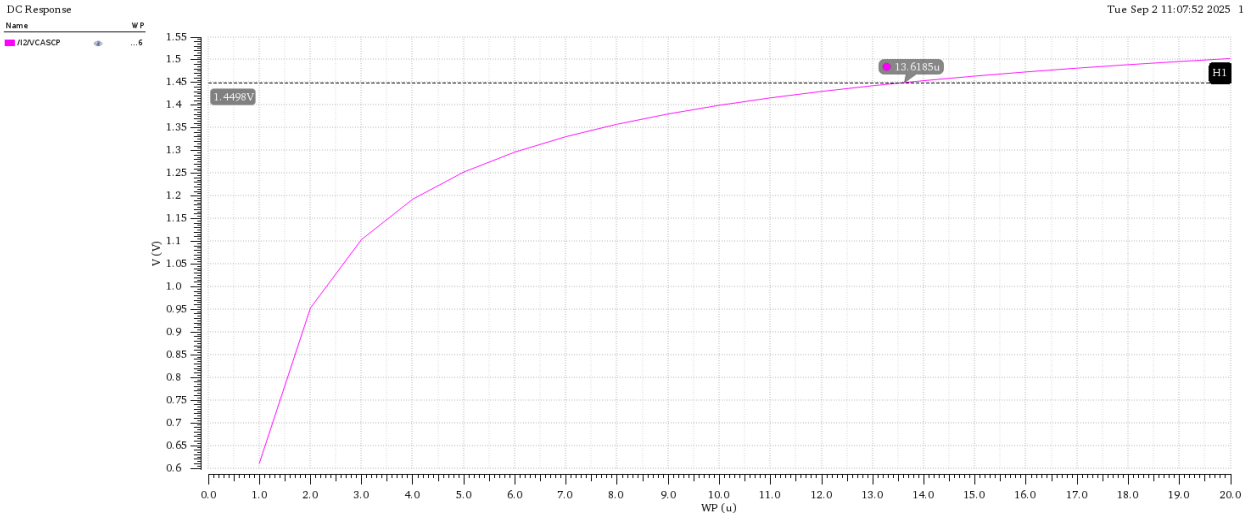


Figure 47:wp vs vcascp

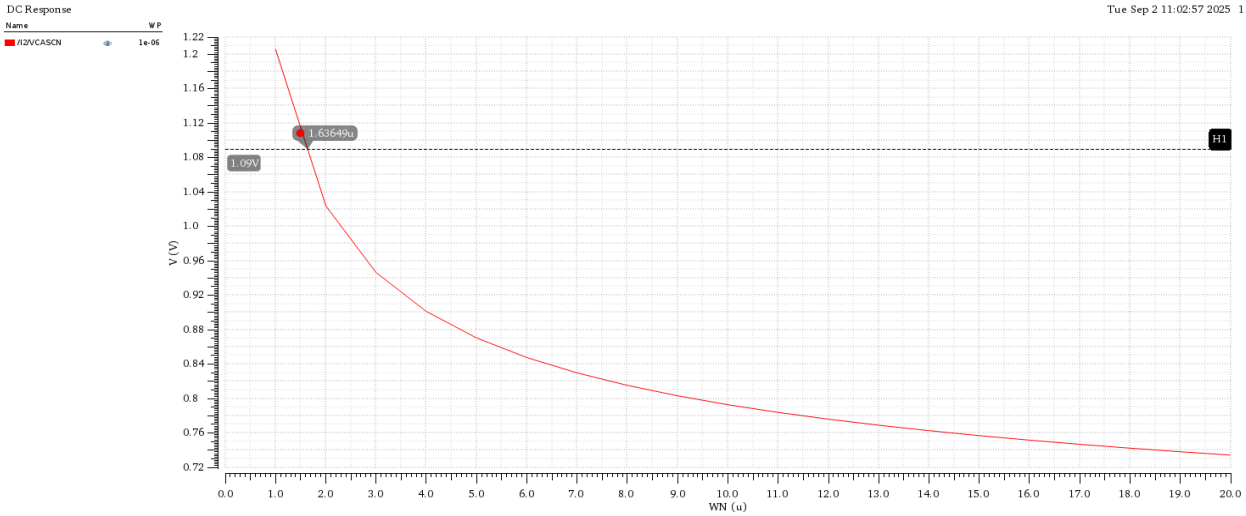


Figure 46:wn vcascn

2) Diff small signal ccs:

Test	Output	Nominal	Spec	Weight	Pass/Fail
ab11_mini_project:BONUS_PART_new:1	AO	2.941k			
ab11_mini_project:BONUS_PART_new:1	AO_dB	69.37			
ab11_mini_project:BONUS_PART_new:1	BW	22.91k			
ab11_mini_project:BONUS_PART_new:1	UGF	67.68M			
ab11_mini_project:BONUS_PART_new:1	GBW	67.55M			
ab11_mini_project:BONUS_PART_new:1	PM	82.43			

Part7(Optional): vcascn & vcascb implementation with magic battery

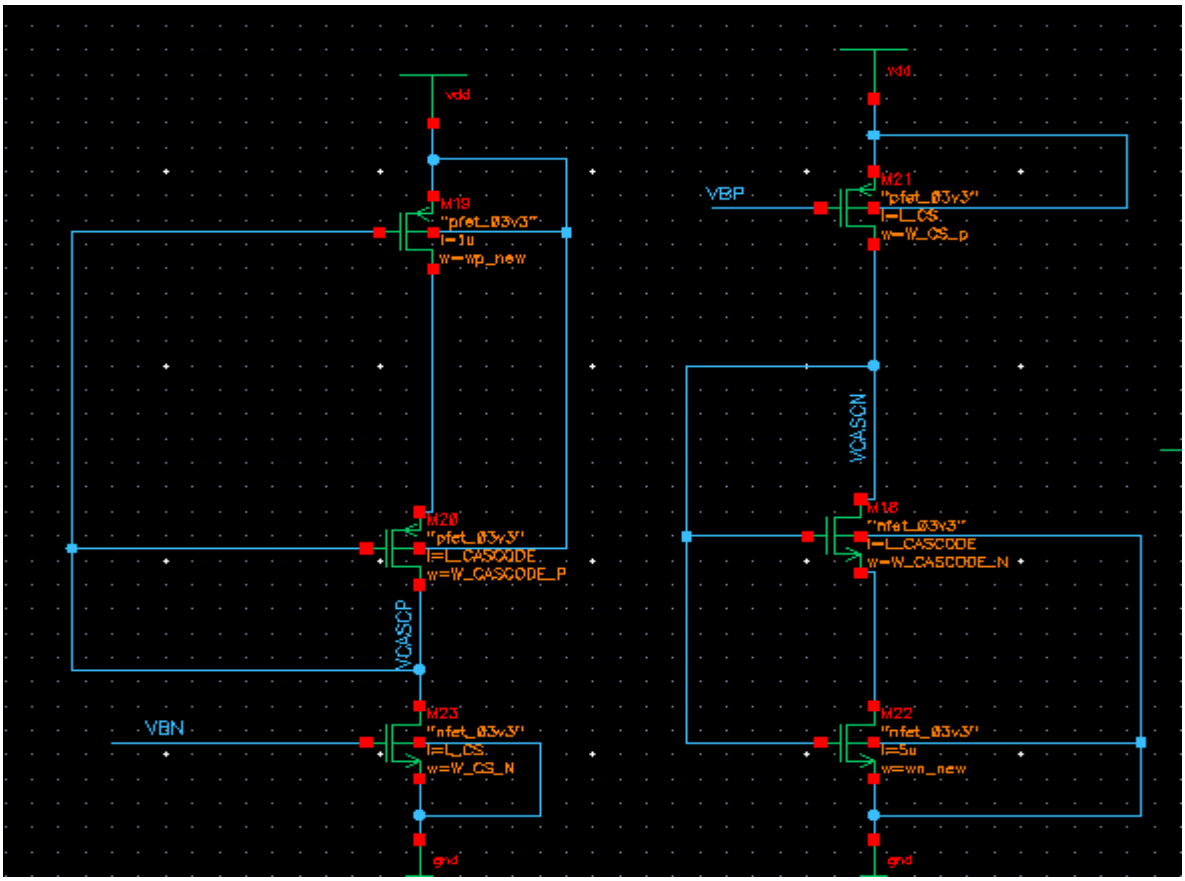


Figure 48: vcascn&vcascp magic battery

I have removed dc sources and replaced them with magic battery as shown and their sizing, now I will run op to sweep vcascn vs wn and vcascp vs wp to compensate dc sources

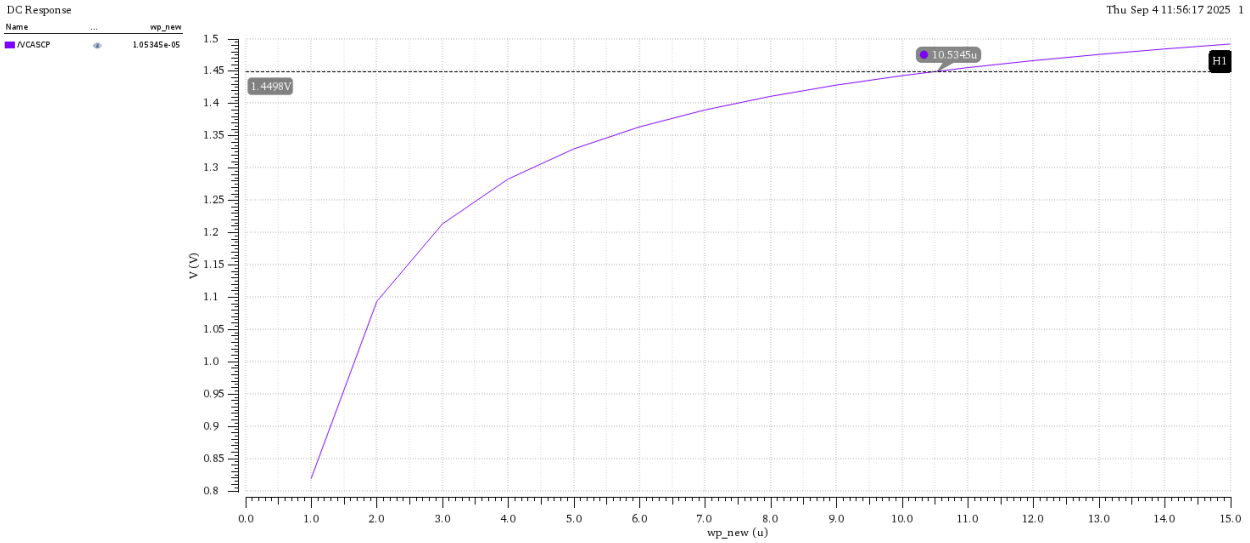


Figure 49:vcascp vs wp

As shown: WP=10.5345u

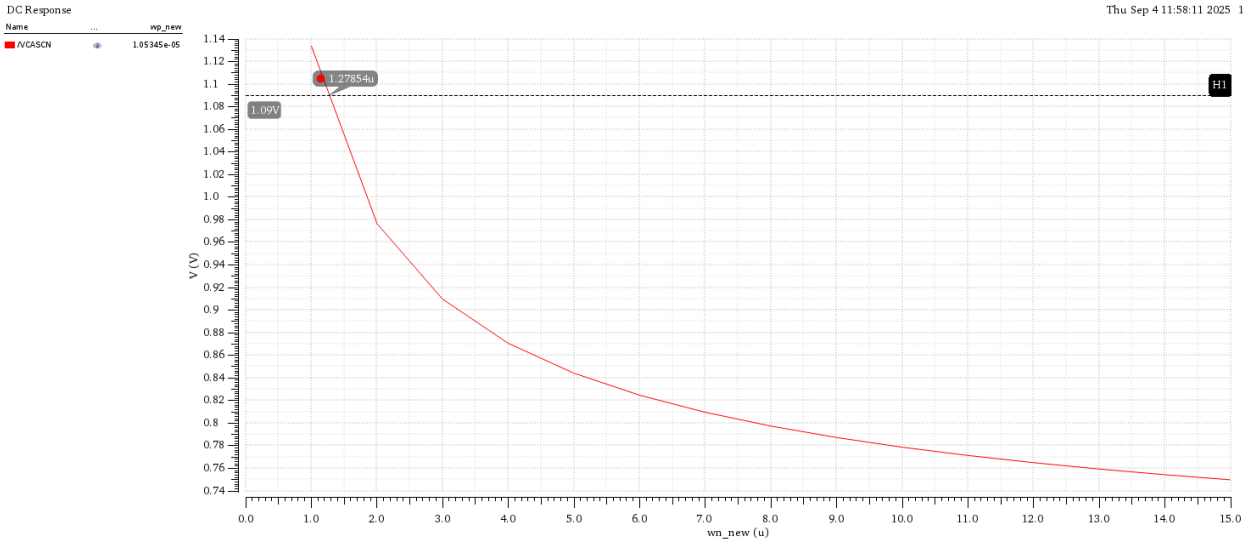


Figure 50:vcascn vs Wn

As shown: Wn=1.27854u

DC OP:

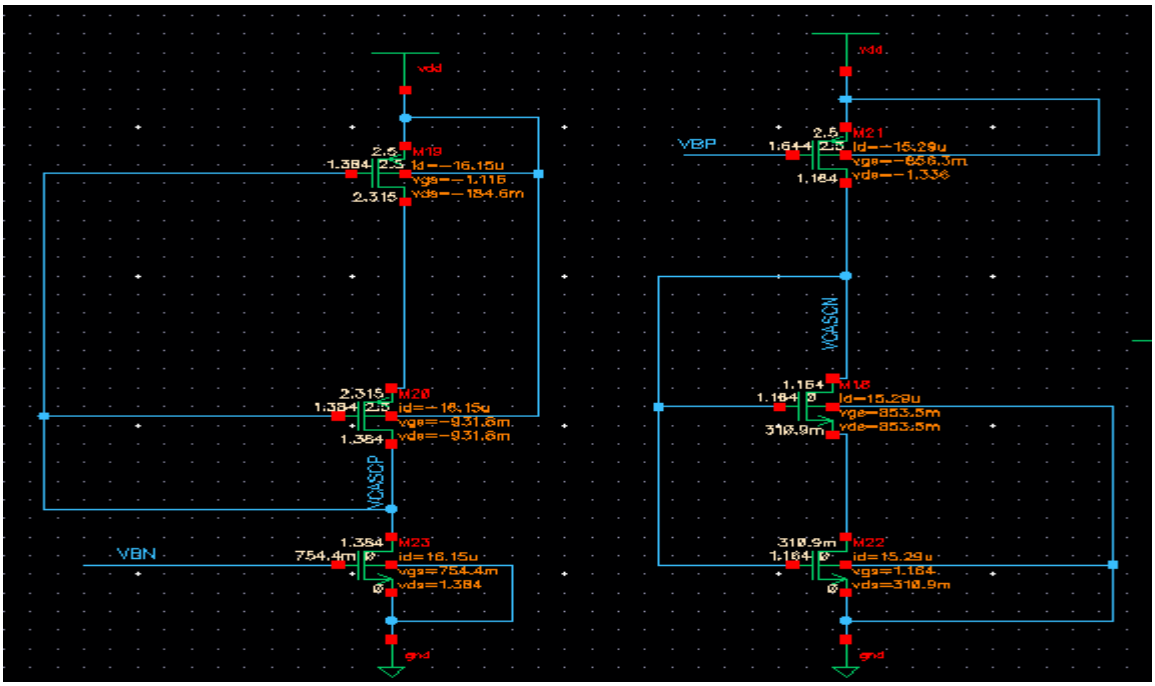


Figure 51: magic battery op annotated

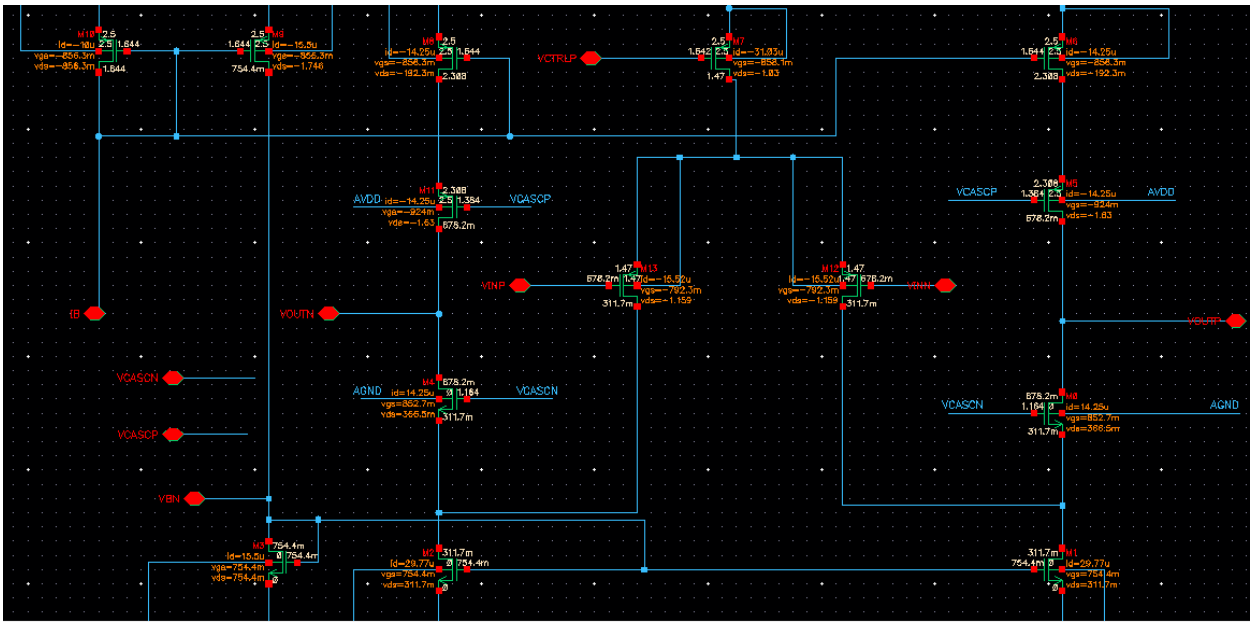


Figure 52: OTA op annotated

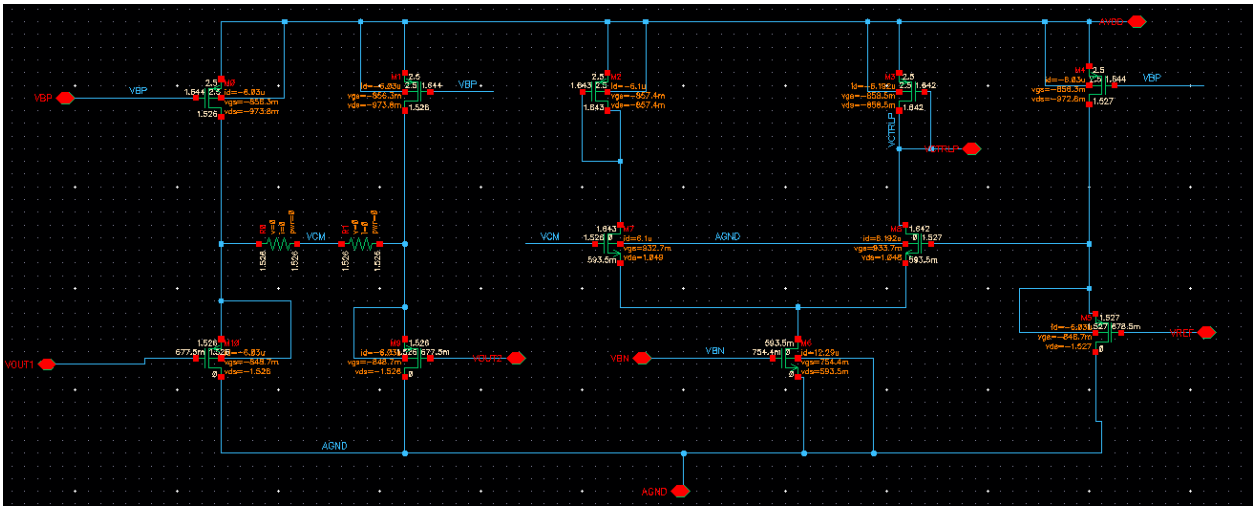


Figure 53: CMFB annotated

Now I will run AC to see (GAIN,BW, GBW,UGF):

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11_mini_project:part_3:1	A0	1.998			
lab11_mini_project:part_3:1	A0_dB	6.013			
lab11_mini_project:part_3:1	BW	11.73M			
lab11_mini_project:part_3:1	UGF	22.42M			
lab11_mini_project:part_3:1	GBW	23.21M			

As shown from op and ac ⟶ from magic battery I could compensate dc sources and I got the same results with magic battery

Thank you for your efforts……..