Ain shams university
Faculty of engineering
Computer engineering and software systems programs

Course: EDA (CSE215)

Project 3

Submitted by: Shehab Ahmed Hassan Kotb

Id: 16p6014

Email : shehabktob@gmail.com

Submitted to: Dr. Mohamed Dessouky
Eng. Michael Hany

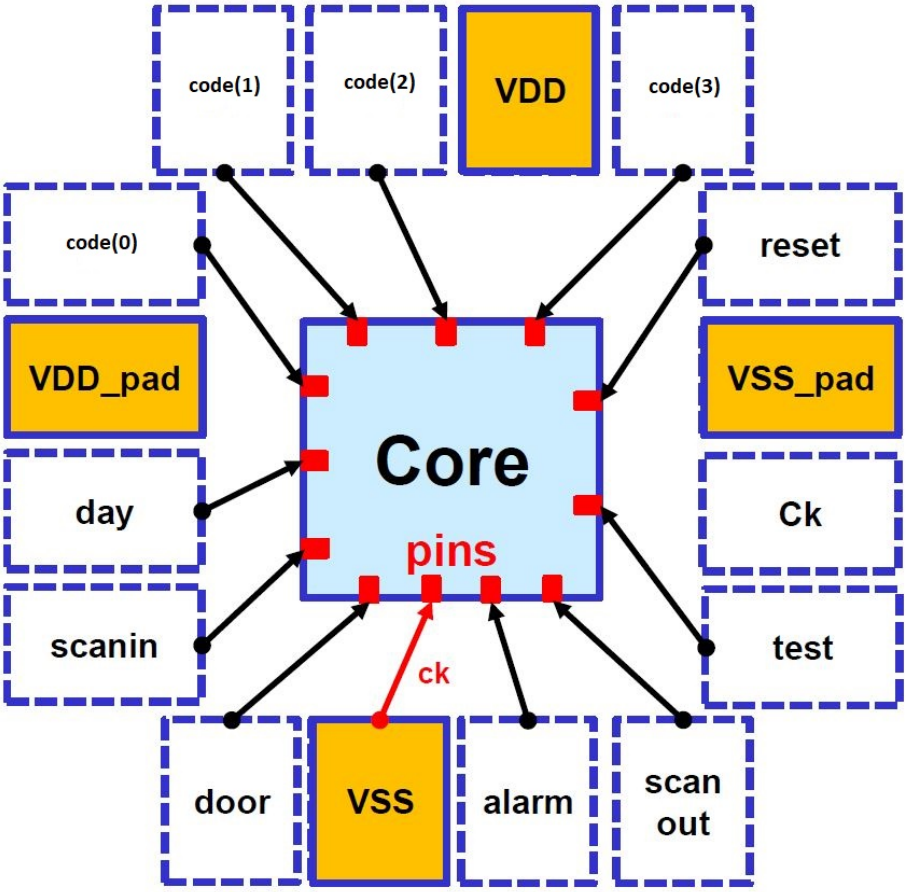
Table of Contents

1.0 Introduction

This document covers the Physical Synthesis portion of a Digital access control system, it's high level design & low-level synthesis was already covered in the previous documents.

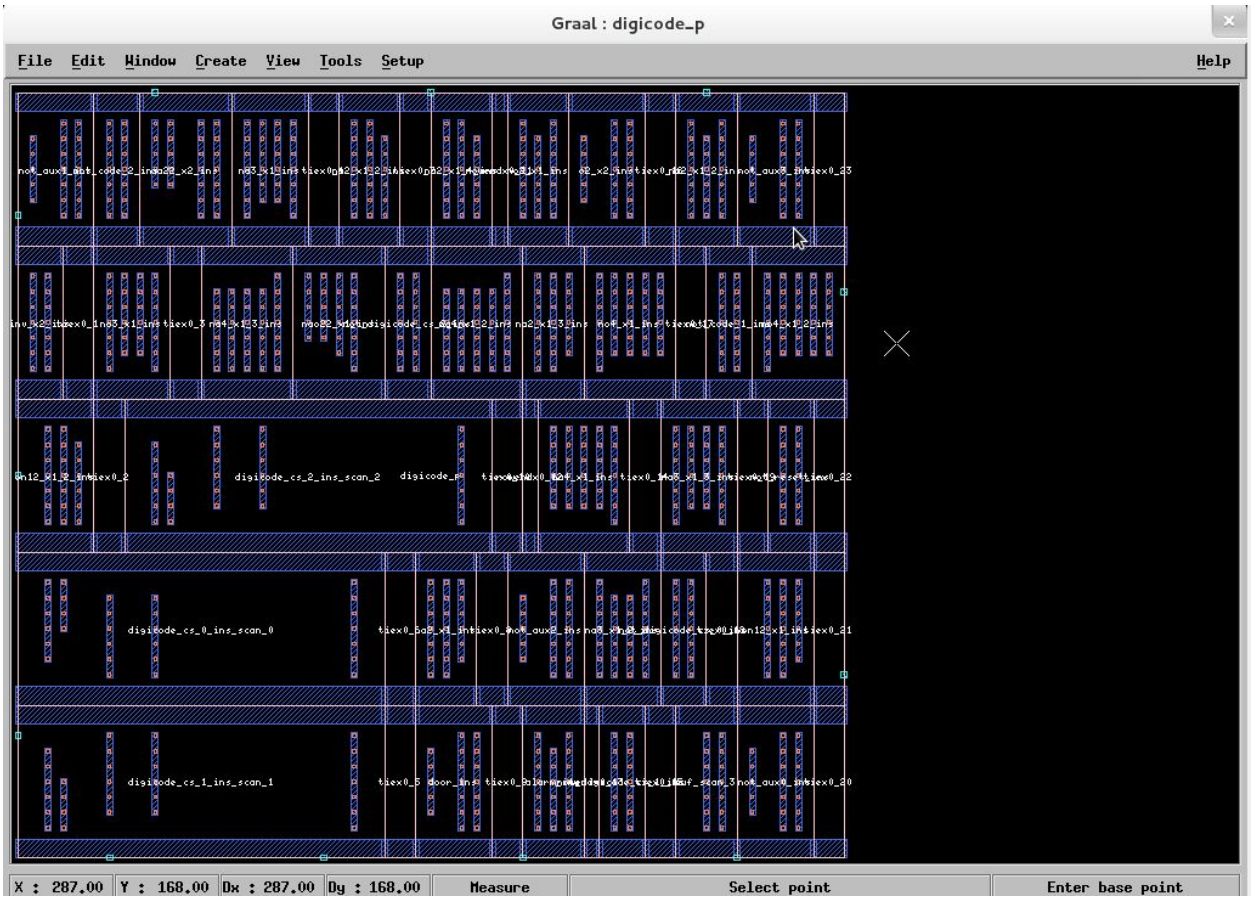
The physical synthesis is achieved by using alliance tool such as ocp, nero, s2r; the output of these tool is detailed bellow.

2.0 Floor plan



3.0 Placement

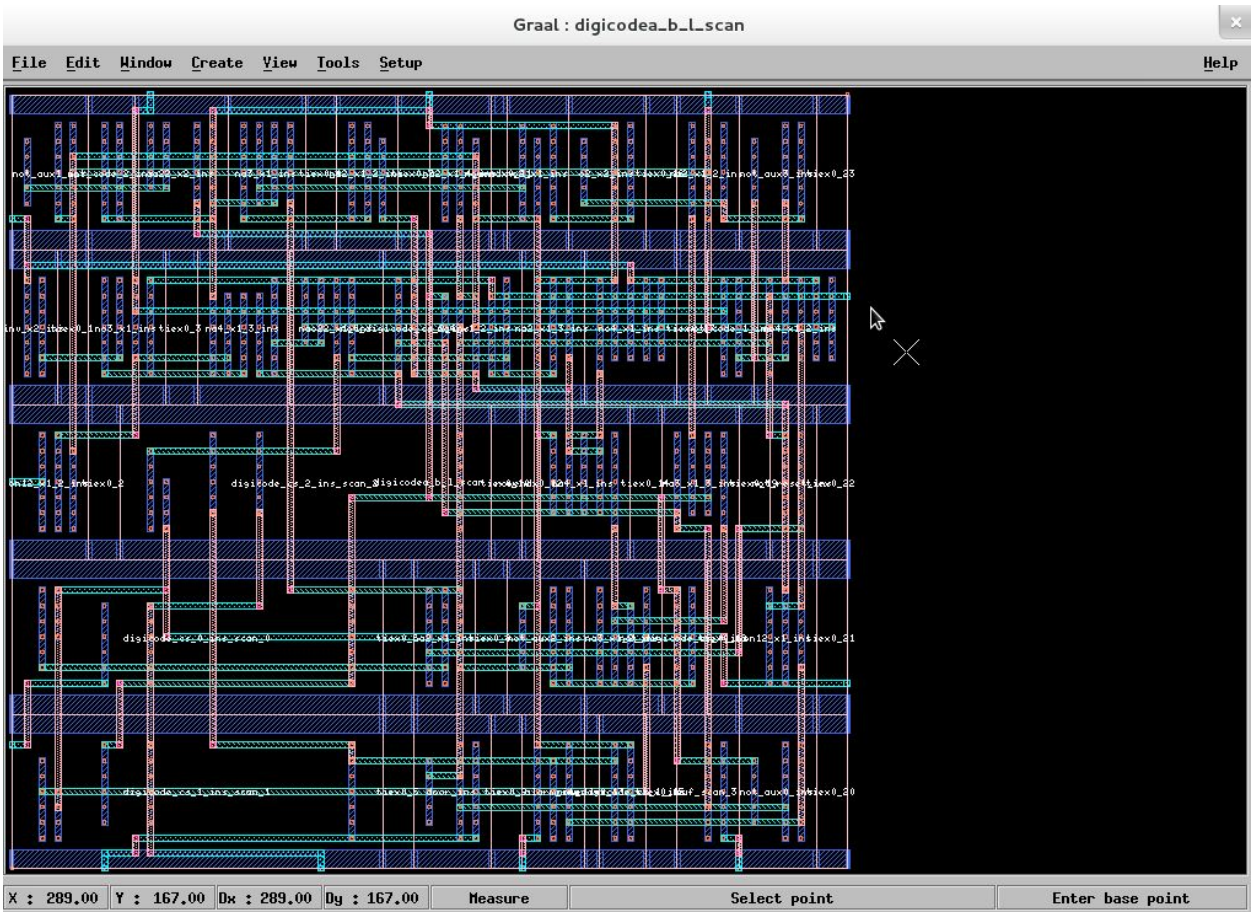
Ocp netlist



.ioc file is found in the appendix.

4.0 routing

Nero netlist

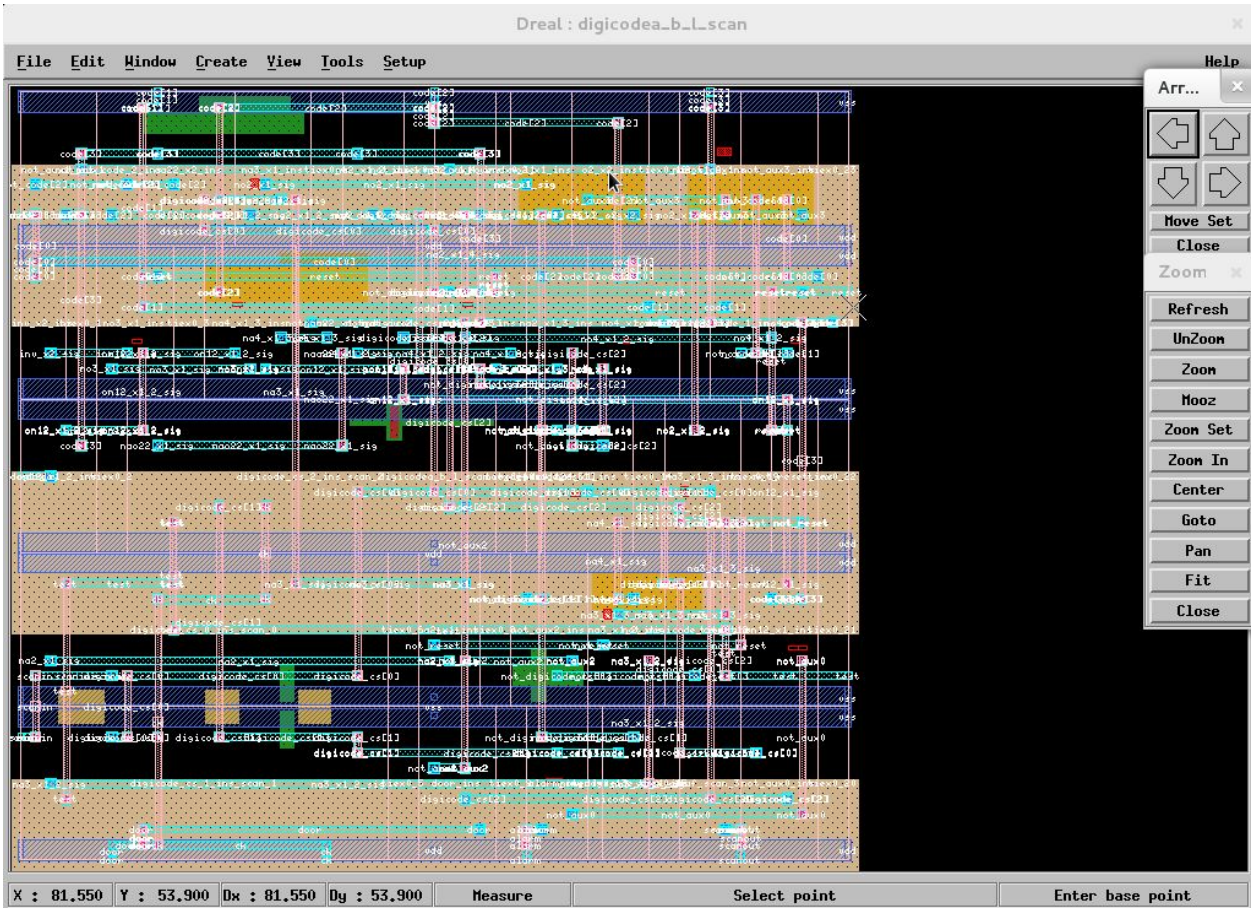


5.0 post-layout verification

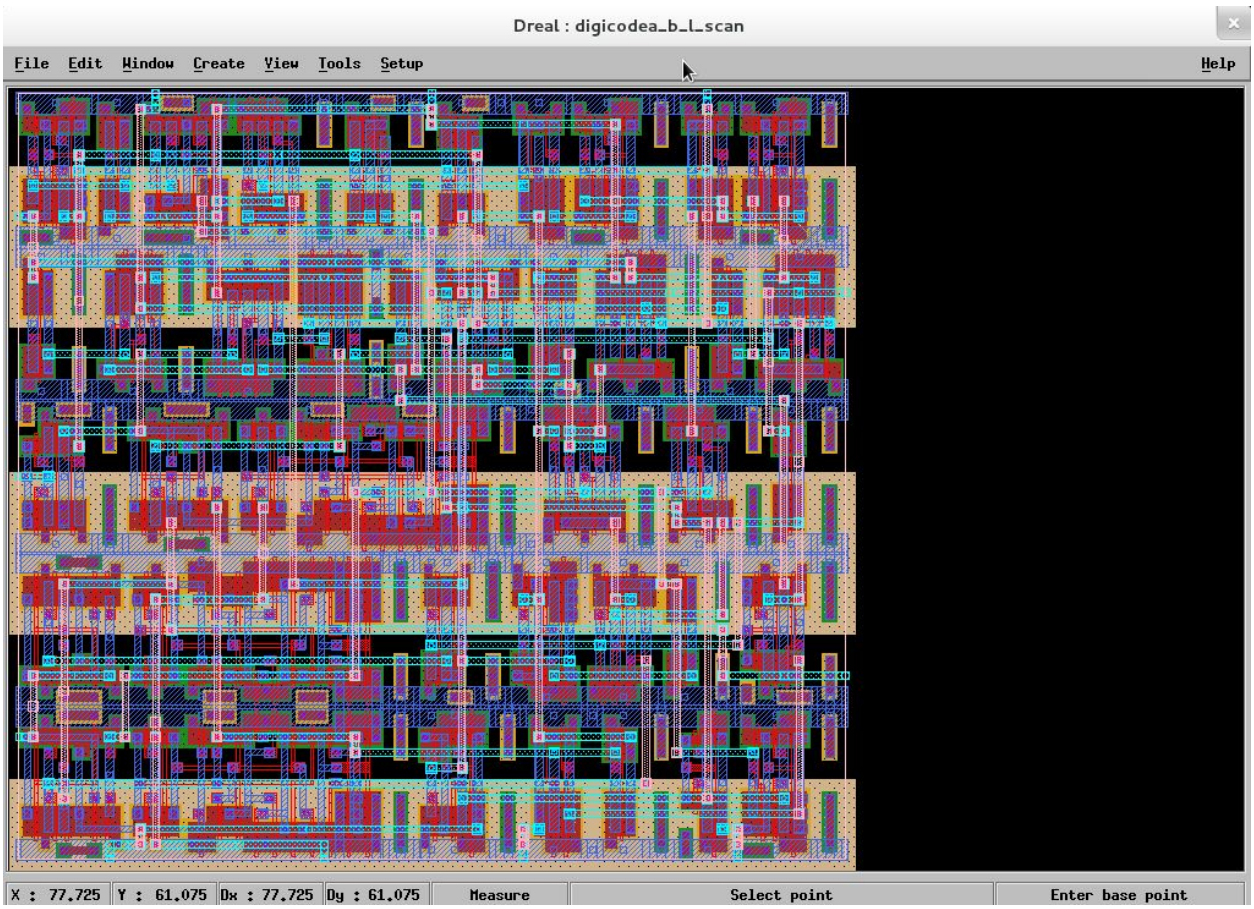
Log file are found in the appendix.

6.0 symbolic to real conversion

Unflattened layout



Flattened layout



Appendix

.ioc file

```
LEFT(
(IOPIN scanin.0 );
(IOPIN day.0 );
(IOPIN code(0).0 ); )
TOP (
(IOPIN code(1).0 );
(IOPIN code(2).0 );
(IOPIN code(3).0 ); )
RIGHT (
(IOPIN test.0 );
(IOPIN reset.0 ); )
BOTTOM (
(IOPIN door.0 );
(IOPIN ck.0 );
(IOPIN alarm.0 );
(IOPIN scanout.0 ); )

```

Cougar log

```
          @@@@ @
         @@    @@
        @@      @
       @@       @    @@@    @@@  @@@@    @@@@@@   @@@@    @@@ @@@
       @@          @@   @@   @@    @@   @@  @@   @@   @    @@@  @@
       @@         @@     @@  @@    @@   @   @@   @@   @@   @@   @@
       @@         @@     @@  @@    @@   @   @      @@@@@   @@
       @@         @@     @@  @@    @@    @@@     @@   @@   @@
        @@      @ @@     @@  @@    @@   @@      @@    @@   @@
         @@    @@  @@   @@   @@   @@@   @@@@@@  @@   @@@   @@
          @@@@      @@@      @@@@  @@ @@   @@@  @@@@  @@ @@@@
                                          @     @
                                           @@@@@

                    Netlist extractor ... formerly Lynx

               Alliance CAD System 5.0 20090901, cougar 1.21
               Copyright (c) 1998-2019,       ASIM/LIP6/UPMC
               Author(s):  Ludovic Jacomme and Gregoire Avot
               Contributor(s):              Picault Stephane
               E-mail        :   alliance-users@asim.lip6.fr

---> Parse technological file ./techno/techno-035.rds

     RDS_LAMBDA        = 24
     RDS_UNIT          = 80
     RDS_PHYSICAL_GRID = 2
     MBK_SCALE_X       = 100

---> Extract symbolic figure digicodea_b_1_scan

   ---> Translate Mbk -> Rds

   ---> Build windows
   <--- 72

   ---> Rectangles    : 1177
   ---> Figure size   : (   -116,   -116 )
                        (  27116,  25116 )

   ---> Cut transistors
   <--- 0
   ---> Build equis
   <--- 52
   ---> Delete windows
   ---> Build signals
   <--- 52
   ---> Build instances
   <--- 60
   ---> Build transistors
   <--- 0
   ---> Save netlist

<--- done !

---> Total extracted capacitance
<--- 0.0pF
```

Lvx log

```
                    @@@@@@      @@@@    @@@ @@@@   @@@@
                      @@         @@      @   @@     @
                      @@         @@      @    @@   @
                      @@          @@     @      @@ @
                      @@         @@     @       @@
                      @@          @@  @         @@
                      @@          @@  @         @@@
                      @@           @@@         @  @@
                      @@      @    @@@        @    @@
                      @@     @       @       @      @@
                    @@@@@@@@@@       @      @@@    @@@@

                         Gate Netlist Comparator

                Alliance CAD System 5.0 20090901,   lvx 1.4
                Copyright (c) 1992-2019,     ASIM/LIP6/UPMC
                E-mail        : alliance-users@asim.lip6.fr


***** Loading and flattening digicodea_b_l_scan (vst)...

***** Loading and flattening digicodea_b_l_scan (al)...


***** Compare Terminals .............
***** O.K.  (0 sec)

***** Compare Instances ..........
***** O.K.  (0 sec)

***** Compare Connections .............
***** O.K.  (0 sec)

===== Terminals .......... 14
===== Instances .......... 37
===== Connectors ......... 213


***** Netlists are Identical. ***** (0 sec)
```

Druc log

```
                    @@@@@@@    @@@@@@@                  @@@@ @
                      @@   @@     @@   @@              @@    @@
                      @@    @@    @@    @@             @@     @
                      @@     @@   @@   @@  @@@  @@@@ @@      @
                      @@     @@   @@  @@    @@   @@ @@
                      @@     @@   @@@@@     @@   @@ @@
                      @@     @@   @@  @@    @@   @@ @@
                      @@     @@   @@   @@   @@   @@ @@
                      @@    @@    @@   @@   @@   @@   @@     @
                      @@   @@     @@    @@  @@  @@@   @@    @@
                    @@@@@@@     @@@@@   @@@  @@@@ @@    @@@@

                              Design Rule Checker

                     Alliance CAD System 5.0 20090901,  druc 5.0
                     Copyright (c) 1992-2019,     ASIM/LIP6/UPMC
                     E-mail        : alliance-users@asim.lip6.fr

Flatten DRC on: digicodea_b_l_scan
Delete MBK figure : digicodea_b_l_scan
Load Flatten Rules : ./techno/techno-symb.rds

Unify : digicodea_b_l_scan

Create Ring : digicodea_b_l_scan_rng
Merge Errorfiles:

Merge Error Instances:
instructionCourante : 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56
End DRC on: digicodea_b_l_scan
Saving the Error file figure
Done
5821

Some errors have been detected, see file: digicodea_b_l_scan.drc for detailled
```

```
#-------digicode-----------------------------------------#

all: digicodea.vbe \
     digicodej.vbe \
     digicodem.vbe \
     digicodeo.vbe \
     digicoder.vbe \
     digicode_boom \
     digicode_boog \
     digicode_loon
         @echo "<-- Generated"

all_vbe: digicodea.vbe \
         digicodej.vbe \
         digicodem.vbe \
         digicodeo.vbe \
         digicoder.vbe
            @echo "<-- Generated"

#-------Finite State Machine Synthesis-----------------#

vhd_to_fsm:
    rename .vhd .fsm *.vhd

digicodea.vbe: digicode.fsm
    @echo "    Encoding Synthesis -> digicodea.vbe"
    syf -CEV -a digicode

digicodej.vbe: digicode.fsm
    @echo "    Encoding Synthesis  -> digicodej.vbe"
    syf -CEV -j digicode

digicodem.vbe: digicode.fsm
    @echo "    Encoding Synthesis  -> digicodem.vbe"
    syf -CEV -m digicode

digicodeo.vbe: digicode.fsm
    @echo "    Encoding Synthesis  -> digicodeo.vbe"
    syf -CEV -o digicode

digicoder.vbe: digicode.fsm
    @echo "    Encoding Synthesis  -> digicoder.vbe"
    syf -CEV -r digicode

#-------BOOM    ------------------------------------#

digicode_boom : digicodea_b.vbe digicodej_b.vbe digicodem_b.vbe \
            digicodeo_b.vbe digicoder_b.vbe
%_b.vbe : %.vbe
    @echo "    Boolean Optimization -> $@ "
    boom -V -d 50 $* $*_b > $*_boom.out

#-------BOOG    ------------------------------------#


digicode_boog : digicodea_b.vst digicodej_b.vst digicodem_b.vst \
            digicodeo_b.vst digicoder_b.vst
%.vst : %.vbe laxfile.lax
    @echo "    Binding and optimizing on Gates -> $@ "
    boog $* $* -l laxfile > $*_boog.out


#-------LOON    ------------------------------------#


digicode_loon : digicodea_b_l.vst digicodej_b_l.vst digicodem_b_l.vst \
```

```
            digicodeo_b_l.vst digicoder_b_l.vst
%_l.vst : %.vst laxfile.lax
    @echo " Netlist Optimization -> $@ "
    loon $* $*_l -l laxfile > $*_loon.out


#-------PROOF   ---------------------------------------#



%_b_l_net.vbe : %_b_l.vst %.vbe
    @echo " Formal checking -> $@ "
    flatbeh $*_b_l $*_b_l_net > $*_flatbeh.log
    proof -d $* $*_b_l_net > $*_proof.log

#-------SCAN   ---------------------------------------#
ac_scapin_registers:
    cat digicodea_b_l.vst | grep sff

%_scan.vst : %.vst scan.path
    @echo " scan-path insertion -> $@ "
    scapin -VRB $* scan $*_scan > scapin.out

#-------OCP   ----------------------------------------#

ocp : digicode_p.ap
digicode_p.ap : digicode.ioc digicodea_b_l_scan.vst
    MBK_IN_LO=vst; export MBK_IN_LO;\
    MBK_OUT_PH=ap; export MBK_OUT_PH;\
    ocp -v -ring -ioc digicode digicodea_b_l_scan digicode_p > ocp.out

#-------NERO   ---------------------------------------#

nero : digicodea_b_l_scan.ap
digicodea_b_l_scan.ap: digicode_p.ap digicodea_b_l_scan.vst
    nero -V -p digicode_p digicodea_b_l_scan digicodea_b_l_scan > nero.out

#------COUGAR-LVX   ----------------------------------------#

%.al : %.ap
    MBK_OUT_LO=al; export MBK_OUT_LO; \
    export RDS_TECHNO_NAME=./techno/techno-035.rds; \
    cougar -v $* > cougar_$*.out
    lvx vst al $* $* -f > lvx_$*.out

#------DRUC   ----------------------------------------#

druc_core : digicodea_b_l_scan.ap
    export RDS_TECHNO_NAME=./techno/techno-symb.rds; \
    druc digicodea_b_l_scan > druc_core.out

#------S2r   ----------------------------------------#
digicode_chip.cif : digicodea_b_l_scan.ap
    export RDS_TECHNO_NAME=./techno/techno-035.rds; \
    export RDS_OUT=cif; \
    s2r -v -r digicodea_b_l_scan > s2r.out

#-------Clean Up----------------------------------------#

clean :
    rm -f  *.vbe *.enc *.vst *.out *.xsc *0.lax *~
    @echo "Erase all the files generated by the makefile"


```