Introduction:

This project uses CMOS to construct an Exclusive-NOR (XNOR) logic circuit. The design uses two inverters and two transmission gates. XNOR is a digital logic gate that outputs high only when both inputs are identical. Using CMOS logic allows for low power consumption and efficient switching, making it ideal for digital systems. This implementation demonstrates how basic CMOS components can be combined to perform complex logic functions effectively.

Literature Review:

The Exclusive-NOR gate is a fundamental component in digital logic design, known for its role in equality checking between binary inputs. CMOS technology is widely used in implementing logic gates due to its:

- Low power consumption.
- High noise immunity.
- Scalability.

Several studies have explored different CMOS designs for XNOR gates. For instance, some designs utilize 8–10 transistors, while others aim to reduce transistor count for improved area efficiency. Compared to traditional methods, our design uses only two inverters and two transmission gates, leading to a more compact and energy-efficient circuit. This approach simplifies the circuit while maintaining correct logic behaviour, which makes it suitable for low-power applications and educational demonstrations.

Our work differs from previous implementations by focusing on a minimalist structure, leveraging basic CMOS components while still achieving correct XNOR functionality. This also facilitates easier simulation and verification through Verilog.

Description of circuit:

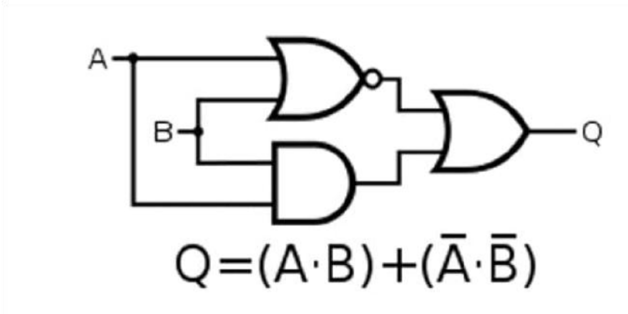
Truth table

A	B	XNOR ($A \odot B$)
0	0	1
0	1	0
1	0	0
1	1	1

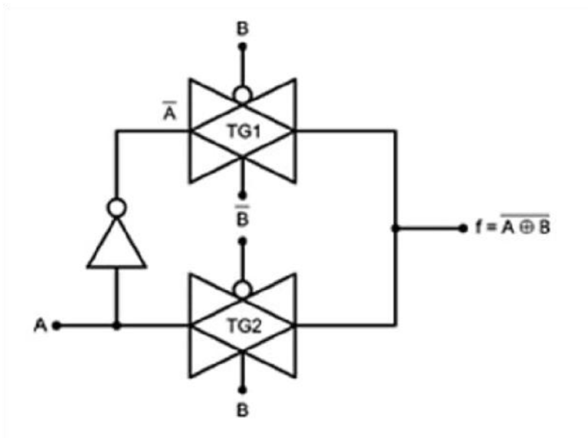
k-map

	0	1
0	1	0
1	0	1

Circuit diagram



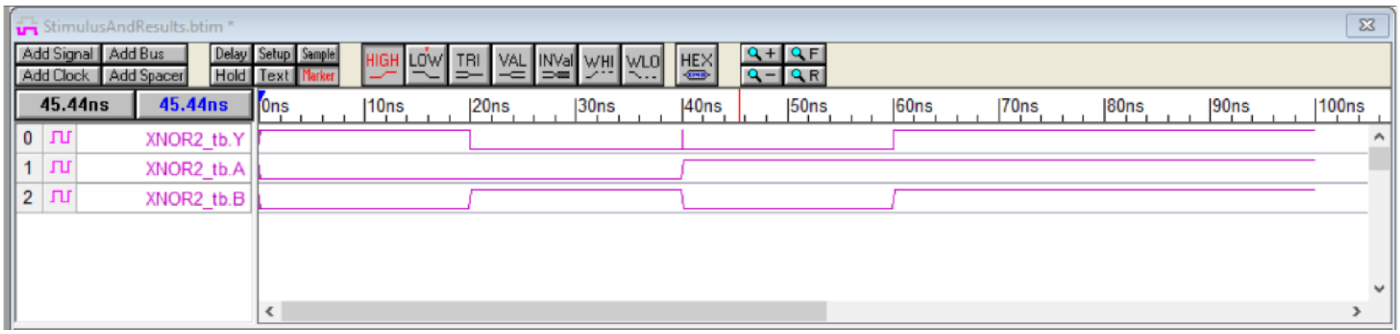
CMOS Circuit diagram



Truth table for output

A	B	$\bar{A}$	$\bar{B}$	T1_out	T2_out	XNOR_out
0	0	1	1	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

Results:



Discussion and comments:

While running the Verilog simulation, our results matched the expected behaviour of an XNOR gate. The output was high (1) when both inputs were the same (either 0 and 0 or 1 and 1), and low (0) when the inputs differed. This confirms that the combination of inverters and transmission gates was correctly modelled and implemented.
One observation is that the design efficiently uses logic resources, confirming the benefits of the transmission gate approach in terms of simplicity and power efficiency. The Verilog code also shows clear modularity, making it suitable for integration into larger digital systems or further optimization in future work.
This project illustrates the practical value of combining theoretical circuit analysis with hardware description languages for simulation and testing, which is an essential skill in modern VLSI design workflows.
From the simulation results, we can see the two input signals, “A” and “B”, and the output signal, “Y”, of the XNOR gate.
To verify the operation of the XNOR gate, we applied all possible cases to the input, and as shown from the timing diagram, the output is similar to the truth table of the XNOR gate, so the circuit is verified.

References:

- Weste, N. H. E., & Harris, D. (2010). *CMOS VLSI Design: A Circuits and Systems Perspective*. Addison-Wesley.
- Mano, M. M., & Ciletti, M. D. (2013). *Digital Design with an Introduction to the Verilog HDL*. Pearson.
- Verilog simulation and design references: https://www.edaplayground.com/
- CMOS logic gate design resources and tutorials from https://www.allaboutcircuits.com/