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Summary

I am a diligent and resourceful engineer with exceptional communication skills and leadership background. My technical interests include machine learning, natural language processing, statistical modeling, reinforcement learning, adversarial learning, systems security and deep learning. I am eager to contribute towards developing technology to move societies forward.

Education

University of California, San Diego, May 2022 GPA: 3.9
Ph.D in Computer Engineering, *Graduate Fellow*
Advised by Prof. Farinaz Koushanfar

University of Massachusetts Amherst, May 2015 GPA: 3.9
Bachelor of Science in Electrical Engineering, *Summa Cum Laude*

Mount Holyoke College, May 2014 GPA: 3.6
Bachelor of Arts in Physics, Minor in Computer Science, *Cum Laude*

Experience

University of California San Diego, CA Aug 2017 - Present
Graduate Research Assistant

- Member of the Adaptive Computing and Embedded Systems Lab focusing on security in machine learning, natural language processing, and hardware acceleration of deep neural networks.
- Presented research and accepted papers at various academic venues, workshops and conferences.

Intel Corporation July 2019 - Present
Santa Clara, CA
Graduate Machine Learning Intern

- Working on reinforcement learning for memory and SSD application as a part of the Non-Volatile Memory Systems Group.

Qualcomm Technologies, Inc. June 2018 – Aug 2018
San Diego, CA
Deep Learning R&D Intern

- Worked with the research team on applying deep reinforcement learning for optimizing power and performance management on Qualcomm chipsets.
- Implemented Dynamic Voltage Scaling using Reinforcement Learning and Recurrent Neural Networks.
- Designed and implemented alignment algorithms for creating the training dataset. Implemented data loader, model, trainers and evaluators using PyTorch.

GLOBALFOUNDRIES July 2015 – Aug 2017
Malta, NY
Process Engineer

- Applied statistical process control principles and created verification test plans to ensure early detection of process irregularities and minimize excursions for 14nm and 7nm technology node.
- Designed and implemented sampling algorithm in MATLAB to model advanced wafer level corrections for lithography scanner applications team. Work has led to scientific publication in SPIE Metrology and Process control for Microlithography journal.

University of Massachusetts, Amherst, MA Aug 2013 - Dec 2014
Teaching Assistant for CS Data Structures & ECE Embedded Systems Lab

- Assisted students with coding assignments and developing firmware projects for junior level embedded systems class such as programming Altera MAX 7000 and Atmel microcontrollers in verilog HDL to read and display serial MIDI input.

Publications

[1] **Universal Adversarial Perturbations for Speech Recognition Systems**
Paarth Neekhara*, Shehzeen Hussain*, Prakhar Pandey, Shlomo Dubnov, Julian McAuley, Farinaz Koushanfar
*INTERSPEECH 2019, [* Equal Contribution]*

[2] **Accelerating Autoregressive Convolutional Neural Networks on FPGA**
Shehzeen Hussain, Mojan Javaheripi, Paarth Neekhara, Ryan Kastner, Farinaz Koushanfar
International Conference On Computer Aided Design 2019 (ICCAD)

[3] **Adversarial Reprogramming of Text Classification Networks**
Paarth Neekhara, Shehzeen Hussain, Shlomo Dubnov, Farinaz Koshanfar
EMNLP 2019 and AAAI 2019 Workshop on Engineering Dependable and Secure Machine Learning Systems

[4] **Overlay optimization of 1x node technology and beyond via rule based sparse sampling**
Nyan Lynn Aung, Woong Jae Chung, Lokesh Subramany, Shehzeen Hussain, Pavan Samudrala, Haiyong Gao, Xueli Hao
Yen-Jen Chen, Juan-Manuel Gomez
SPIE 9778, Metrology, Inspection, and Process Control for Microlithography XXX, 2016

Projects

Acceleration of Audio Synthesis using Deep Neural Networks on FPGA Jan 2019

- Developed the first accelerator framework for autoregressive convolutional neural networks. Deployed a fast inference model Fast-Wavenet on Xilinx XCVU13P FPGA which achieves 11 times faster generation speed than a high-end GPU and 66 times faster generation speed than a high-end CPU, when performing audio/speech synthesis.
- Developed reconfigurable basic blocks pertinent to autoregressive convolutional networks i.e., dilated causal convolutional layers, convolutional queues, and fully connected layer for FPGA. Framework utilizes fully-customizable matrix-multiplication engine with two levels of parallelism.

Universal Adversarial Perturbations for Speech Recognition Systems Mar 2019

- Developed universal adversarial perturbations in the audio domain. Studied the vulnerabilities and blind spots of deep neural network based automatic speech recognition (ASR) systems, and provided insights for building more robust neural networks.
- Proposed an algorithm to find a single quasi-imperceptible perturbation, which when added to any arbitrary speech signal, will cause mis-transcription by victim speech recognition model.

Generative Adversarial Network for Audio Reconstruction Apr 2018

- Developed a framework: Audio-RecGAN for generating raw audio from lossy training dataset, using improved Wasserstein GAN loss (WGAN-GP) to optimize the Audio-RecGAN objective.
- Designed a generative adversarial training technique to explore different noisy measurement settings tailored for raw audio, and recover the underlying data distribution from a training dataset containing only lossy audio signals.
- Investigated an optimization objective to project lossy audio signals from natural data space back to the latent space of the trained Audio-RecGAN generator, in order to recover clean audio signals.

Hyper spectral Image Segmentation using Graphs and Clustering Mar-May 2014

- Analyzed Hyperspectral image data captured over hundreds of wavelengths from space rocks to determine composition of imaged materials.
- Analyzed efficiency of Graph Cuts and K means clustering algorithms in hyper spectral image segmentation.
- Developed MATLAB and Python code to study robustness of algorithm in handling non-linear data sets.
- Generated graphs to outline material composition signatures with varying cluster frequencies.

Relevant Coursework

Neural Networks & Machine Learning, Algorithm Design, Data Structures, Deep Learning for Sequences, Principles of AI: Probabilistic Reasoning, Optimization and Acceleration of Deep Learning on Hardware Platforms, Security of Embedded Systems, Sensing and Estimation in Robotics, Computer Architecture, Probability & Random Processes, Mathematical Methods, Statistical Mechanics.

Leadership & Awards

- Charles Lee Powell Foundation Fellowship at University of California, San Diego. Sep 2017
- Invited Member of Electrical and Computer Engineering Honors Society Eta Kappa Nu (HKN). Nov 2017, 2015
- Vice President for IEEE at University of Massachusetts, Amherst. Sep 2014 - May 2015
- Secretary for IEEE at University of Massachusetts, Amherst. Sep 2012 - May 2014
- Organized the first student run Embedded Systems Hackathon (HackUMass) at University of Massachusetts, Amherst alongside the IEEE board. Apr 2014
- Organized open Arduino Uno workshop to teach embedded programming basics to non-engineering students. Mar 2014
- Awarded 2nd Place at HackHolyoke Hackathon for Project MyCam, framework that tracks faces in a webcam using automated facial recognition. Nov 2014
- Invited Member of National Physics Honor Society Sigma Pi Sigma and Society of Physics Students at Mount Holyoke College. May 2014
- Simon & Satenig Ermonian Memorial Engineering Scholarship – Award for Academic Excellence August 2014
- Howard Hughes Medical Institute (HHMI) Award– A competitive grant awarded from among 300 applicants for summer research in physics May 2012

Skills

- C & C++
- Java
- Python
- Tensorflow, Pytorch, Keras
- Mathematica & MATLAB
- Vivado HLS & Verilog
