CSE 306: Computer Architecture Sessional

Submission Date: December 19, 2022

Assignment-1: 4-bit ALU Simulation

Section: A1

Group: 2

Group Members:

1. 1905017
2. 1905028
3. 1905003
4. 1905023
5. 1805066

1 Introduction

An Arithmatic Logic Unit(ALU) is a multi-operation, combinational-logic digital function. It can perform a set of basic arithmatic operations and a set of logic operations. The ALU has a number of selection lines to select particular operation in the unit. The selection lines are decoded within the ALU so that k selection variables can specify up to 2^k distinct operations.

In our experiment, we have three selection variables which can enable us to perform $2^3 = 8$ distinct operations. The four data inputs from A are combined with the four inputs from B to generate an operation at the F outputs. A combination circuit is used to modify data inputs. A and B to produce the inputs for the parallel adders to get the desired F outputs.

In our ALU design, we use a 4-bit status register. This status register contains 4 status bits that are denoted by C(Carry), S(Sign), V(Overflow) and Z(Zero). These status buts change during arithmatic operations. They indicate the following changes:

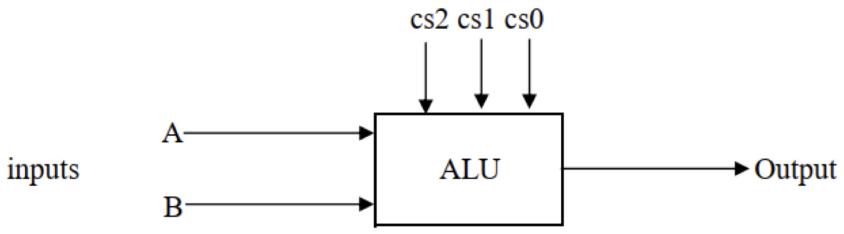
- **CF :** Bit C is set 1 when the output carry of the ALU is 1, otherwise it is set to 0.
- **SF :** Bit S is set 1 when the highest order bit of the output of the ALU is 1, it is set 0 when the highest order bit is 0.
- **OF :** Bit V is set 1 if the X-OR of carries C_4 and C_5 is 1. Otherwise it is set 0.
- **ZF :** Bit Z is set 1 if the result is zero, otherwise the Z bit is set 0.

2 Problem Specification

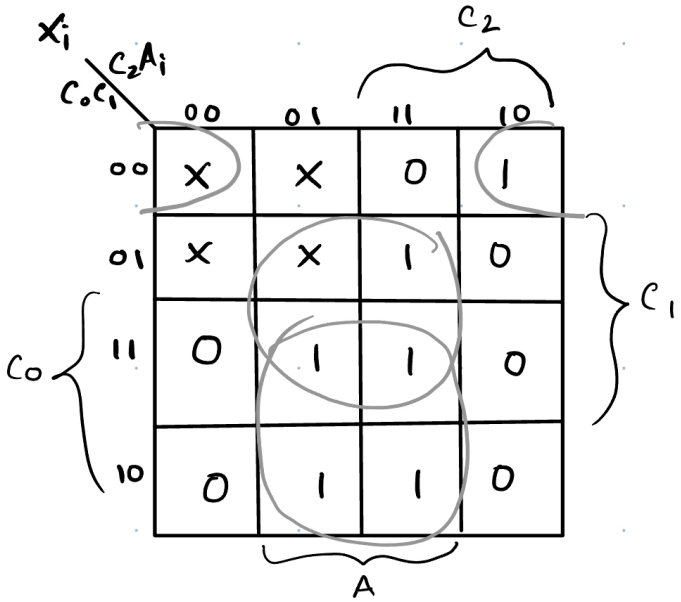
Design a 4-bit ALU with three selection bits cs0,cs1 and cs2 for performing the following operations:

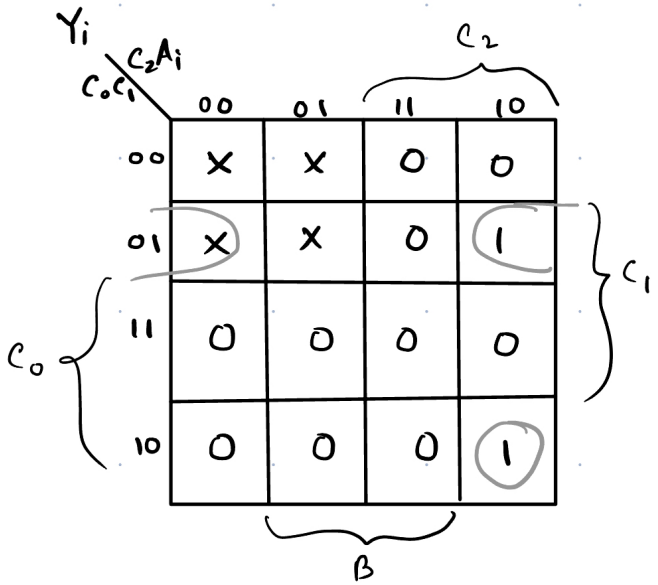
cs2	cs1	cs0	Functions
0	X	0	OR
0	0	1	Complement A
0	1	1	Sub
1	0	0	Increment A
1	0	1	Sub with borrow
1	1	X	Transfer A

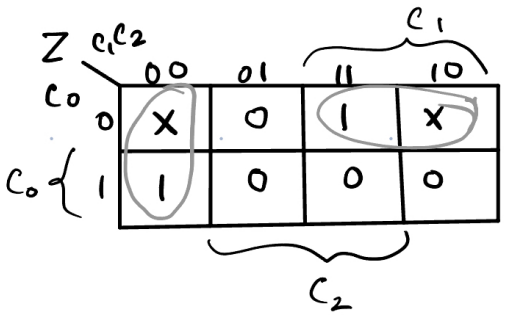
Table 1: Operation Table



3 Required K-Maps:





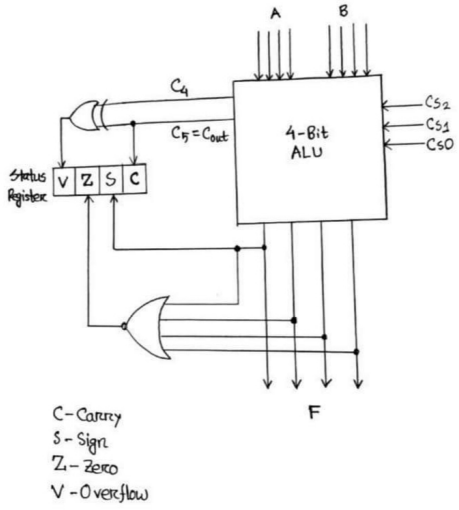


4 Truth tables:

cs2	**cs1**	**cs0**	**Functions**	X_i	Y_i	**Carry**
0	X	0	A v B	A_i V B_i	0	0
0	0	1	Complement A	A'	0	0
0	1	1	Sub	A	B'	1
1	0	0	Increment	A	0	1
1	0	1	Sub with borrow	A	B'	0
1	1	X	Transfer A	A	0	0

Table 2: Operation Table

5 Block Diagram:



6 Equations:

$$X_i = C_0' C_1' A_i' + C_1 A_i + C_0 A_i$$
$$Y_i = C_0 C_1' C_2 B_i' + C_0' C_1 B_i'$$
$$Z = C_0' C_1 + C_1' C_2'$$

7 Complete Circuit Diagram

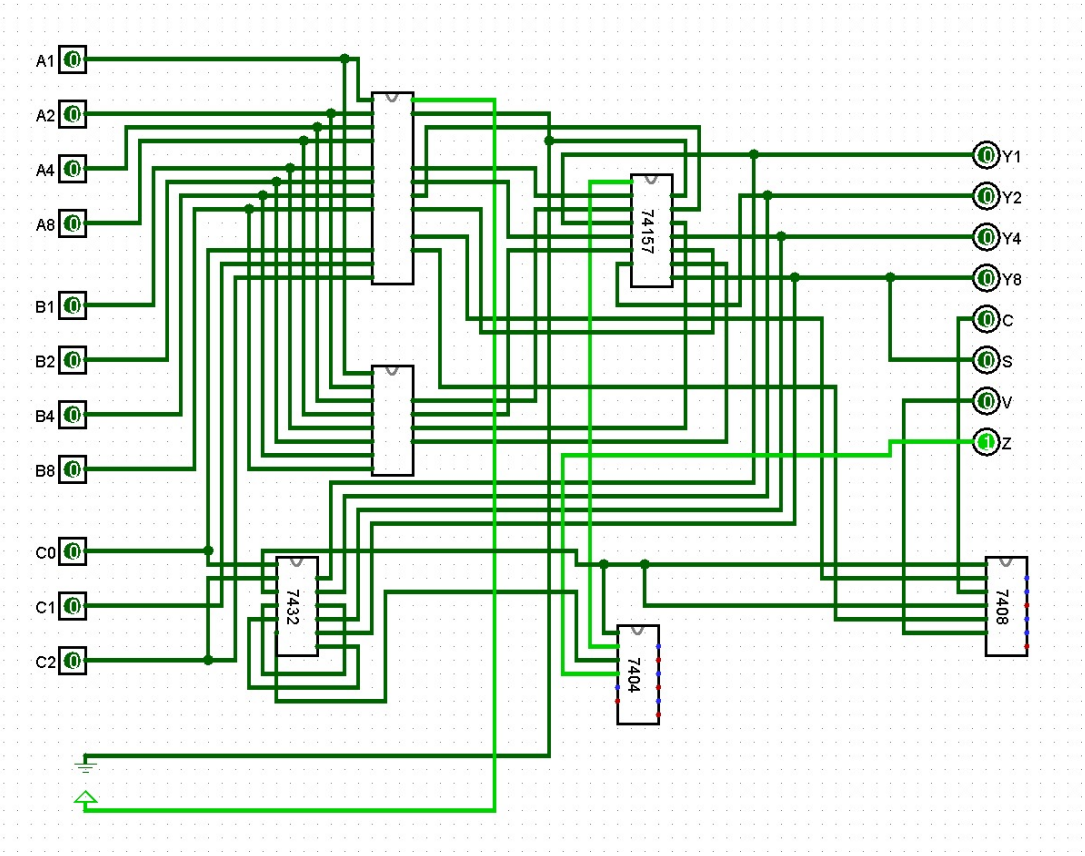


Figure 1: ALU

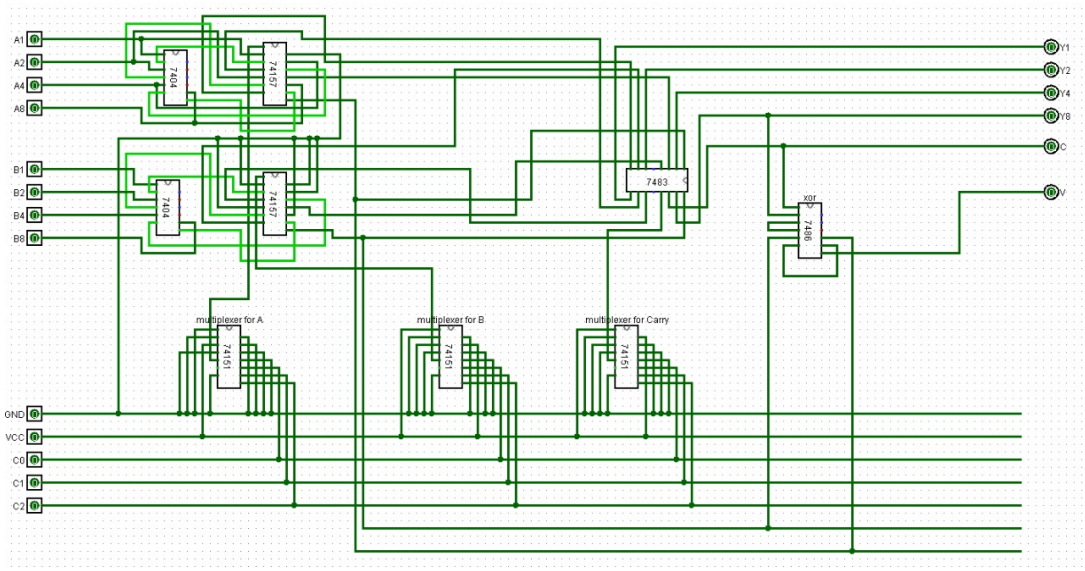


Figure 2: Arithmetic Unit

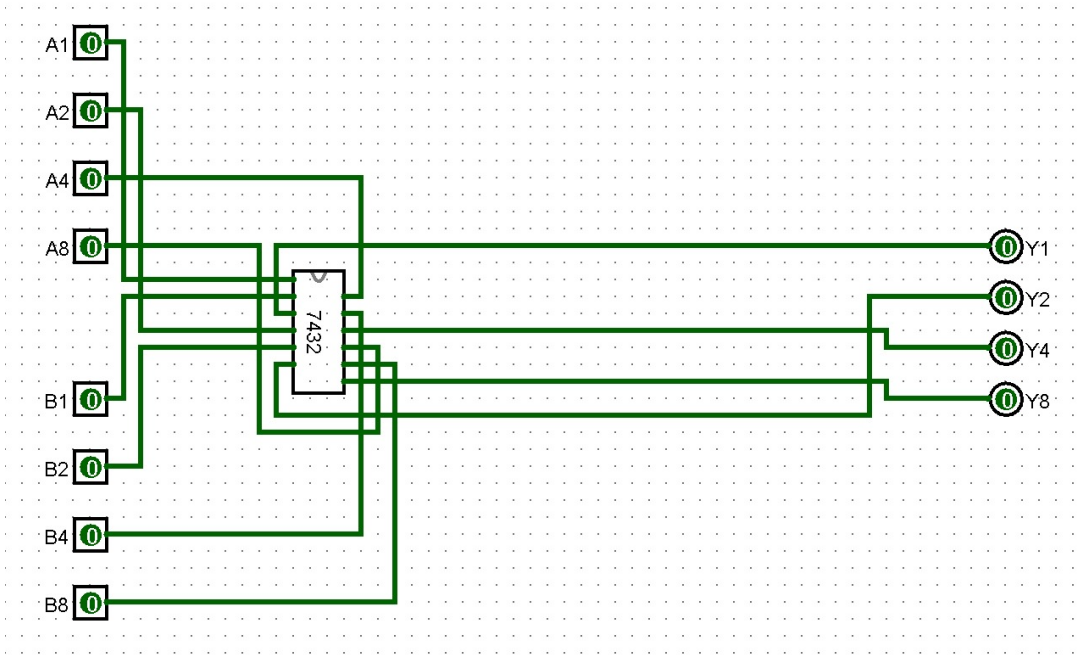


Figure 3: Logical Unit

8 Required ICs:

IC Name	Count
IC 7432	2
IC 7404	3
IC 74157	3
IC 74151	3
IC 7483	1
IC 7486	1
IC 7408	1

Table 3: Required IC Table

9 Simulator Used:

Logisim-Win-2.7.1

10 Discussion:

In this experiment, we were tasked to implement an ALU that can perform four arithmetic operations and two logical operations. We implemented ALU in such a way that it can perform both arithmetic and logica operations in a single circuit, instead of requiring two different circuits. Number of IC that was used was kept as minimal as possible. Logisim-Win-2.7.1 simulation software was used to simulate the circuit.