East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 5
Title: Decoder and Its Use in Combinational Logic Implementation

Objectives:

1. To implement and test a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates.
1. To implement and test combinational logic functions using IC 74138 (3-to-8-lines decoder with active-LOW outputs).

Theory:

Design of decoders using random gates is discussed in Section 8.3 of textbook 1. The IC 74138 (3-to-8-line decoder with active-LOW outputs) is introduced in Section 8.3 of textbook 1. Combinational logic implementation using decoders is also discussed in Section 8.3 of textbook 1.

Pre-Lab Report Questions:

Implementing and testing a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates:

1. Draw the logic diagram for a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input.
2. Write the truth table of the above decoder.

Implementing and testing combinational logic functions using the IC 74138 (3-to-8-lines decoder with active-LOW outputs):

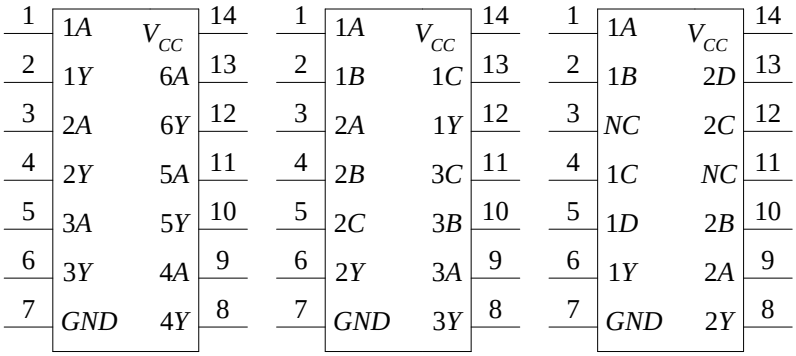
3. Draw the schematic diagram for implementing the following two combinational logic functions using the IC 74138 (3-to-8-lines decoder with active-LOW outputs).

$$F_1(A,B,C) = \sum(1,2,4,7)$$
$$F_2(A,B,C) = \sum(0,5,6,7)$$

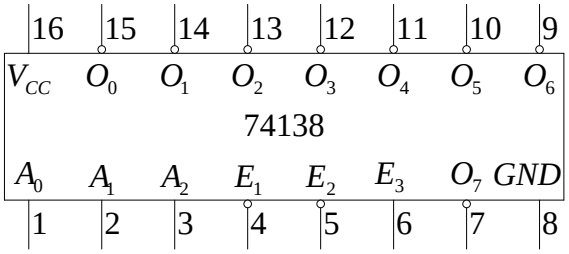
ICs Required:

7404 Hex Inverters (NOT gates)
7410 Triple 3-input NAND gates
7420 Dual 4-input NAND gates
74138 3-to-8-line decoder with active-LOW outputs

Pin Diagram of the Required ICs:



7404 (6 NOT) **7410** (3 3-In NAND) **7420** (2 4-In NAND)



Lab Procedure:

Implementing and testing a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates:

1. Construct the logic diagram for a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input from your pre-lab report using random gates. Connect the three inputs (A_1, A_0, and E) of the circuit to three data switches and four outputs to four LED indicators.
2. Apply binary 00 to 11 to A_1A_0 address inputs and observe the outputs by changing E enable input. Verify the operation.

Implementing and testing combinational logic functions using the IC 74138 (3-to-8-lines decoder with active-LOW outputs):

3. Construct the circuits for implementing the given combinational logic functions from your pre-lab report. Connect enable inputs E_1 and E_2 to fixed 0s and E_3 to a data switch. Use E_3 as active-HIGH enable input. Connect the input lines ABC ($A_2A_1A_0$) to three data switches. Connect the two function outputs to two LED indicators.
4. Prepare the truth tables of the circuit and verify that it implements the two given combinational logic functions.

Post-Lab Report Questions:

1. Verify that all experimental outputs agree with your pre-lab report.
2. Write structural Verilog code for the logic diagram for a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input from your pre-lab report and simulate it using Quartus II software.
3. Write behavioral Verilog code for 3-to-8-lines decoder with active-LOW outputs and simulate it using Quartus II software.