Timing Analysis: Dynamic, Static, and an Augmented Approach

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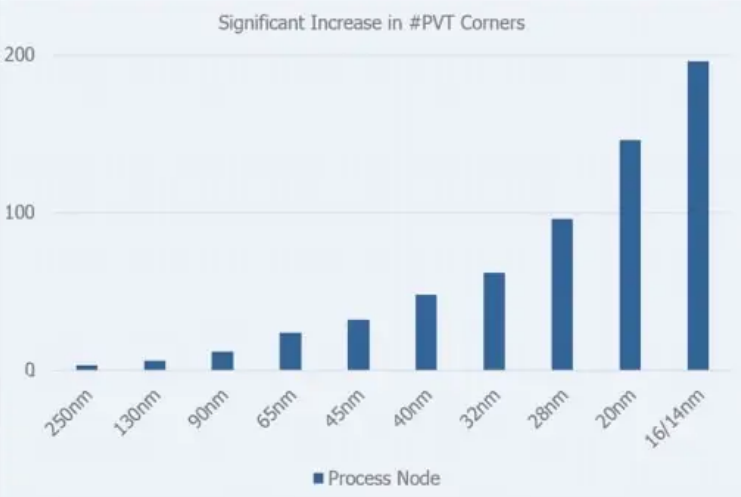
VLSI designs have become increasingly complex with every new process node, leading to complications in timing analysis techniques. In this paper, we'll discuss how timing analysis methods have evolved to meet designer needs and examine how new technologies like the Apex Semiconductor STA Timing Estimator are providing innovative solutions to industry-wide challenges.

Introduction

One of the most crucial and challenging aspects of VLSI design is timing closure, which ensures that a circuit can operate at its intended frequency and meet power, performance, and area specifications. After designing the chip, designers must validate the speed that it runs, the speed at which it interacts with other chips, and other timing interactions that affect performance.

To test these timing interactions, designers use timing analysis to measure the delay of the design at various stages and make subsequent design fixes. As VLSI designs become increasingly complex and the number of timing paths and operating conditions has grown, however, modern timing analysis methods have developed runtime, coverage, and accuracy issues.

Figure 1: Increase in PVT corners with shrinking process nodes



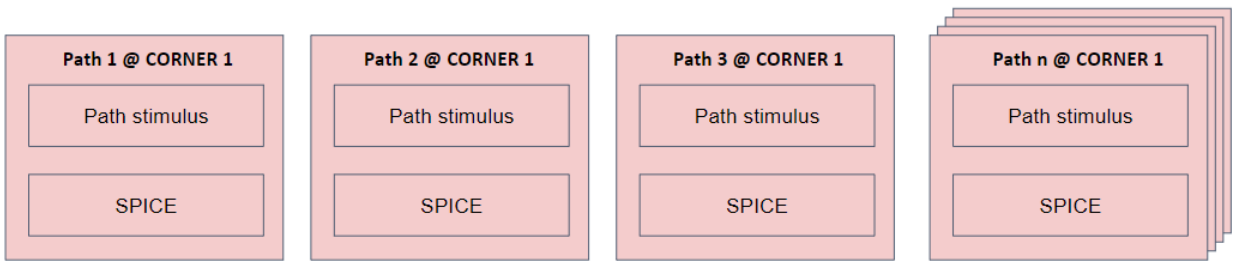
Dynamic timing analysis

The traditional timing analysis method is dynamic timing analysis (DTA), which uses tools such as SPICE and Spectre to simulate the entire logical operation of a circuit. Given a set of comprehensive input vectors, this method simulates the circuit and verifies timing by checking for correct output vectors. Conceived to model circuit behavior of non-linear circuit devices and components in the 1960s, DTA is the gold standard of accuracy for passive and active circuit elements alike.

While DTA has strengths in accuracy, it suffers from coverage and runtime issues. Because this method only performs timing analysis on circuitry that is exercised by test stimulus, it may leave some critical paths untested and timing issues undiscovered. DTA also relies on the time-consuming generation of test vectors, which cannot be generated through a manual process due to the complexity of modern designs.

The increasing complexity of chip designs has exacerbated the runtime issues of DTA. DTA cannot reasonably scale to more than 100~1000 timing paths, while the modern design now has at least 10 million timing paths. There are so many simulation combinations of gate and timing paths that it is no longer feasible to comprehensively simulate the entire design and identify the critical paths in a reasonable timeframe.

Figure 2: DTA analysis architecture model



In the modern chip design process, DTA now serves as the foundation for a newer timing analysis method: static timing analysis.

Static timing analysis

Becoming prevalent in VLSI in the 1980s, static timing analysis (STA) was developed to alleviate the runtime and coverage issues of dynamic timing analysis. Given characterized libraries from DTA and a design netlist, STA uses tools such as PrimeTime and Innovus to identify all timing paths through graph- or path-based algorithms.

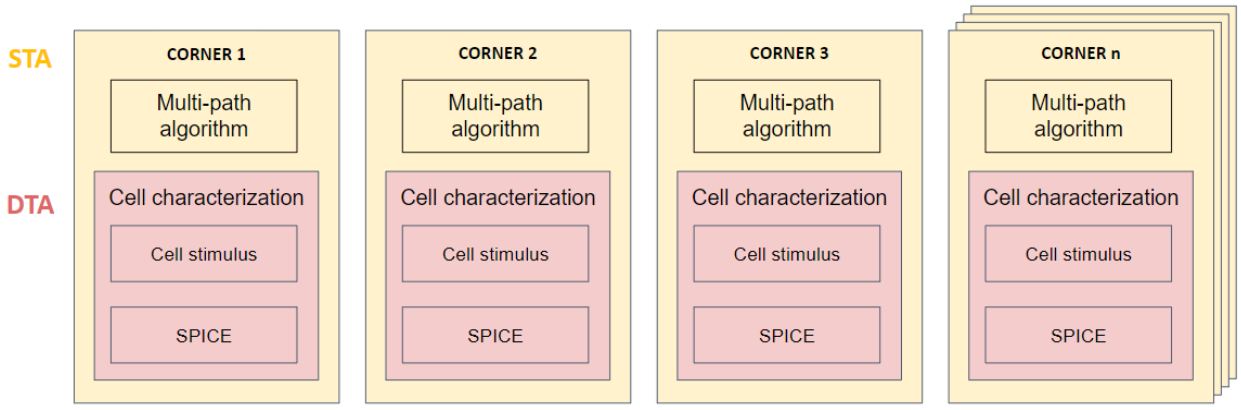
The process of STA begins by abstracting cell-based design components into smaller building blocks. This method relies on DTA to perform library characterization for all possible combinations of the building blocks. Because these building blocks are simpler compared to full timing paths, their timing relationships can be simulated by DTA in a more reasonable timeframe. STA is then performed on the unique combinations of the simple building blocks rather than the traditional process of using DTA to simulate every possible full timing path.

STA does not require simulating the entire circuit, which greatly reduces runtime compared to DTA. STA also features improved coverage because it checks all possible timing paths rather than only the logical conditions that are sensitized by a set of test vectors.

However, a major drawback of STA is that it depends on library characterization to obtain an accurate representation of the cell. When a circuit behaves differently in different operating conditions, library characterization must be performed before any analysis can begin. As modern integrated circuits become increasingly complex, however, the number of corners has also grown with each process node. The average number of sign-off corners in modern designs is now 20~30, while STA can only manually analyze 1~3 corners at a time.

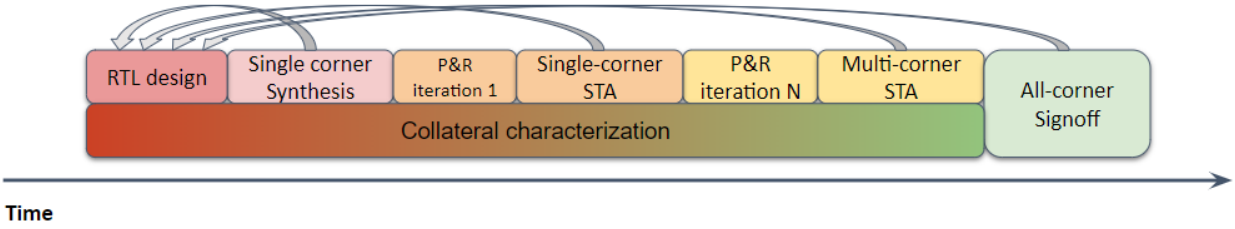
Figure 3 below displays the STA analysis architecture model, which incorporates the cell characterization of DTA. See Figure 2 for the DTA analysis architecture model.

Figure 3: STA analysis architecture model



The conventional design process now requires numerous runs of library characterization and consists of a long and continuous loop of design iteration, library characterization, and STA. Runtime has significantly increased, which has subsequently led to issues with integration. Because timing results are generated so late in the design cycle, designers cannot make meaningful fixes to early design stages.

Figure 4: Conventional STA design flow



The increasing complexity of chip designs has led to runtime, accuracy, and integration issues in the two classic STA integration models: single-corner analysis and all-corner analysis for sign-off.

Single-corner static timing analysis

Single-corner analysis is used when characterized libraries for some corners are unavailable. In this model, designers develop the chip based on currently available information while waiting for the remaining characterized libraries. Because the process of library characterization is so lengthy and only 1~3 operating conditions can be tested at a time, timing violations are typically revealed too late in the design cycle for designers to correct all errors.

Figure 5: Single-corner STA design phase integration

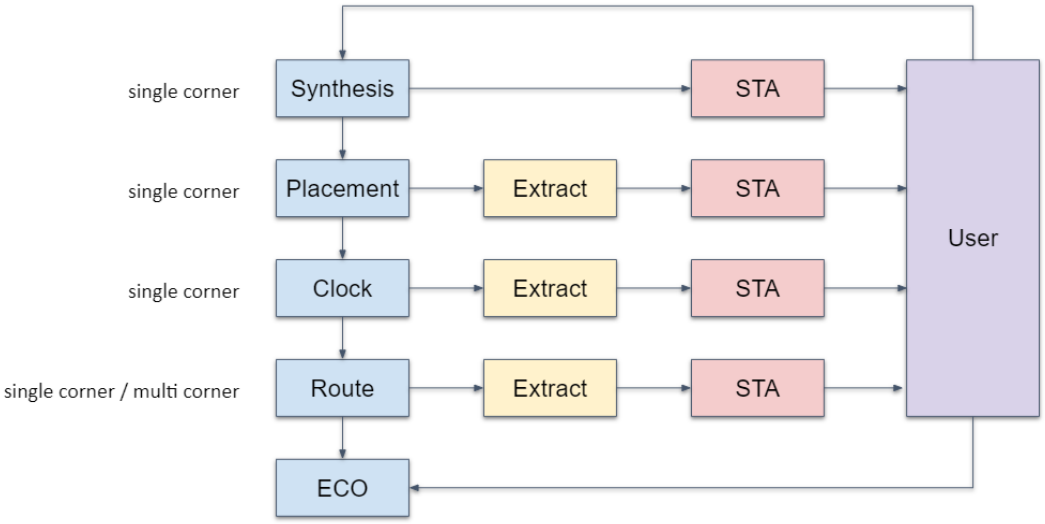


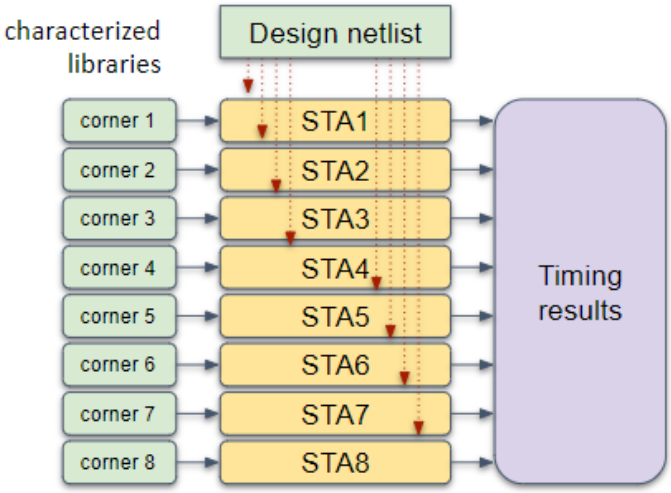
Figure 5 above displays that single-corner timing information is typically used to drive logic design and design optimization beginning from the synthesis phase into subsequent phases. At various stages of the design cycle, designers must work with a limited subset of timing information and

ultimately make design optimization trade-offs. The process of waiting for corners to become available also incurs a significantly longer runtime because library characterization can take weeks or even months to complete.

All-corner static timing analysis for sign-off

All-corner STA for sign-off requires all characterized libraries to be available before performing any analysis. The drawback of this sign-off integration model is that the lengthy process of library characterization typically isn't completed until late in the design cycle, when the design is already finalized. As a result, the results of all-corner STA cannot be used to meaningfully improve early stages of the design.

Figure 6: All-corner STA for sign-off usage model



Designers can alternatively avoid waiting for library characterization by mixing and matching currently available corners with STA conditions. In Figure 6 above, a designer may want to check corner 6 with STA condition 6. If the characterized libraries for corner 6 are not yet available, the designer can use corner 5 with STA condition 6 to generate timing results. While this usage model decreases runtime, it incurs a considerable decrease in accuracy. Ultimately, the classic STA integration models suffer from runtime, accuracy, and integration issues.

Apex Semiconductor's solution for efficient timing analysis

The Apex Semiconductor STA Timing Estimator is an early-stage timing feedback tool that builds on DTA and STA while alleviating the runtime and integration issues of both timing analysis methods. Using machine learning technology, the Timing Estimator uses DTA characterized libraries and STA results from a single corner to estimate frequency and critical paths in all corners.

Because the Timing Estimator does not rely heavily on characterized DTA data, it has a significantly lower runtime compared to the classic STA usage model displayed in Figure 6.