University of Pennsylvania
Department of Electrical and System Engineering
System-on-a-Chip Architecture

ESE532, Fall 2020 — 200Mb/s Milestone — Wednesday, November 18

Due: Friday, December 4, 5:00PM

Group: Achieve target speed and writeup progress (Items 1, 2, 3)

1. Accelerate your deduplication and compression task; try to achieve 200 Mb/s overall performance.
   (a) Report throughput achieved. Include details on the throughput supported by each major operation as well as the overall throughput.
   (b) Report current compression rate achieved.
   (c) Describe all validation performed on your accelerated implementation.
   (d) Identify where this design is in your design space. Explain additional design-space axes beyond your previous milestone as necessary.
   (e) Describe the techniques you used to achieve the speedup. Be clear where each component runs and the resources it uses.
   (f) Support your description with a performance model.
   (g) Describe who did what.
2. Turn in a tar file for your code above to the designated assignment component in canvas (one per group).
3. Turn in a tar or zip file with binaries to support execution of your code to the designated assignment component in canvas (one per group).
   (a) `encoder.xclbin` for FPGA kernel
   (b) `encoder` for OpenCL host code executable
   (c) `decoder` executable configured to work with your encoded file and that can be run on the Ultra96. (Most likely, this is just a compilation of the `Decoder.cpp` we supplied; however, if you chose a different maximum block size, you may need to change `CODE_LENGTH`; so give us back one with that change made.)
   Make sure to compile it with the `aarch64-linux-gnu-g++` compiler and test it on the Ultra96. While you could run the decoder on your host machine (which could be Linux/Mac OS/Windows), we will run your decoder on the Ultra96.