Bharat
Acharya
Education

COA Viva Questions

Learn the full subject at:
www.BharatAcharyaEducation.com

6 Months | Unlimited Views | @999/-

Website	www.BharatAcharyaEducation.com
Mobile	+91 9820408217
Email	bharatsir@hotmail.com
Youtube	youtube.com/c/BharatAcharyaEducation
Instagram	@BharatAcharyaEducation
Facebook	facebook.com/BharatAcharyaEducation

Examiner

What are the three types of buses?

Question 1:

You

Address bus | Carries the address for the current memory or I/O operation.

Data bus | Transfers data between the processor and memory or I/O.

Control bus | Issues control signals to decide the type of operation like read, write etc.

Together they are called the SYSTEM bus

Bharat Acharya Education

Examiner

What is an instruction cycle?

Question 2:

You

The total process of fetching an instruction from the memory, decoding the opcode to understand the operation and finally executing the instruction is called an instruction cycle.

Bharat Acharya Education

Examiner

What is PC?

Question 3:

You

PC | Program Counter

It is a register present inside the processor. It contains address of the next instruction. PC gets incremented as soon as any instruction is fetched.

Bharat Acharya Education

Examiner

What is SP?

Question 4:

You

SP | Stack Pointer

It is a register present inside the processor. It contains address of the top of stack. SP gets decremented in every Push and incremented in every Pop operation.

Bharat Acharya Education

Examiner

What are GPRs?

Question 5:

You

GPRs | General Purpose Registers

These are registers present inside the processor. They are available to the programmer for storing operands and getting results in a program.

Bharat Acharya Education

Examiner

What is a compiler?

Question 6:

You

A compiler is a program that converts a higher language code (E.g.: C, C++) into machine language that can be executed by the processor.

Bharat Acharya Education

Examiner

What is the difference between Von Neumann and Harvard Model?

Question 7:

You

Von Neumann Model

Common memory used to store programs and data. E.g.:: 8085, 8086.

Harvard Model

Separate program memory and data memory. E.g.:: 8051.

Bharat Acharya Education

Examiner

Explain Flag register?

Question 8:

You

It gives the status of the current result. It has flag bits that indicate if there was a carry, if the result was zero, the sign of the result, its parity etc. Flags are changed by the ALU after every operation.

Bharat Acharya Education

Examiner

Why are signed numbers stored in 2's complement form?

Question 9:

You

Because it does not produce a negative zero. 2's complement of any number gives –(that number) but 2's complement of 0 gives back 0 itself.

Bharat Acharya Education

Examiner

Why did you choose engineering?
To mug up answers or to
understand the subject?

You

(Answer this one Yourself!)

Lets "Understand" the subject!
www.BharatAcharyaEducation.com

Computer Organisation & Architecture

List of Video topics

- Introduction
- Von Neumann Model
- Number representation
- Adder Subtractor circuits
- Multiplication including Booth's Algorithm
- Restoring Division
- Non Restoring Division
- Floating Point Number Representation
- Floating Point Conversion Numericals
- Floating Point Addition Algorithm
- Instruction Formats and Types
- Instruction cycle state transition
- Addressing Modes with Examples of 8085/ 8086 etc.
- Pipelining
- Micro-Operations
- Hardwired Control Units
- Microprogrammed Control Units
- Micro-Instruction Sequencing
- Horizontal v/s Vertical Micro Instruction Formats
- Nano-Programming
- Memory Hierarchy
- Memory characteristics
- Virtual Memory Management - Paging & TLB
- Page Replacement Theory & Numericals
- Cache Architectures
- Cache Mapping Techniques
- Bus Arbitration
- Memory Mapped I/O v/s I/O Mapped I/O
- Interrupt Driven I/O
- DMA based I/O
- Flynn's Classification
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Internal Examiner

What is half adder and a full adder?

Question 10:

You

Half Adder | Adds the two current bits. Produces a sum and a carry. Cannot be scaled to a bigger adder.

Full Adder | Adds the two current bits along with the carry of the previous stage. Produces a sum and a carry. Can be scaled (combined) to form a bigger adder.

Refer Video: **COA | Adder Circuits**
www.BharatAcharyaEducation.com

Examiner

How is subtraction performed?

Question 11:

You

We never really “subtract”
Subtraction is performed by the same circuit used for addition by simply adding the 2’s complement of the number.

Draw and show the adder/Subtractor circuit if asked!

Refer Video: **COA | Adder Circuits**
www.BharatAcharyaEducation.com

Internal Examiner

Why cant we do multiplication by repeated addition?

Bonus Question

You

Because it is too slow!
1000 x 1000 will require 1000 steps!

Hence we use faster algorithms like Booth's Algorithm!

Refer Video: **COA | Booth's Algorithm**
www.BharatAcharyaEducation.com

Examiner

Briefly explain Booth's algorithm?

Question 12:

You

Keep checking bit transitions in the multiplier from right to left starting with an imaginary 0 beyond the LSB. Do the following actions:

0 to 1 | Subtract Multiplicand, Right Shift

1 to 0 | Add Multiplicand, Right Shift

0 to 0 | Right Shift

1 to 1 | Right Shift

Refer Video: **COA | Booth's Algorithm**

www.BharatAcharyaEducation.com

Internal Examiner

Why cant we do division by repeated subtractions?

Bonus Question

You

Because it is too slow!
1000 ÷ 1 will require 1000 steps!

Hence we use faster algorithms like restoring and non restoring division!

Refer Video: **COA | Division**
www.BharatAcharyaEducation.com

Examiner

Explain restoring division in brief?

Question 13:

You

At each step, **left shift** the dividend and **subtract** the divisor.

If result is positive (or 0) then successful. Quotient bit is 1. Restoration not needed.

If result is negative, unsuccessful. Quotient bit is 0. Restore by adding back the divisor.

Repeat for all bits of dividend.

Refer Video: **COA | Division**
www.BharatAcharyaEducation.com

Examiner

Explain non restoring division in brief?

Question 14:

You

At each step, **left shift** the dividend and **subtract** the divisor.

If result is positive (or 0) then successful. Quotient bit is 1. Restoration not needed.

If result is negative, unsuccessful. Quotient bit is 0. Don't Restore! Next step will be addition instead of subtraction.

Repeat for all bits of dividend.

Refer Video: **COA | Division**

www.BharatAcharyaEducation.com

Examiner

Describe Normalization and normalized form of a number ?

Question 15:

You

Normalization represents a number such that there must be only one non-zero digit to the left of the point.

Normalized form of a number

$(-1)^S \times 1.M \times 2^E$

S: Sign | M: Mantissa | E: Exponent

Refer Video: **COA | Floating Pt. Formats**
www.BharatAcharyaEducation.com

Examiner

Convert 0101.001 into Normalized form?

Question 16:

You

$(-1)^0 \times 1.0101001 \times 2^2$

Ref Video: **COA | Floating Pt. Formats**
www.BharatAcharyaEducation.com

Computer Organisation & Architecture

List of Video topics

- Introduction
- Von Neumann Model
- Number representation
- Adder Subtractor circuits
- Multiplication including Booth's Algorithm
- Restoring Division
- Non Restoring Division
- Floating Point Number Representation
- Floating Point Conversion Numericals
- Floating Point Addition Algorithm
- Instruction Formats and Types
- Instruction cycle state transition
- Addressing Modes with Examples of 8085/ 8086 etc.
- Pipelining
- Micro-Operations
- Hardwired Control Units
- Microprogrammed Control Units
- Micro-Instruction Sequencing
- Horizontal v/s Vertical Micro Instruction Formats
- Nano-Programming
- Memory Hierarchy
- Memory characteristics
- Virtual Memory Management - Paging & TLB
- Page Replacement Theory & Numericals
- Cache Architectures
- Cache Mapping Techniques
- Bus Arbitration
- Memory Mapped I/O v/s I/O Mapped I/O
- Interrupt Driven I/O
- DMA based I/O
- Flynn's Classification
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Examiner

Explain Single Precision format?

Question 17:

You

IEEE754 32bit Single Precision

S	E	M
(1)	(8)	(23)

Bias value: 127

Ref Video: **COA | Floating Pt. Formats**
www.BharatAcharyaEducation.com

Examiner

Explain Double Precision format?

Question 18:

You

IEEE754 64bit Double Precision

S	E	M
(1)	(11)	(52)

Bias value: 1023

Ref Video: **COA | Floating Pt. Formats**
www.BharatAcharyaEducation.com

Examiner

Explain Floating point Addition in brief?

Question 19:

You

Compare exponents. If Equal, add the mantissas, else Shift the mantissa till exponent becomes equal, then add the mantissa.

Ref video: **COA | Floating Pt. Addition**
www.BharatAcharyaEducation.com

Examiner

What is Floating point overflow exception?

Question 20:

You

When the exponent is too large to be stored. It is denoted by exponent all 1's. Such a number is also called NaN.

Don't waste Your chance to learn such a wonderful subject by mugging up answers.

Learn the concepts at:
www.BharatAcharyaEducation.com

Examiner

What is Floating point overflow exception?

Question 21:

You

When the exponent is too small to be stored. It is denoted by exponent all 0's. Such a number is also called a DeNormal Number.

Don't waste Your chance to learn such a wonderful subject by mugging up answers.

Learn the concepts at:
www.BharatAcharyaEducation.com

Examiner

How do you represent 0 and 1 in Single precision format?

Question 22:

You

0:

S = 0 | E = 0 | M = 0

1:

S = 0 | E = $(127)_2$ | M = 0

Don't waste Your chance to learn such a wonderful subject by mugging up answers.

Learn the concepts at:

www.BharatAcharyaEducation.com

Examiner

What is the difference between a subroutine (procedure) and a macro?

Question 23:

You

When we CALL a subroutine, the program control shifts from the main program to the subroutine, and after execution, returns to the next instruction after CALL.
When we invoke a macro, the macro code is pasted into our program at the location where the macro was invoked.

Bharat Acharya Education

Examiner

What is an instruction format?

Question 24:

You

Label: Opcode, Operands; Comment

Label | Location Identifier (optional)
Opcode | Binary code of the operation (compulsory)
Operands | Values taking part in the operation (optional)
Comment | Purpose of the instruction (optional)

Ref Video: **COA | Instructions**
www.BharatAcharyaEducation.com

Examiner

What are the types of instructions?

Question 25:

You

Data Transfer
E.g.: MOV, LOAD, STORE etc.

Data Processing
E.g.: ADD, SUB, AND etc.

Control instructions
E.g.: JMP, CALL etc.

Ref Video: **COA | Instructions**
www.BharatAcharyaEducation.com

Examiner

What is instruction level pipelining?

Question 26:

You

Overlapping different stages of an instruction is called pipelining.
E.g.:: Fetch, Decode, Execute, Store etc.

Ref Video: **COA | Pipelining**
www.BharatAcharyaEducation.com

Internal Examiner

Give examples of pipelined processors?

Question 27:

You

8086 | 2 stage
Fetch, Exec.

80386 | 3 stage
Fetch, Decode, Exec.

Pentium | 5 stage
Fetch, Decode, Addr Gen, Exec, Store

Ref Video: **COA | Pipelining**
www.BharatAcharyaEducation.com

Computer Organisation & Architecture

List of Video topics

- Introduction
- Von Neumann Model
- Number representation
- Adder Subtractor circuits
- Multiplication including Booth's Algorithm
- Restoring Division
- Non Restoring Division
- Floating Point Number Representation
- Floating Point Conversion Numericals
- Floating Point Addition Algorithm
- Instruction Formats and Types
- Instruction cycle state transition
- Addressing Modes with Examples of 8085/ 8086 etc.
- Pipelining
- Micro-Operations
- Hardwired Control Units
- Microprogrammed Control Units
- Micro-Instruction Sequencing
- Horizontal v/s Vertical Micro Instruction Formats
- Nano-Programming
- Memory Hierarchy
- Memory characteristics
- Virtual Memory Management - Paging & TLB
- Page Replacement Theory & Numericals
- Cache Architectures
- Cache Mapping Techniques
- Bus Arbitration
- Memory Mapped I/O v/s I/O Mapped I/O
- Interrupt Driven I/O
- DMA based I/O
- Flynn's Classification
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Examiner

What are Pipelining Hazards?

Question 28:

You

Data Hazard
Structural Hazard
Control Hazard

Ref Video: **COA | Pipelining**
www.BharatAcharyaEducation.com

Examiner

What do you mean by addressing modes. List some with examples?

Question 29:

You

It is the manner in which an operand is given in the instruction.
Most popular ones are…
Immediate | Register | Direct | Indirect | Implied

For examples:
Ref Video: **COA | Addressing Modes**
www.BharatAcharyaEducation.com

Examiner

What are the micro-operations required for fetching?

Question 30:

You

T1: MAR ← PC
T2: MBR ← instruction from memory
T3: IR ← MBR
PC ← PC + 1

Ref Video: **COA | Micro Operations**
www.BharatAcharyaEducation.com

Examiner

What is an instruction cycle, machine cycle and T-state?

Question 31:

You

Instruction cycle |Total process of fetching, decoding and executing an instruction.

Machine cycle | One complete operation of the system bus.

T-state | One clock cycle.

Instruction cycle has several machine cycles. Machine cycles have several T-states.

www.BharatAcharyaEducation.com

Examiner

Give characteristics of a RISC processor?

Question 32:

You

RISC | Reduced Instruction Set Computers

- Fixed sized instructions
- Mainly Register based operations
- Fewer addressing modes
- Smaller instruction set
- Simpler instructions
- Prefer Hardwired Control Units
- Suited for µControllers

Ref Video: **COA | Control Units**
www.BharatAcharyaEducation.com

Examiner

Give characteristics of a CISC processor?

Question 33:

You

CISC | Complex Instruction Set Computers

- Variable sized instructions
- Mainly Memory based operations
- More addressing modes
- Bigger instruction set
- Complex instructions
- Prefer μ-Programmed Control Units
- Suited for μProcessors

Ref Video: **COA | Control Units**
www.BharatAcharyaEducation.com

Examiner

What are the two main types of Control Units?

Question 34:

You

Hardwired Control Unit
Microprogrammed Control Unit

Ref Video: **COA | Control Units**
www.BharatAcharyaEducation.com

Examiner

What is a Hardwired Control Unit?

Question 35:

You

It generates control signals using dedicated HARDWARE.
Common types are
1) State Table method
2) Delay Element method
3) Sequence Counter method

Video: **COA | Hardwired Control Unit**
www.BharatAcharyaEducation.com

Examiner

What is a Microprogrammed Control Unit?

Question 36:

You

It generates control signals for any instruction using its μ instructions.

Typical modern Microprogrammed Control Units are made following Wilke's Design.

COA | Microprogrammed Control Unit

www.BharatAcharyaEducation.com

Examiner

What are μ Programs?

Question 37:

You

A set of μ instructions responsible for generating control signals for a particular instruction is called its μ program. μ programs are stored in the control memory.

This subject lays Your foundation for understanding deep machine learning concepts. Don't waste this opportunity by mugging up the answers.

Learn the concepts at:
www.BharatAcharyaEducation.com

Computer Organisation & Architecture

List of Video topics

- Introduction
- Von Neumann Model
- Number representation
- Adder Subtractor circuits
- Multiplication including Booth's Algorithm
- Restoring Division
- Non Restoring Division
- Floating Point Number Representation
- Floating Point Conversion Numericals
- Floating Point Addition Algorithm
- Instruction Formats and Types
- Instruction cycle state transition
- Addressing Modes with Examples of 8085/ 8086 etc.
- Pipelining
- Micro-Operations
- Hardwired Control Units
- Microprogrammed Control Units
- Micro-Instruction Sequencing
- Horizontal v/s Vertical Micro Instruction Formats
- Nano-Programming
- Memory Hierarchy
- Memory characteristics
- Virtual Memory Management - Paging & TLB
- Page Replacement Theory & Numericals
- Cache Architectures
- Cache Mapping Techniques
- Bus Arbitration
- Memory Mapped I/O v/s I/O Mapped I/O
- Interrupt Driven I/O
- DMA based I/O
- Flynn's Classification
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Examiner

What are μ instruction sequencing techniques?

Question 38:

You

Two main techniques

1) Dual Address Field

2) Single Address Field

COA | Microprogrammed Control Unit

www.BharatAcharyaEducation.com

Examiner

What are μ instruction formats?

Question 39:

You

Two main formats

1) Horizontal μ instructions

2) Vertical μ instructions

COA | Microinstruction Formats

www.BharatAcharyaEducation.com

Examiner

Compare Hardwired Control Unit and Microprogrammed Control Unit?

Question 40:

You

Hardwired Control Unit

Faster | No Control Memory needed | Suited for RISC

Hardwired Control Unit

Flexible | Supports Emulation | Control Memory needed | Suited for CISC

COA | Microprogrammed Control Unit

www.BharatAcharyaEducation.com

Examiner

List “typical” sizes of these memories?

Question 41:

You

Hard Disk | **1 TB**
CD | **700 MB**
DVD | **4.7 GB**
Pen Drives | **2 GB – 128 GB**
RAM | **4GB, 8GB, 16GB, 32GB**
Cache | **1 MB – 4 MB**

Ref video: **COA | Memory Hierarchy**
www.BharatAcharyaEducation.com

Examiner

Compare SRAM and DRAM?

Question 42:

You

Static RAM

Faster | Uses Flip-Flops | Expensive | used in Cache

Dynamic RAM

Slower | Uses Capacitors | Cheaper | used in main memory

Ref video: **COA | Memory Hierarchy**
www.BharatAcharyaEducation.com

Examiner

What are advanced DRAMs?

Question 43:

You

RDRAM | Rambus DRAM
SDRAM | Synchronous DRAM

Ref video: **COA | Memory Hierarchy**
www.BharatAcharyaEducation.com

Examiner

What are the types of ROM?

Question 44:

You

ROM | Read Only Memory
PROM | Programmable ROM
EPROM | Erasable PROM
EEPROM | Electrically EPROM
Flash ROM | Electrically EPROM Most Popular in modern systems

Ref video: **COA | Memory Hierarchy**
www.BharatAcharyaEducation.com

Examiner

Where does your phone store images, songs etc?

Question 45:

You

In secondary storage implemented using Flash ROM

Ref video: **COA | Memory Hierarchy**
www.BharatAcharyaEducation.com

Examiner

What does primary memory consist of?

Question 46:

You

RAM and ROM.
RAM for operations
ROM mainly fro the BIOS

Ref video: **COA | Memory Hierarchy**
www.BharatAcharyaEducation.com

Examiner

List important Page replacement policies?

Question 47:

You

FIFO, LRU, LFU, OPT

For solved examples on each of them, refer the video:

COA | Numericals on Page Replacement
www.BharatAcharyaEducation.com

Examiner

What are dirty pages ;-)

Question 48:

You

These are pages modified in the main memory.

Ref video: **COA | Paging**
www.BharatAcharyaEducation.com

Computer Organisation & Architecture

List of Video topics

- Introduction
- Von Neumann Model
- Number representation
- Adder Subtractor circuits
- Multiplication including Booth's Algorithm
- Restoring Division
- Non Restoring Division
- Floating Point Number Representation
- Floating Point Conversion Numericals
- Floating Point Addition Algorithm
- Instruction Formats and Types
- Instruction cycle state transition
- Addressing Modes with Examples of 8085/ 8086 etc.
- Pipelining
- Micro-Operations
- Hardwired Control Units
- Microprogrammed Control Units
- Micro-Instruction Sequencing
- Horizontal v/s Vertical Micro Instruction Formats
- Nano-Programming
- Memory Hierarchy
- Memory characteristics
- Virtual Memory Management - Paging & TLB
- Page Replacement Theory & Numericals
- Cache Architectures
- Cache Mapping Techniques
- Bus Arbitration
- Memory Mapped I/O v/s I/O Mapped I/O
- Interrupt Driven I/O
- DMA based I/O
- Flynn's Classification
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Examiner

What is TLB?

Question 49:

You

TLB | Translation Look-aside Buffer
Contains the most recently used entries of the page table to make page translation faster.

Ref video: **COA | Paging**
www.BharatAcharyaEducation.com

Examiner

What is a page fault?

Question 50:

You

Page Fault

When the desired page is not present in the main memory it is called a miss or a page fault.

Ref video: **COA | Paging**
www.BharatAcharyaEducation.com

Examiner

List some memory characteristics?

Question 51:

You

Reliability, Storage Capacity, Hit Ratio, Avg. Access Time, Avg. Cost/bit, location, Access mode, Access type etc…

Ref Video: **COA | Memory Characteristics**
www.BharatAcharyaEducation.com

Examiner

What are interleaving tecniques?

Question 52:

You

Lower order interleaving and higher order interleaving.

Ref Video: **COA | Memory Interleaving**
www.BharatAcharyaEducation.com

2 options: Mug up all this and bore yourself
Or, learn the subject the right way and
Enjoy its Vast concepts!

Examiner

What is cache consistency?

Question 53:

You

When data in cache memory and main memory has same value, the cache is consistent. Main policies: Write Through and Write back.

Ref Video: **COA | Cache memory**
www.BharatAcharyaEducation.com

Examiner

What are cache layouts?

Question 54:

You

Look Through Cache and Look Aside Cache.

Ref Video: **COA | Cache Memory**
www.BharatAcharyaEducation.com

Examiner

What is MESI protocol?

Question 55:

You

Modified, Exclusive, Shared, Invalid.

Video Ref: **COA | Cache Memory**
www.BharatAcharyaEducation.com

Examiner

What are cache mapping techniques?

Question 56:

You

Associative Mapping
Direct Mapping
Set Associative Mapping

This is one of the BEST topics you learn in this subject. My favorite amongst all!

COA | Cache Mapping Techniques
www.BharatAcharyaEducation.com

Examiner

What are the main types of multi-processor systems?

Question 57:

You

Closely Coupled and Loosely Coupled systems.

www.BharatAcharyaEducation.com

Examiner

What are Bus Arbitration techniques?

Question 58:

You

Daisy Chaining, Polling and Independent requests.

Ref Video: **COA | Bus Arbitration**
www.BharatAcharyaEducation.com

Examiner

What are I/O data transfer techniques?

Question 59:

You

Polling/ Programmed I/O
Interrupt driven I/O
DMA
I/O Processors

Ref Video: **COA | I/O Data Transfers**
www.BharatAcharyaEducation.com

Examiner

What are I/O mapping techniques?

Question 60:

You

Memory mapped I/O and I/O mapped I/O (also called Isolated I/O)

Ref Video: **COA | I/O Mapped I/O**
www.BharatAcharyaEducation.com

Examiner

Give characteristics of interrupts?

Question 61:

You

Software, hardware, vectored, non-vectored, edge triggered, level triggered, Maskable, non Maskable.

Ref Video: **COA | Interrupt Driven I/O**
www.BharatAcharyaEducation.com

Examiner

What are some popular DMA transfer techniques?

Question 62:

You

Block Transfer (Burst Mode)
Cycle Stealing (Single Byte Transfers)
Demand Transfer
Hidden Mode (Transparent Mode)

Ref Video: **COA | Direct Memory Access**
www.BharatAcharyaEducation.com

Examiner

Name a popular I/O Processor?

Question 63:

You

8089 I/O Processor is used with 8086 μ P.

Ref Video: **COA | I/O Processor**
www.BharatAcharyaEducation.com

Examiner

Give Flynn's Classification?

Question 64:

You

It classifies multiprocessor systems into 4 different categories, based on the instruction stream and the data streams.

1) **SISD** | Single Instruction Single Data
2) **SIMD** | Single Instruction Multiple Data
3) **MISD** | Multiple Instruction Single Data
4) **MIMD** | Multiple Instruction Multiple Data

www.BharatAcharyaEducation.com

Examiner

What is serial and parallel communication?

Question 65:

You

Serial Communication

One bit at a time | Slower | Cheaper | Long Distance

Parallel Communication

Multiple bits at a time | Faster | Costlier | Short Distance

www.BharatAcharyaEducation.com

www.BharatAcharyaEducation.com

Video Courses for You

- Microprocessor | 8085
- Microprocessor | 8086
- Microprocessor | 80386
- Microprocessor | Pentium
- Microcontroller | 8051
- Microcontroller | ARM
- Computer Organisation & Architecture

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Bharat Acharya Education

Computer Organization
& Architecture
VIVA | 2019

Computer Organisation & Architecture

List of Video topics

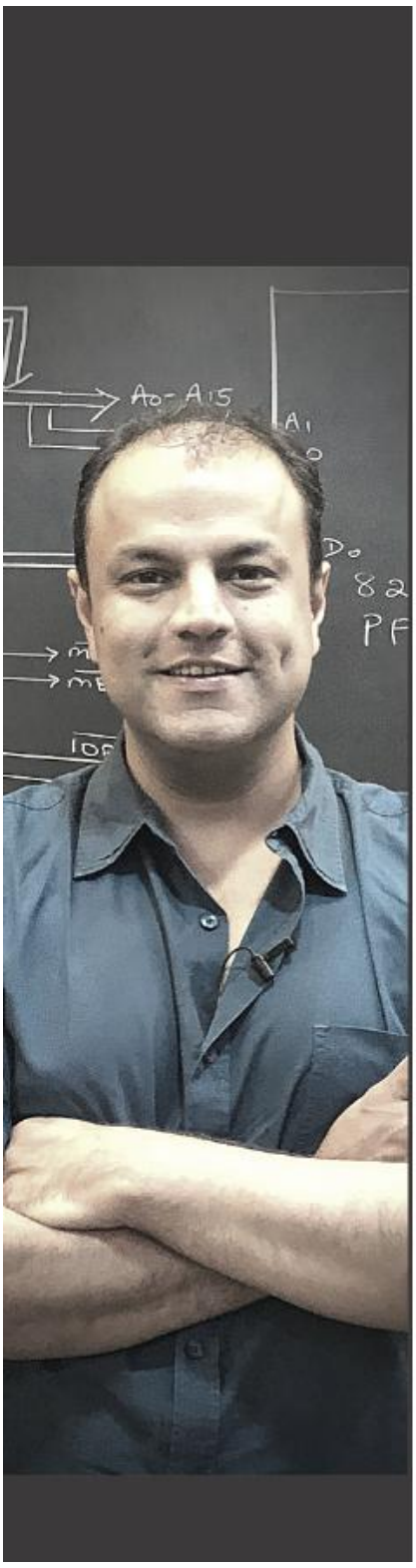
- Introduction
- Von Neumann Model
- Number representation
- Adder Subtractor circuits
- Multiplication including Booth's Algorithm
- Restoring Division
- Non Restoring Division
- Floating Point Number Representation
- Floating Point Conversion Numericals
- Floating Point Addition Algorithm
- Instruction Formats and Types
- Instruction cycle state transition
- Addressing Modes with Examples of 8085/ 8086 etc.
- Pipelining
- Micro-Operations
- Hardwired Control Units
- Microprogrammed Control Units
- Micro-Instruction Sequencing
- Horizontal v/s Vertical Micro Instruction Formats
- Nano-Programming
- Memory Hierarchy
- Memory characteristics
- Virtual Memory Management - Paging & TLB
- Page Replacement Theory & Numericals
- Cache Architectures
- Cache Mapping Techniques
- Bus Arbitration
- Memory Mapped I/O v/s I/O Mapped I/O
- Interrupt Driven I/O
- DMA based I/O
- Flynn's Classification
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Bharat Acharya Education

Computer Organization & Architecture VIVA | 2019



Microprocessor 8085

List of Video topics

- Introduction
- Architecture
- Flag Register
- Addressing Modes
- Instruction Set (Every Instruction with examples)
- Assembly Programming (Several Videos)
- Timing Diagrams of Machine cycles
- Timing Diagrams of Instructions
- Stacks & Subroutines
- Delays & Delay Routines
- Interrupt Structure
- SIM and RIM Instructions with Sq. Wave Program
- 8259 PIC (Theory, Programs, Interfacing)
- 8255 PPI (Theory, Programs, Interfacing)
- 8254 PIT (Theory, Programs, Interfacing)
- 8237 DMAC (Theory, Programs, Interfacing)
- Full System Memory & I/O Designing
- Memory Mapped I/O and I/O Mapped I/O
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

Bharat Acharya Education

Computer Organization & Architecture VIVA | 2019

Microprocessor 8086

List of Video topics

- Introduction
- Pipelining
- Memory Segmentation
- Memory Banking
- Architecture
- Flag Register
- Addressing Modes
- Instruction Set (Every Instruction with examples)
- Assembler directives
- Assembly Programming (Several Videos)
- DOS Interrupt - INT 21H
- Interrupt structure with IVT
- Minimum Mode with Timing Diagrams
- Maximum Mode with Timing Diagrams
- 8086-8087 Interfacing
- 8259 PIC (Theory, Programs, Interfacing)
- 8255 PPI (Theory, Programs, Interfacing)
- 8254 PIT (Theory, Programs, Interfacing)
- 8237 DMAC (Theory, Programs, Interfacing)
- Full System Memory & I/O Designing
- Many more...

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com

www.BharatAcharyaEducation.com

Registration Process

- Log into our website: www.BharatAcharyaEducation.com
- Select your desired course
- Make your payment
- Start Learning!

Payment options

Our website accepts the following payment methods:

- Netbanking
- Debit/ Credit Cards
- Wallets like Paytm etc

For Any further Payment assistance
OR
For International Students
Please call/ Whatsapp us on:

+91 9820408217

6 Months | Unlimited Views | 999/-
GST applicable @18% as per Govt. of India

www.BharatAcharyaEducation.com

www.BharatAcharyaEducation.com

Additional Benefits

- Free PDF with almost every video containing full theory answers and circuit diagrams
- Certificate at the end of the course
- Doubt solving via WhatsApp on +919829498217 subject to availability of the faculty

Rules and regulations

- All videos are copyright protected.
- UNAUTHORISED DOWNLOADING OR CIRCULATION of any content on our website or mobile app are subject to LEGAL ACTION as per INDIAN COPYRIGHT ACT.
- One Login Id and the subsequent subscription is for one individual and can be used on upto 4 devices, though not simultaneously.
- GST applicable as per Govt. rules.

Contact Us

Address: 1, Vagholkar Apts, RS Road, Thane (W) -400601
E: bharatacharyaeducation@gmail.com
M: +91 9820408217

6 Months | Unlimited Views | 999/-

www.BharatAcharyaEducation.com