5780_Postlab_03

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1 :

$$ARR = \frac{\omega_{source}}{(PSC+1)\omega_{target}} = \frac{8 \cdot 10^6 Hz}{(PSC+1) \cdot 60Hz} = \frac{133333}{PSC+1}$$

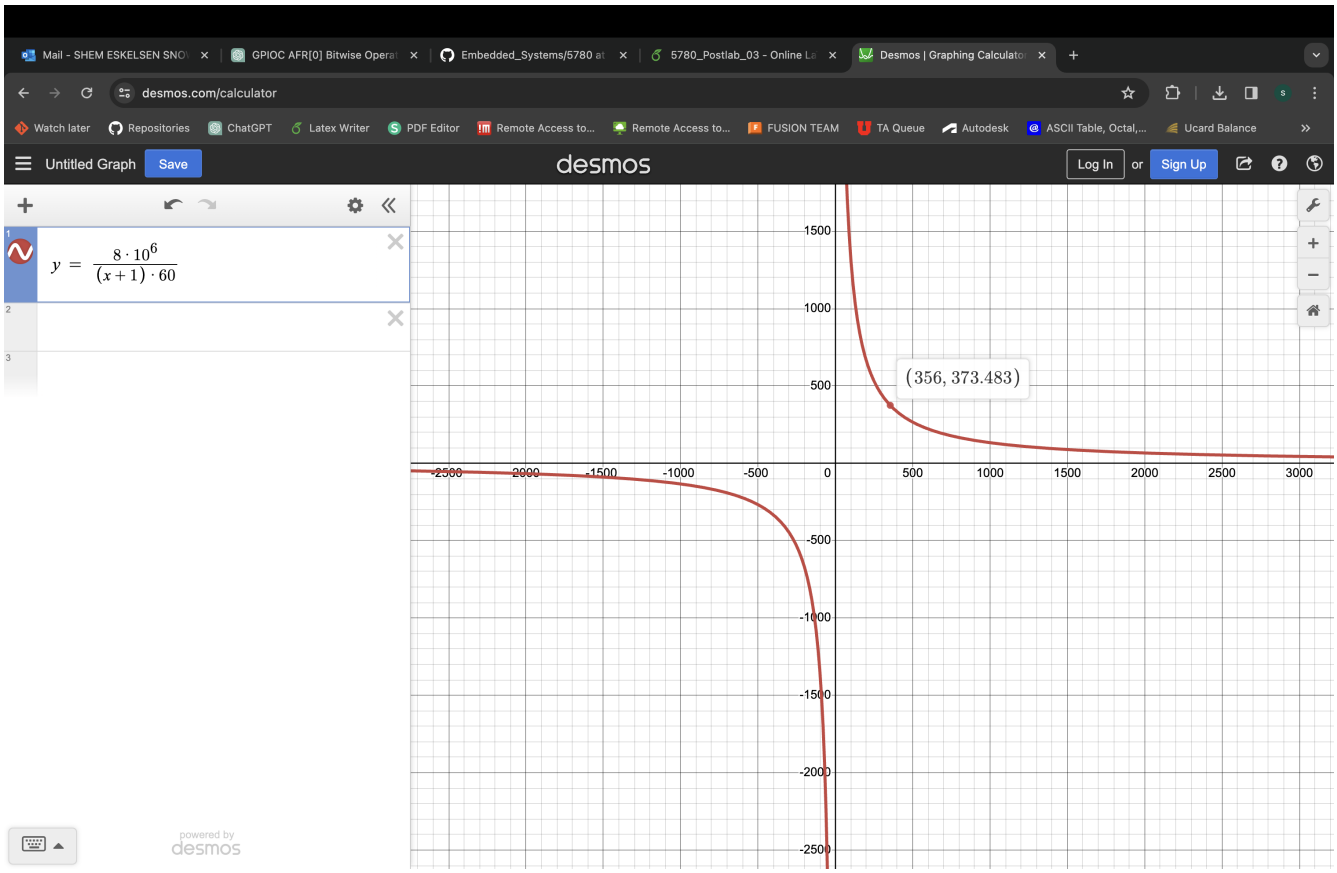

Figure 1: The plotted relationship between ARR and PSR registers with one example value shown.

I chose a point somewhere close to the middle where the two curves are closest.

2 :

From table 14 "STM32F072x8/xB pin definitions" in the chip datasheet, here are all the pins that can have the timer 3 capture/compare channel 1 alternate function.

Pin name	Alternate function number to select it on the LQFP64 package
PE3	$\emptyset$
PA6	22
PC6	37
PB4	56

3 :

Figure 2 shows the time delay between triggering an interrupt (which was done with the push-button) and the handler function responding (the green LED changing its state which is the first task performed in the interrupt handler). **It takes approximately 140 μs.**

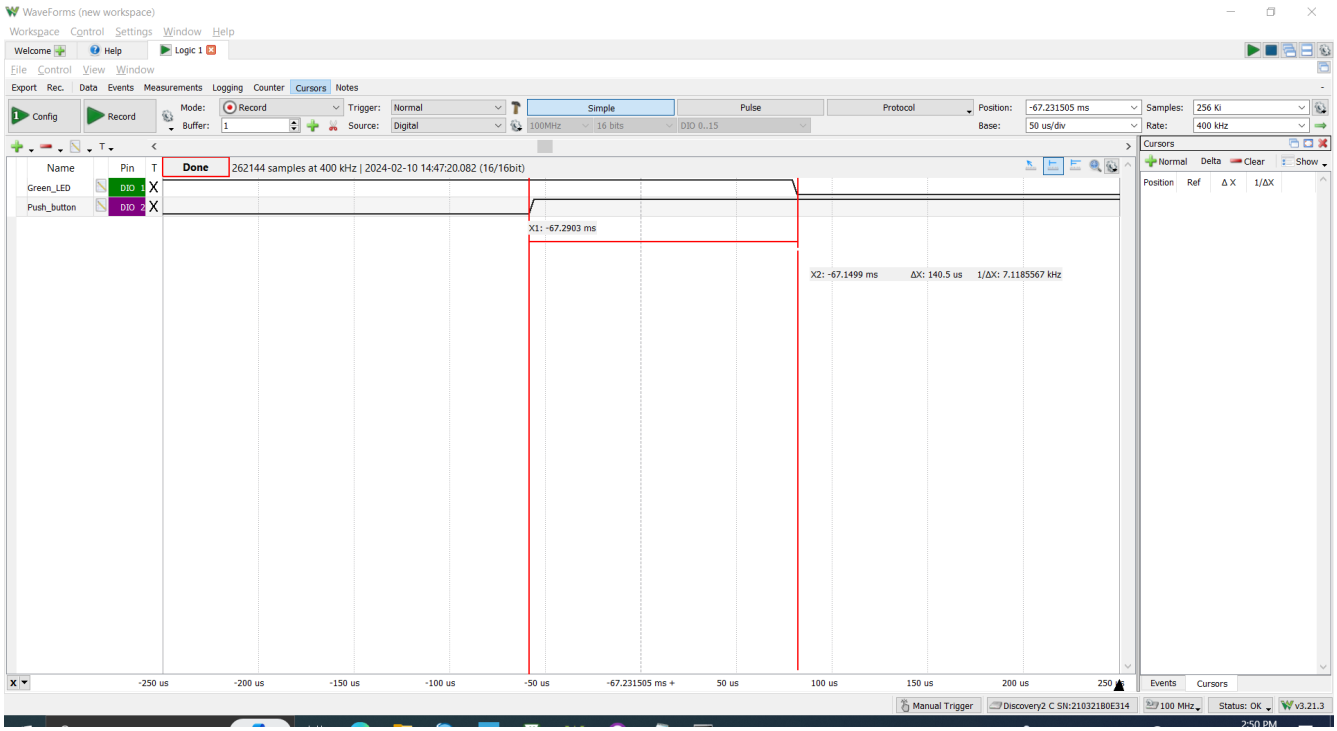

Figure 2: Timing from part 3.1

4 :

The Duty Cycle depends on the relative values of the capture/compare register (CCRx) and the Timer's Auto Reload Register (ARR) as well as the the operation mode selected by the capture/compare MODE registers (CCMRx). The relationship is shown in figure 3.

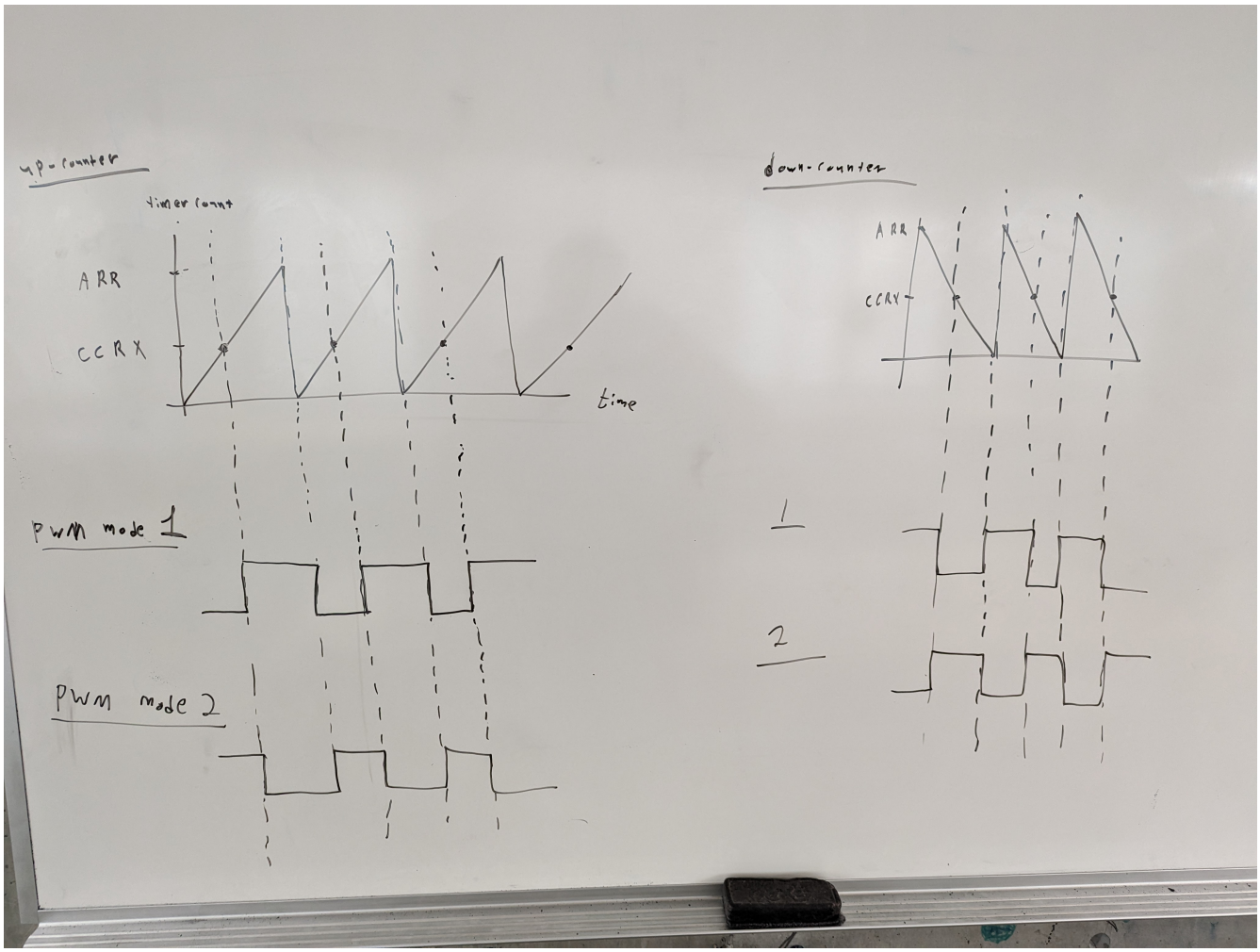

Figure 3: Sketch of PWM principle

Whether our discovery board's timer uses an up or down counter doesn't change the affect on the duty cycle. **When PWM mode is 1 and the CCRx value is increased, the duty cycle decreases because the active signal is compressed** (refer to figure 3).

5 :

Whether our discovery board's timer uses an up or down counter doesn't change the affect on the duty cycle. **When PWM mode is 2 and the CCRx value is increased, the duty cycle increases because the inactive signal is compressed** (refer to figure 3).

6 :

The Duty Cycle depends on the relative values of the capture/compare register (CCRx) and the Timer's Auto Reload Register (ARR) as well as the the operation mode selected by the capture/compare MODE registers (CCMRx). The relationship is shown in figure 3. Whether our discovery board's timer uses an up or down counter doesn't change the affect CCRx has on the duty cycle.

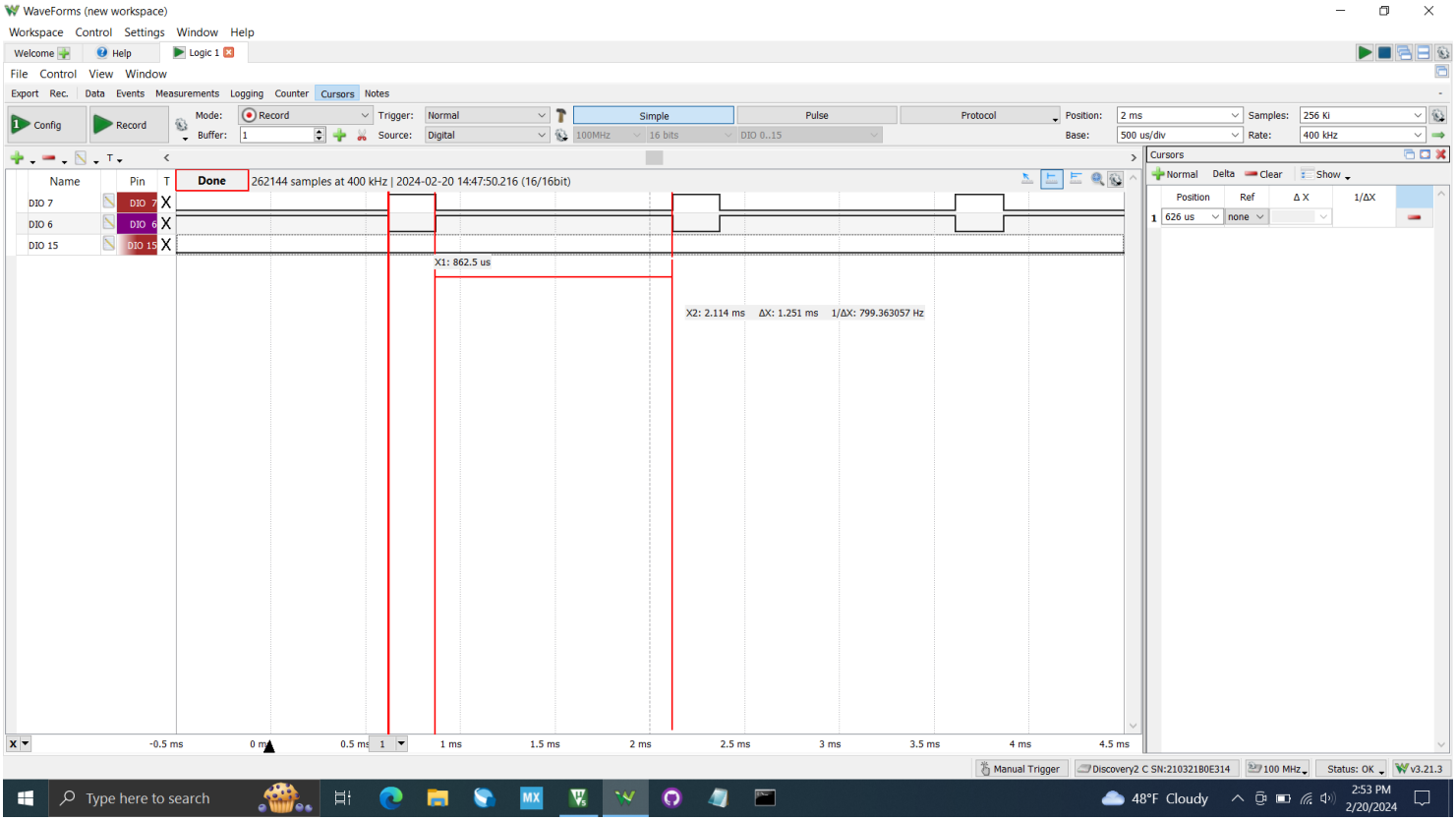

Figure 4: One of the screenshots I obtained when messing with the PWM ratios.

7 :

Figure 3.6 from the lab uses PWM mode 1. I know because the peripheral manual section 18.4.7 (pg 457) says bits [6:4] control the output compare mode.

It says

> 110: PWM mode 1 - In upcounting, channel 1 is active as long as TIMx_CNT<TIMx_CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF='0) as long as TIMx_CNT>TIMx_CCR1 else active (OC1REF=1).
> 111: PWM mode 2 - In upcounting, channel 1 is inactive as long as TIMx_CNT<TIMx_CCR1 else active. In downcounting, channel 1 is active as long as TIMx_CNT>TIMx_CCR1 else inactive.

Figure 5: This snippet is from the peripheral manual.