5780_Prelab_02

Shem Snow

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1 :

The Nested Vectored Interrupt Controller (NVIC) peripheral prioritizes (in levels of 0-192 in steps of 64 for each interrupt) and **controls the handling (enabling and disabling) of interrupts from various sources**. Indicating requests waiting for servicing, canceling pending interrupt requests, and establishing how multiple interrupts interact through configurable priorities.

2 :

Interrupt tail-chain and nesting are two different approaches for handling more than one interrupt at a time.

- **Interrupt nesting** is when a processor is currently servicing an interrupt (ISR - Interrupt Service Routine) but a higher-priority interrupt occurs so the processor temporarily stops executing the current ISR, jumps to the higher-priority ISR, and continues processing. Once the higher-priority ISR is completed, the processor returns to the original ISR.
- **Interrupt Tail-chaining** allows the processor to automatically start processing the next pending interrupt without returning to the main program after completing an ISR. This can improve the efficiency of interrupt handling by reducing the overhead associated with returning to the main program and then re-entering the interrupt service routine. This is especially useful when dealing with a series of closely occurring interrupts because they execute one after each other in succession according to the hardware priority. It has the disadvantage of allowing a rapidly-triggering or long-running interrupt high on the hardware priority to "starve", or prevent lower interrupts from executing.

3 :

We have the choice of controlling the NVIC through the CMSIS library or register access. The CMSIS functions are located after the peripheral structure and register definitions **in the core_cm0.h file**.

4 :

The purpose of the External Interrupt (EXTI) peripheral is **to handle external interrupts generated by external events**. Its first 16 inputs are used for that.

5 :

In the STM32F0 family, only 16 available input lines connect to the EXTI. The System Configuration peripheral (SYSCFG) pin multiplexors **allow us to map specific GPIO pins to these 16 external interrupt lines, defining which pins can trigger external interrupts**.

6 :

The functions for interrupt handlers identify the interrupt to be modified by a number representing its index in the Vector table. These **interrupt numbers have been given defined names in the IRQn_Type enumeration within the "stm32f072xb.h" file**.

7 :

The MDK:ARM toolchain includes a set of **function names used for interrupt handlers in the Vector table located in "startup_stm32f072xb.s"**.