5780_Postlab_06

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1 : Consider a system where the DAC is updated every 4us (250 kHz) with a value from a 200- element wave table containing a single cycle of a waveform. What would be the frequency of the output wave?

$$\omega_{output} = \frac{\omega_{update}}{Table\ Size} = \frac{250}{200} kHz = 1.25\ kHz = 1,250\ Hz$$

This is the same concept as a clock divider where the update frequency is the fast clock and the output frequency is the slow clock. The table size is the reset value where after that many updates on the slow clock (ω_{update}) have occurred one update on the fast clock (ω_{out}) occurs. Except in literal terms, the slow clock is really the complete drawing of a single wave.

2 : Consider that the ADC in 12-bit mode divides the input voltage range (0-3V) into 4096 steps (where 0V is 0, and 3V is 4095).
• What is the voltage/measurement resolution (how much does the voltage change per bit) of the ADC?
• What would be the ADC output value (nearest integer) if the input voltage was 1.75V?

- The voltage/measurement resolution is

$$resolution = \frac{range}{\#\ discrete\ elements - 1} = \frac{3}{4095} V = 0.7326\ mv$$

- The ADC output value for the input of 1.75 V is

$$ADC\ output = \frac{inputvoltage}{resolution} = \frac{1.75\ V}{0.7326\ mv} \approx 2389 = (100101010101)_2$$