5780_Prelab_05

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1 : Describe two differences between I2C master and slave devices?

1. Master devices initiate communication with slave devices however slave devices can respond to a master device only when requested. They can't start a new transaction on their own.
2. Each slave device has an unique hardware I2C address and the master selects a specific slave by sending its address on the bus.

2 : What are the two connections in an I2C bus? Describe their purpose.

1. Serial Data (SDA) is the wire that actually holds the data being sent. Masters and slaves can both read from and write to it during the right condition.
2. Serial CLock (SCL) controls if and how data is sent on the SDA. The master drives transitions here and the slave can hold the signal low if it needs more time to process (called clock stretching). Both the master and the slave can adjust this line to acknowledge their reception of data.

3 : What is the difference between open-drain and push-pull outputs?

The difference is the use of transistors. Push-pull uses both PMOS and NMOS (CMOS) so they can be pushed high by connecting to ground and pulled low by connecting to VDD. Open-drain uses only NMOS with a pull-up resistor so the device can be pushed high (NMOS transistors not being stimulated will remain 'shut') but this requires an external signal to be connected to the pull-up resistor.

The reason open-drain configurations are preferred for communication is so that conflicting signals (high and low at the same time) do not stress/damage the transistor or waste power. This works because the pull-up resistor limits the current flow through the NMOS transistor.

4 : What is the purpose of the I2C restart condition?

Every time a stop condition occurs, any master competing for the BUS may potentially hijack it. So when we want to perform 'chained transactions', we will not drive the stop condition and instead will drive a new start condition from the same master. This maintains the BUS controlled by the same master for each transaction in the chain.

5 : What peripheral register would you use to set the read/write direction of the next I2C transaction?

Control Register 2 (I2C_CR2) manages the current transaction. Specifically, the RD_WRN bit sets the direction of data transfer.

6 : The 10-bit SADD bit-field holds the slave device address. Since standard I2C addresses only use 7 bits, to which bits in the bit-field would you write the shorter address?

The default 7-bit addressing mode uses bits [7:1].

7 : Name one thing you found confusing or unclear in the lab.

I still have some confusion about how data frames relate to the two wires (SDA and SCL). I know the information I submitted for question 2. I would assume that a frame is just a set of signals that start with the start condition and end with the end condition. So then what about in the special cases like reset signals with multiple start conditions? Are there sub-frames or does the whole thing count as a frame?