NClaunch Tutorial

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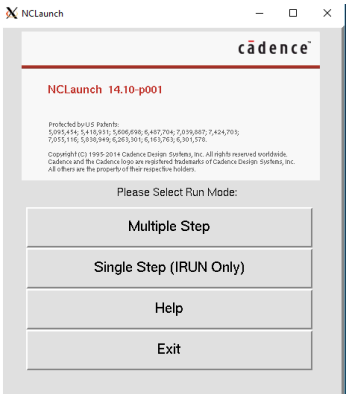
NClaunch Tutorial

Download the lab folder from Canvas, which includes all the necessary files for this lab. Then copy these files to the Wilkinson lab server.

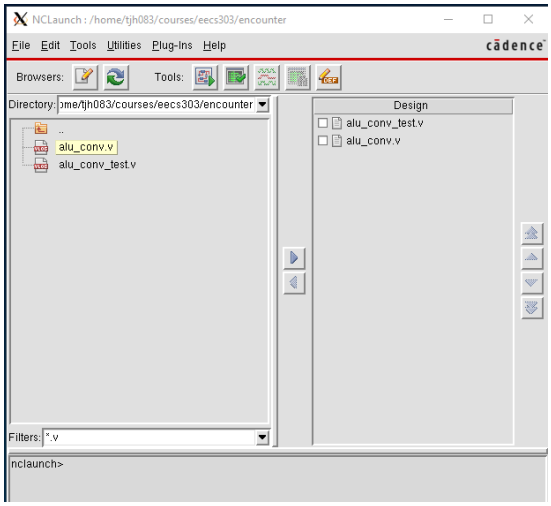
1. RTL simulation

In this part, you only need the verilog code (RTL) "alu_conv.v" and its testbench "alu_conv_test.v".

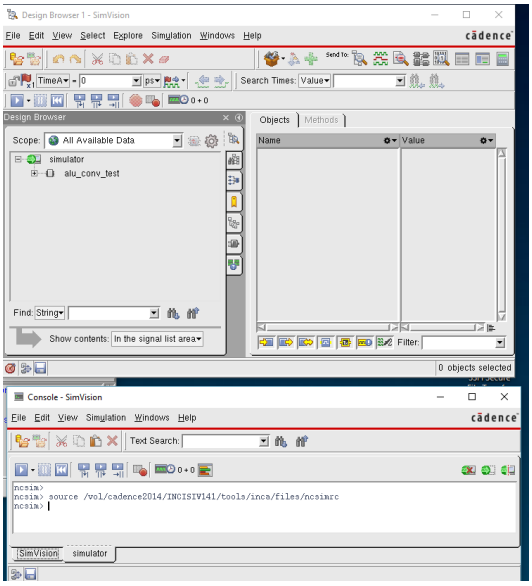
1) Enter the following commands to source the cadence environment
   source /vol/ece303/encounter_tutorial/cadence.env
2) Type "nclaunch" and press enter to run the cadence tool. In this case you will see a new open window like this:



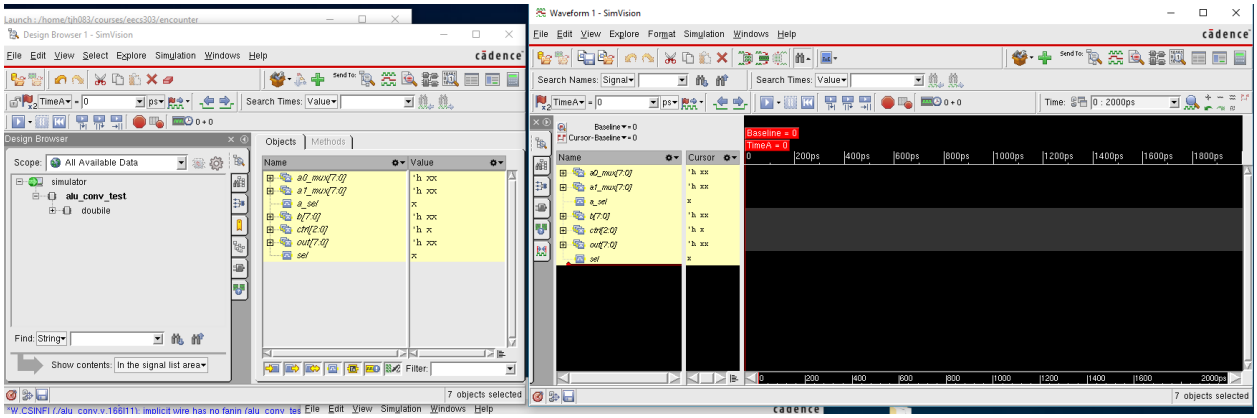
   Then choose "Single Step (IRUN Only)".
3) Make sure your Design Directory is set properly (important)
   File -> Set Design Directory
4) Switch into single step mode
   File -> Switch to Single Step
5) Add all the needed files into right sub-window and make sure "alu_conv.sdf" file is in is the Design Directory as well (important)
   a. Test bench (alu_conv_test.v)
   b. RTL verilog code (alu_conv.v)



6) Launch IRUN in Tools -> IRUN.
   With Default setting, click OK. Then there will be a **SimVison** window pop-up.



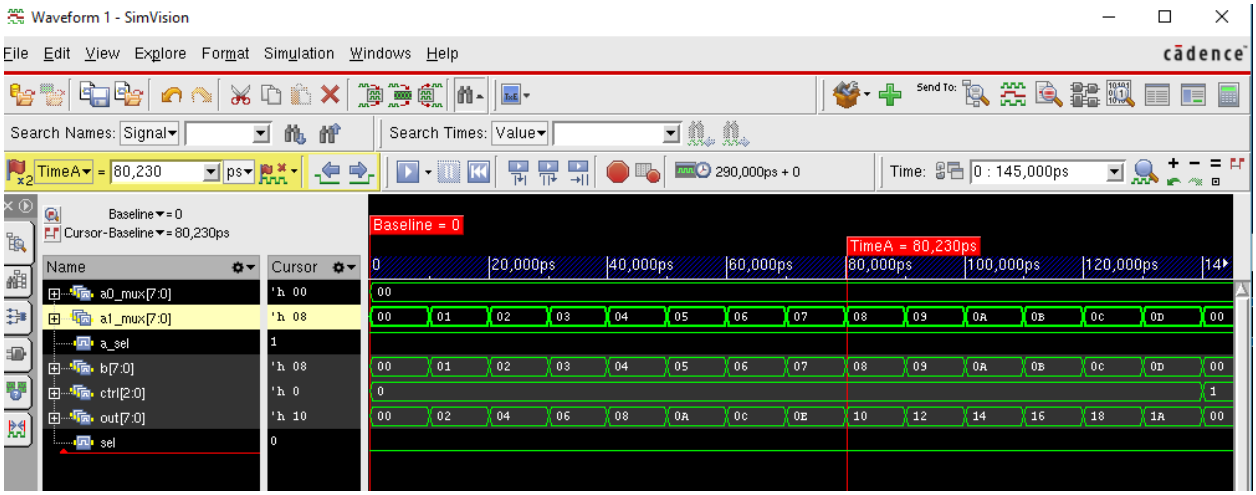
7) In this window you can select the signal you want to send to the **Waveform Window** (right click a signal -> Send to Waveform Window)



8) In the Waveform SimVison window you can simulate your design.

Simulation->Run. Note: You need to use zoom in/out function to pick the expected observation time period.

Based on the observation, you can confirm whether the function is correct of your RTL code.



2. Gate level netlist simulation:

To do this part, you need first finish the Encounter lab. Check the other tutorial "Encounter Tutorial".

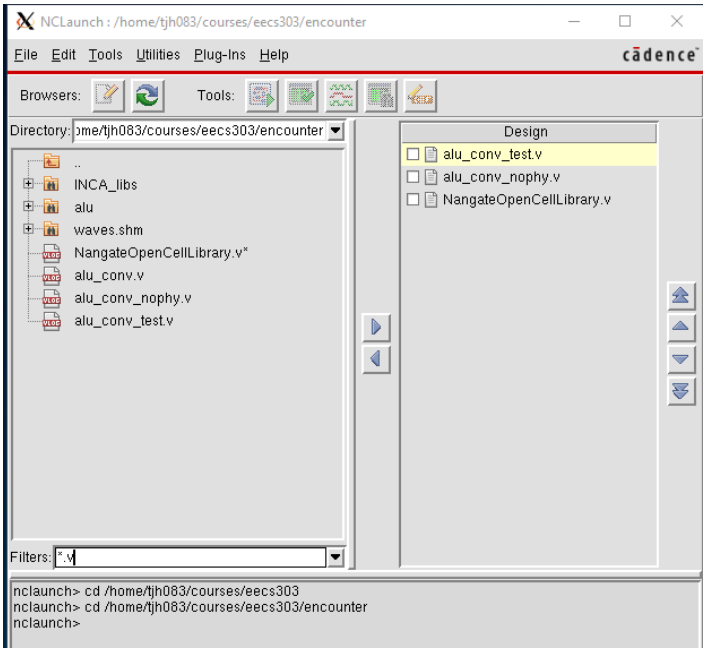
After you finish the Encounter lab, you should have two files:

1. **alu_conv_nophy.v (This is the gate level netlist file)**
2. **alu_conv.sdf (This is the timing file for your design)**

Copy these two files from the "backend" folder to your NClaunch simulation directory.

Also copy file /vol/ece303/encounter_tutorial/NangateOpenCellLibrary.v to the local directory.

1) Launch NClaunch again.
2) Add all the needed files into right sub-window
   a. Test bench (alu_conv_test.v)
   b. Gate level netlist (alu_conv_nophy.v)
   c. Lib file (NangateOpenCellLibrary.v)

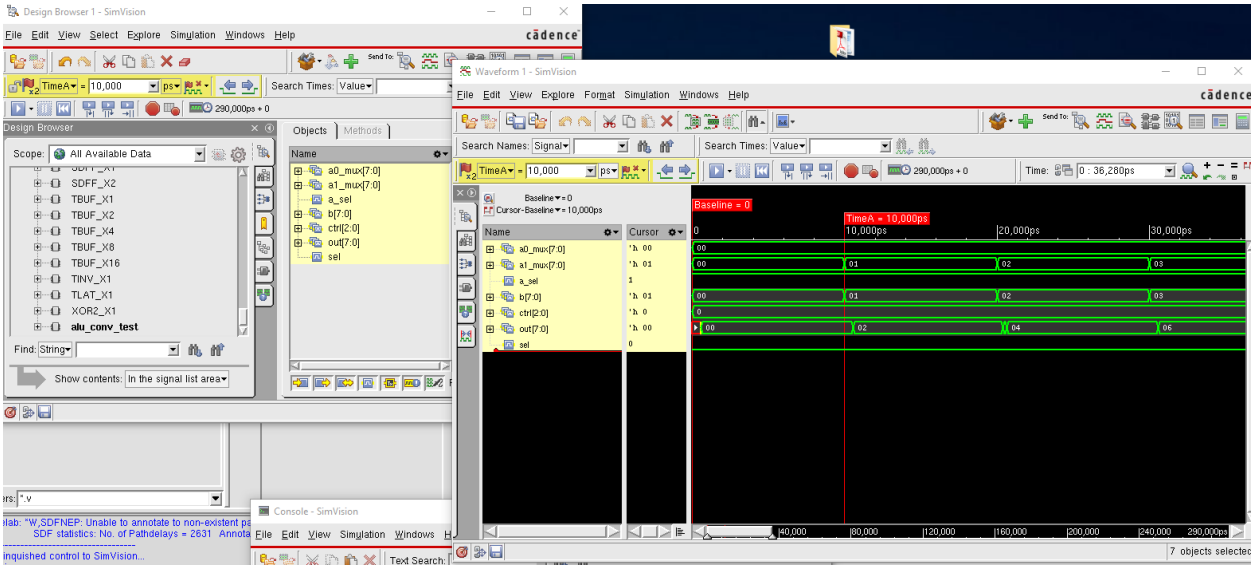


3) Modify IRUN options

Tools -> IRUN -> Advanced Options

   a. IRUN Options:
      Click **Elaborator Options** and write: -autosdf
   b. Performance Tuning:
      Click **Delay Modes** and pick **None (+delay_mode_none)**
   c. Timing
      Delay Modes: **None (+delay_mode_none)**
      Delay Types: Maximum(+maxdelays)
   d. Pulse Control
      Delay Modes: **None (+delay_mode_none)**
      Delay Types: Maximum(+maxdelays)
   e. Errors and Messages
      Click **Screen Startup/Finish Output (-q)**

4) After Click OK in the IRUN window, there will be a **SimVison** window pop-up, in this window you can select the signal you want to send to the **Waveform Window** (right click a signal -> Send to Waveform Window). In the Waveform SimVison window you can simulate your design.



The result of the gate level simulations should match with the RTL simulations. But there is obvious timing delay between the inputs and outputs, as shown in the figure above.