Encounter Tutorial

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Download the lab folder from Canvas, which includes all the necessary files for this lab. Then copy these files to the Wilkinson lab server.

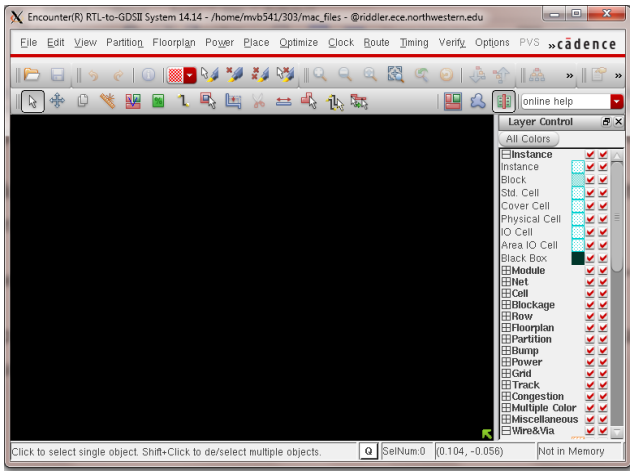
Before going to next steps, please note that those lines that start with '#' are explanation and you need to follow them in GUI. Otherwise, they are commands and you need to write them in your command prompt and press enter.

1) # Type command: "source /vol/ece303/encounter_tutorial/cadence.env".

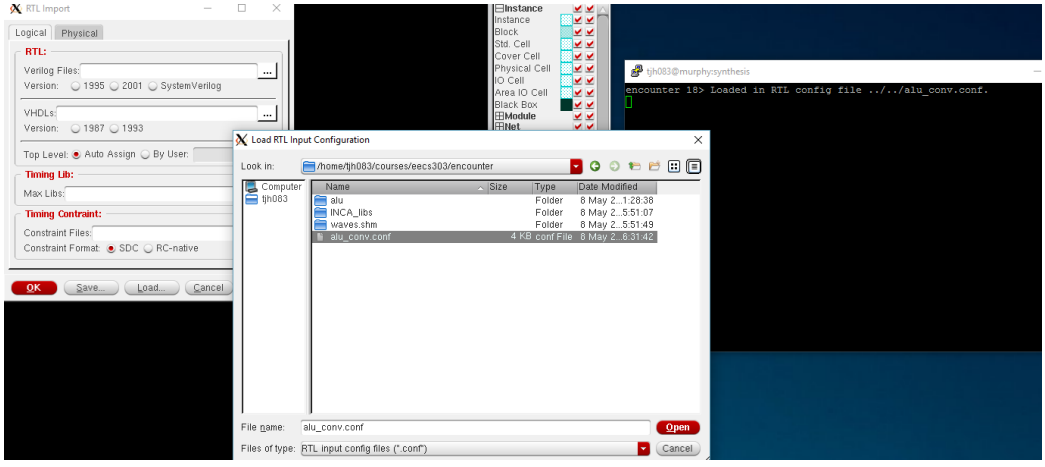
2) # Create "alu" folder under your working directory, for example "Lab1", and then create "synthesis" and "backend" folders under "alu" folder using "mkdir folder_name". **Important: The download files should be located at top folder, e.g. Lab1. Otherwise the path link in alu_conv.conf file should be modified.** The folder structure looks likes:

Lab1 folder contains: alu_conv.v , alu_conv.conf , alu_conv.sdc , alu (folder). Inside alu folder, you have two folders: synthesis and backend.

3) # Go to **synthesis** folder and then type "encounter" and press enter to run the cadence tool. In this case you will see a new open window like this:



4) # use GUI to **load** RTLConfig file (File -> Import RTL -> Load -> '../../alu_conv.conf'), and click **Cancel** instead of **OK**!!

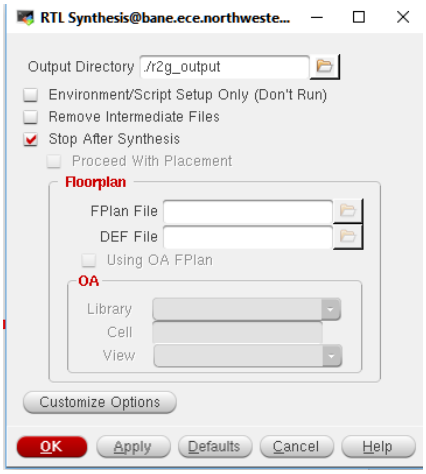


5) # Run RTL Synthesis (File -> RTL Synthesis)

   a. Click **Stop After Synthesis**

   b. Click **OK**

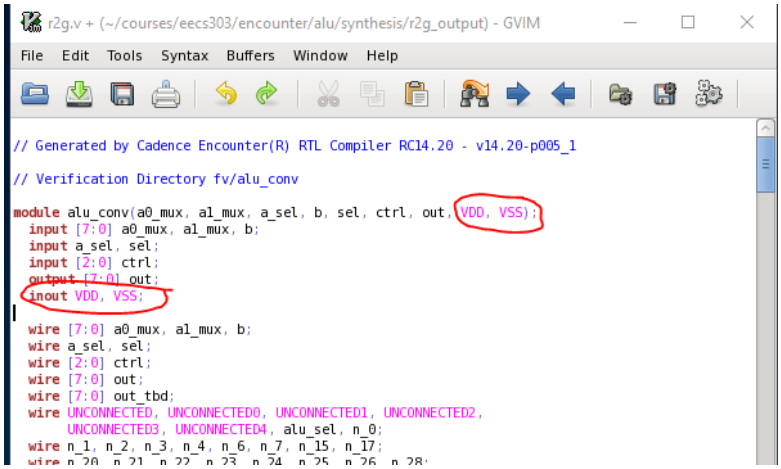
Now you will have your gate level *.v and *.sdc files ready in ./r2g_output/...



6) # Add "VDD" and "VSS" into the file in ./r2g_output/alu_conv.v as below and save the file:

   a. Go to the directory ./r2g_output/

   b. **Open** r2g.v and add "VDD" and "VSS":



7) # Close encounter and go to "backend" folder and reopen encounter (**important,** otherwise you have to modify the paths in "alu_conv.view" file by yourself)

8) # Import Design (File -> Design Import)

   a. **Verilog**: use the gate level r2g.v (../synthesis/r2g_output/r2g.v) with **Top Cell** by clicking **Auto Assign**

   b. **LEF Files**: "/vol/ece303/encounter_tutorial/NangateOpenCellLibrary.lef"

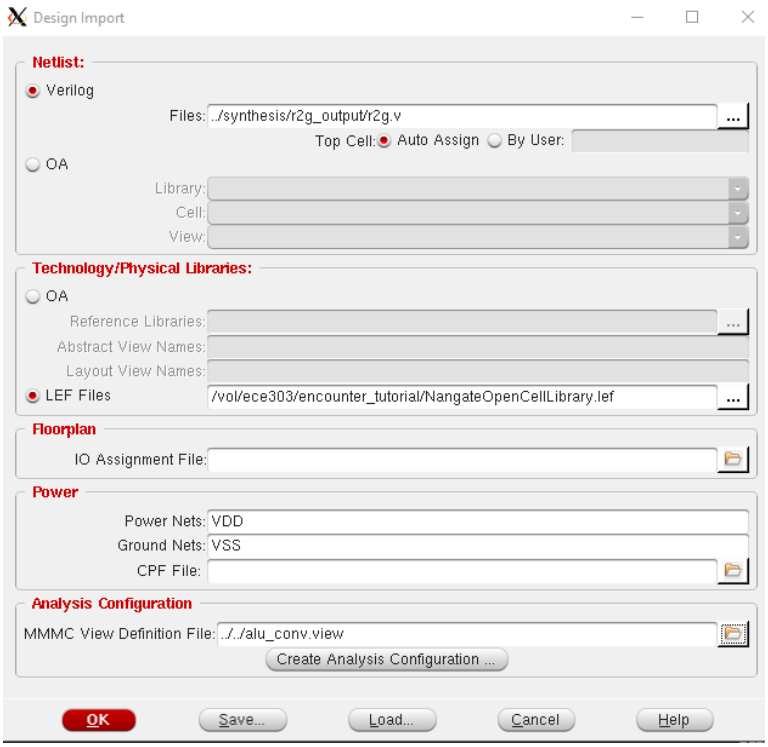
   c. **MMMC View Definition File**: "../../alu_conv.view" (comes from the download folder)

   d. **Power**:

      i. Power Nets: VDD

      ii. Ground Nets: VSS

   e. Click **OK**



9) #commitConfig. **For the following lines without "#", you should copy, and then paste into the Terminal, which means you will not use the GUI to operate any more.**

```
fit
setDrawView fplan
getIoFlowFlag
```

10) # This command prepares your floor plan layout and assign its option. You can find the details in the GUI.

```
floorPlan -site CORE -r 1.0 0.63 0 0 0 0
uiSetTool select
getIoFlowFlag
```

11) # the following two commands set your VDD and VSS pins.

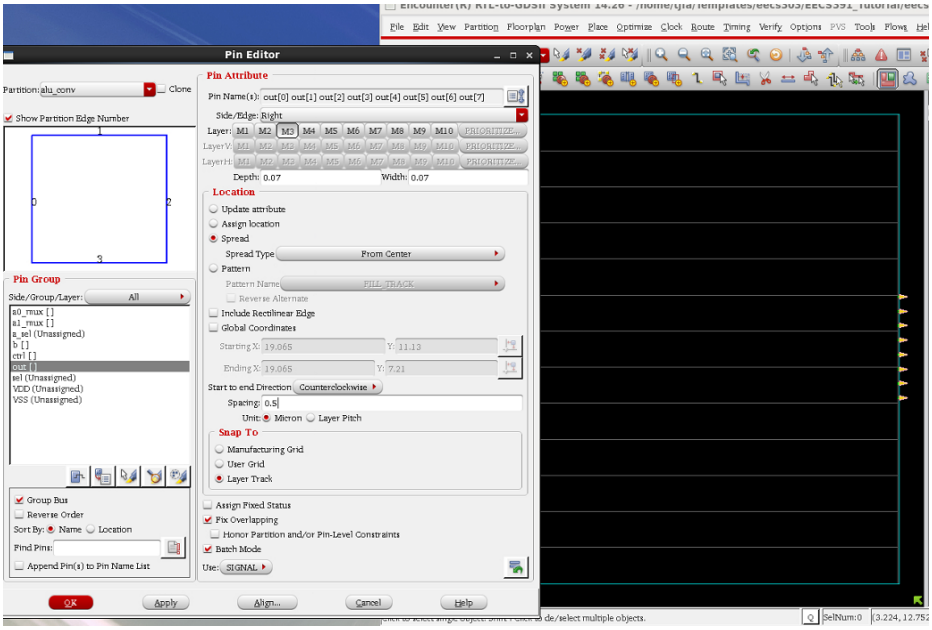
```
globalNetConnect VDD -type pgpin -pin VDD -inst *
globalNetConnect VSS -type pgpin -pin VSS -inst *
globalNetConnect VDD -type tiehi
globalNetConnect VSS -type tielo
```

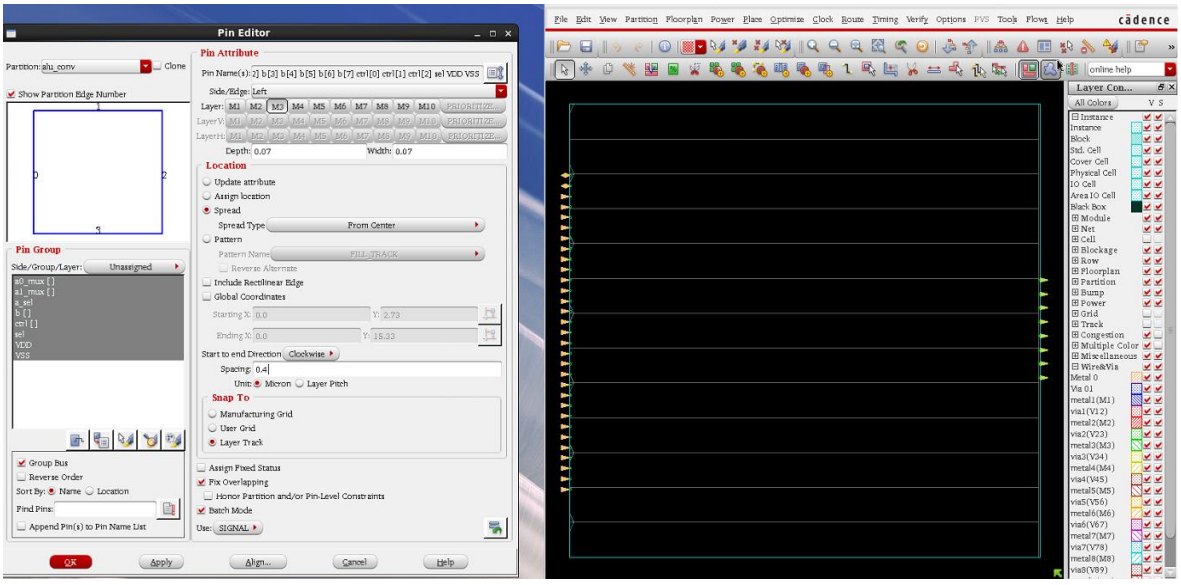
12) # **Edit Pin Locations** (Edit -> Pin Editor) **(Use GUI for this step)**

For example, you can allocate the OUT at the right edge, M3 layer, spread from Center, with the space 0.5.

The rest pins allocated on the left side with space 0.4.

The location and space value is not fixed. As long as all the pins are well allocated and shown, it is also ok.



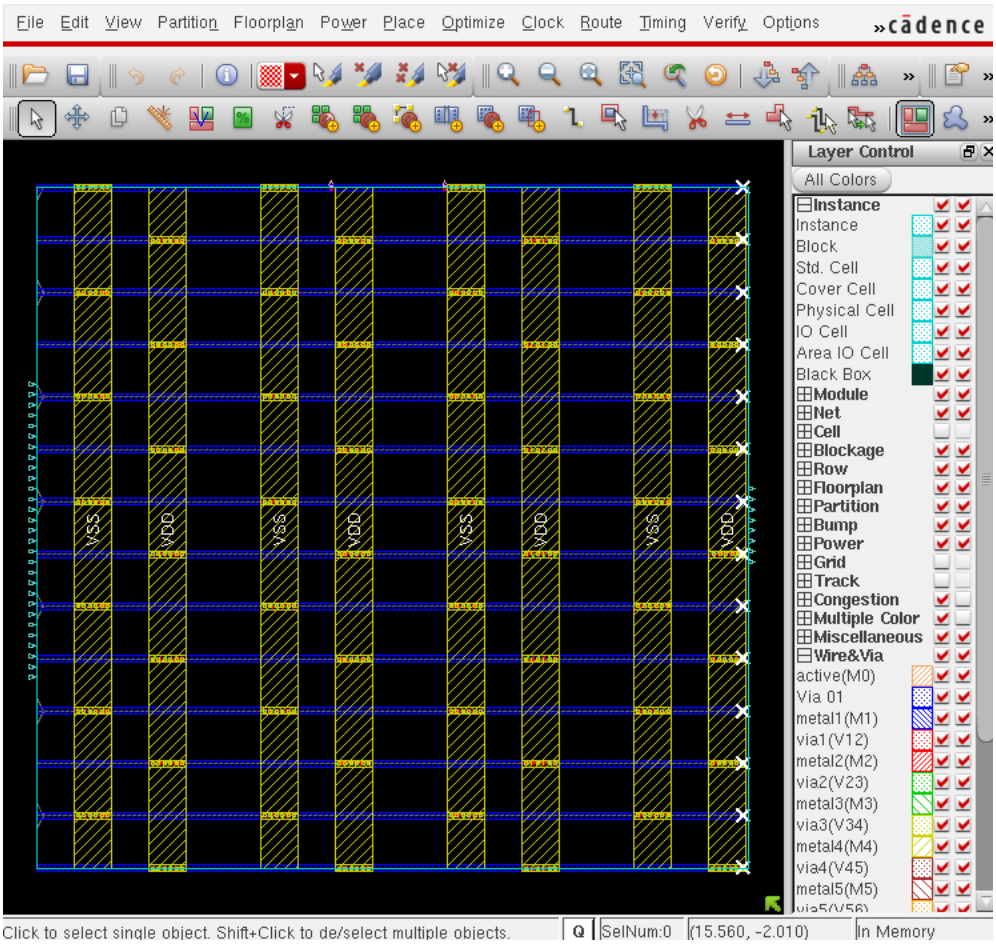


13) saveDesign alu_conv_fl.enc

14) # The following command create power ring and stripes.

addStripe -block_ring_top_layer_limit metal5 -max_same_layer_jog_length 1.6 -padcore_ring_bottom_layer_limit metal3 -set_to_set_distance 5 -stacked_via_top_layer metal10 -padcore_ring_top_layer_limit metal5 -spacing 1 -xleft_offset 1 -merge_stripes_value 0.095 -layer metal4 -block_ring_bottom_layer_limit metal3 -width 1 -nets {VSS VDD } -stacked_via_bottom_layer metal1

sroute -connect { blockPin padPin padRing corePin floatingStripe } -layerChangeRange { 1 10 } -blockPinTarget { nearestRingStripe nearestTarget } -padPinPortConnect { allPort oneGeom } -checkAlignedSecondaryPin 1 -blockPin useLef -allowJogging 1 -crossoverViaBottomLayer 1 -allowLayerChange 1 -targetViaTopLayer 10 -crossoverViaTopLayer 10 -targetViaBottomLayer 1 -nets { VSS VDD }



15) saveDesign alu_conv_power.enc

16) # The following command place standard cells

editPowerVia -skip_via_on_pin Standardcell -bottom_layer metal1 -add_vias 1 -top_layer metal8

saveDesign alu_power.enc

setEndCapMode -reset

setEndCapMode -boundary_tap false

setPlaceMode -reset

setPlaceMode -congEffort auto -timingDriven 1 -modulePlan 1 -clkGateAware 1 -powerDriven 0 -ignoreScan 1 -reorderScan 1 -ignoreSpare 0 -placeIOPins 0 -moduleAwareSpare 0 -preserveRouting 0 -rmAffectedRouting 0 -checkRoute 0 -swapEEQ 0

setPlaceMode -fp false

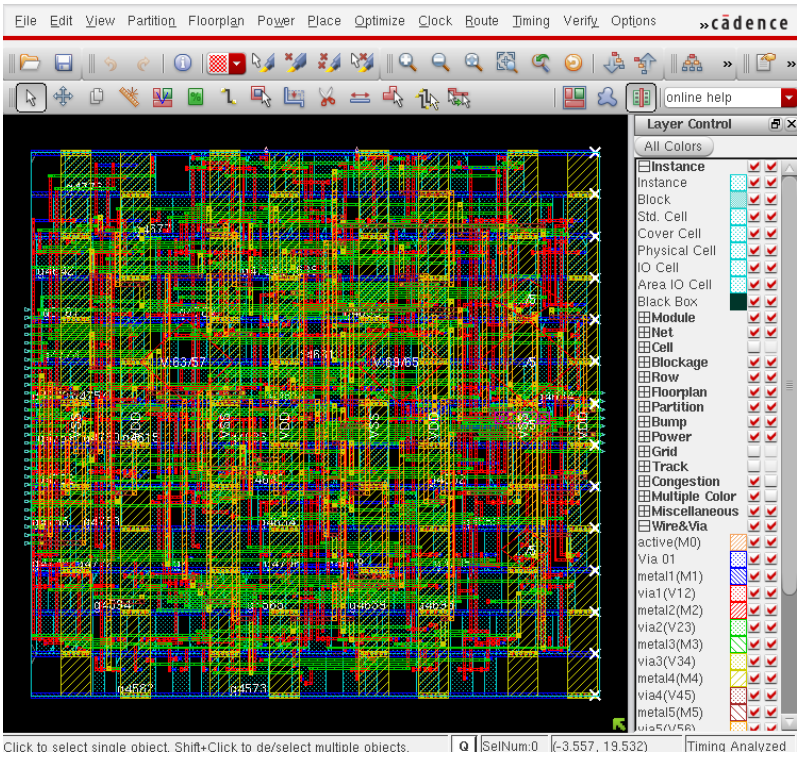
placeDesign

timeDesign -preCTS -numPaths 200

optDesign -preCTS -numPaths 200

setDrawView place

saveDesign alu_conv_pl.enc



17) #The clock system will be established. Detailed clock specification is in Clock.ctstch.

setCTSMode -engine ck

clockDesign -specFile Clock.ctstch -outDir clock_report -unfixedInstBeforeCTS

checkPlace alu.checkPlace

timeDesign -postCTS -numPaths 200

timeDesign -postCTS -hold -numPaths 200

optDesign -postCTS -numPaths 200

optDesign -postCTS -hold -numPaths 200

timeDesign -postCTS -hold -numPaths 200

timeDesign -postCTS -numPaths 200

saveDesign alu_clk.enc

18) # The following command add filler cells to the design

getFillerMode -quiet

addFillerGap 0.6

addFiller -cell FILLCELL_X1 FILLCELL_X2 FILLCELL_X4 FILLCELL_X8 -prefix FILLER -markFixed

saveDesign alu_powerroute_clk_filler.enc

setAnalysisMode -cppr none -clockGatingCheck true -timeBorrowing true -useOutputPinCap true -sequentialConstProp false -timingSelfLoopsNoSkew false -enableMultipleDriveNet true -clkSrcPath true -warn true -usefulSkew false -analysisType onChipVariation -log true

setNanoRouteMode -quiet -drouteFixAntenna false

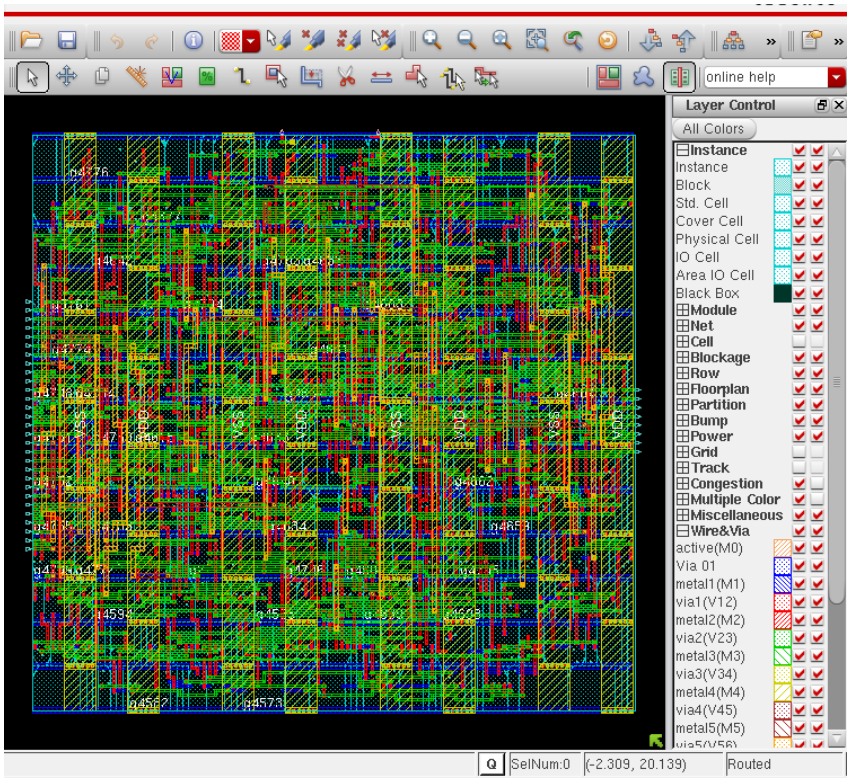
setNanoRouteMode -quiet -routeTopRoutingLayer default

setNanoRouteMode -quiet -routeBottomRoutingLayer default

setNanoRouteMode -quiet -drouteEndIteration default

setNanoRouteMode -quiet -routeWithTimingDriven false

setNanoRouteMode -quiet -routeWithSiDriven false
setNanoRouteMode -quiet -routeTopRoutingLayer 6
routeDesign -globalDetail
saveDesign alu_conv _powerroute_clk_filler.enc



19) # Timing analysis are established by the following commands

timeDesign -postRoute -pathReports -drvReports -slackReports -numPaths 400 -prefix alu_conv_postRoute -outDir timingReports

clearClockDomains

timeDesign -postRoute -hold -pathReports -slackReports -numPaths 400 -prefix alu_conv_postRoute -outDir timingReports

saveDesign alu_final_layout.enc

20) # Generate "alu_conv_nophy.v: used for gate level netlist simulation (NClaunch)

saveNetlist -phys -includePowerGround alu_conv_phy.v -excludeLeafCell

saveNetlist alu_conv_nophy.v -excludeLeafCell

write_sdf alu_conv.sdf

21) At this point, you finish all the Encounter flow operations.

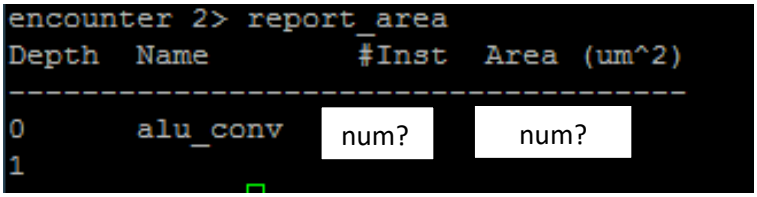
You should already generate two files for the following NClaunch simulations:

1. **alu_conv_nophy.v (This is the gate level netlist file)**
2. **alu_conv.sdf (This is the timing file for your design)**

Some commands you need to know for the assignment. Use these commands when you finish all the steps above, and obtain the final layout design.

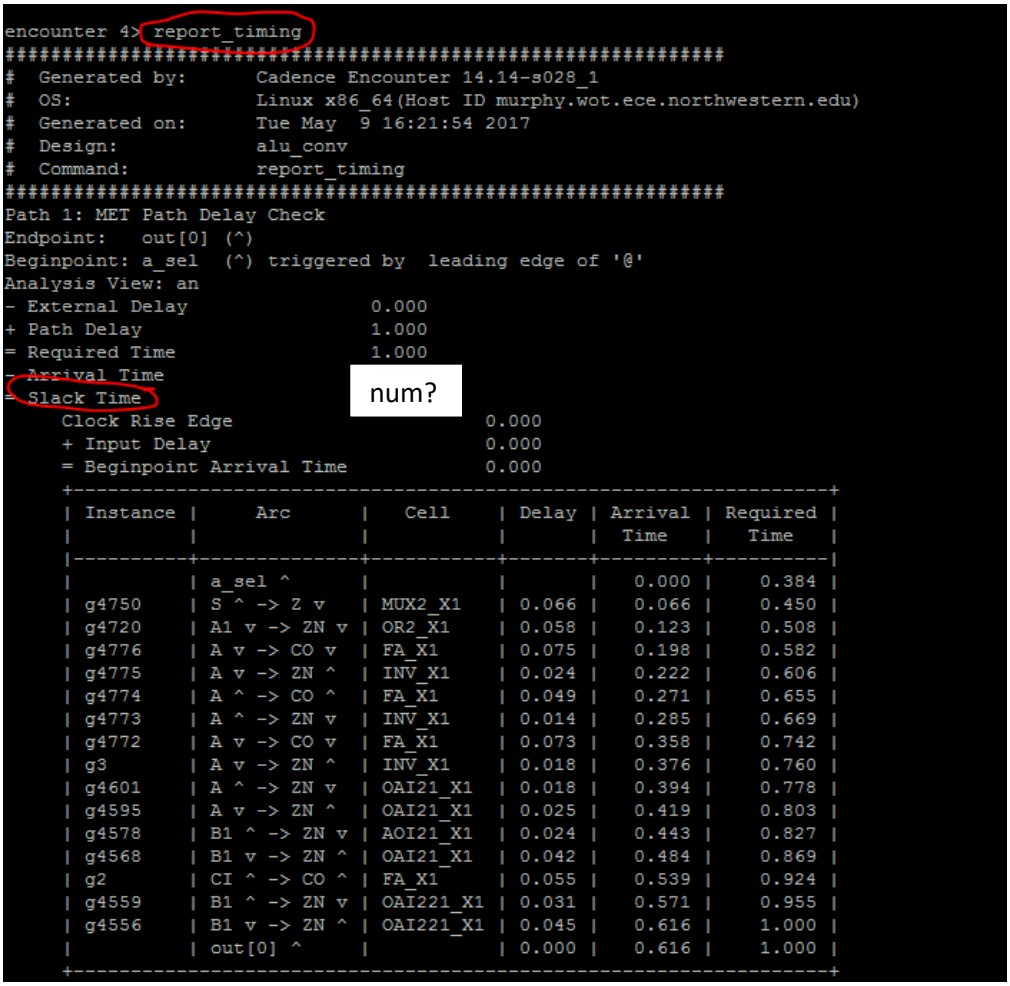
1. **Report_area**

   Enter report_area in Encounter, and it will return the design name, design area, and gate numbers. #Inst is the gate number of your design.



2. **Report_timing**

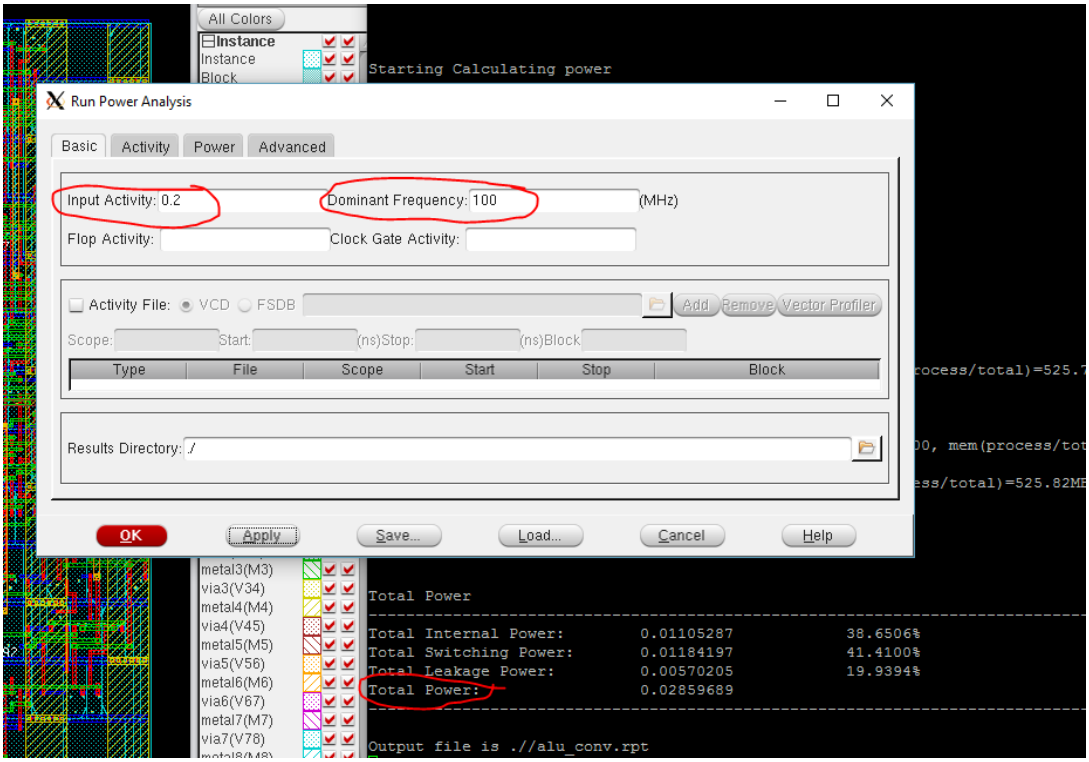
   Enter report_timingarea in Encounter, and it will return longest logic path, and the timing slack of the design.



3. **Design power**

   To measure the design power, you can go to Power -> Power analysis -> Run.

   Set to the expected activity factor and frequency, OK, then you can observe the design power in the terminal.


All Colors
Instance
Instance
Block
Starting Calculating power
Run Power Analysis
Basic
Activity
Power
Advanced
Input Activity: 0.2
Dominant Frequency: 100
(MHz)
Flop Activity:
Clock Gate Activity:
Activity File:
VCD
FSDB
Add
Remove
Vector Profiler
Scope:
Start:
(ns)Stop:
(ns)Block
Type
File
Scope
Start
Stop
Block
Results Directory: ./
OK
Apply
Save...
Load...
Cancel
Help
metal3(M3)
via3(V34)
metal4(M4)
via4(V45)
metal5(M5)
via5(V56)
metal6(M6)
via6(V67)
metal7(M7)
via7(V78)
Total Power
Total Internal Power: 0.01105287 38.6506%
Total Switching Power: 0.01184197 41.4100%
Total Leakage Power: 0.00570205 19.9394%
Total Power: 0.02859689
Output file is .//alu_conv.rpt