Lab #1

EECS 303: Advanced Digital Logic Design

(Due by 3:30pm 5/16/17)

1. Following the “NClanuch Tutorial” part 1, complete the RTL simulation. In the report, attach the screen shot of your simulation waveform, and show the input (a1_mux, b) and output (out) waveforms when ctrl = 3’b001 (subtraction) and verify the operation is correct.

2. Following the “Encounter Tutorial”, list the following items in your report:

    a. Screen shot of the final layout.

    b. Design area.

    c. Design gate numbers.

    d. Design power with activity 0.2 at 1GHz.

3. Following the “NClanuch Tutorial” part 2, simulate the generated gate level netlist.

    a. Compare the gate level simulation results with the previous RTL simulations.

    b. Pick one pair input and output, for example, from a1_mux[0] to out [0]. Check the delay between that input pin to output pin.