

## 9.4 Interrupt Descriptor Table

The interrupt descriptor table (IDT) associates each interrupt or exception identifier with a descriptor for the instructions that service the associated event. Like the GDT and LDTs, the IDT is an array of 8-byte descriptors. Unlike the GDT and LDTs, the first entry of the IDT may contain a descriptor. To form an index into the IDT, the processor multiplies the interrupt or exception identifier by eight. Because there are only 256 identifiers, the IDT need not contain more than 256 descriptors. It can contain fewer than 256 entries; entries are required only for interrupt identifiers that are actually used.

The IDT may reside anywhere in physical memory. As [Figure 9-1](#) shows, the processor locates the IDT by means of the IDT register (IDTR). The instructions [LIDT](#) and [SIDT](#) operate on the IDTR. Both instructions have one explicit operand: the address in memory of a 6-byte area. [Figure 9-2](#) shows the format of this area.

[LIDT](#) (Load IDT register) loads the IDT register with the linear base address and limit values contained in the memory operand. This instruction can be executed only when the CPL is zero. It is normally used by the initialization logic of an operating system when creating an IDT. An operating system may also use it to change from one IDT to another.

[SIDT](#) (Store IDT register) copies the base and limit value stored in IDTR to a memory location. This instruction can be executed at any privilege level.

Table 9-2. Priority Among Simultaneous Interrupts and Exceptions

Priority	Class of Interrupt or Exception
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HIGHEST     Faults except debug faults  
Trap instructions INTO, INT n, INT 3  
Debug traps for this instruction  
Debug faults for next instruction  
NMI interrupt  
LOWEST     INTR interrupt

Figure 9-1. IDT Register and Table

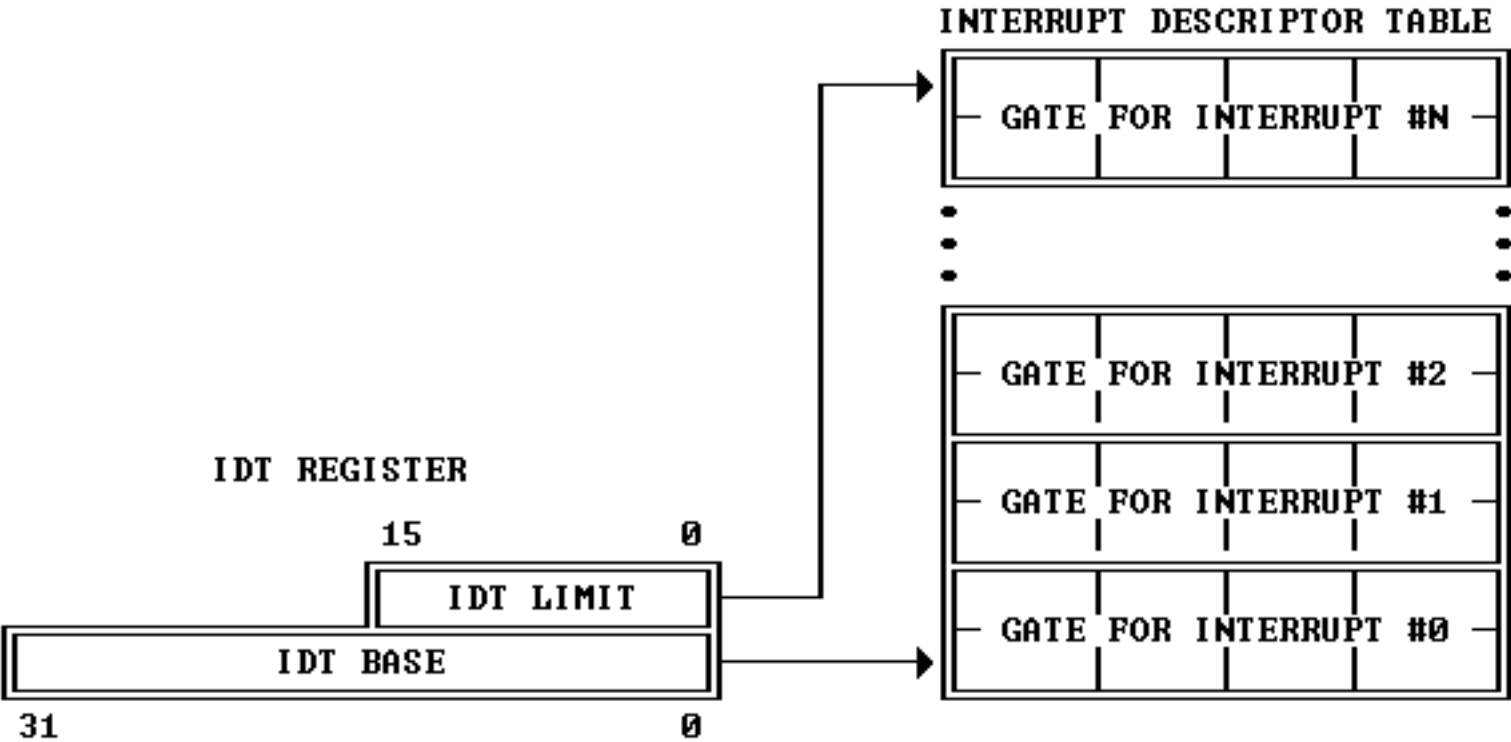
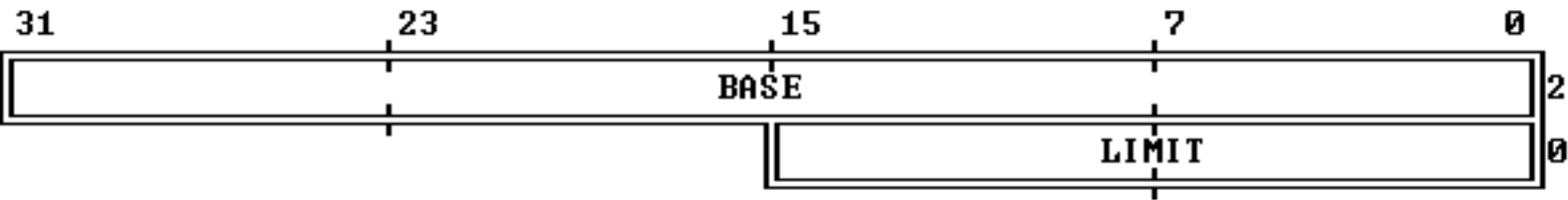


Figure 9-2. Pseudo-Descriptor Format for LIDT and SIDT



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