# Pseudo-Ramp Current Balance (PRCB) Technique With Offset Cancellation Control (OCC) in Dual-Phase DC-DC Buck Converter

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***Abstract*— To cope with monolithic controller replicas and the current unbalance situation in multiphase converters, a pseudo-ramp current balance technique is proposed to achieve time-multiplexing current balance in voltage-mode multiphase DC–DC buck converter. With only one modulation controller, silicon area and power consumption caused by the replicas of controller can be reduced significantly. Current balance accuracy can be further enhanced since the mismatches between different controllers caused by process, voltage, and temperature variations are removed. Moreover, the offset cancellation control embedded in the current matching unit is used to eliminate intrinsic offset voltage existing at the operational transconductance amplifier for improved current balance. An explicit model, which contains both voltage and current balance loops with non-ideal effects, is derived for analyzing system stability. Experimental results show that current difference between each phase can be decreased by over 83% under both heavy and light load conditions.**

***Index Terms*— Offset cancellation control (OCC), pseudo-ramp current balance (PRCB), pulse frequency modulator (PFM), pulse width modulator (PWM), skipping modulator, time-multiplexing (TM) current balance.**

## I. Introduction

THE demands for stringent power constrains in electronic devices requires DC–DC converters with many strict and challenging specifications. Especially, in high-performance microprocessor applications, multiphase DC–DC converters are essential owing to their high current driving capability, small output voltage ripples, and thermal management improvement [1]–[3]. A conventional N-phase DC–DC buck converter is shown in Fig. 1. Since N-phase voltage regulator modules (VRMs) in parallel simultaneously provide energy to load, high current driving capability and output ripple suppression can be achieved.

Owing to multiphase operation, N interleaving ramp signals, $\text{Ramp}_1$–$\text{Ramp}_N$, are needed to compare with the error signals ($V_{C1}$–$V_{CN}$) carried out from the error amplifier (EA) for generating N interleaving duty cycles, $D_1$–$D_N$, for each phase. Similar to conventional single-phase voltage-mode DC–DC buck converter, each VRM is controlled by one of the N independent controllers. Each controller contains a ramp signal, a comparator, and a control logic circuit. Obviously, the replicas of the controller derive large area and power dissipation.

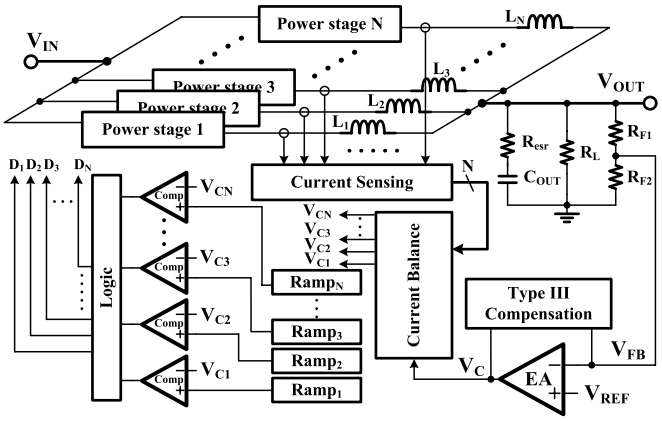


Fig. 1. Conventional structure of the N-phase voltage-mode DC–DC buck converter.

Furthermore, mismatches inevitably exist among N phases which include power MOSFETs, external inductors, and controllers. Extremely small mismatches among each phase cause enormously unbalanced current distribution. Simulation and measurement results show that one phase carries twice the current of another phase when current sharing function is disabled [4] and [5]. Moreover, the mismatches caused by the power path on the printed circuit board (PCB) also have to be considered essentially.

To conquer these problems, a paralleled DC-DC converter with average-current-sharing control is analyzed in [6]. Except N controllers which contain N ramps, N comparators, and N logic circuits, $N-1$ error amplifiers are adopted additionally comparing to conventional architecture for realizing current balance function. Several complicated current balance circuit are also proposed for thermal management improvement [7]–[11]. However, the current balance circuit can merely manage the mismatches of external components between phases. The mismatches among N controllers, which are caused by the process, voltage, and temperature variations, bring about the unbalance situation and are unable to be compensated.

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Besides, the area occupation and power loss carried out by N replica controllers grow proportionally as the phase number increases. Thus, to eliminate the mismatches of N controllers and suppress area and power consumption simultaneously, a multiphase voltage-mode hysteretic controlled DC–DC converter with only one controller was proposed in [4]. However, the duty cycle, which cannot exceed $1/N$ of the whole switching period, limits the output voltage conversion range. Therefore, a multistage interleaved synchronous buck converter with a simple phase shifter and a single current-mode comparator is presented in [12] to decrease area and power consumption. Still, the balanced distribution of inductor current in each phase could not be assured.

In this paper, the PRCB technique is proposed to improve performance and reduce circuit complexity in voltage-mode controlled multiphase DC–DC buck converter. The PRCB technique simply uses one controller operation with high precision current balance compared with prior arts. The time-multiplexing (TM) current balance in the PRCB technique is described in Section II. The system stability and offset analysis is illustrated in Section III. Detailed circuit implementations are presented in Section IV. Experimental results are shown in Section V. Finally, a conclusion is made in Section VI.

## II. Proposed Multiphase Structure and the PRCB Technique

Fig. 2 shows the proposed structure of N-phase DC–DC buck converter with the PRCB technique. The N-phase power stages, which are controlled by a single controller to achieve an area-efficient operation, can simultaneously deliver energy to the output to improve the driving capability. Each power stage contains power MOSFETs of one P-type and one N-type. The driver with dead-time control can prevent the short-through current. The voltage divider, composed of $R_{F1}$ and $R_{F2}$, feeds the output voltage information to the controller.

The main control scheme of the proposed multiphase converter is the voltage-mode operation [5], [6], and [9]. Thus, Type III compensation, which is composed of $R_1$–$R_3$ and $C_1$–$C_3$, generates three poles and two zeros to ensure system stability. Two zeros are generated to cancel LC double poles formed by $L_1$–$L_N$ and $C_{\rm OUT}$. The dominant pole locates at the origin. Tow parasitic poles are placed above unit-gain frequency. Thus, Type III compensation helps extend the system bandwidth and obtain an adequate system phase margin. Particularly, only one saw-tooth signal and one comparator are used to control the N-phase power stages. In other words, in the PRCB technique, N-phase converter can be achieved with the elimination of the $N-1$ controllers.

The pseudo-ramp operation and the TM current balance mechanism constitute the PRCB technique. The pseudo-ramp generator circuit generates the fixed-frequency system clock $V_{\rm clk}$ to realize PWM control. The multiphase clocks, $V_{\rm ck1}$–$V_{\rm ckN}$, are also generated to ensure synchronization. In addition, the saw-tooth signal $V_{\rm SAW}$ is used to determine the control signal $V_{\rm PWM}$ through the comparison of the error signals $V_C$, carried out by EA. Here, the proposed pseudo-ramp operation uses only one physical saw-tooth signal to obtain multiple pseudo-ramp signals for multiphase operation. The phase control logic is able to realize the duty cycles, $D_1$–$D_N$, for the $N$-phase power stages according to $V_{\rm ck1}$–$V_{\rm ckN}$

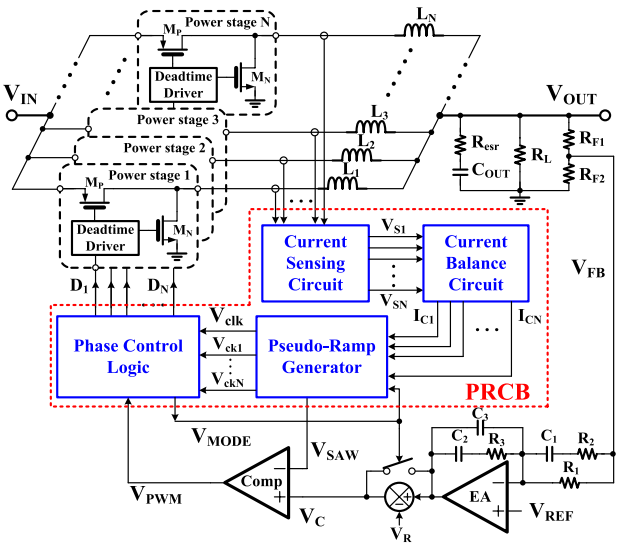



Fig. 2. Structure of the N-phase DC–DC buck converter with the proposed PRCB technique.

and $V_{\rm PWM}$. Moreover, the mode control signal $V_{\rm MODE}$ is used to determine the operation modes of the pseudo-ramp operation under different duty cycles. Specifically, the auxiliary reference voltage $V_R$ is utilized to ensure smooth mode transition operation.

On the other hand, the TM current balance mechanism is composed of the current sensing circuit and the current balance circuit. To ensure equal energy distribution in each phase, the current sensing circuit senses the inductor current information during each phase. The sensed inductor current information, $V_{S1}$–$V_{\rm SN}$, is sent to the current balance circuit for generating the signals, $I_{C1}$–$I_{\rm CN}$, to adjust the duty cycles of each phase. Therefore, the energy delivered by each phase will be matched regardless of the mismatch problem derived between the N-phase power stages, external components, and PCB.

### A. Pseudo-Ramp Operation

Fig. 3 shows the pseudo-ramp operation. Dual-phase topology is adopted to verify the proposed PRCB technique in this paper. The dual-phase PRCB operation can be divided into two modes: Mode I and Mode II, depending whether the duty cycle is smaller or larger than 50%, respectively. The two clock periods, $2*V_{\rm clk}$, constitute one complete switching cycle, $T_s$, for the dual-phase operation, i.e., one pseudo-ramp is composed of two physical ramps in one switching period.

In Mode I, both the duty cycles of Phases 1 and 2, $D_1$ and $D_2$, are smaller than 50%. When $V_{\rm MODE}$ is high, the duty cycle $D_1$ of Phase 1 is determined by the intersection of the odd physical ramps of $V_{\rm SAW}$ and $V_C$ as shown in Fig. 3. Because the duty cycle is smaller than 50%, $D_1$ can be determined within $T_S/2$ (i.e., within a physical ramp). In contrast, the $D_2$ of the Phase 2 is decided by the even ramps of $V_{\rm SAW}$. That means $D_1$ and $D_2$ are carried out by the odd and even physical ramps, respectively. In other words, the even physical ramps in the period from $T_S/2$ to $T_S$, work on the determination of $D_2$ and have no effect on the determination of $D_1$. In Mode I, only one saw-tooth signal $V_{\rm SAW}$ with a

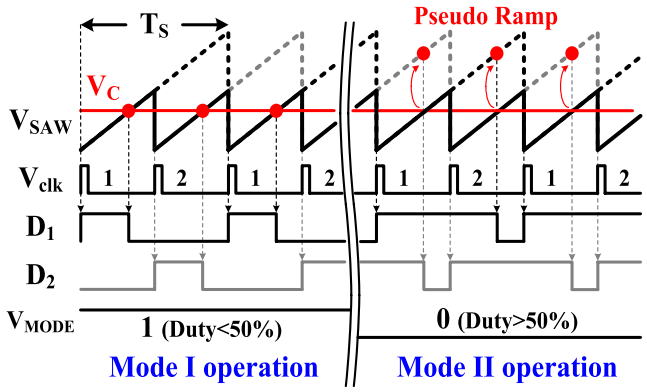



Fig. 3. Illustration of the PRCB technique in the Mode I and the Mode II.

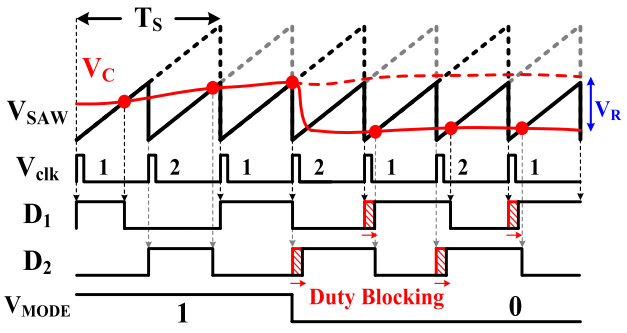



Fig. 4. Timing diagrams of mode transition with auxiliary reference voltage and the DBP.

fixed frequency is used to realize $D_1$ and $D_2$ for the dual-phase operation.

If the duty cycle is larger than 50%, the proposed PRCB technique will enter Mode II by setting the $V_{\rm MODE}$ low. Alternatively, $D_1$ is determined by the even ramps of $V_{\rm SAW}$. As a consequence, $D_2$ is decided by the odd ramps of $V_{\rm SAW}$. $D_1$ is high at the beginning of the odd ramps and becomes low when the even ramps intersect with $V_C$. In this regard, the intersection of the pseudo-ramp is extended by more than 50% of $T_S$. Thus, the duty cycle can be larger than 50%.

At the right-side of Fig. 3, the advantage of the PRCB technique is shown to break through the limitation of 50% duty cycles in dual-phase operation. Similarly, the duty cycle $D_2$ can be larger than 50%. Both $D_1$ and $D_2$ can be well-interleaved, regardless of the value of the duty cycle. Most importantly, only one physical ramp is needed to determine the two interleaving duty cycles.

However, an unstable scenario may occur when the duty cycle is exactly 50% because this condition occurs at the change of $V_{\rm SAW}$ from high to low. In other words, the transition induces a step increase in $V_C$. To solve the transition between Mode I and Mode II, deduction of the auxiliary reference voltage $V_R$ from the output of EA is activated, thereby speeding up the response of $V_C$. As shown in Fig. 4, $V_R$ helps smooth the mode transition when the duty cycle is near 50%. Moreover, the duty blocking period (DBP) is also utilized in Mode II to avoid duty cycle determination in the undistinguishable region. DBP results in the phase shift of the duty cycle in Mode II for stable operation because the proper duty cycle can be carried out. DBP helps define a hysteretic region to avoid abnormal mode transitions being triggered by switching noise.

### B. TM Current Balance Mechanism

Ideally, if each individual phase derives the identical duty cycles, $D_1 = D_2 = \cdots D_N$, the inductor current in each individual phase will be theoretically equal in the multiphase operation. However, the inevitable mismatches existing among the $N$ power stages and PCBs cause enormously unbalanced current distribution. Thus, current balance mechanism is required to compensate for the unbalanced scenario by automatically adjusting the duty cycles by $\hat{d}_i(t)$, (where $i = 1, 2, 3, \ldots, N$). Thus, the adjusted duty cycle of each phase becomes $d_i(t) = D_i + \hat{d}_i(t)$, (where $i = 1, 2, 3, \ldots, N$) to achieve current balance. Fig. 5 shows the implemented current balance mechanism in the proposed PRCB technique.

If one of the two phases has a large driving current, the duty cycle, that causes the large driving current, needs to decrease. In contrast, the other duty cycle is required to increase. Owing to the voltage-mode operation in the monolithic control scheme, the duty cycles are determined through the comparison of $V_{\rm SAW}$ and $V_C$ [5], [6], and [9] However, in the PRCB technique, adjusting $V_C$ for current balance is impossible because the change in $V_C$ will cause both duty cycles to simultaneously increase or decrease. Alternatively, the modulation in $V_{\rm SAW}$ is used to achieve the dual-phase current balance in the PRCB technique [13].

The TM current balance mechanism in the PRCB technique is activated according to the distinct operation modes. In Mode I, the ramp adjustments for $d_1(t)$ and $d_2(t)$ act on the odd and even ramps, respectively. If the inductor current $I_{L1}$ in Phase 1 is larger than $I_{L2}$ in Phase 2, the increase of the odd ramp slopes will lead to the decrease of $d_1(t)$ to reduce the current driving capability in Phase 1. In addition, the increasing $d_2(t)$ in Phase 2 will enhance its current driving capability by decreasing the even ramp slopes. Similarly, in case of large $I_{L2}$ and small $I_{L1}$, current balance can also be ensured in Mode I.

In contrast, if the duty cycle is larger than 50% in Mode II, the ramp adjusts alternatively to fit the pseudo-ramp operation. The odd ramp slopes are decreased whereas the even ramp slopes are increased, in order to reduce $d_1(t)$ and to enlarge $d_2(t)$ when $I_{L1}$ is larger than $I_{L2}$. A similar operation is achieved when $I_{L1}$ is smaller than $I_{L2}$ in Mode II. Therefore, current balance mechanism can be realized by adjusting the ramp signals in both Mode I and Mode II.

## III. System Stability and Offset Analysis

The pseudo ramp control as well as the TM current balance must be accurately modeled to ensure dual-phase converter's stability.

### A. Model of the Pseudo-Ramp Technique

The equivalent model of the dual-phase converter with pseudo ramp technique is shown in Fig. 6 [14]. In the frequency domain, the duty cycle can be expressed as

$$d_i(s) = D_i + \hat{d}_i(s) \text{ where } i = 1 \text{ or } 2 \tag{1}$$

where $\hat{d}_i(s)$ is the duty cycle variation caused by the TM current balance, and $D_i$ is the duty cycle without the current

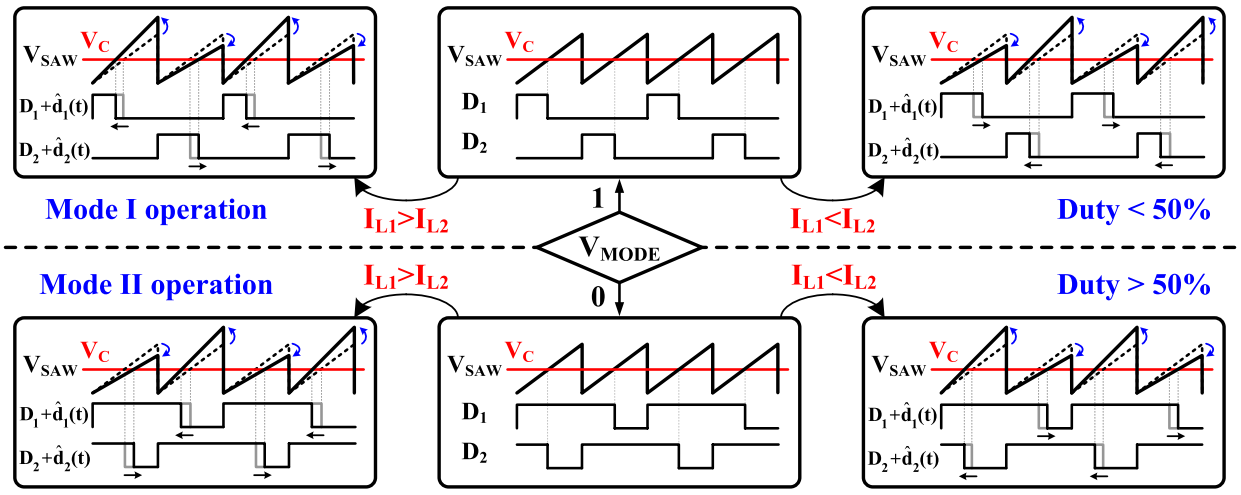



Fig. 5. Time-multiplexing current balance mechanism implemented with pseudo-ramp operation in the proposed dual-phase DC–DC buck converter.

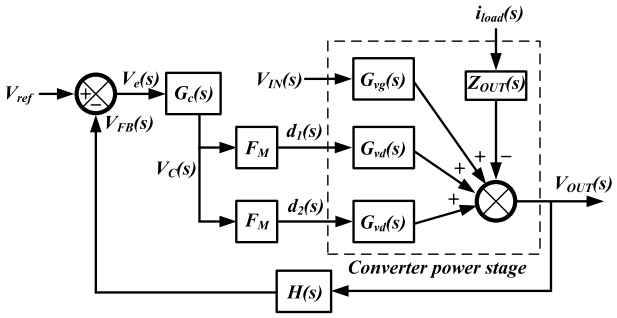



Fig. 6. Equivalent model of the dual-phase converter with the pseudo ramp technique.

balance function. Theoretically, $D_1$ and $D_2$ are equal to the average duty cycle as

$$D = \frac{d_1(s) + d_2(s)}{2}. \tag{2}$$

The feedback voltage $V_{\rm FB}$(s) is acquired by the voltage divider with a gain of $H$(s). The difference between $V_{\rm ref}$ and $V_{\rm FB}$(s) is amplified by the error amplifier to produce the error signal $V_C$(s). The modulator compares $V_C$(s) with the ramp signal to generate duty cycles, $d_1(s)$ and $d_2(s)$, for Phase 1 and Phase 2, respectively.

The open-loop output impedance $Z_{\rm OUT}$(s), line-to-output transfer function $G_{\rm vg}$(s), and duty-to-output transfer function $G_{\rm vd}$(s) are expressed in the following:

$$Z_{\rm OUT}(s) = \frac{sL}{1 + s\frac{L}{R_L} + s^2LC} \tag{3}$$

$$G_{\rm vg}(s) = D \cdot \frac{1}{1 + s\frac{L}{R_L} + s^2LC} \tag{4}$$

$$G_{\rm vd}(s) = \frac{V_{\rm OUT}}{D} \cdot \frac{1}{1 + s\frac{L}{R_L} + s^2LC}. \tag{5}$$

$L$, $C$, and $R_L$ are the filter inductor, capacitor, and equivalent load resistance, respectively.

To compensate the complex poles contributed by $L$ and $C$ as shown in (3)–(5), Type III compensation, which contains three poles and two zeros, is adopted and expressed in (6). The advantage of the PRCB is that only one Type III compensator is required because the PRCB technique has only a single controller. The PCB area can be effectively reduced. Besides, Type III compensation in this paper is similar to that in single-phase operation

$$G_c(s) = \frac{A_{\rm EA}(1 + sC_2R_3)(1 + sC_1R_1)}{s(1 + sC_3R_3)(1 + sC_1R_2)}. \tag{6}$$

Similar to conventional architecture of multiple controllers, separately modeling the modulator of each phase is convenient. In the pseudo ramp control, all phases share the same ramp. The effective magnitude of the pseudo-ramp is twice that of the physical ramp amplitude $V_M$. Thus, the modulator gain, $F_M$, can be written as

$$F_M = \frac{1}{2V_M}. \tag{7}$$

### *B. TM Current Balance Model*

TM current balance can be achieved by comparing the adjusted ramp with the error signal $V_C(s)$. To fit the characteristic of the adjusted ramp, the PWM model needs to be modified, as shown in Fig. 7(a). The difference between the current sensing signals $V_{S1}$ and $V_{S2}$ in Fig. 2, derived from the current sensing circuit, is amplified to generate the current-balance control current signals $\hat{I}_{C1}(s)$ and $\hat{I}_{C2}(s)$. $\hat{I}_{C1}(s)$ and $\hat{I}_{C2}(s)$ are injected to the ramp signal capacitor $C_{\rm ramp}$ to adjust the amplitude by $\Delta V_{\rm Mi}(i = 1$ or 2), as shown in Fig. 7(b). The equivalent variation in the duty cycle is equal to $\hat{d}_1(s)$ (or $\hat{d}_2(s)$), which causes the duty varies from $D_1$ (or $D_2$) to $D_1 + \hat{d}_1(s)$ (or $D_2 + \hat{d}_2(s)$). Thus, the modified duty cycles $d_1(s)$ and $d_2(s)$ can achieve good current balance.

In the absence of the current balance, the duty cycle is obtained by comparing the error signal $V_c(s)$ with the original ramp. In dual-phase control, the original duty cycles are $D_1$ and $D_2$ as

$$D_i(s) = \frac{V_C(s)}{m_o} = \frac{V_C(s)}{2V_M}(i = 1 \text{ or } 2) \tag{8}$$

where $m_o$ is the slope of the original ramp.

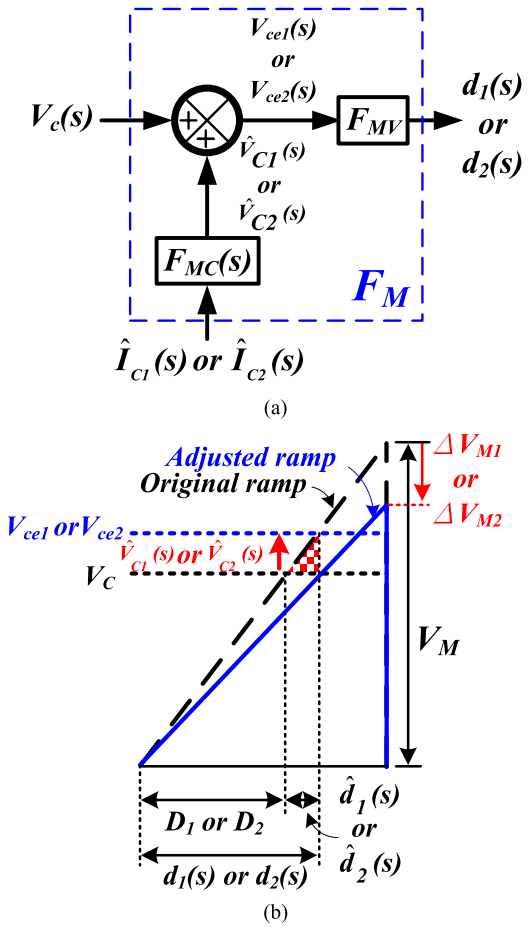



Fig. 7. (a) Equivalent model of the PWM with the current balance. (b) Relationship between the duty cycle and the adjusted ramp.

Here, $\Delta V_{\mathrm{Mi}}$, either a positive or a negative value, is contributed by the current balance circuit, and compensates the current unbalance situation to adjust the ramp amplitude as $V_M + \Delta V_{\mathrm{Mi}}$ ($i$ =1 or 2). Comparing the adjusted ramp with $V_c$(s), the duty cycle $d_i$(s) ($i$ =1 or 2) with the current balance can be expressed as

$$d_i(s) = \frac{V_C(s)}{m_{\mathrm{cbi}}} = \frac{V_C(s)}{2(V_M - \Delta V_{\mathrm{Mi}})} (i = 1 \text{ or } 2) \tag{9}$$

where $m_{\mathrm{cbi}}$ is the slope of the adjusted ramp $i$.

$\Delta V_{\mathrm{Mi}}$ can be derived as (10) because $\Delta V_{\mathrm{Mi}}$ is produced by injecting the current balance control current signal $\hat{I}_{C1}(s)$ (or $\hat{I}_{C2}(s)$) into the ramp signal capacitor $C_{\mathrm{ramp}}$ within $T_s/2$ for each phase

$$\Delta V_{\mathrm{Mi}} = -\hat{I}_{\mathrm{Ci}}(s) \cdot \frac{T_s}{2} \cdot \frac{1}{C_{\mathrm{ramp}}} \text{ (where } i = 1 \text{ or } 2). \tag{10}$$

Based on (8), (9), and (10), the duty cycle variation is given by

$$\hat{d}_i(s) = d_i(s) - D_i = \frac{V_C(s)}{2} \cdot \frac{\Delta V_{\mathrm{Mi}}}{V_M(V_M - \Delta V_{\mathrm{Mi}})}$$
$$\approx D\frac{\Delta V_{\mathrm{Mi}}}{V_M} = -\frac{D\hat{I}_{\mathrm{Ci}}(s)T_s}{2V_M C_{\mathrm{ramp}}} (i = 1 \text{ or } 2). \tag{11}$$

As a result, the adjusted current-to-duty transfer function can be derived as

$$\frac{\hat{d}_i(s)}{\hat{I}_{\mathrm{Ci}}(s)} \approx -\frac{DT_s}{2V_M C_{\mathrm{ramp}}}. \tag{12}$$

The PRCB modeling with current balance is complicated since the duty cycle is determined by many factors. To simplify the model, the duty cycle variation $\hat{d}_1(s)$ (or $\hat{d}_2(s)$) is transferred to the error signal variation $\hat{V}_{C1}(s)$ (or $\hat{V}_{C2}(s)$). Thus, the pseudo ramp modulator can be divided in to two blocks, the voltage modulator $F_{\mathrm{MV}}$ and the current modulator $F_{\mathrm{MC}}(s)$. Using the TM current balance technique, the error signal variation $\hat{V}_{C1}(s)$ (or $\hat{V}_{C2}(s)$) is added to the original error signal $V_C(s)$ to generate the effective error signal $V_{\mathrm{ce1}}(s)$ (or $V_{\mathrm{ce2}}(s)$). Comparing $V_{\mathrm{ce1}}(s)$ (or $V_{\mathrm{ce2}}(s)$) with the original ramp signal is able to obtain the duty cycle $d_1(s)$ (or $d_2(s)$), which is equal to the comparison of the error signal $V_C(s)$ and the adjusted ramp signal. Here, the voltage modulator $F_{\mathrm{MV}}$ in (13) remains the same as in (7)

$$F_{\mathrm{MV}} = F_M = \frac{1}{2V_M}. \tag{13}$$

The current modulator $F_{\mathrm{MC}}(s)$ is derived as

$$F_{\mathrm{MC}}(s) = \frac{\hat{V}_{\mathrm{Ci}}(s)}{I_{\mathrm{Ci}}(s)}$$
$$= \frac{\hat{V}_{\mathrm{Ci}}(s)}{\hat{d}_i(s)} \cdot \frac{\hat{d}_i(s)}{\hat{I}_{\mathrm{Ci}}(s)}$$
$$= -m_o \cdot \frac{DT_s}{2V_M C_{\mathrm{ramp}}}$$
$$= -\frac{DT_s}{C_{\mathrm{ramp}}} (i = 1 \text{ or } 2). \tag{14}$$

### C. System Stability Analysis

Eventually, in spite of the disturbance of input voltage and load current, the equivalent PRCB modeling with the TM current balance is shown in Fig. 8. Here, $V_{\mathrm{OS,eq}}$ is set to zero to neglect the effect of offset, which will be discussed later. In addition to the voltage loop, the TM current balance loop and the cross coupling loop are also included. The voltage loop is defined as

$$T_v(s) = G_c(s)F_{\mathrm{MV}}G_{\mathrm{vd}}(s)H(s). \tag{15}$$

In the current balance loop, the two-phase inductor currents are sensed and held by the $R_i$ and the sample-and-hold circuit, respectively, to generate the signals, $V_{\mathrm{SH1}}$(s) and $V_{\mathrm{SH2}}$(s). The sensing and sampling effect with a transfer function in (16) introduces a pair of complex right-half-plane (RHP) zeros at half the switching frequency [15]

$$H_e(s) \approx \frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q_n} + 1 \tag{16}$$

where $Q_n = -\frac{2}{\pi}$ and $\omega_n = \frac{\pi}{T_s}$.

The difference between $V_{\mathrm{SH1}}$(s) and $V_{\mathrm{SH2}}$(s) is amplified by operational transconductance amplifier (OTA), $A_{\mathrm{OTA}}$(s), to obtain the current balance control voltages, $V_{\mathrm{IC1}}$(s) and $V_{\mathrm{IC2}}$(s). The V-to-I converter, $G_{V-I}$(s), converts $V_{\mathrm{IC1}}$(s) and $V_{\mathrm{IC2}}$(s) to the current balance control currents, $I_{C1}$(s) and

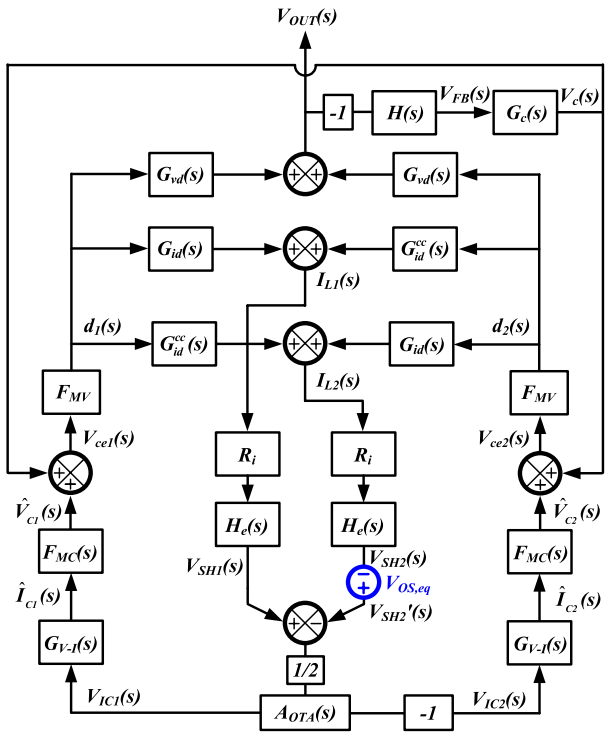



Fig. 8. Equivalent model of dual-phase buck converter with the pseudo ramp control and the TM current balance.

$I_{C2}(s)$, respectively, which can individually adjust $d_1(s)$ and $d_2(s)$. The duty-to-current transfer function for each phase is derived in

$$G_{id}(s) = \frac{V_{OUT}}{D} \frac{1 + sC(R_L + R_{esr})}{s^2 LCR_1 + s\omega_0 Q_0 + R_{DCR} + R_L} \quad (17)$$

where $\omega_0 Q_0 = L + C[R_L(R_{DCR} + R_{esr})] + R_{DCR}R_{esr}$ and $R_1 = R_L + R_{esr}$.

Ideally, a stable current balance loop will not influence the output voltage. The operation of current balance loop is independent of load current. However, current balance loop relies on the difference of the dual-phase inductor currents. Therefore, the output can be regarded as shorted to ground. The duty-to-current transfer function is modified as

$$G_{id}(s)\Big|_{\hat{V}_{OUT}=0} = \frac{V_{OUT}}{D} \cdot \frac{1}{sL + R_{DCR}}. \quad (18)$$

The small signals in the two phases are the same in magnitude and opposite in phase because the TM current balance scheme is based on the average current balance control [6]. That is, $\hat{V}_{SH1} = -\hat{V}_{SH2}$, $\hat{V}_{IC1} = -\hat{V}_{IC2}$, $\hat{I}_{C1} = -\hat{I}_{C2}$, $\hat{d}_1 = -\hat{d}_2$, and $\hat{I}_{L1} = -\hat{I}_{L2}$. Consequently, the two loops in the dual-phase operation become symmetric and are added as shown in Fig. 9. Thus, the TM current balance loop gain is derived as

$$T_{cb}(s) = A_{OTA}(s)G_{V-I}(s)F_{MC}(s)F_{MV}G_{id}(s)\Big|_{\hat{V}_{OUT}=0} R_i H_e(s). \quad (19)$$

The inductor current of each phase is controlled by its own current balance control signal. However, the inductor current in one phase is inevitably affected by the change in duty cycle of the other phase [16]. Therefore, the cross coupling effect,

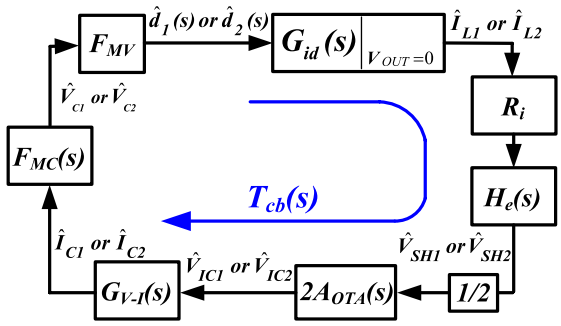



Fig. 9. Small signal model of the TM current balance loop.

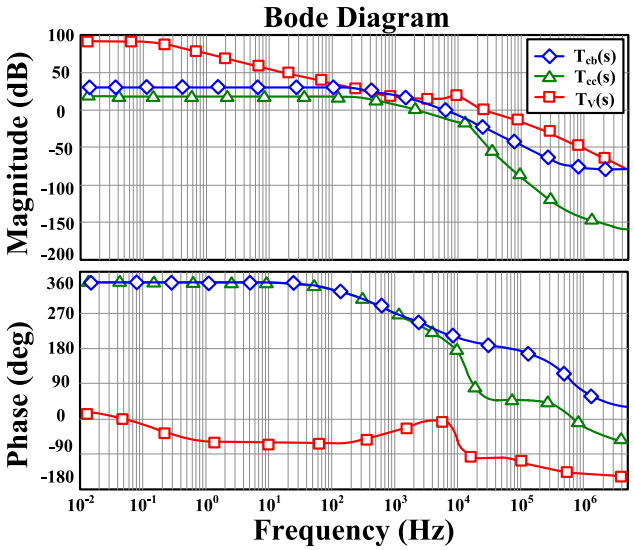



Fig. 10. Frequency response of the $T_v(s)$, $T_{cb}(s)$, and $T_{cc}(s)$ with $V_{IN}$ of 3.3 V and $V_{OUT}$ of 2 V.

the duty-to-current transfer function $G_{id}^{cc}(s)$ in (20), has to be considered in the system stability analysis

$$G_{id}^{cc}(s) = -\frac{V_{OUT}}{D} \frac{R_L(1 + sCR_{esr})}{(sL + R_{DCR})} \times \frac{1}{s^2 LCR_1 + s\omega_{cc}Q_{cc} + R_{DCR} + 2R_L} \quad (20)$$

where $\omega_{cc}Q_{cc} = L + C[R_L(R_{DCR} + 2R_{esr})] + R_{DCR}R_{esr}$ and $R_1 = R_L + R_{esr}$.

The cross coupling duty-to-current transform must be zero if $\hat{V}_{OUT} = 0$ to obtain further observation. As a result, 1/sC = 0, $R_{esr} = 0$, and $R_L = 0$ are substituted into (20). The shorted cross coupling duty-to-current transfer function can be derived as

$$G_{id}^{cc}(s)\Big|_{\hat{V}_{OUT}=0} = 0. \quad (21)$$

The result is consistent with the derivation of the TM current balance loop gain since the cross coupling term is not considered. Therefore, the cross coupling duty-to-current transfer function is correctly proved. The cross coupling loop can be defined as

$$T_{cc}(s) = -\frac{1}{2} A_{OTA}(s)G_{V-I}(s)F_{MC}(s)F_{MV}G_{id}^{cc}(s)R_i H_e(s). \quad (22)$$

The stability of the cross coupling loop needs to be guaranteed under stable voltage and the current balance loops.

In the proposed structure, a compensation capacitor is located at the output of the OTA. The added compensation pole ensures stability of the current balance loop $T_{\rm cb}(s)$ and compensates for the cross coupling loop $T_{\rm cc}(s)$. The Bode plot of voltage loop $T_v(s)$, current balance loop $T_{\rm cb}(s)$, and cross coupling loop $T_{\rm cc}(s)$ is shown in Fig. 10. The DC gain and the phase margin of the $T_v(s)$ are 91.9 dB and 51°, respectively. On the other hand, the DC gains and the phase margins of the $T_{\rm cb}(s)$ and the $T_{\rm cc}(s)$ are (30.1 dB, 44°) and (17.6 dB, 67°), respectively. With the stabilized loops, system stability is assured.

Moreover, the voltage loop dominates the operation of the whole multiphase system. In other words, the voltage loop gain is designed to be higher than the current balance loop gain. The bandwidths of both loops are desired to be as large as possible to accelerate the transient response. However, the enlarged bandwidth of the current balance loop slows down the load transient response because of the lack of rapidly increasing inductor current. For instance, in the case of light-to-heavy load variation, one of the phases must quickly prolong the on-time to cope with the lack of energy, inevitably causing current unbalance as a consequence. Simultaneously, the current balance loop will start to pull down the unbalance inductor current. Owing to the enlarged bandwidth, suppression of the energy provided to the output will be reduced by the fast current balance loop. More switching cycles are needed to regulate the output voltage. Therefore, the loop gain and the bandwidth of the two loops have to be carefully designed to meet the specification.

### D. Offset Analysis

Theoretically, the current balance performance depends on the current balance loop gain and mismatches between the two phases. Basically, current difference caused by the mismatches existing intrinsically among power MOSFETs, inductance, DC resistance of the inductors and PCB boards can be defined as

$$\Delta I_{L,O}(s) = I_{L1,O}(s) - I_{L2,O}(s). \tag{23}$$

The $I_{L1,O}(s)$ and the $I_{L2,O}(s)$ are the channel currents in Phase 1 and Phase 2, respectively, without implementing any current balance function. With the current balance function, the current difference is suppressed and can be written as

$$\Delta I_{L,\rm cb}(s) = \frac{\Delta I_{L,O}(s)}{T_{\rm cb}(s)}. \tag{24}$$

The larger the current balance loop gain is designed, the smaller current difference will be obtained. However, performance of current balance is influenced by the offset in the operational transconductance amplifier (OTA). The effect of device mismatches, threshold voltage mismatches and difference bias conditions can be equalized to the input-referred offset voltage, $V_{\rm OS,eq}$, between the two inputs of the differential pair. Equivalent model of dual-phase buck converter using the pseudo ramp control and the TM current balance with the offset voltage in the OTA is shown in Fig. 8. Through the current balance loop, the offset current difference of the two channels, $\Delta I_{L,\rm OS}$, can be derived as

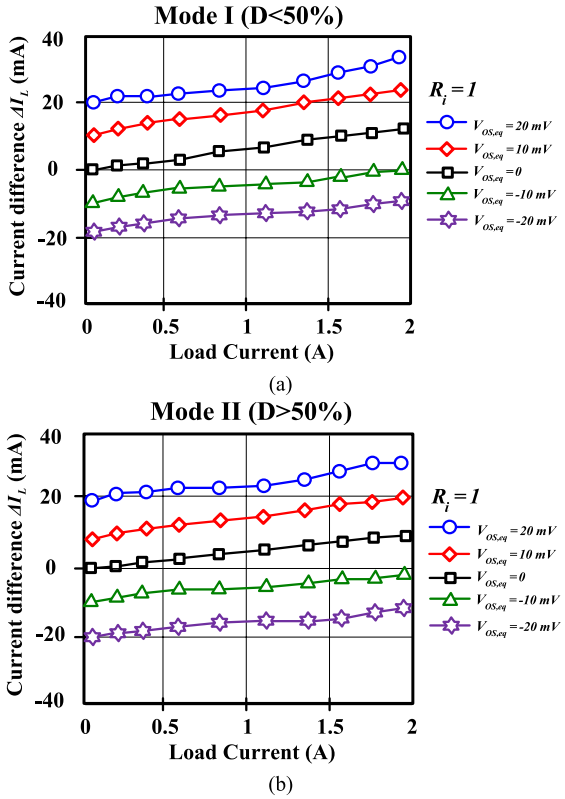



Fig. 11. Current balance performance with the proposed PRCB technique considering different input-referred offset voltage values of the OTA. (a) Operating in the Mode I. (b) Operating in the Mode II.

$$\begin{aligned}\Delta I_{L,\rm OS}(s) &= V_{\rm OS,eq} \\ &\quad \times \frac{A_{\rm OTA}(s)G_{V-I}(s)F_{\rm MC}(s)F_{\rm MV}G_{\rm id}(s)\Big|_{\hat{V}_{\rm OUT}=0}}{1+T_{\rm cb}(s)} \\ &\approx \frac{V_{\rm OS,eq}}{R_i H_e(s)}.\end{aligned} \tag{25}$$

Consequently, the overall current difference, $\Delta I_L$, is composed of current gain error term, $\Delta I_{L,\rm cb}$, and offset term, $\Delta I_{L,\rm OS}$, and can be written as

$$\begin{aligned}\Delta I_L(s) &= \Delta I_{L,\rm cb}(s) + \Delta I_{L,\rm OS}(s) \\ &= \frac{\Delta I_{L,O}(s)}{T_{\rm cb}(s)} + \frac{V_{\rm OS,eq}}{R_i H_e(s)}.\end{aligned} \tag{26}$$

Fig. 11 demonstrates current balance performance with the proposed PRCB technique considering different input-referred offset voltage values of the OTA. When the offset voltage, $V_{\rm OS,eq}$, is equal to zero, the offset term disappears. Current balance performance is consistent with the designed value. Since the offset voltage is not zero in most of the cases, the curve of current balance is shifted with a DC level which can be calculated according to the offset term. Therefore, current balance performance is not in expectation with a large offset voltage.

To decrease the current difference, increasing current balance loop gain without limitation only diminishes the current gain error term. The offset term dominates the performance of current balance and cannot be eliminated. Even though increasing current sense gain, $R_i$, is able to suppress the offset current difference, the performance of current balance is still

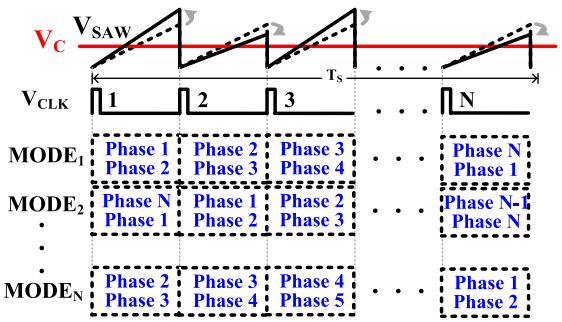



Fig. 12. Timing flow chart of N-phase converter with the time-multiplexing current balance.

confined. Therefore, the offset cancellation mechanism must be adopted to solve the problem.

To alleviate massive area and cost by extending the converter to N-phase in large power applications, current balance of N-phase is achieved by multiplexing two-phase current balance circuit. Timing flow chart is shown in Fig. 12. The operation is divided in to N modes, $\text{MODE}_1$-$\text{MODE}_N$ to cope with the wide output voltage range. The $N$ clock periods, $N*V_{\text{clk}}$, constitute one complete switching cycle, $T_s$, for the N-phase operation, i.e., one pseudo-ramp is composed of $N$ physical ramps in one switching period. If the output voltage ranges from 0 to $V_{\text{IN}}/N$, the system operates in $\text{MODE}_1$. During the first ramp, currents of phase 1 and 2 are selected and sent into the two-phase current balance circuit for minimizing current difference. During the second ramp, currents of phases 2 and 3 are selected and sent into the two-phase current balance circuit for minimizing current difference. Finally, current balance of N-phase can be achieved after several switching cycles. Thus, the proposed method not only removes N-1 replicas of the modulator, but also minimizes current balance circuit. Additionally, mismatches between N-current balance circuits are eliminated since only current balance of two-phase and multiplexers are required. Moreover, the model of PRCB remains the same in N-phase operation. Here, the model analysis and transfer functions derived in Section III are summarized in Table I.

TABLE I
SMALL SIGNAL TRANSFORM FUNCTIONS

| TRANSFER FUNCTIONS |
|---|
| Duty cycle to output voltage<br>$G_{vd}(s)=\frac{V_{OUT}}{D}\cdot\frac{1}{1+s\frac{L}{R_L}+s^2LC}$ |
| Duty cycle to output current:<br>$G_{id}(s)=\frac{V_{OUT}}{D}\frac{1+sC\left(R_L+R_{esr}\right)}{s^2LCR_1+s\omega_0Q_0+R_{DCR}+R_L}$ |
| Cross-coupling duty cycle to output current:<br>$G_{id}^{cc}(s)=-\frac{V_{OUT}}{D}\frac{R_L(1+sCR_{esr})}{(sL+R_{DCR})}\cdot\frac{1}{s^2LCR_1+s\omega_{cc}Q_{cc}+R_{DCR}+2R_L}$ |
| Compensator:<br>$G_c(s)=\frac{A_{EA}(1+sC_2R_3)(1+sC_1R_1)}{s(1+sC_3R_3)(1+sC_1R_2)}$ |
| Voltage modulator:<br>$F_{MV}=\frac{1}{2V_M}$ |
| Current modulator:<br>$F_{MC}(s)=-\frac{DT_s}{C_{ramp}}(i=1 \text{ or } 2)$ |
| Sampling effect:<br>$H_e(s)\approx\frac{s^2}{\omega_n^2}+\frac{s}{\omega_nQ_n}+1$ |
| Voltage loop gain:<br>$T_v(s)=G_c(s)F_{MV}G_{vd}(s)H(s)$ |
| Current-balance loop gain:<br>$T_{cb}(s)=A_{OTA}(s)G_{V-I}(s)F_{MC}(s)F_{MV}G_{id}(s)\big\vert_{\hat{v}_{OUT}=0}R_iH_e(s)$ |
| Cross-coupling loop gain:<br>$T_{cc}(s)=-\frac{1}{2}A_{OTA}(s)G_{V-I}(s)F_{MC}(s)F_{MV}G_{id}^{cc}(s)R_iH_e(s)$ |
| PARAMETERS |
| $R_1=R_L+R_{esr}\quad Q_n=-\frac{2}{\pi}$ and $\omega_n=\frac{\pi}{T_s}$<br>$\omega_0Q_0=L+C\left[R_L(R_{DCR}+R_{esr})\right]+R_{DCR}R_{esr}$<br>$\omega_{cc}Q_{cc}=L+C\left[R_L(R_{DCR}+2R_{esr})\right]+R_{DCR}R_{esr}$ |

## IV. CIRCUIT IMPLEMENTATION

### A. Current Sensing Circuit

For current balance, the inductor current information must be detected to modulate the individual duty cycle. The simplest way to achieve current sensing is to implement an auxiliary resistor in series with the power switch; however, this induces large power dissipation, thereby deteriorate the power conversion efficiency [17]–[18]. Fig. 13 shows the utilized current sensing circuit with the replica current flowing through the sensing switch [19]. The power transistor $M_P$ conducts the inductor current during its turn-on period. The common-gate amplifier, which is composed of $M_2$–$M_5$, can ensure near source-to-drain voltages between the $M_P$ and the sensing MOSFET $M_{S1}$. Thus, the sensing current $I_{\text{sen}}$ as a replica of the inductor current depends on the aspect ratio between $M_P$ and $M_{S1}$.

$I_{\text{sen}}$ flows through $M_6$ and the sensing resistor $R_S$ to carry out the current sensing signal $V_S$. Additionally, to enhance the current sensing accuracy, $M_7$, which has the same aspect ratio as the current mirror structure, $M_2$ and $M_3$, are added to provide a compensation current, $I_B$. Moreover, the sensing speed of the proposed current sensing circuit can be improved as the common-gate gain stage derives large operating bandwidth because no compensation component is demanded in this structure [20].

### B. Current Balance Circuit With Offset Cancellation Control

The current balance mechanism in the multiphase structure can ensure equivalent current driven capability of each phase. As shown in Fig. 14, the proposed current balance circuit, which contains the current matching unit and the voltage averaging element, is used to adjust the saw-tooth signal generated by the pseudo-ramp generator circuit, as well as the duty cycles for matched inductor current levels. The sensing signals, $V_{S1}$ and $V_{S2}$, derived from the current sensing circuits, are sent into the current matching unit. The sample-and-hold

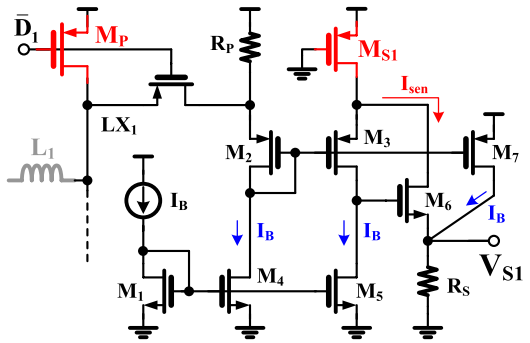



Fig. 13. Current sensing circuit.

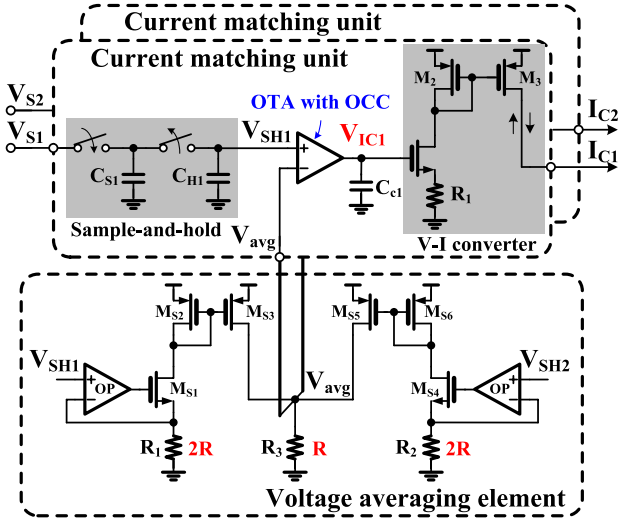



Fig. 14. Current balance circuit.

(SH) circuit is activated to obtain the voltages, $V_{SH1}$ and $V_{SH2}$, which represent the average inductor current level of each phase.

The voltage average element can derive the average value $V_{avg}$ for the phase current distribution to obtain an accurate current balance. Briefly, an OTA is realized to reflect the current difference between the average value and each of the phases. The voltage difference is amplified to generate the current balance control signals, $V_{IC1}$ and $V_{IC2}$. Then, $V_{IC1}$ and $V_{IC2}$ are converted to the different injection currents $I_{C1}$ and $I_{C2}$, respectively, and injected into the pseudo-ramp generator for current balance. As the OTA is chosen to enhance the current balance accuracy, the capacitor $C_{c1}$ and $C_{c2}$ is used to stabilize the current-loop operation.

Besides, the offset cancellation control (OCC) is embedded in the OTA to avoid inaccuracy occurring in the current balance control signals, $V_{IC1}$ and $V_{IC2}$ [21]–[22]. As a result, the on/off-chip mismatch issues will be well compensated through the current balance control scheme. Here, only one controller is utilized to achieve high accuracy and area and conversion efficiency in the proposed PRCB technique.

Assuming that an offset voltage exists at the positive input node of the OTA, one offset term is brought into the current balance control signal, $V_{IC1}$ or $V_{IC2}$, as expressed in

$$V_{ICi} = (V_{SHi} - V_{avg})A_{OTA} + V_{OS} \cdot A_{OTA} \text{ where } i = 1 \text{ or } 2. \quad (27)$$

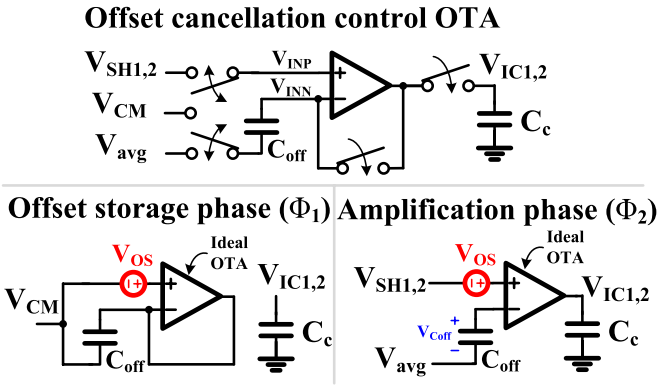



Fig. 15. Operation of the OTA with the OCC circuit.

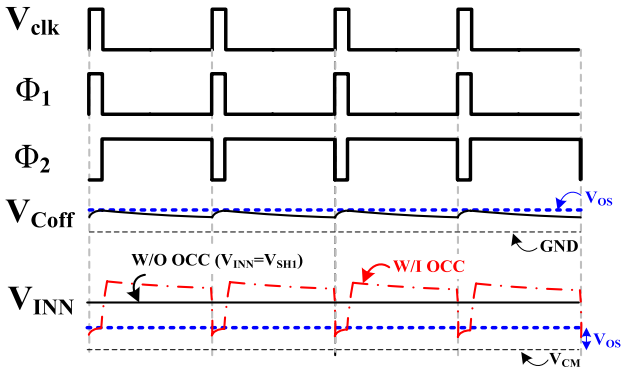



Fig. 16. Timing diagram of the OCC circuit.

The undesirable offset term is caused by the amplification of input-referred offset voltage and deteriorates the current balance performance. As a result, the offset cancellation control, which introduces a capacitor, $C_{off}$, for offset voltage storage, is embedded in the OTA as illustrated in Fig. 15. The operation is divided into the offset storage phase ($\Phi_1$) and the amplification phase ($\Phi_2$). In offset storage phase, the common mode reference voltage, $V_{CM}$, is sent into the offset cancelation OTA instead of $V_{SH1}$ or $V_{SH2}$ and $V_{avg}$. Owing to the negative feedback topology, the offset voltage is stored on the $C_{off}$. The voltage of the negative-input node is written as

$$V_{INN} = V_{CM} + V_{OS}\frac{A_{OTA}}{A_{OTA}+1} \approx V_{CM} + V_{OS}. \quad (28)$$

At the same time, the value of current balance control signal, $V_{IC1}$ or $V_{IC2}$, is kept by the compensation capacitor, $C_c$, to maintain the balance of the two channels. Once the OTA switches to the amplification phase, the offset voltage is able to be removed because the prestored offset voltage is added to the $V_{avg}$ before amplification. The successful cancellation can be proved in

$$\begin{aligned} V_{ICi} &= \left[V_{SHi} - (V_{avg} + V_{OS})\right] A_{OTA} + V_{OS} \cdot A_{OTA} \\ &= (V_{SHi} - V_{avg})A_{OTA} \text{ where } i = 1 \text{ or } 2. \end{aligned} \quad (29)$$

Considering the offset voltages, $V_{os1}$ of Phase 1 and $V_{os2}$ of Phase 2, the equivalent offset voltage, $V_{OS,eq}$, in Fig. 11 can be described as

$$V_{OS,eq} = V_{OS2} - V_{OS1}. \quad (30)$$

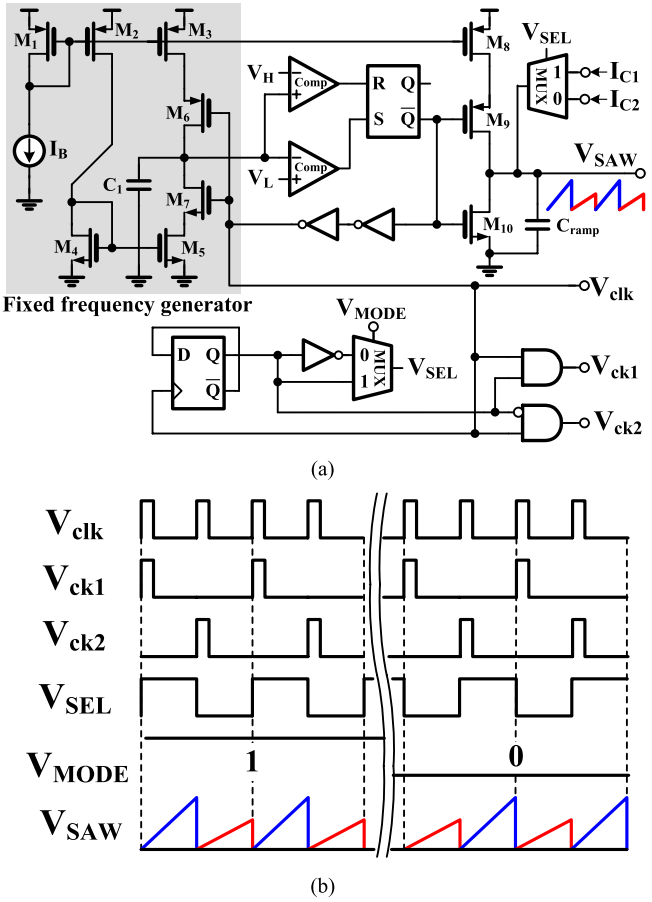



Fig. 17. (a) Schematic of the pseudo-ramp generator. (b) Timing diagrams of the pseudo-ramp generator.

The timing diagram of the OCC, which is synchronous with the clock signal, $V_{\rm clk}$, is illustrated in Fig. 16. When the $V_{\rm clk}$ is logic high, the OTA with the OCC circuit operates in the offset storage phase ($\Phi_1$) and the voltage ($V_{\rm Coff}$) across the $C_{\rm off}$ is charged to the $V_{\rm OS}$. When the $V_{\rm clk}$ is logic low, the OTA with the OCC circuit operates in the amplification phase ($\Phi_2$). Comparing with the OTA without the OCC, the modified $V_{\rm INN}$ is shifted by the $V_{\rm OS}$ to cancel the offset of $V_{\rm IC1}$ or $V_{\rm IC2}$.

### C. Pseudo-Ramp Generator

Fig. 17(a) shows the schematic of the pseudo-ramp generator. A fixed frequency signal $V_{\rm clk}$ is derived through the fixed frequency generator composed of $M_1$-$M_7$ and the capacitor $C_1$. The reference voltages $V_H$ and $V_L$ are derived from the bandgap circuit to determine the frequency of $V_{\rm clk}$ with the bias current $I_B$. Thus, $V_{\rm clk}$ can be used to control the switches, $M_9$ and $M_{10}$, to generate the saw-tooth signal $V_{\rm SAW}$ by the charging and discharging of $C_{\rm ramp}$.

If the dual-phase inductor currents are well balanced, $I_{C1}$ and $I_{C2}$ must be equal. In other words, each of the ramps of $V_{\rm SAW}$ must be identical to realize the same duty cycle for the dual-phase operation. However, once current unbalance happens, the current balance circuit detects current difference between the two phases to modulate $I_{C1}$ and $I_{C2}$, thereby modifying the $V_{\rm SAW}$. By alternately injecting $I_{C1}$ and $I_{C2}$, the odd and even ramps in $V_{\rm SAW}$ change to adjust the duty cycles and the phase inductor currents adaptively. The compensated current injection is also controlled by the $V_{\rm MODE}$ to generate properly pseudo-ramp signal for different operation modes. The timing diagram of the pseudo-ramp generator circuit is depicted in Fig. 17(b). Moreover, a frequency divider is implemented to carry out the two phase clocks, $V_{\rm ck1}$ and $V_{\rm ck2}$, for the dual-phase operation. Here, $V_{\rm ck1}$ and $V_{\rm ck2}$, indicate the beginning of the switching cycle of Phase 1 and Phase 2, respectively. Consequently, the phase control logic can produce individual duty cycle for each power stage.

TABLE II
DESIGN SPECIFICATIONS OF THE PROPOSED PRCB TECHNIQUE CONVERTER

| | |
|---|---|
| Technology | 0.25m μm CMOS process |
| Inductor / DCR | 4.7 μH/ 100 mΩ (nominal) |
| Capacitor /ESR | 47 μF/ 50 mΩ (nominal) |
| Switching frequency | 600 kHz |
| Input voltage ($V_{IN}$) | 3.3 V – 5 V |
| Output voltage range ($V_{OUT}$) | 0.8 V – 3 V ($V_{\rm IN}$ = 3.3 V) |
| Load current range ($I_{Load}$) | 0 mA – 2000mA |
| Current balance improvement (%) | Min. 83% |
| Power conversion efficiency | Max. 88 % |
| Chip size | 2.779 mm$^2$ |

### D. Phase Control Logic

Fig. 18 shows the implementation and the operation of phase control logic. Fig. 18(a) shows the schematic of phase control logic, composed of the duty generator unit and the mode transition unit. The signals $V_{\rm clk}$, $V_{\rm ck1}$, and $V_{\rm ck2}$ are generated from the pseudo-ramp generator. $V_{\rm ck1}$ and $V_{\rm ck2}$ are used to indicate Phase 1 and Phase 2, respectively, because there is only one saw-tooth signal to determine the duty cycle. $V_{\rm PWM}$ is the resultant duty determination derived from the comparison of $V_{\rm SAW}$ and $V_C$ in the proposed pseudo-ramp operation. $V_{\rm ck1}$ and $V_{\rm ck2}$ activate $D_1$ and $D_2$, respectively. In the meanwhile, the rising edge of $V_{\rm PWM}$ is used to reset the duty cycles and thus wait for the next triggering. The timing diagrams are shown in Fig. 18(b).

The mode transition unit can decide the operating mode according to the duty cycle. With a continuously increasing duty cycle in Mode I, $D_1$ or $D_2$ would overlap with $V_{\rm ck2}$ or $V_{\rm ck1}$, respectively. Thus, $V_{M1}$ or $V_{M4}$ indicates the exceeding duty cycle over 50%. The overlapping of $D_1$ and $V_{\rm ck2}$ (or that of $D_2$ and $V_{\rm ck1}$) represents that the duty cycle in Mode I has taken a full period of one physical ramp in $V_{\rm SAW}$. The operation mode will transit from Mode I to Mode II to obtain sufficient duty cycles in the PRCB technique.

On the other hand, if the duty cycle continuously decreases in Mode II, mode determination would enter into the boundary region of Mode I Mode II. When both $D_1$ and $D_2$ do not cover the entire period of $V_{\rm ck2}$ and $V_{\rm ck1}$, respectively, the duty cycle is smaller than 50%. To ensure the proper pseudo-ramp operation, the operation mode will change from Mode II to Mode I. The detailed flow chart of the mode transition operation is shown in Fig. 18(c).

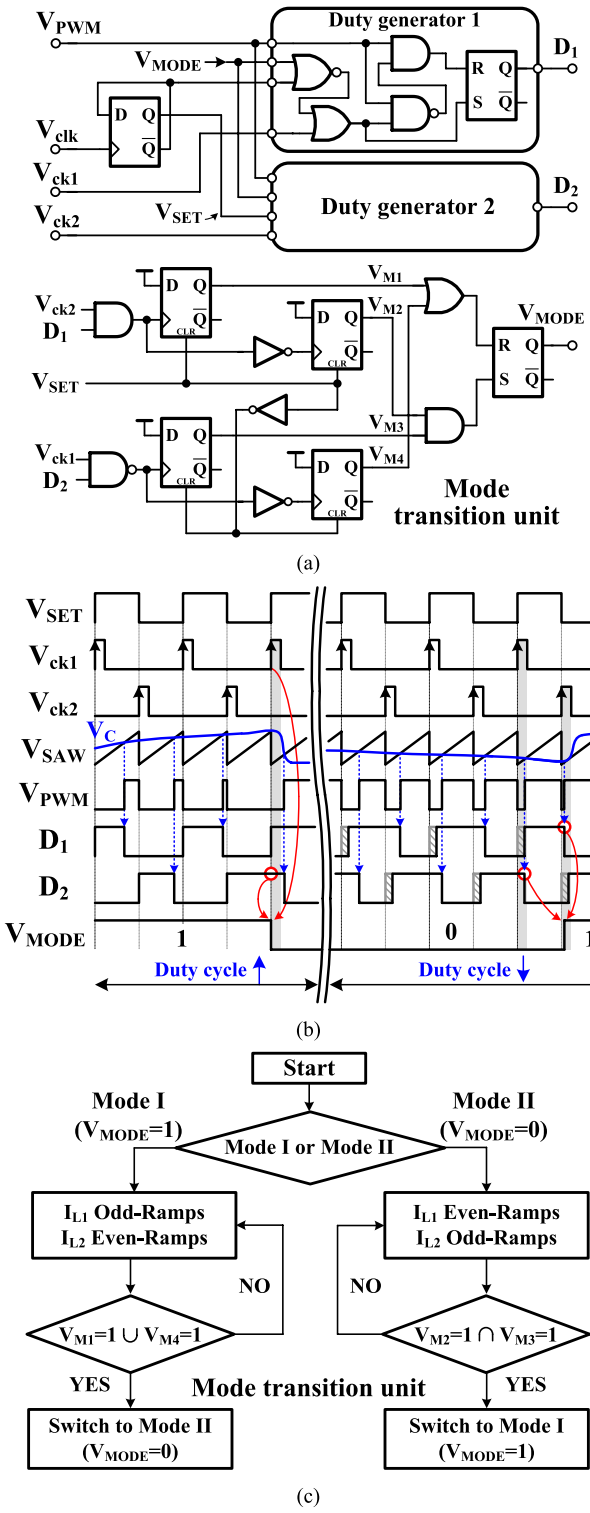



Fig. 18. (a) Implementation of the phase control logic. (b) Timing diagrams of the phase control logic. (c) Flow chart of the mode transient operation.

## V. Experimental Results

The proposed multiphase DC–DC buck converter with the PRCB technique was fabricated in 0.25 $\mu$m CMOS process. Dual power stages are embedded in the test chip for verification. The utilization values of the off-chip inductors and capacitors are 4.7 $\mu$H and 47 $\mu$F, respectively. The chip

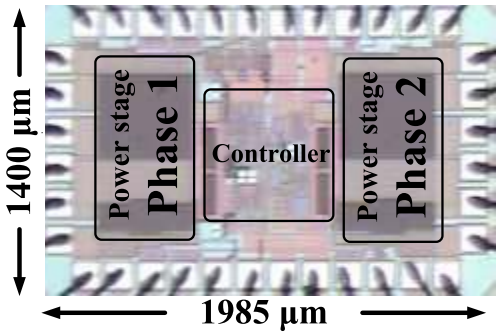



Fig. 19. Chip micrograph.

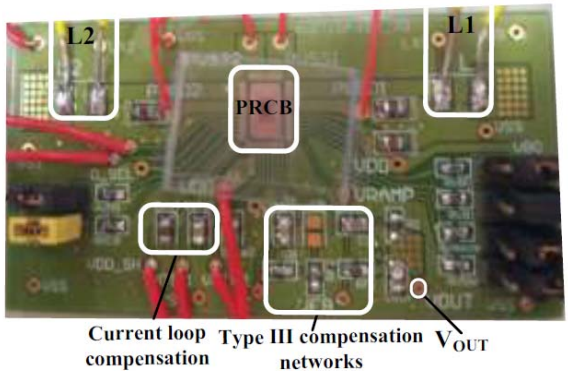



Fig. 20. System board of the PRCB dual-phase DC–DC converter.

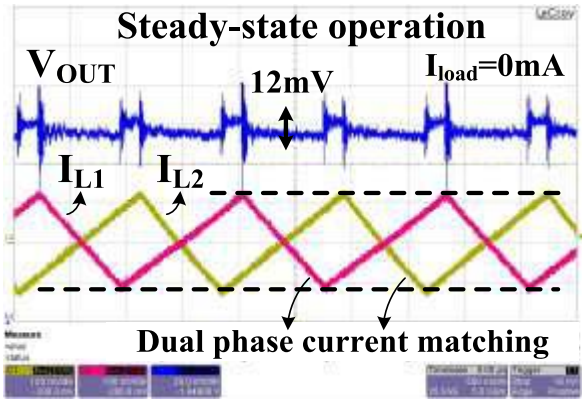



Fig. 21. Measured steady-state operation with the $V_{IN}$ of 3.3 V.

micrograph with an active silicon area of 2.779 mm$^2$ is shown in Fig. 19. The power stages of Phase 1 and Phase 2 are placed closed to bonding pads. Only one controller is implemented in the middle of the chip to minimize the mismatches issues for both power stages. Fig. 20 demonstrates the system PCB of the proposed PRCB dual-phase DC-DC converter. The key design specifications are listed in Table II.

Fig. 21 shows the measured steady-state operation. With an input voltage $V_{IN}$ of 3.3 V, the nominal output voltage $V_{OUT}$ is 2 V. The switching frequency is 600 kHz. The mismatch from the size of the power MOSFETs and the DCR of inductors between each phase results in current unbalance. The proposed pseudo-ramp operation can generate proper duty cycles for dual-phase operation with a 12 mV output

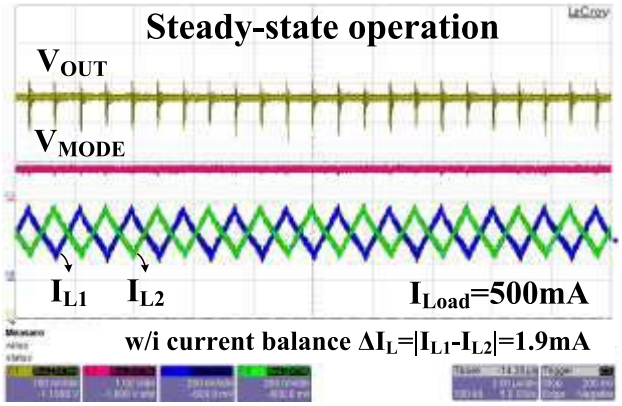
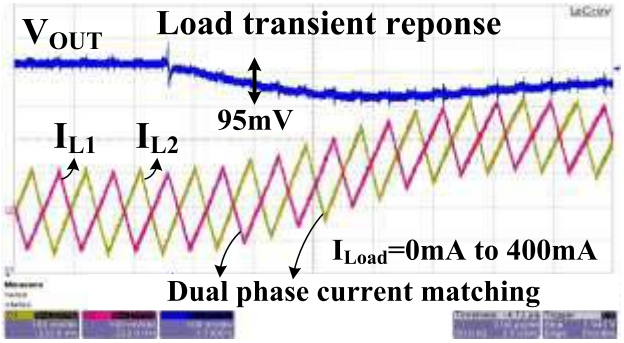
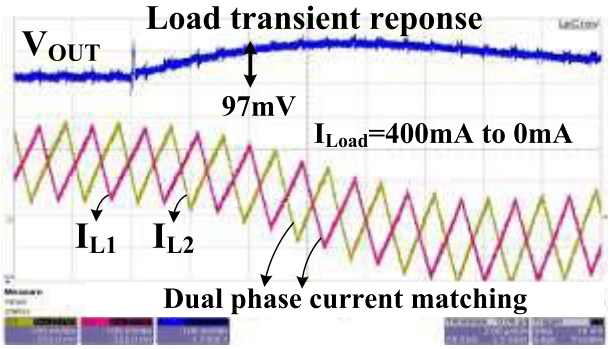



Fig. 22. Measured steady-state operation in the Mode I when the $V_{IN}$ is 3.3 V and load current is 500 mA.




(a)




(b)

Fig. 23. Measured load-transient response with the current balance mechanism when load current changes from 0 to 400 mA in (a) or vice versa in (b).

voltage ripple. Besides, the current balance mechanism achieves current matching. Fig. 22 shows the measured steady-state operation with a load current of 500 mA. The pseudo-ramp can decide correct duty cycles to guarantee output voltage regulation. The current difference between the two phases is reduced to 1.9 mA, thereby verifying the operation of the proposed current balance mechanism in the PRCB technique.

Fig. 23 shows the measured load transient response with the load changes from 0 to 400 mA and vice versa. The voltage drop and overshoot are 95 and 97 mV, respectively. The current balance mechanism is also achieved in the period of load transient response. The mode transition operation is shown in Fig. 24. The operating mode would be changed from Mode I

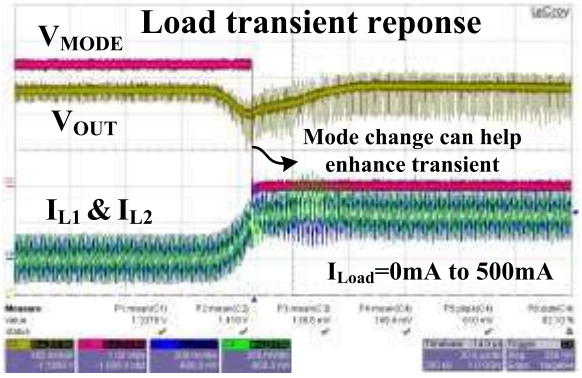
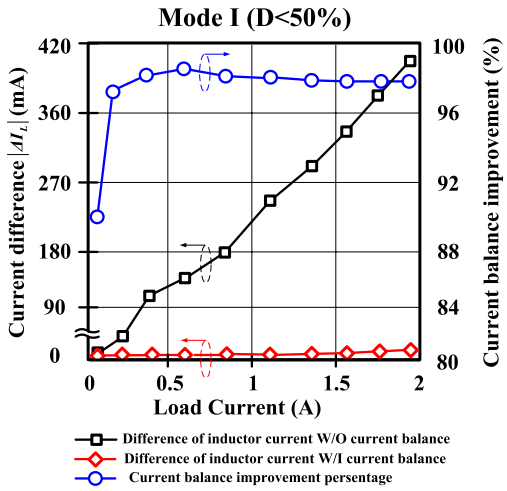
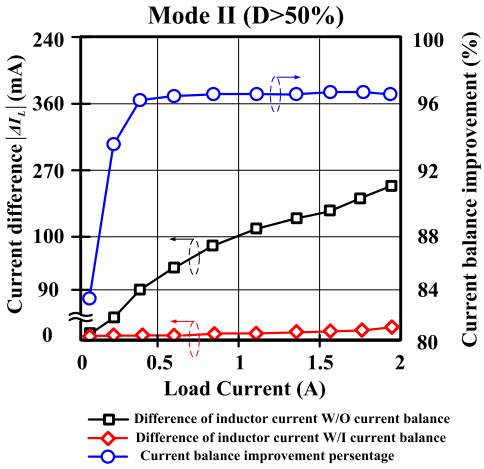



Fig. 24. Measured load transient response when load current changes from 0 to 500 mA.




(a)




(b)

Fig. 25. Statistic summary of the current balance mechanism in the proposed PRCB technique. (a) Operating in Mode I. (b) Operating in Mode II.

to Mode II during the load-transient period to enlarge the duty cycles and derive extra energy. Thus, the mode transition operation helps minimize the voltage drop and shortens the transient response time to enhance load transient operation. The operating mode may be switched back to Mode I once the load transient period is terminated. However, the DBP mechanism helps define a hysteretic region to avoid abnormal mode transitions triggered by switching noise. Therefore, the

TABLE III
PERFORMANCE COMPARISON OF MULTIPHASE CONVERTERS

| | [4] | [9] | [6] | This work |
|---|---|---|---|---|
| Year | 2004 | 2002 | 2008 | 2012 |
| Control method | Hysteretic | Droop method | Average-current sharing | PRCB |
| Phase number | 2 | 2 | 2 | 2 |
| Input voltage | 5 V | N/A | 12 V | 3.3 V |
| Switching frequency per phase | 0-600 kHz | N/A | 330 kHz | 600 kHz |
| Comparators per phase | 3/2 | 0 | 1 | 1/2 |
| Amplifiers per phase | 1/2 | 4 | 3 | 1/2 |
| Ramps per phase | 0 | 0 | 1 | 1/2 |
| Current balance improvement | Max. 98% | Min. 70%<br>Max. 96% | N/A | Min. 83%<br>Max. 98.7% |

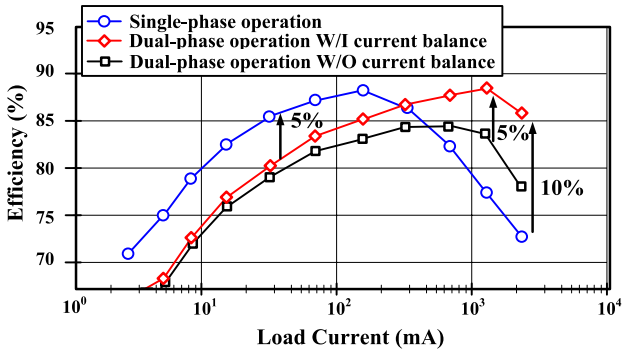



Fig. 26. Power conversion efficiency.

converter keeps operating in Mode II until the surplus energy is detected at the output.

The statistical summaries of the current balance mechanism operating in Mode I and Mode II are shown in Fig. 25(a) and (b), respectively. Owing to mismatch, the difference of the inductor current between the two phases dramatically increases as an increment of load current. With the PRCB technique, the current difference remains smaller than 10 mA over the whole load range. The current balance improvement percentage, which is the decrement percentage of the difference of the inductor current, is over 95% at mostly load conditions. With the adoption of the offset cancelation technique, the performance of current balance is regardless of the device mismatches in the OTA. The improvement is at least 83% at very light loads and the maximum improvement is 98.7%.

Fig. 26 shows the power conversion efficiency. If the load current is smaller than 150 mA, the processor can change the converter to single-phase operation for high efficiency. The efficiency improvement can reach 5%. However, the converter with the dual-phase operation has better efficiency at heavy loads. A peak efficiency of 88% is derived with the load of 1150 mA. Improved efficiencies of 5 and 10% are achieved when comparing to the dual-phase operation without current balance function and the single-phase operation, respectively.

Table III shows the performance comparison of multiphase converters. Among the integrated converters [1], [6], and [9], great quantities of comparators, amplifiers, and ramps have to be adopted according to different designs. Only the proposed multiphase converter with the PRCB technique is controlled by one modulation controller regardless of the phase number. Small footprint area and high current balance improvement percentage are achieved.

## VI. CONCLUSION

The proposed PRCB technique for the voltage-mode multiphase DC–DC buck converter with single controller has been presented to achieve high current balance performance and the area-efficient solution. The pseudo-ramp operation uses only one physical saw-tooth signal to generate two individual control duties for dual-phase operation. In addition, the current balance mechanism also forms a current-loop, which can dynamically adjust each of the duty cycles, to ensure identical driving capability in the multiphase structure. The OCC circuit for the current balance loop is used to prevent the deterioration of the current balance performance caused by intrinsic offset voltage of the operational transconductance amplifier. Moreover, the mode transition operation is activated when the point of duty cycle determination is approximately 50% to prevent undesired mode transitions and help enhance the load transient response. Experimental results demonstrate the different mode operation with distinct duty cycles. The current in each phase is well balanced under both light and heavy load conditions with an improvement of 83% in current balance.

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