Absolute Value, 1% Linear and Lossless Current-Sensing Circuit for the Step-Down DC-DC Converters With Integrated Power Stage

Vratislav Michal

***Abstract*—A circuit allowing to accurately measure the average output current of the step-down DC-DC converter operating in PWM mode is presented. It relies on the measurement of the average voltage drop across the PMOS-NMOS or dual-NMOS power stage. The average voltage drop is measured by a simple RC filter, as a difference between the power-stage average output voltage and the average output voltage of an auxiliary "ideal" power stage. Obtained voltage drop is applied to an element labeled as "composite load". This approach allows to remove the dominant errors originating from the use of a standard sense-FET circuit. Obtained output current image exhibits very low linearity error <1% in 10 mA to 2.1 A range, and high ±4% accuracy of the conversion gain over supply voltage, temperature and statistical chip-by-chip variations. The performances of integrated current sensor are demonstrated by measurements on 3.2 MHz step down DC-DC converter integrated in 0.5 µm CMOS process.**

***Index Terms*—Lossless current sensing, current estimator, linear sense-FET, step-down DC-DC converter, current sharing, multiphase DC-DC converter control, fragmented differential pair, DC offset voltage compensation.**

I. Introduction

MEASUREMENT of the output current nowadays presents an important topic in the design of switched-mode high power DC-DC converters. Main purpose of the current-sensing circuit is to provide information about the DC-DC converter output current I_{OUT} [1], [2]. This information is required in many applications aiming the control or optimization of the power-flow in electronic systems. For example, one of intended applications is the software development for the mobile-phone and tablets platforms based on the ARM® application processors. Here, monitoring of the processor power-consumption enables to optimize the code of embedded software, with aim to increase the battery life time. Another concerned application is the implementation of the accurate current-sharing algorithm for the four-phase 8 and 20 Amp DC-DC converters [3], [4], [16]. Generally, knowledge of the output current is helpful in almost all fields of the power-management applications.

Manuscript received July 10, 2013; revised December 22, 2013 and January 28, 2014; accepted February 08, 2014. Date of publication March 14, 2014; date of current version April 21, 2014. This paper was approved by Associate Editor Ken Shepard.

The author is with STMicroelectronics, 38000 Grenoble, France (e-mail: vratislav.michal@st.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2014.2309696

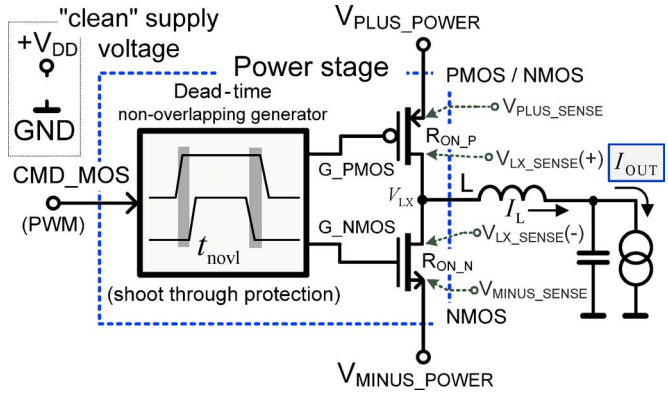

Fig. 1. Typical step-down converter power stage with output LC filter. V_{DD} and GND are the "clean" power supply rails connected with power supply lines.

Current sensing circuit presented here therefore aims to provide the image I_{SENSE} of the DC-DC converter average output current I_{OUT}:

$$I_{\mathrm{SENSE}} = k \cdot I_{\mathrm{OUT}} \tag{1}$$

where k is the scaling constant $k \ll 1$. In the case where value k is guaranteed, absolute value current measurement is provided.

In order to facilitate the description of the current-sensing approach, we focus on the simplified schematic of the step-down DC-DC converter power stage shown in Fig. 1. In this schematic, we notice the input PWM control signal CMD_MOS, and the dead-time circuit producing non-overlapping gate signals G_PMOS and G_NMOS. These signals G_PMOS and G_NMOS are directly the gate voltages of the power transistors. The power stage considered in this paper can be realized as NMOS-PMOS, or dual-NMOS configuration. The output of the converter is a standard LC filter with load represented by the current source I_{OUT}. Accurate measurement of this output current is therefore goal of the presented circuit.

The most-widely used techniques of the lossless current sensing are extensively described in [1] and [2]. Among others, we can refer to:

a) *Current-replica sense-FET circuits*,
b) *Inductor serial resistance DC voltage sensing*.

A. Sense-FET Approach

The sense-FET approach is based on the sensing of the power MOSFET V_{DS} voltage appearing across the channel ON resistance. This voltage is then applied to an auxiliary "sense-FET"

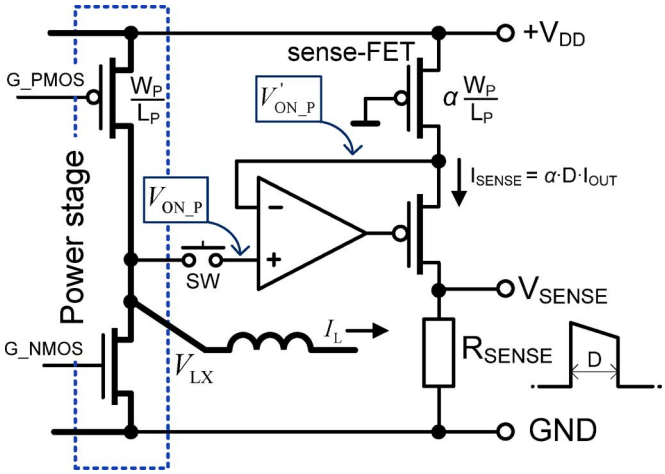

Fig. 2. Standard configuration of the sense-FET circuit used to measure the drain current of the power PMOS in the buck converter power stage.

transistor [5], [6]. As the MOS transistor ON resistance is inversely-proportional to W:

$$R_{ON_{(N,P)}} \cong \frac{1}{KP_{(N,P)}\frac{W}{L}\left(V_{\mathrm{GS}} - V_{\mathrm{TH}} - \frac{V_{\mathrm{DS}}}{2}\right)} \tag{2}$$

using the α-scaled sense-FET MOS transistor ($W_{\mathrm{SENSE-FET}} = \alpha \cdot W_{\mathrm{POWER}}, L_{\mathrm{SENSE-FET}} = L_{\mathrm{POWER}}$) with $\alpha \ll 1$ allows to obtain the output current image I_{SENSE}:

$$I_{\mathrm{SENSE}} = \alpha I_{\mathrm{OUT}}. \tag{3}$$

An example of the sense-FET circuit used with the step-down DC-DC converter power stage is shown in Fig. 2. The voltage follower based on the operational amplifier allows to apply the voltage $V_{\mathrm{ON\_P}} = R_{\mathrm{ON\_P}} \cdot I_L(t)$ present during the PMOS conduction phase to the drain terminal of the sense-FET. This voltage creates the sense current $I_{\mathrm{SENSE}}(t) = \alpha R_{\mathrm{ON\_P}} \cdot I_L(t)$ which in turn generates the output voltage V_{SENSE} across the sense-resistance R_{SENSE}. In the remaining time (i.e., when PMOS transistor is OFF), the voltage across the sense-FET is set to zero by disconnecting the switch SW. It follows, that obtained average voltage V_{SENSE} has a duty-cycle (D) dependency:

$$\widehat{V}_{\mathrm{SENSE}} = \alpha R_{\mathrm{SENSE}} I_{\mathrm{OUT}} D. \tag{4}$$

As a matter of course, the duty-cycle introduces high nonlinearity error in V_{SENSE}. This duty cycle dependence can be removed by using a sample&hold circuit S/H as shown in Fig. 3 [7]. However, this approach is affected by an error $\beta\Delta I_L$ originating from the triangular shape of the inductor current (ΔI_{L} is the peak-to-peak amplitude of inductor current, see Fig. 6). The value of β is a constant related to the sampling time position with respect to the PMOS conduction phase. The obtained voltage V_{SENSE} can be then written as

$$V_{\mathrm{SENSE}} = \alpha \left\{ I_{\mathrm{OUT}} + \beta \Delta I_L(t) \right\} R_{\mathrm{SENSE}}. \tag{5}$$

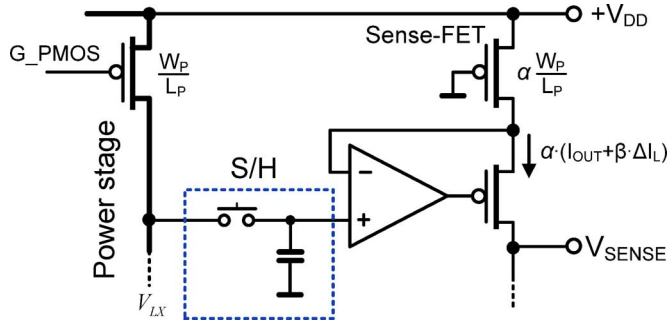

Fig. 3. Sample&Hold (Track&Hold) sense-FET circuit allowing to decrease the duty-cycle error.

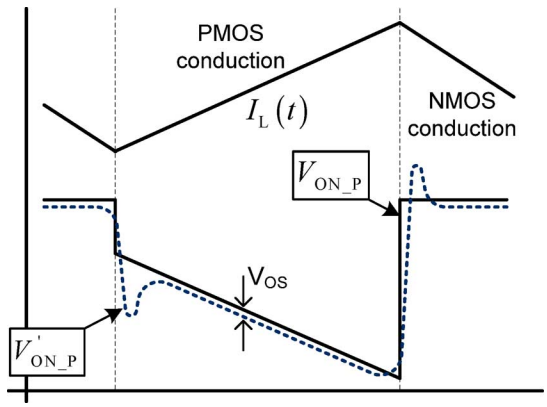

Fig. 4. Error of the sense-FET circuit created by the DC offset and finite speed of the operational amplifier.

For example, the sampling performed at the end of the PMOS transistor conduction phase results in $\beta = -0.5$ (valley inductor current is measured).

Errorless sensing ($\beta = 0$) can be provided by sampling exactly in the middle of the PMOS conduction phase (Fig. 6). This can be advantageously used e.g., for the constant-ON time control scheme, where the mid-time sampling instant can be accurately predicted. However, in order to provide very-low charge injection and the protection against the V_{LX} voltage ringing, advanced S/H design techniques are to be used (e.g., differential sampling).

A second non-negligible error present in the sense-FET circuit originates from the operational amplifier DC offset voltage V_{OS} and finite settling time. This is illustrated in Fig. 4, where the voltage image $V'_{\mathrm{ON\_P}}$ is not perfectly tracking the drain voltage $V_{\mathrm{ON\_P}}$, and creating thus a non-negligible error of I_{SENSE}. This error is dominating namely for the low output current range.

Due to these mentioned limitations, sense-FET circuit requires low offset and very fast (not for the S/H variant) operational amplifier. Including these design constraints, obtained accuracy is in the order of tens of percent without the knowledge of the output current absolute value.

B. Inductor Parasitic Resistance DC Voltage Sensing

Second widely used technique reaching better linearity is based on the sensing of DC voltage drop across the converter's output inductor L [1], [8], [9]. As the ideal inductor voltage

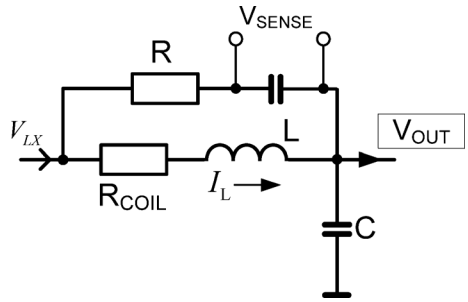

Fig. 5. Equivalent circuit of the output LC filter with inductor parasitic resistance R_{COIL}.

drop is zero during the steady-state operations, the sole DC component is related to the serial parasitic resistance R_{COIL}. As shown in Fig. 5, this DC component can be measured by a simple RC-filter.

In order to provide absolute value measurement, accurate knowledge of R_{COIL} is required. However, the value of R_{COIL} changes radically between different inductors (different L, package etc.), and presents relatively high ($\pm 20\%$) statistical dispersion for inductors of the identical type. As an example, this dispersion is one of the origins of the current unbalancing in the multiphase DC-DC converters. In order to obtain the conversion gain k, calibration allowing to determine the value of R_{COIL} is usually implemented. Generally, this calibration requires injection of a reference current and measurement of the voltage drop across the inductor. Due to generally small R_{COIL} values ($\sim$ tens of mΩ), this current is to be high enough to provide an exploitable DC voltage. It is therefore difficult to ensure this calibration during the test in a mass production. Nevertheless, technique based on the coil DC drop measurement can provide decent accuracy in order of $\pm 15\%$ with high linearity [8].

As alternative to inductor DC voltage drop sensing, method based on the measurement of PCB trace resistance or method based on inductor's magnetic field measurement are also present in the literature [10], [11].

In this paper, system allowing to obtain accurate, linear, and absolute value image of the output current I_{OUT} in PWM mode is described. The method relies on the measurement of the average composite voltage drop V_{AVG} across the power stage transistors, and on the simultaneous use of the element labeled as the composite load. An important feature of presented technique is that it does not require any external calibration for achieving the final few percent accuracy of I_{SENSE} down to a few mA output current. In the target application, circuit was used also to measure the current also in PSK mode by short forcing the PWM mode (several tens of conduction cycles before A/D sampling). This allowed to emulate a steady state PWM condition without a significant drop of efficiency.

This paper contains the description of the current sensing approach based on the V_{DS} voltage averaging in Section II. Main structure of the current sensor based on the composite voltage drop measurement is presented in Section II-B. The design aspects allowing to preserve high current-sensor accuracy in switching (noisy) environment are presented in detail in Section III. A brief description of the operational amplifier offset compensation is presented in Section IV, and the results obtained by measurements on the integrated DC-DC converter are provided in Section V.

II. Current Sensing Based on V_{DS}-Averaging

A. V_{DS} Voltage Averaging

As previously mentioned, the nonlinearity in the sense-FET circuit given by (4) can be removed by Sample&Hold circuit shown in Fig. 3. However, due to triangular inductor current I_L, sampling time related error (5) is present.

As shown in Fig. 6 detailing the main signals of Fig. 1 power-stage, the triangular form of the inductor current $I_{\mathrm{L}}(t)$ creates the time-dependent voltages $V_{\mathrm{ON\_N}}$ and $V_{\mathrm{ON\_P}}$ across the power MOS ON resistances (ON resistance is constant during the conduction phase).

In the steady-state, the average output current I_{OUT} is equal to the average inductance current $\widehat{I_L}$. It follows, that the drain currents of NMOS and PMOS power transistors averaged during their conduction cycles are also both equal to I_{OUT}. It turns out that I_{OUT} can be measured by averaging only one of V_{ON_N} or V_{ON_P} voltages during their respective conduction cycles. If this average voltage is continuously applied on the P or N channel type sense-FET, absolute-value image of I_{OUT} is be obtained.

A solution allowing to remove the time-dependency from (5) is therefore to replace the Sample&Hold circuit shown in Fig. 3 by an averaging circuit such as a RC filter. In particular, the input terminal of the RC filter is to be connected to, e.g., PMOS drain voltage $V_{\mathrm{ON\_P}}$ only during the PMOS conduction phase. In the remaining time, the input terminal is to be set to the high impedance. In other words, the RC filter realizes a sort of moving average function during the PMOS transistor conduction, whereas the capacitor stores the averaged value during the remaining non-conduction time (Fig. 7). The obtained steady-state output voltage of RC filter is therefore

$$\widehat{V}_{ON\_P\_AVG} = R_{ON\_P} \cdot I_{\mathrm{OUT}} \tag{6}$$

which has no duty-cycle dependence. In the circuit shown in Fig. 7, a cascade switch implementation is used. The cascade switch improves the off-state isolation between the V_{LX} and RC-filter input nodes. This allows to avoid the leakage during the V_{LX} oscillation or PMOS body-diode conduction, when M_1 can become partially open. The solution shown in Fig. 7 offers acceptable performance, although it suffers from high and asymmetrical charge injection error.

In fact, when transistor M_3 turns OFF, the switch output turns to the high impedance and part of the channel charge and switching current I_{SW} is absorbed by the RC filer. This results in a few mV offset voltage, decreasing the accuracy in the low-current area.

B. Main Concept of the Current Sensor

The method allowing to overcome the previously mentioned drawbacks is based on the measurement of the composite voltage drop across the DC-DC converter power stage operating in PWM mode. This voltage drop is then applied to

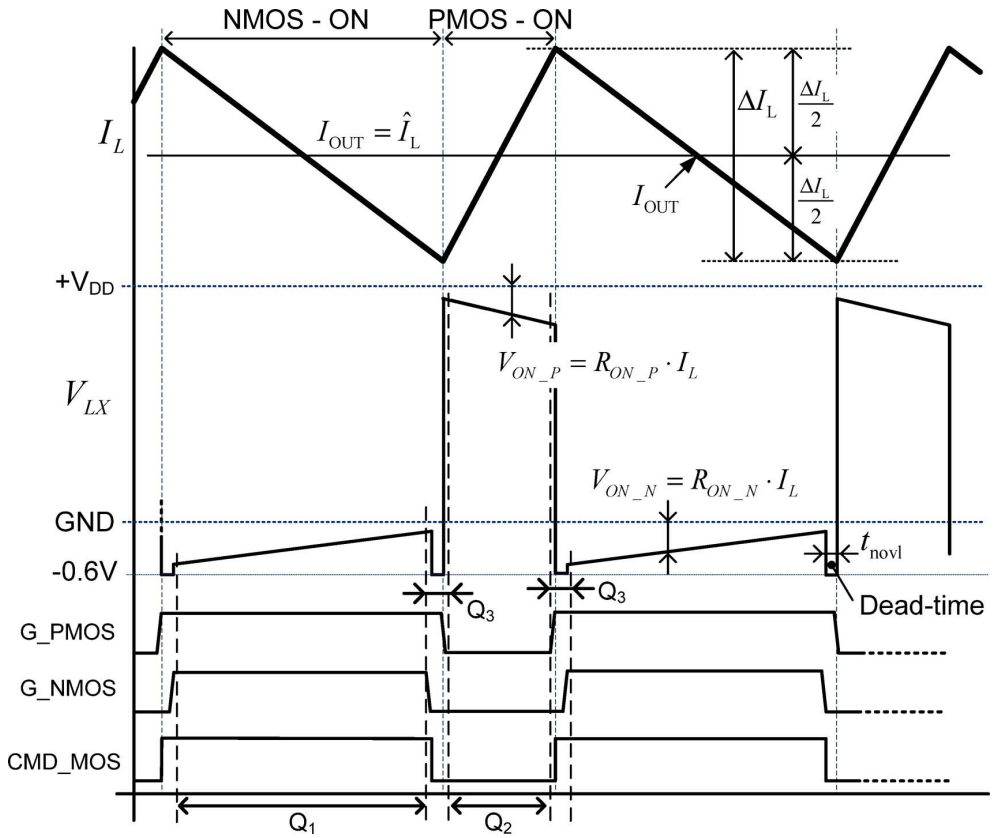

Fig. 6. Signals of step-down (PMOS-NMOS) power stage from Fig. 1 for $I_L > 0$. I_L stands for inductor current, V_{LX} for the power-stage output voltage, G_PMOS and G_NMOS for gate voltages of power MOS transistors, and CMD_MOS the control PWM signal.

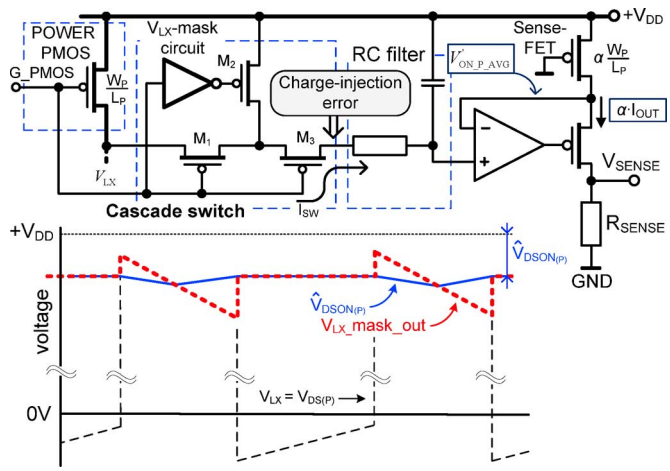

Fig. 7. Current-sensing circuits with averaging RC filter allowing to removing the duty-cycle dependence from I_{SENSE}.

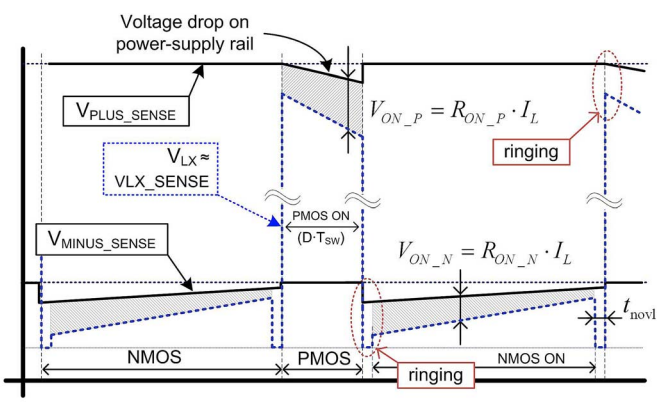

Fig. 8. Detail of V_{LX} voltage affected by $R_{\mathrm{ON\_N}}$ and $R_{\mathrm{ON\_P}}$ ON-resistances, and power-rails voltages affected by theirs parasitic access resistances.

the element labeled "composite load". The average composite voltage drop V_{AVG} is obtained by averaging RC filters, which allows to realize accurate measurement without frequency limitation. In other words, the most sensitive operation of V_{DS} voltage measurement (from the fast-switching, noisy and ringing V_{LX} and power rails voltages) is done by simple passive RC-filters.

The average voltage drop V_{AVG} is defined as the difference between the average output voltage of the ideal (lossless) power-stage, and the average output voltage of the real power-stage, affected by the output current I_{OUT} and power transistors' ON-resistances. In reality, the ideal power-stage consists of small MOS-transistors driving zero output current and therefore having zero V_{DS} voltage.

It follows that V_{AVG} is obtained as a linear combination of $V_{\mathrm{ON\_N}}$ and $V_{\mathrm{ON\_P}}$ voltages present across the power-MOS transistors during their respective conduction phases.

The origin of the composite voltage drop V_{AVG} results from the time plot shown in Fig. 8, detailing the node voltages of the Fig. 1 power stage. Here, we can see that the power-stage output voltage V_{LX} is affected by the power MOS resistances $R_{\mathrm{ON\_N}}$ and $R_{\mathrm{ON\_P}}$, but also by the

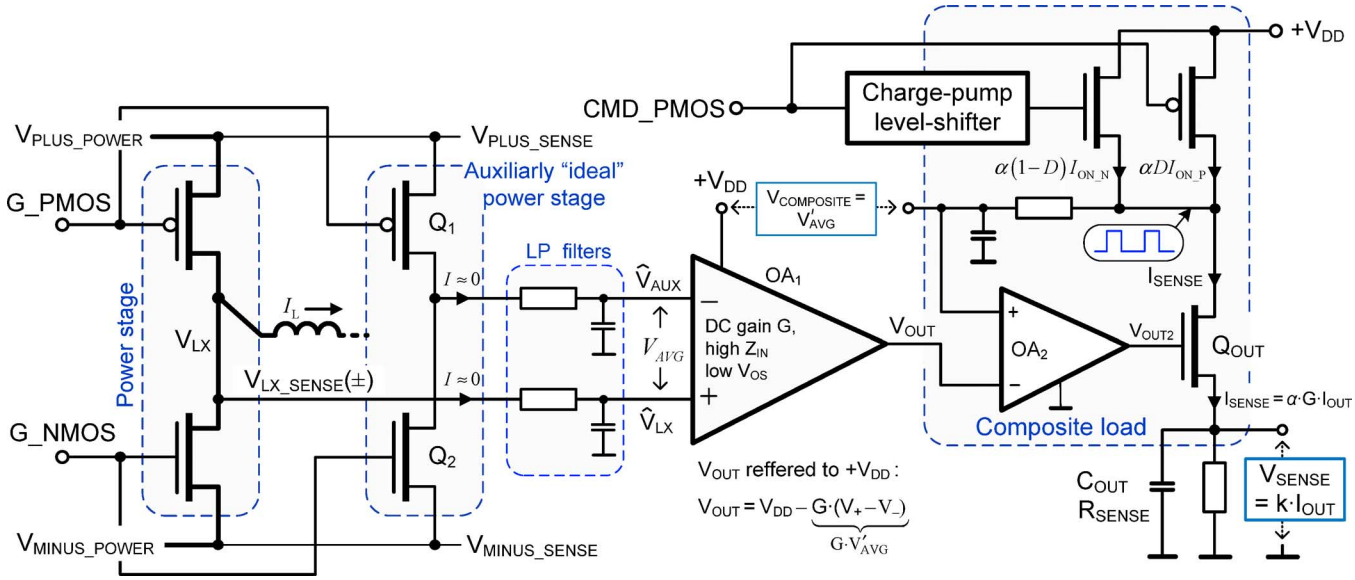

Fig. 9. Simplified circuit of absolute-value current sensor for NMOS-PMOS power-stage with R_{SENSE} referred to GND.

power rail voltages $V_{\mathrm{PLUS\_POWER}} \approx V_{\mathrm{PLUS\_SENSE}}$ and $V_{\mathrm{MINUS\_POWER}} \approx V_{\mathrm{MINUS\_SENSE}}$. These $V_{\mathrm{PLUS\_SENSE}}$ and $V_{\mathrm{MINUS\_SENSE}}$ voltages are shifted from the "clean" V_{DD} and GND by the voltage drops on the power-rails connections.

As mentioned in Section II-A, currents averaged during the ON-times of the bottom and upper power switches are both equal to I_{OUT} (Fig. 6). In this account, ON-state average voltages $V_{\mathrm{ON\_N}}$, and $V_{\mathrm{ON\_P}}$ of the bottom and upper power switches can be written as

$$\begin{aligned} \hat{V}_{\mathrm{ON\_N}} &= R_{\mathrm{ON\_N}} \cdot I_{\mathrm{OUT}} \\ \hat{V}_{\mathrm{ON\_P}} &= R_{\mathrm{ON\_P}} \cdot I_{\mathrm{OUT}} \end{aligned} \tag{7}$$

where $R_{\mathrm{ON\_N}}$ and $R_{\mathrm{ON\_P}}$ are strongly V_{DD}, temperature, and process dependent (2). The average composite voltage drop V_{AVG} is obtained as the weighted contribution of $\hat{V}_{\mathrm{ON\_N}}$ and $\hat{V}_{\mathrm{ON\_P}}$. As $\hat{V}_{\mathrm{ON\_P}}$ is averaged during $D \cdot T_{\mathrm{SW}}$ time and $\hat{V}_{\mathrm{ON\_N}}$ is averaged during $(1-D) \cdot T_{\mathrm{SW}}$ time, V_{AVG} can be expressed as

$$\begin{aligned} V_{\mathrm{AVG}} &= D \cdot R_{\mathrm{ON\_P}} \cdot \hat{I}_L + (1-D) R_{\mathrm{ON\_N}} \cdot \hat{I}_L \\ &= I_{\mathrm{OUT}} \left\{ D \cdot R_{\mathrm{ON\_P}} + (1-D) \cdot R_{\mathrm{ON\_N}} \right\}. \end{aligned} \tag{8}$$

This voltage is amplified by the differential amplifier by an arbitrary gain G (~2 to 5):

$$V'_{\mathrm{AVG}} = G \cdot V_{\mathrm{AVG}}. \tag{9}$$

The simplified schematic of the current sensor is shown in Fig. 9. Here, we can see that V_{AVG} is measured as the difference between:

1) power stage average output voltage $\hat{V}_{\mathrm{LX}}$, and
2) average output voltage $\hat{V}_{\mathrm{AUX}}$ of the auxiliary "ideal" power stage connected between the power-sense nodes.

More accurately, RC filters perform averaging of the voltage drop between $V_{\mathrm{PLUS\_SENSE}}$ and $V_{\mathrm{LX\_SENSE(+)}}$ during the PMOS conduction phase, and between $V_{\mathrm{MINUS\_SENSE}}$ and $V_{\mathrm{LX\_SENSE(-)}}$ during the NMOS conduction phase (Fig. 1). The value of V_{AVG} is therefore labeled "composite voltage drop", because it contains compounds of the NMOS and PMOS $V_{\mathrm{ON\_N}}$ and $V_{\mathrm{ON\_P}}$ drain-to-source voltages.

However, function V_{AVG} given by (8) is strongly nonlinear due to the duty-cycle D, R_{ON} resistances, temperature and process dependencies. Therefore, composite load element is used to obtain a linear relationship between the DC-DC converter output current I_{OUT}, and measured image I_{SENSE} of the output current.

C. Composite Load

In order to obtain the absolute value α-scaled replica I_{SENSE}, duty-cycle depending resistance $R_{\mathrm{COMPOSITE}} = \{D \cdot R_{ON\_P} + (1-D) \cdot R_{\mathrm{ON\_N}}\}/\alpha$, which is matched to the power stage average resistance $D \cdot R_{\mathrm{ON\_P}} + (1-D) \cdot R_{\mathrm{ON\_N}}$ needs to be created. As shown in Fig. 9, this duty-cycle depending resistance $R_{\mathrm{COMPOSITE}}$ is created by a parallel connection of the NMOS and PMOS sense-FET transistors.

These transistors are switched in the ohmic regime simultaneously with the power NMOS and PMOS transistors, and are biased by a constant DC current I_{SENSE}. This current I_{SENSE} represents the output value generated by the current sensor. Its value is obtained by the control loop containing the operational amplifier OA_2, averaging RC filter, and constant current-source created by transistor Q_{OUT}. The transistor Q_{OUT} operates with constant (DC) voltage V_{GS} provided by the OA_2 output V_{OUT2}.

The average voltage across the composite load is obtained by the RC filter as weighted contributions of $V_{\mathrm{DS\_SENSE\_N}}$ and $V_{\mathrm{DS\_SENSE\_P}}$. $V_{\mathrm{DS\_SENSE\_N}} = I_{\mathrm{SENSE}} \cdot R_{\mathrm{ON\_N}}/\alpha$ during the NMOS conduction phase, and $V_{\mathrm{DS\_SENSE\_P}} = I_{\mathrm{SENSE}} \cdot R_{\mathrm{ON\_P}}/\alpha$ during the PMOS conduction phase. It results that the voltage on the composite load transistors contains a square wave compound as shown in Fig. 9.

The average voltage across the composite load obtained by the RC filter can be written as

$$V_{\mathrm{COMPOSITE}} = I_{\mathrm{SENSE}} \left((1-D) \frac{R_{\mathrm{ON\_N}}}{\alpha} + D \frac{R_{\mathrm{ON\_P}}}{\alpha} \right) \tag{10}$$

which results in the average resistance $R_{\mathrm{COMPOSITE}}$:

$$R_{\mathrm{COMPOSITE}} = \frac{V_{\mathrm{COMPOSITE}}}{I_{\mathrm{SENSE}}} = (1-D)\frac{R_{ON\_N}}{\alpha} + D\frac{R_{ON\_P}}{\alpha}. \quad (11)$$

The down-scaled image I_{SENSE} of the output current I_{OUT} can be obtained from (8) as $V_{\mathrm{AVG}}/R_{\mathrm{COMPOSITE}}$:

$$I_{\mathrm{SENSE}} = \alpha \cdot G\frac{D \cdot R_{\mathrm{ON\_P}} + (1-D)\cdot R_{\mathrm{ON\_N}}}{D \cdot R_{\mathrm{ON\_P}} + (1-D)R_{\mathrm{ON\_N}}} \cdot \hat{I}_L = \alpha \cdot G \cdot I_{\mathrm{OUT}}. \quad (12)$$

For this purpose, average voltage $V_{\mathrm{COMPOSITE}}$ across the composite load is regulated by OA_2 to be equal to the OA_1 output V'_{AVG} (8). The output of OA_1 is therefore referred to $+V_{\mathrm{DD}}$ which means that its transfer function is $V_{\mathrm{OUT}} = V_{\mathrm{DD}} - G(V_+ - V_-)$. The current I_{SENSE} is sinked from the composite load by Q_{OUT}, and is generated either by the PMOS or NMOS sense-FET transistors, depending on the actual power-stage conduction phase. The use of composite load referred to $+V_{\mathrm{DD}}$ is advantageous, because it allows to refer the sensing resistance R_{SENSE} to GND. **Note:** A variant of R_{SENSE} referred to $+V_{\mathrm{DD}}$ can also be envisaged and was tested on silicon (this configuration allows to avoid the level shifter for the dual-NMOS power stage configuration). The driving of the sense transistors is to be done in a way that one of the sense transistors is always conducting (unless a supplementary transistor is used; see the end of Section III-D). If both transistors are simultaneously non-conducting even for a short time, the constant current I_{SENSE} produces a high voltage which creates a non-negligible error after the filtering.

One benefit of the circuit shown in Fig. 9 is that I_{SENSE} can be measured with high accuracy, i.e., without current mirror in the I_{SENSE} current path. Indeed, using the current mirror can generate unnecessary extra mismatch error of up to $\pm 5\%$.

As results from the sense transistors switching, the I_{SENSE} contains short current spikes. This requires use of a small RC filter allowing to obtain a low-noise DC output voltage V_{SENSE}. If a sensing resistance R_{SENSE} is used to convert the output current I_{SENSE} to V_{SENSE}, the output voltage across R_{SENSE} is

$$V_{\mathrm{SENSE}} = I_{\mathrm{SENSE}} \cdot R_{\mathrm{SENSE}} \quad (13)$$

and the measured DC-DC converter output current corresponds to

$$I_{\mathrm{OUT}} = \frac{V_{\mathrm{SENSE}}}{\alpha \cdot G \cdot R_{\mathrm{SENSE}}}. \quad (14)$$

It is evident that R_{SENSE} value is to be known. For this purpose, an accurate external (off-chip) discrete resistor, or internal (on-chip) calibrated resistor is to be used. On the contrary, if the current-sensor is used in the current-sharing control loop, only accurate matching between sense resistors $R_{\mathrm{SENSE}(1-n)}$ of concerned phases is to be provided.

As already mentioned, both operational amplifiers operate with slow DC input voltage. On this account, a simple low-consumption two-stage operational amplifier (OA_1) (Fig. 18) and single stage OA_2 (Fig. 17) can be used.

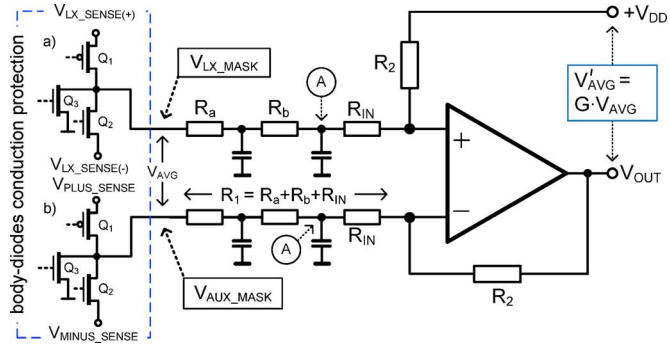

Fig. 10. Detail of the differential amplifier with input low pas filters and V_{LX}-transition masking circuit.

III. Circuit Implementation

In this section, a detailed description of the blocs depicted in the current sensor of Fig. 9 is provided. In particular, we focus on the implementation of: (a) differential amplifier OA_1 including input RC filters, (b) V_{LX}-transition masking circuit allowing to protect the circuit against errors created by the V_{LX}-transitions and power transistors substrate diode conductions, (c) composite load, (d) analysis of the gain error created by the V_{LX} transition times, and (e) serial fingers sense-FET structure. Last subsection resumes the final implementation of the current sensor for the PMOS-NMOS power stage.

A. Differential Amplifier

The simplicity of the concept depicted in Fig. 9 relies on the fact that the composite voltage drop V_{AVG} is obtained by the passive-RC filters. This signifies that the differential amplifier operates with "slow" DC input voltages, whereas the RC filters are exposed to the high-frequency spikes and oscillations created by fast V_{LX} transitions and parasitic V_{LX} voltage ringing. Realization of the differential amplifier including RC filters is shown in Fig. 10. This figure includes the low-offset operational amplifier described in Section IV, second-order averaging RC filters, feedback resistors R_2, and input transistors of the V_{LX} transition-masking circuit described in Section III-B.

Using the second-order filters shown in Fig. 10 helps to improve the detection speed of the current sensor and also to improve the attenuation of the higher order harmonics of V_{LX} and V_{AUX} signals. Their design is described in [12] (see also [13] for further detection speed improvement). The filter's cut-off frequency F_0, as well as the cut-off frequency of the filter in the composite load, is directly related to the detection speed. As an example, a high F_0 shortens the time-response, while it decreases the attenuation in the node Ⓐ and vice versa. Generally, the cut-off frequency is to be at least one decade below the switching frequency F_{SW}, which results in few μs (several conduction cycles) time response of the current sensor output voltage V_{SENSE} ($F_{\mathrm{SW}} = 3.2$ MHz, see Table I).

Provided that both Fig. 10 RC filters have perfectly identical characteristics, the differential input voltage of the operational

TABLE I
PARAMETERS OF THE INTEGRATED STEP-DOWN DC-DC CONVERTER

DC-DC CONVERTER	VALUE
V_{DD} (V)	2.5 to 4.8
V_{OUT} (V)	1.8
I_{OUT_MAX} (A)	2.0
F_{SW} (MHz)	3.2
L (µH)	1 or 0.47
CURRENT SENSOR	
Total accuracy (%)	± 4
Linearity[1] (%)	1
V_{SENSE}/I_{OUT} gain (V/A)	0.2
Input RC filters F_0 (kHz)	300
Quiescent current[2] (µA)	80
Area (µm^2)	360 × 82

[1] V_{DD} = 3.6V, I_{OUT} = 0.06 - 2.1A
[2] V_{DD} = 3.6V, I_{OUT} = 0A

amplifier (between nodes Ⓐ) is a constant DC voltage with a small common-mode AC voltage, oscillating on the switching frequency $F_{\rm SW}$. This common-mode AC oscillation is attenuated by the CMRR of the operational amplifier. On this account, constant DC voltage $V'_{\rm AVG}$ (8) is generated by the $\rm OA_2$ output. Generally, oscillation of a few millivolts in the points Ⓐ is acceptable for the correct circuit operation.

In the amplifier feedback network, resistances $R_{\rm IN}$ are mandatory as they protect the second capacitors against a short circuit from the operational amplifier virtual zero. The value of $R_{\rm IN}$ is to be selected so that $R_{\rm IN} \approx R_{\rm a} + R_{\rm b}$. Moreover, the value of $R_{\rm a}$ is to be high, in order to decrease the current sink from $V_{\rm LX}$ and $V_{\rm PLUS\_SENSE}$ terminals ($R_{\rm a} > 100$ kΩ). The DC gain G of differential amplifier is given as:

$$G = \frac{V'_{\rm AVG}}{\hat{V}_{\rm AVG}} = \frac{R_2}{R_a + R_b + R_{\rm IN}}. \qquad (15)$$

and can be preferably 2 to 5. When the $\rm OA_1$ is compensated for offset, the gain G allows to decrease the offset generated by second $\rm OA_2$. The $V_{\rm OS}$ of $\rm OA_2$ is referred to the input of $\rm OA_1$ as $V_{\rm OS2}/G$. In order to obtain high current-sensor accuracy, very good matching of all resistors in the structure is required (∼1%). This is to be provided by a symmetrical layout of both Fig. 10 RC filters, as well as by the surface optimization following from Pelgrom's rule. It is also to be noted that DC gain (15) is defined as the voltage gain between the RC-filters inputs and the operational amplifier output. On this account, average DC voltages $\hat{V}_{\rm LX}$, $\hat{V}_{\rm AUX}$, and $\hat{V}_{\rm AVG}$ are not physically present in the Fig. 10 circuit.

B. V_{LX}-Transition Masking Circuit

Due to the high gate capacitance of the power transistors, their ON/OFF switching is not instantaneous. The slow gate voltages G_NMOS and G_PMOS result in undefined transient resistances $R_{\rm ON\_(N,P)}$ (2) and finite $V_{\rm LX}$ slew-rate. Moreover, during the dead-time body-diode conduction, the $V_{\rm LX}$ voltage

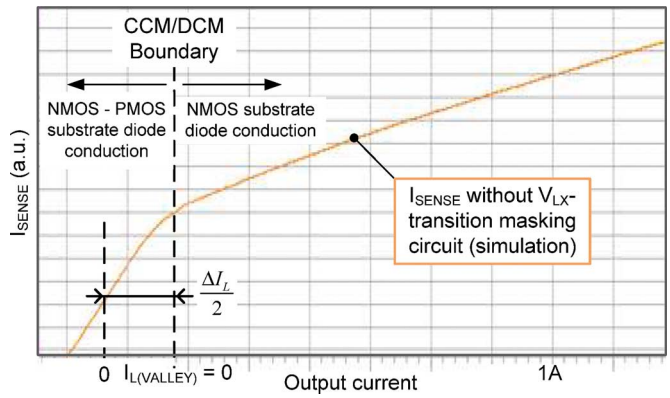

Fig. 11. Example of the characteristic with error created by the $V_{\rm LX}$ transitions and substrate diode conductions.

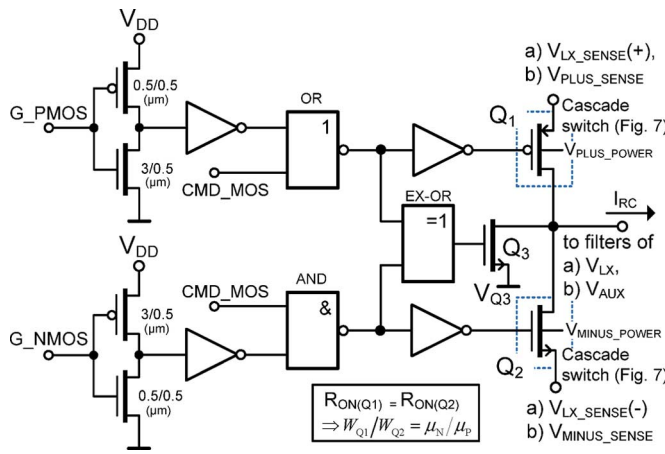

Fig. 12. $V_{\rm LX}$-transition masking circuit (implemented two times for (a) $\rm V_{LX}$-path and (b) $\rm V_{AUX}$-path). Transistors Q_1 and Q_2 are to be implemented as the cascade switch as shown in Fig. 7.

is also undefined (see Fig. 6). These effects generate an undefined voltage during the transition phases $\rm T_{Q3}$ (Fig. 6), which is integrated by RC filters in the Fig. 9 current sensor circuit.

An example of the error resulting from the $V_{\rm LX}$ transitions phases is shown by a simulation in Fig. 11. This simulation was performed on the ideal schematic of Fig. 9. In Fig. 11, two linear regions of $I_{\rm SENSE}$ can be identified, whereas either NMOS or PMOS substrate diode conduction occur.

In order to decrease the error related to the $V_{\rm LX}$ transition phases, RC-filter inputs are to be disconnected from $V_{\rm LX}$ and $V_{\rm AUX}$ nodes during the $V_{\rm LX}$ transitions and during the body-diode conduction (i.e., during $\rm T_{Q3}$ in Fig. 6). At this time, inputs of both RC filters are connected together to, e.g., GND or $V_{\rm DD}$.

The circuit allowing to realize the $V_{\rm LX}$-transition masking is shown in Fig. 10 and detailed in Fig. 12. As shown in Fig. 10, the whole circuit from Fig. 12 is to be implemented twice: once for $V_{\rm LX}$ and once for $V_{\rm AUX}$ signals paths.

The $V_{\rm LX}$-transition masking circuit consists of three switches Q_1, Q_2, and Q_3, connected to RC-filter inputs. These switches are driven by the signals allowing to anticipate the $V_{\rm LX}$ transitions phases, i.e., allowing to disconnect the filters sufficiently before and reconnect them back sufficiently after the $V_{\rm LX}$ transition. Detection of $V_{\rm LX}$ transitions is driven by signals available in Fig. 1 power stage: CMD_MOS, G_PMOS and G_NMOS

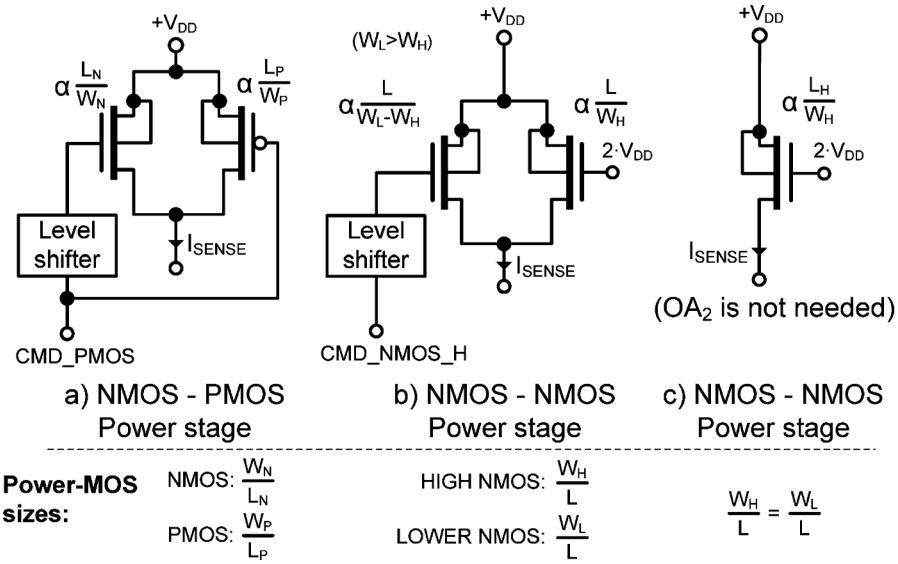

Fig. 13. Variants of the composite-loads for various configurations of the power stages. CMD_PMOS is a digital (sharpened) image of G_PMOS.

(Fig. 6). In particular, triggering of the $V_{\rm LX}$-transition masking circuit is based on the delay of the power-transistor gate buffers, and on the asymmetrical inverters shown in Fig. 12. The use of asymmetrical inverters (with switching point close to PMOS or NMOS $V_{\rm TH}$) allows to detect that power transistors reached sufficient gate voltage to be in stable ohmic region. The switching phases of transistors Q_1–Q_3 are shown in Fig. 6 inset, and are labeled accordingly. It is to be noted that transistors Q_1 and Q_2 contribute to the RC filters input resistances $R_{\rm a}$. In order to ensure linear characteristic of the input RC filters, the sizes of Q_1 and Q_2 are to be chosen so that both transistors exhibit approximately identical (preferably low) channel resistance $R_{\rm ON}$ (i.e., $W_N/W_P = \mu_P/\mu_N$, $\mu_{\rm N}$ and $\mu_{\rm P}$ are electron/hole motilities). Moreover, as pointed out in Fig. 12, the Q_1 and Q_2 are realized as cascade switch such as shown in Fig. 7. The using of cascade switch allows to improve the isolation during the $V_{\rm LX}$ oscillations and during the conduction of power transistors' body diodes.

Since both RC-filters inputs are connected together during the "masking" time T_{Q3}, they integrate identical voltage. The error resulting from this approach is a constant gain deviation being very close to 1, and is analyzed in Section III-D. One important feature of the circuit shown in Fig. 12 is that the inputs of the RC-filter remain in low impedance during the entire conduction cycle. This allows to attenuate the error generated by charge injection and clock feedtrough of Q_1–Q_3 switches, as encountered in the solution shown in Section II-A (Fig. 7). Any residual charge-injection error is removed here thanks to the symmetry of the transition masking circuits, since identical charge injection occurs in $V_{\rm LX}$ and $V_{\rm AUX}$ signal paths. It is also to be noted that transistors Q_1 and Q_2 in $V_{\rm AUX}$ masking circuit (b) create directly the transistors of "ideal" power-stage shown in Fig. 9 (see the final schematic in Fig. 16).

In order to achieve high-accuracy output current measurement, sensing of $V_{\rm ON\_N}$ and $V_{\rm ON\_P}$ is to be provided on the physical terminals of the power transistors (Fig. 1). This allows to prevent the $V_{\rm AVG}$ from the parasitic access-resistance errors. In the silicon implementation, several "representative" sense connection points connected in parallel was integrated, helping to average the non-uniform $V_{\rm DS}$ distribution across the large power-MOS transistor. The sensing points of the power-transistor terminals are highlighted in Fig. 1.

C. Composite Load

As mentioned in Section II-C, the composite load is used to remove the nonlinear term $D\cdot R_{\rm ON\_P}+(1-D)\cdot R_{\rm ON\_N}$ from the composite voltage $V_{\rm AVG}$ (8). Although the concept presented here is focused on the PMOS-NMOS power stage (see Figs. 1 and 9), three configurations of power stage can be envisaged:

a) PMOS-NMOS power stage,
b) Dual NMOS power stage with different high and low side transistors,
c) Dual NMOS power stage with identical high and low side transistors.

In the following, we consider the power-MOS transistors being driven by $V_{\rm GS}$ voltage equal to $V_{\rm DD}$. If this is not the case, the gate-driving signals of the composite-load must be adjusted accordingly (e.g., by a level shifter). The composite load switching is triggered by CMD_PMOS signal (see Section III-D), which is a sharpened image of G_PMOS.

The configurations of the composite load for the particular cases (a), (b), and (c) are shown in Fig. 13. For the case (c), the composite transistor is made of a single NMOS transistor, because (8) becomes linear (i.e., $R_{\rm ON\_N} = R_{\rm ON\_P}$). In this case, the $\rm OA_2$ is not needed, as the voltage across the sense transistor can be regulated by $\rm OA_1$ directly. For the dual-NMOS configuration (b) with different high and low transistors' sizes (for instance, $W_{\rm L} > W_{\rm H}$ which is convenient for $D < 0.5$), the composite load Fig. 13(b) is composed of: (*i*) a transistor $\alpha W_{\rm H}/L$ being continuously in the ohmic region, and (*ii*) a transistor $\alpha(W_{\rm L} - W_H)/L$, which is switched ON when the lower power transistor is activated (i.e., when $\rm CMD\_PMOS = H$). The reason for using one continuously conducting MOS transistor is to reduce the switching noise at the $\rm OA_2$ output.

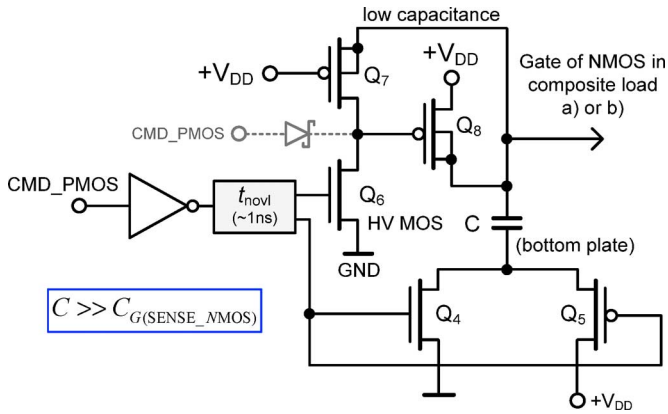

Fig. 14. Voltage doubler level shifter for gate control of NMOS sense-FET.

In the case of the PMOS-NMOS power stage, the composite load shown in Fig. 13(a) is built of NMOS and PMOS sense-FET transistors (see also Figs. 9 and 16). When $\mathrm{CMD\_PMOS} = \mathrm{H}$, the NMOS sense transistor is set in the ohmic region. On the other hand, when $\mathrm{CMD\_PMOS} = \mathrm{L}$ (PMOS power transistor is conducting), the PMOS sense-FET is set in the ohmic region. However, as the source of the sense NMOS transistor is connected to V_{DD}, gate voltage $2 \cdot V_{\mathrm{DD}}$ is required to reach the required ohmic region. This voltage $2 \cdot V_{\mathrm{DD}}$ can be obtained by a simple charge-pump level shifter, shown in Fig. 14. However, it is to be noted that the V_{GS} voltage of the sense-FET NMOS transistor is increased by $V_{\mathrm{DS(ON)}}$. Nevertheless, as $V_{\mathrm{DS(ON)}} \ll V_{\mathrm{GS}}$, we can consider $V_{\mathrm{GS}} = V_{\mathrm{GD}}$, which allows to accurately reproduce the image of the power MOS ON resistance given by (2).

The operation of the level shifter shown in Fig. 14 can be described as follows: when CMD_PMOS is L (power PMOS is conducting), capacitor C is charged to V_{DD} via transistors Q_4 and Q_8. When CMD_PMOS is H (power PMOS is OFF), Q_5 is conducting and connects the bottom plate of C to $+V_{\mathrm{DD}}$. The second terminal of C therefore moves to $2 \cdot V_{\mathrm{DD}}$ and transistor Q_7 become conducting. As the Q_6 is non-conducting, gate of Q_8 shifts to $2 \cdot V_{\mathrm{DD}}$ and also becomes non-conducting. Then, the output remains at $2 \cdot V_{\mathrm{DD}}$, enabling the sense-NMOS to be in ohmic (linear) region. As shown in Fig. 14, a small non-overlap is introduced between the gate signals of $Q_{4,5}$ and Q_6. Together with an optional Schottky diode, this helps to close the transistor Q_8 faster, thus limiting a peak current in Q_8 when Q_5 turns on. In order to obtain accurate multiple $2 \cdot V_{\mathrm{DD}}$, the capacitance in the output node is to be minimized, and the bottom plate of C is to be connected to the low-impedance node Q_4–Q_5. An eventual error in the generated $2 \cdot V_{\mathrm{DD}}$ gate driving voltage can be adjusted by a slight increase of the NMOS sense transistor channel width (the relative error of the voltage doubling ratio is considered independent on V_{DD}).

D. V_{LX}-Transition Error

In the case that the duration of V_{LX} transitions $2 \cdot \mathrm{T_{Q3}}$ (i.e., V_{LX} rise/fall times and dead-times t_{novl}) is non-negligible compared to the conduction cycle period $1/F_{\mathrm{SW}}$, an adjustment of the gain constant $\alpha \cdot G$ given by (12) is to be done. As shown in Figs. 6 and 8, the conduction times of the power transistors differ slightly from the ideal duty cycle ratio value. Particularly, the $\mathrm{T_{ON}}$ and $\mathrm{T_{OFF}}$ times of the Fig. 1 power-stage control signals in CCM mode ($I_{\mathrm{L}} > 0$) can be listed as:

a) CMD_MOS: $\mathrm{T_{ON}} = \mathrm{T_{Q1}} + \mathrm{T_{Q3}}, \mathrm{T_{OFF}} = \mathrm{T_{Q2}} + \mathrm{T_{Q3}}$,
b) G_PMOS: $\mathrm{T_{ON}} = \mathrm{T_{Q1}} + 2 \cdot \mathrm{T_{Q3}}, \mathrm{T_{OFF}} = \mathrm{T_{Q2}}$,
c) G_NMOS: $\mathrm{T_{ON}} = \mathrm{T_{Q1}}, \mathrm{T_{OFF}} = \mathrm{T_{Q2}} + 2 \cdot \mathrm{T_{Q3}}$,

where $\mathrm{T_{ON}}$, $\mathrm{T_{OFF}}$ correspond to the high and low levels of the related signals, and $\mathrm{T_{Q2}} \cong \mathrm{D} \cdot \mathrm{T_{SW}}$, $\mathrm{T_{Q1}} \cong (1 - \mathrm{D}) \cdot \mathrm{T_{SW}}$ (Fig. 6).

It results that the composite average voltage drop V_{AVG} obtained after the V_{LX}-masking circuit can be written more accurately as

$$V_{\mathrm{AVG\_MASK}} = \frac{I_{\mathrm{OUT}}}{T_{\mathrm{SW}}} \{T_{Q1} \cdot R_{ON\_N} + T_{Q2} \cdot R_{ON\_P} + 2T_{Q3} \cdot 0V\} \quad (16)$$

which is close to (8) for $\mathrm{T_{Q3}} \ll \mathrm{T_{SW}}$. As already mentioned, the composite load node is not allowed to be in high impedance. On this account, the sense transistors are driven by a complementary signal, e.g., CMD_PMOS in Fig. 9. It follows that $R_{\mathrm{COMPOSITE}}$ can now be expressed by using the previously mentioned $\mathrm{T_{ON}}$ and $\mathrm{T_{OFF}}$ times as

$$R'_{\mathrm{COMPOSITE}} = \frac{1}{T_{\mathrm{SW}}} \left(T_{\mathrm{OFF}} \frac{R_{ON\_P}}{\alpha} + T_{\mathrm{ON}} \frac{R_{ON\_N}}{\alpha} \right). \quad (17)$$

For $\mathrm{T_{Q3}}$ being not negligible compared to $\mathrm{T_{SW}}$ (e.g., for high switching frequency), the current sensor gain initially given by (12) is to be adjusted to

$$I_{\mathrm{SENSE}} = G \cdot \frac{V_{\mathrm{AVG\_MASK}}}{R'_{\mathrm{COMPOSITE}}} = K\,(\alpha \cdot G \cdot I_{\mathrm{OUT}}) \quad (18)$$

where K is to be close to 1. The function (18) can be easily evaluated in any mathematical software in order to reach the best stability of K. The choice of the composite load driving signal *a*), *b*) or *c*) is mainly given by $R_{\mathrm{ON\_N}}/R_{\mathrm{ON\_P}}$ ratio and by target duty-cycle range.

It is worth mentioning that the best accuracy can be obtained by driving the sense transistors independently by non-complementary signals G_NMOS and G_PMOS. In this case, the value of K is ideally 1. For this purpose, the third transistor conducting during the non-overlapping time of the G_NMOS and G_PMOS signals is to be added to the composite load. This supplementary transistor helps to maintain zero voltage across the sense transistors when both sense-FETs are off. In our particular application, the benefit of this sense transistor driving was negligible (error lowered by ~0.5% over 2.5–4.8 V V_{DD} range) compared to driving by CMD_PMOS.

E. Serial-Fingers Sense-FET

In order to obtain low current measurement ratio $k = I_{\mathrm{SENSE}}/I_{\mathrm{OUT}}$, a very small scaling factor α is to be used. This can result in very low surface of the sense-FET transistors. However, following the general Pelgrom's surface rule [14], the area of the sense-FET transistor is proportional to the quality of matching, or

$$\mathrm{matching} \approx \frac{1}{\sqrt{W \cdot L}}. \quad (19)$$

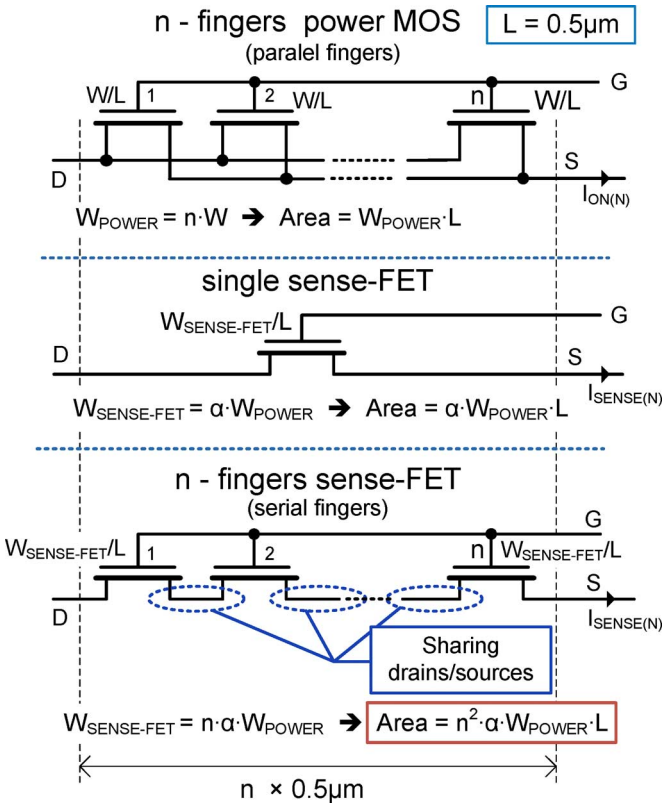

Fig. 15. Serial finger structures of the sense-FET allowing to $\sim n$ times improve the matching with power-MOS transistor.

Accordingly, the low effective surface of the composite load results in a poor matching with the power-MOS transistors.

This effect can be demonstrated on the 2-A PMOS-NMOS power stage presented in the previous section. This power stage was integrated with $W_{\rm P} = 165.888$ mm (n = 6 fingers) and $W_{\rm N}$ of 70.2464 mm (n = 4 fingers) transistors with $L = 0.5\ \mu$m ($W_{\rm P}$ and $W_{\rm N}$ is the total physical length of the power transistors). Required current sensor gain $I_{\rm SENSE}/I_{\rm OUT} = 66\ \mu$ results in $\alpha = 22\ \mu$ ($G = 3$, see (12)). The W/L of the sense-FET transistors is therefore very small, i.e., 3.65/0.5 (μm) for PMOS sense-FET and 1.55/0.5 (μm) for NMOS sense-FET.

In order to increase the effective area $W \cdot L$ of the composite load transistors, the serial fingers layout approach shown in Fig. 15 can be used (see also [15] for another solution based on time averaging). Compared to the layout of the power-transistor in which the fingers are physically connected in parallel (standard multi-finger structure), the sense-FET in the Fig. 15 transistor is also fractionated to the fingers, but these fingers are connected serially. Preferably, these fingers have overlapping source and drain terminals. This allows to generate the layout of the sense-FET with geometry identical to the parallel multi-finger power-MOS transistor. By doing so, all metallic access resistances in the sense-FET and also the mechanical constraints such as the lateral stress STI are accurately reproduced.

Moreover, in order to obtain identical $R_{\rm ON}$ of the serial-fingers sense-FET and its simple sense-FET counterpart, the $W_{\rm SENSE-FET}$ of serial-finger structure is to be increased to $\alpha \cdot {\rm n} \cdot W_{POWER\_N}$ (see (2), Fig. 15). As a result, the channel width of one sense-FET finger is now $\alpha \cdot n \cdot W_{POWER_N} = 4 \times 1.545\ \mu{\rm m} = 6.18\ \mu$m and $\alpha \cdot {\rm n} \cdot W_{\rm POWER_P} = 6 \times 3.65\ \mu{\rm m} = 21.93\ \mu$m, respectively. As n fingers are serially connected, the area of the sense-FET increases n^2 times. This results in $\sim n$ times improvement of the matching between the sense-FETs and power MOS transistors (19).

The weak point of the serial finger structure is a non-equal $V_{\rm GS}$ and $V_{\rm GB}$ voltage for each sense-FET finger. The impact of this inaccuracy is to be verified for every particular implementation. As already mentioned, operations with $V_{\rm DS} \ll V_{\rm G}$ are preferred, which helps to limit this error. Low $V_{\rm DS}$ voltage can be obtained by adjusting the gain G.

F. Current Sensor Integration

In order to provide a global view of the current sensor implemented on the silicon, a schematic including all blocks discussed in the previous section is shown in Fig. 16. In this schematic, we can see two $V_{\rm LX}$-transition masking circuits connected to the sensing nodes of Fig. 1 power stage ($V_{\rm LX\_SENSE(+/-)}, V_{\rm PLUS\_SENSE}, V_{\rm MINUS\_SENSE}$). The outputs of $V_{\rm LX}$-masking circuits are directly connected to the input RC-filters. Here, the high value of the input resistors $R_{\rm a}$ is highlighted. In fact, high value of $R_{\rm a}$ helps to limit the current entering into the filters.

This current is sinked from $V_{\rm LX\_SENSE(+)}$ and $V_{\rm PLUS\_SENSE}$ terminals and therefore contributes to the total quiescent-current budget of the circuit. Moreover, the high value of $R_{\rm a}$ allows to lower the error from the asymmetrical access resistances of sense nodes and asymmetrical $R_{\rm ON}$ of Q_1 and Q_2 described in Section III-B.

It is important that the $V_{\rm DD}$ terminal of the composite load is connected to the identical point as the feedback resistor R_2. By doing so, $V'_{\rm AVG}$ is applied exactly across the composite load, despite any parasitic layout resistances and noise present in $V_{\rm DD}$ voltage. In fact, the positive supply terminal of the operational amplifier and the filter capacitors are also referred to this point. This connection allows to increase the overall noise immunity of the current sensor. Except the composite load transistors where the sizes are given by $\alpha \cdot n \cdot W_{\rm POWER(P,N)}$, all transistor sizes ($Q_1$–$Q_8$) are about 10/0.5 μm. This allows to provide compact low-surface layout of the current sensor. Operational amplifier ${\rm OA}_2$ is realized as a single-stage amplifier, and is shown in Fig. 17. In the design of ${\rm OA}_1$, the output stage must handle the voltage going very close ($\sim$ mV) to $V_{\rm DD}$. This can be obtained by the structure presented in the following Section IV. As already mentioned, the offset voltage of ${\rm OA}_2 V_{\rm OS2}$ is referred to the input of ${\rm OA}_1$ as $V_{\rm OS,IN} = V_{\rm OS1} + V_{\rm OS2}/G$. On this account, the high value of G allows to decrease the requirements on the ${\rm OA}_2$ input offset voltage.

IV. Static Offset Compensation

If the high accuracy of the current sensor is required (namely for the low output currents $I_{\rm OUT}$), the input offset voltage of the operational amplifier ${\rm OA}_1$ is to be designed very low, preferably $V_{\rm OS} < \pm 1$ mV. Obtaining this low $V_{\rm OS}$ can be achieved either by post-fabrication trimming or by using a design technique of the offset reduction. Except for the oversized input differential pair, the offset reduction technique can use any static or dynamic offset compensation. However, except for a higher

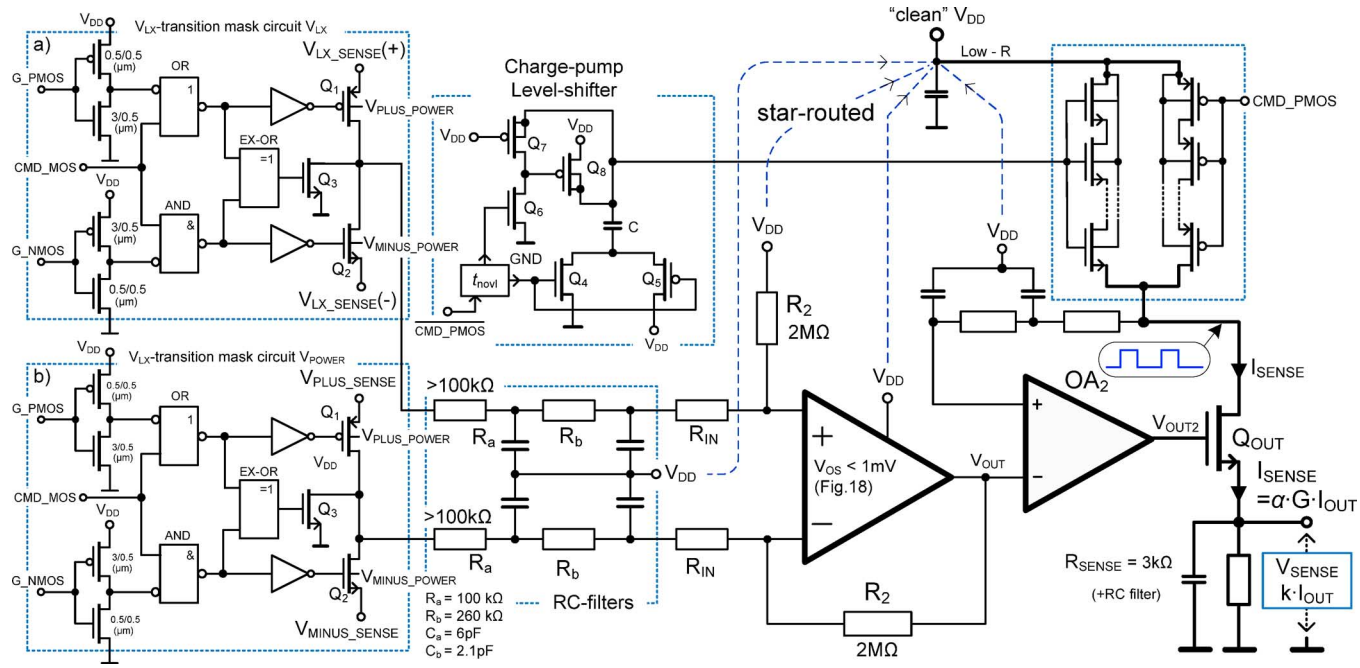

Fig. 16. Detailed view of the integrated current-sensor.

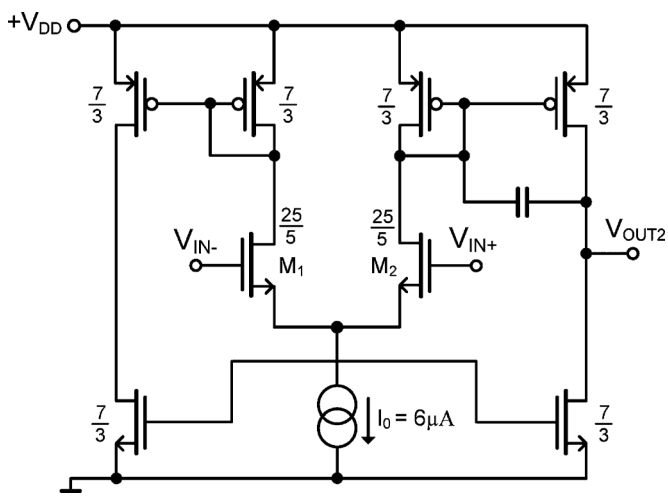

Fig. 17. Single stage operational amplifier OA_2 used to regulate the average voltage V'_{AVG} across the composite load.

temperature drift, the static offset compensation offers the advantage of continuous-time operations of the operational amplifier. Static offset compensation (trimming) usually relies on the injection of an error current into the drain terminal of one of the differential-pair transistors [17], or techniques described, i.e., in [18] or [19].

The method of static offset reduction used in the current sensor is based on the fragmented differential pair shown in Fig. 18. The fragmented differential pair consists of two input transistors: M_2 composed of the fixed amount n of small W/L elementary transistors, and M_1 composed of fixed amount $(n-k)$ of W/L elementary transistors and $(2k-1)$ programmable elementary transistors ($2k$ stands for the amount of the calibration steps). All fixed and programmable elementary transistors therefore have identical (small) W/L. During the calibration, the programmable transistors can be progressively connected to M_1 *via* programmable switches SW_{x}. The channel width of transistor M_1 can thus be modulated by $\pm k \cdot W$ around the ideal (equilibrium) value $n \cdot W$. In the steady state, each conducting elementary transistor drives identical current $I \cong I_0/(2 \cdot n)$. The currents I_1 and I_2 can therefore be adjusted by $2k$ discrete steps of I.

During the calibration, the operational amplifier is configured as an open-loop comparator. This is achieved by disconnecting the inputs from the feedback network and by disconnecting the compensation capacitor. Before calibration, $\mathrm{SW}_{\mathrm{IN1}}$ and $\mathrm{SW}_{\mathrm{IN2}}$ in Fig. 18 connect the input gates together to any fixed voltage. This connection provides ideal zero input differential voltage required for the calibration. In order to avoid an overcurrent of the output transistor Q_{OUT}, the composite load (or Q_{OUT}) is set to high impedance during the calibration.

The calibration starts every time that the circuit turns on (for instance before the soft-start phase of DC-DC converter). At the beginning, all programmable transistors are disconnected and V_{OUT} is in positive saturation. In the following time, the asynchronous counter in the Fig. 18 calibration logic block is incremented with f_{CLK}, until the output V_{OUT} reaches the switching point $V_{\mathrm{DD}}/2$. At this time, the clock signal is stopped and asynchronous counter stores the calibration result for the remaining time of the circuit operations. After calibration, the differential pair gates are connected back to the feedback network and the operational amplifier operates normally without any extra power consumption.

An example of the calibration gain over temperature is shown by Monte-Carlo simulation in Fig. 19. This figure compares the calibrated and non-calibrated offset voltages of identical operational amplifier, obtained with 300 Monte-Carlo runs. It can be seen that the calibrated offset reaches higher temperature drift than its non-calibrated counterpart. The origin of this temper-

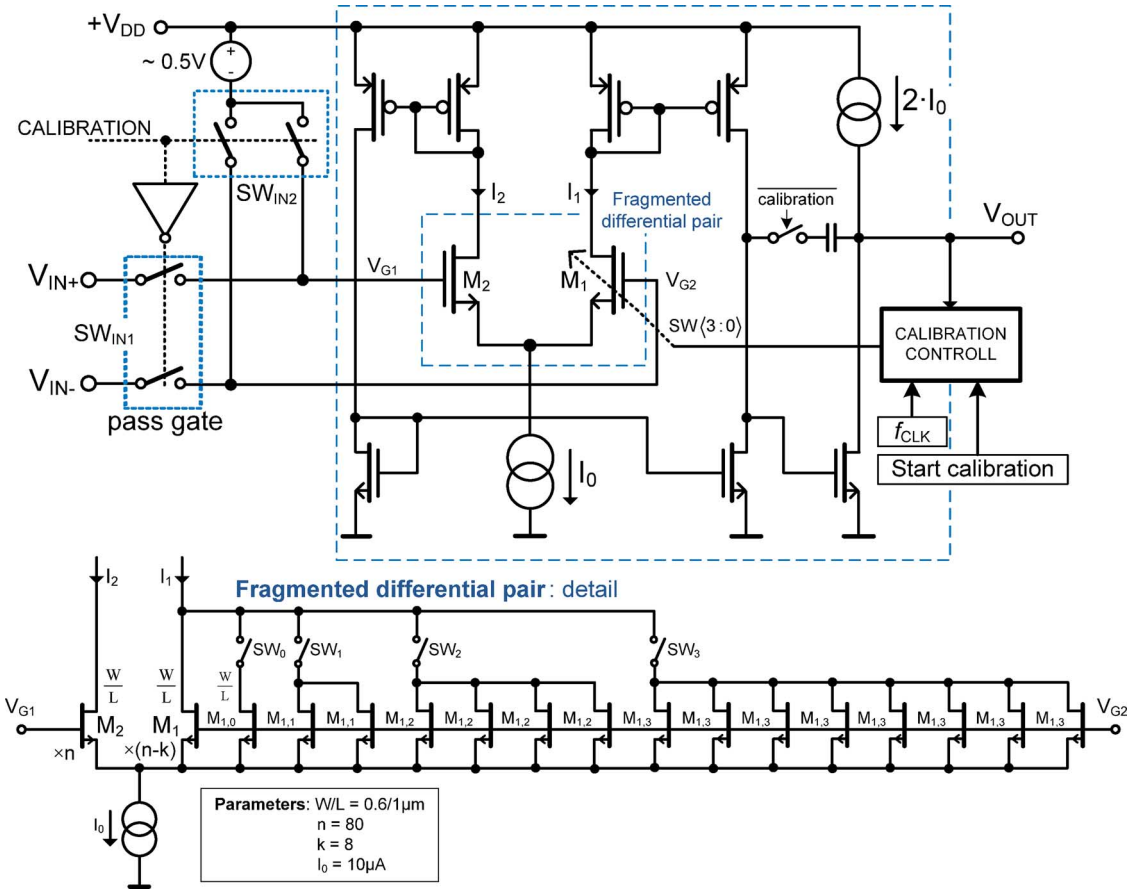

Fig. 18. Detail of the fragmented differential pair used for the static voltage offset compensation of the operational amplifier.

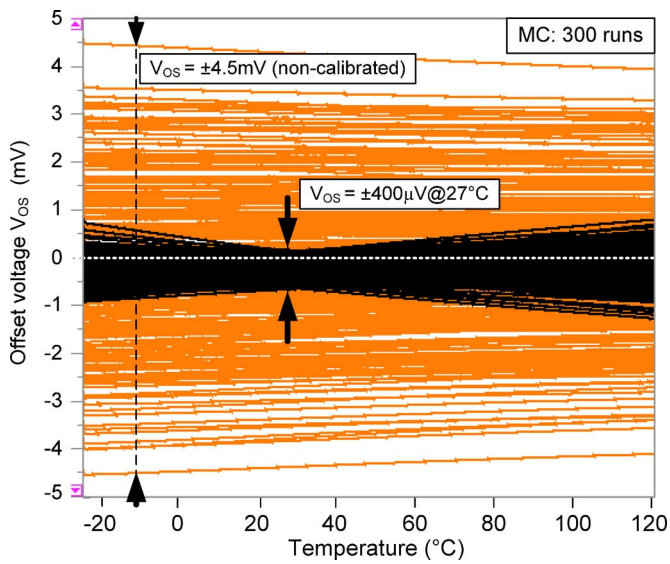

Fig. 19. Comparison of thermal characteristic of compensated and non-compensated operational amplifier offset voltage. Maximum temperature drift of calibrated $V_{\rm OS}$ is $\pm 12\ \mu$V/°C.

ature drift is the different thermal behavior of the $\Delta V_{\rm TH}$ and $\Delta\beta/\beta$ components of the $V_{\rm OS}$ voltage. It can be seen that the lowest offset voltage is obtained at the temperature of calibration, in our case $\rm T = 27°C$.

Due to the high amount of elementary transistors in the Fig. 18 fragmented differential pair, layout in a matrix form was used. Namely, the fixed transistors were placed in the center, and the programmable transistors and auxiliary dummy transistors were placed on the periphery. This matrix array of the differential pair is shown in the current sensor photograph (Fig. 25).

V. Measured Results

The current-sensor circuit from Fig. 16 was integrated in standard 120 nm 5 V ($L_{\rm MIN} = 0.5\ \mu$m) Cu metal CMOS process on $360 \times 82\ \mu$m^2 surface. The 3 kΩ sensing resistance can be configured as integrated internal (calibrated) or discrete external (accurate). The photo of the circuit on the active level is shown in Fig. 25. The current sensor is used for the measurement of the output current of a 2-A step-down DC-DC converter operating at $F_{\rm SW} = 3.2$ MHz, and for driving the current-sharing of the four-phase 8-A DC-DC converter. A new current sensor is also developed in the BCD process for current-sharing control of 4 × 3-A DC-DC converter. The integrated 2-A power stage was built with NMOS-PMOS transistors of $W_{\rm P} = 165.888$ mm and $W_{\rm N} = 70.2464$ mm ($L = 0.5\ \mu$m) resulting in $R_{\rm ON\_P} = 40$ mΩ and $R_{\rm ON\_N} = 28$ mΩ ($V_{\rm DD} = 3.6$ V, $\rm T = 27°C$). The basic performances are summarized in Table I.

The characteristics presented in the following section show the performance of the current sensor as a function of the following parameters: $V_{\rm DD}$ supply voltage 2.5–4.8 V, $V_{\rm OUT}$ =

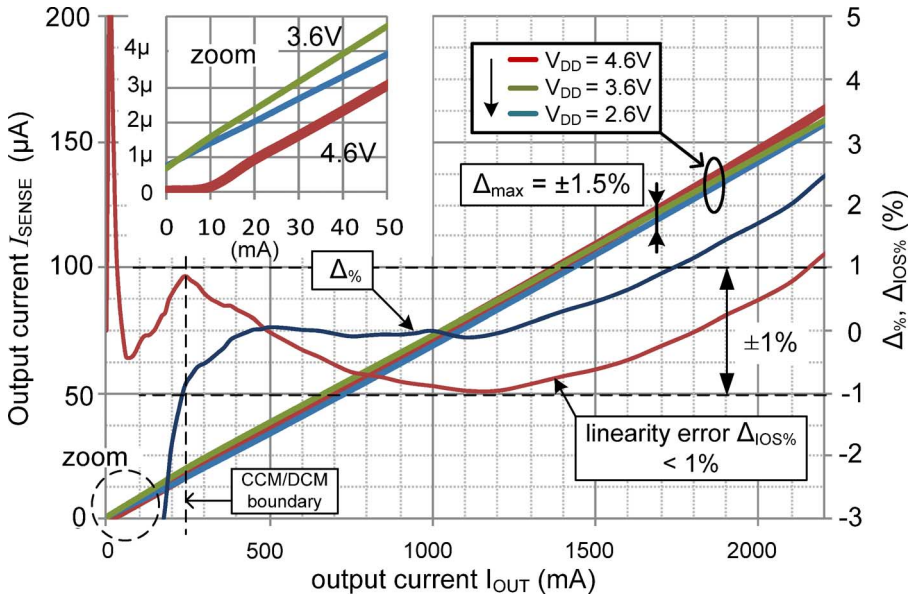

Fig. 20. DC characteristic I_{SENSE} vs. I_{OUT} for $V_{\mathrm{DD}} = 2.6, 3.6$ and 4.6 V, with highlighted errors $\Delta_{\%}$, $\Delta_{\mathrm{IOS}\%}$ for $V_{\mathrm{DD}} = 3.6$ V.

1.8 V, output current range 0–2.2-A, and inductor value $L = 1\ \mu$H and 0.5 μH. Temperature characteristics were measured in $-10°$C to $+120°$C range, and frequency characteristic between 1 to 10 MHz.

A. Output Characteristic, Linearity

The target of the work was to provide linear and absolute value measurement of the DC-DC converter output current I_{OUT}. On this account, the main focus is on the measurements of the static DC characteristics. In order to quantify the accuracy of the current-sensor gain $k = I_{\mathrm{SENSE}}/I_{\mathrm{OUT}}$, the relative error $\Delta_{\%}$ is defined in the following form:

$$\Delta_{\%} = \frac{I_{\mathrm{SENSE}} - kI_{\mathrm{OUT}}}{kI_{\mathrm{OUT}}} \cdot 100\% \tag{20}$$

whereas the value of I_{SENSE} is given ideally by (12). For very low I_{OUT}, the I_{SENSE} is affected by a constant DC current offset I_{OS} of the current sensor so, that $I'_{\mathrm{SENSE}} = I_{\mathrm{OS}} + kI_{\mathrm{OUT}}$. However, for any non-zero offset I_{OS}, the error (20) reaches naturally very high values at low current area. Therefore, in order to evaluate the linearity as the important proof of the concept, measured offset is subtracted from I_{SENSE}. The error removing the DC-offset is then defined as follows:

$$\Delta_{\mathrm{IOS}\%} = \frac{(I_{\mathrm{SENSE}} - I_{\mathrm{OS}}) - kI_{\mathrm{OUT}}}{kI_{\mathrm{OUT}}} \cdot 100\%. \tag{21}$$

The $I_{\mathrm{SENSE}}/I_{\mathrm{OUT}}$ characteristic for $V_{\mathrm{DD}} = 2.5$ V, 3.6 V, and 4.8 V with relative $\Delta_{\%}$ and $\Delta_{\mathrm{IOS}\%}$ errors for $V_{\mathrm{DD}} = 3.6$ V are detailed in Fig. 20.

Here, we can see that high linearity and accurate gain were achieved in a wide output current range. It can be seen that the linearity gain error (21) is within ±1% range for output currents ranging between $I_{\mathrm{OUT}} = 60$ mA and 2.2 A. In the evaluation, the considered I_{OS} generated by current sensor was $I_{\mathrm{OS}} = 670$ nA. This very low I_{OS} value is obtained thanks to the offset calibration of the operational amplifier OA_1 described in Section IV. It is to be noted that the integrated power stage contains an option allowing to reduce the size of the active power transistor for low output currents I_{OUT}. It means that the original W_{P} and W_{N} can be downsized to 20% by setting a control bit. Thanks to this, the accuracy can be extended for low-current area. In this case, the linearity error was obtained below 1% down to $I_{\mathrm{OUT}} = 10$ mA.

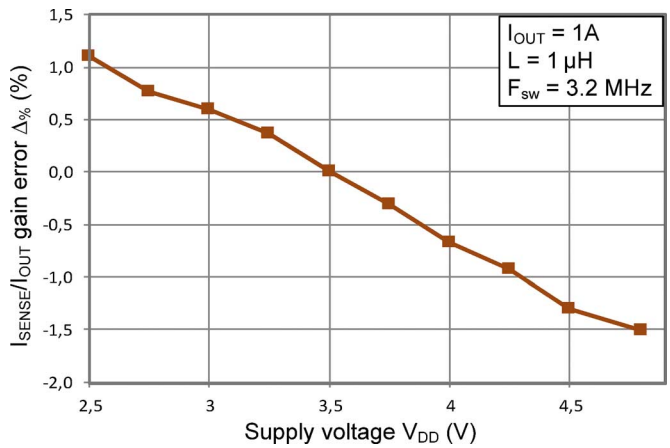

Fig. 21. Relative error of I_{SENSE} in V_{DD} ranging of 2.5 V to 4.8.

The inaccuracy originating from V_{DD} variation is shown in Fig. 21 for $V_{\mathrm{DD}} = 2.5$–4.8 V, and is in ±1.5% range.

A very important result concerns the accuracy obtained between several fabricated samples. From the measurements performed on seven boards, the extracted error of k was ±1%. This accuracy is achieved thanks to the use of the serial fingers composite-load transistors, described in Section III-E, Fig. 15. Relative error $\Delta_{\%}$ (20) together with $I_{\mathrm{SENSE}}/I_{\mathrm{OUT}}$ characteristic resulting from measurements on seven boards is shown in Fig. 22. The measurement was done with an accurate $R_{\mathrm{SENSE}} = 3$ kΩ.

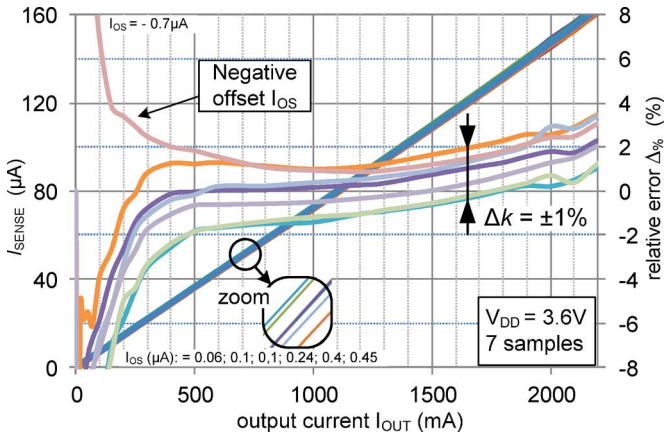

Fig. 22. Mismatch error measured between seven fabricated samples. The variation of I_{OS} is related to the final resolution of the operational amplifier offset compensation.

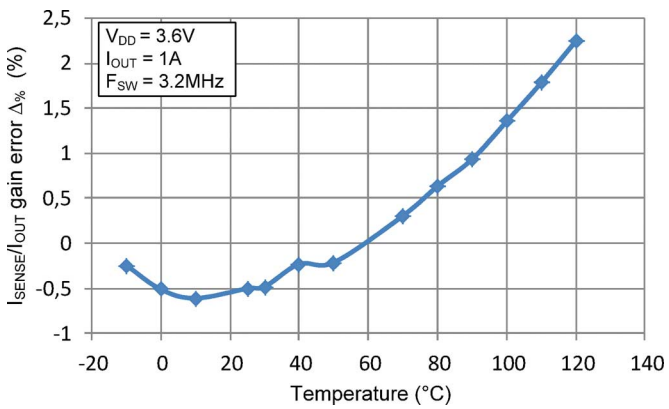

Fig. 23. Relative error of I_{SENSE} vs. temperature.

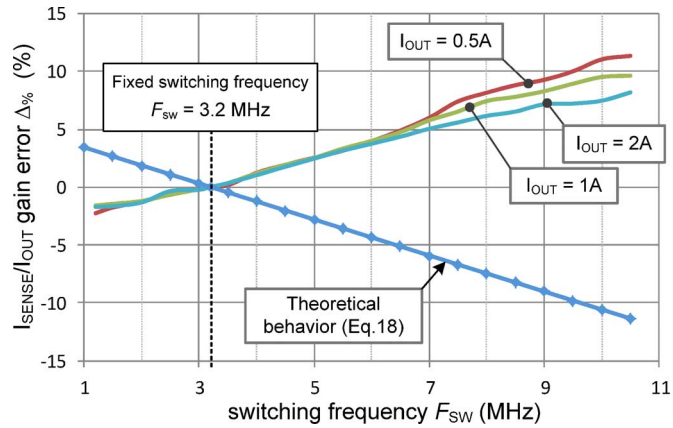

Fig. 24. Relative error of I_{SENSE} vs. switching frequency in the 1–10 MHz range for various I_{OUT}. The discrepancy between theoretical and measured frequency behavior can be removed by improving the isolation of Q_1 and Q_2 switches in Figs. 12 and 17 V_{LX}-masking circuits by cascade switches (Fig. 7). The frequency stability can also be improved by using technique described at the end of Section III-D.

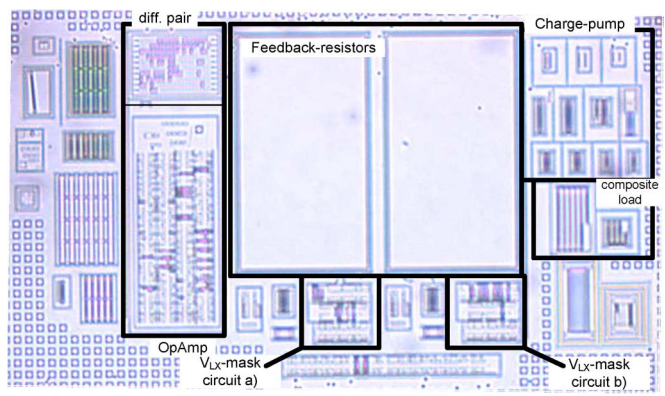

Fig. 25. Photo of the fabricated current sensor at active level, after chemical deprocessing (some polysillicium residual is still present).

An important fact also concerns the influence of the inductor value L. This is fundamental for the use of the current sensor in the current-sharing control of the multi-phase DC-DC converter. The obtained shift of I_{SENSE} was undetectable (0.023%) for inductor values 1 μH and 0.5 μH. Concerning the obtained transient settling time, the time response for 0 to 1-A step of I_{OUT} was approximately 8 μs ($V_{\mathrm{DD}} = 3.6$ V, simulated value).

B. Temperature Behavior

The measurement of the current sensor was done in -10°C to $+120^{\circ}$C range and the relative error $\Delta_{\%}$ is shown in Fig. 23. Due to the inherent matching between the composite load and the power-stage, the system exhibits stability on the order of $\pm 1\%$ within -10 to 80°C range.

C. Frequency Sensitivity

Frequency sensitivity is an important parameter for DC-DC converters operating with variable switching frequency (hysteretic mode, constant ON-time architecture, etc.). The frequency sensitivity of the current-sensor is examined in Section III-D, where the requirement of fast V_{LX} transitions and short dead-time t_{novl} is highlighted. As it can be observed from Fig. 24, the sensing error varies from $+2\%$ to -10% in 1–10 MHz frequency range. However, as the DC-DC converters usually operate in a narrow frequency range, the considered error becomes insignificant (estimated Q_3 conduction intervals are 9 ns (V_{LX} L $\rightarrow$ H) and 6 ns for V_{LX} transition H $\rightarrow$ L). If high accuracy over a large frequency range is required, the method of independent sense transistor driving as mentioned at the end of Section III-D can be used.

In Fig. 24, we can also see that the frequency behavior is opposed to the theoretical one, described by (18). This phenomenon results from the insufficient isolation of the Q_1 and Q_2 transistors in V_{LX}-masking circuit Fig. 12 during the V_{LX}-transitions and body-diode conductions. The cascade switches shown in Fig. 7 were not used in the presented silicon implementation, but are used in the new developed current sensor in the BCD process.

VI. Conclusion

The current sensor circuit presented in this paper enables to measure the output current of the DC-DC converter with a few percentage accuracy, and without the need of any external calibration. This result is obtained thanks to the detailed considerations of various errors, which are treated in this paper. The described circuit enables measurement in PWM mode only, whereas the modifications allowing the operation in PSK mode

can be envisaged. In the final application, measurement in PSK mode was enabled by forcing the DC-DC converter into PWM mode a few μs before the A/D converter sampling. This allows to take advantage of the high current-sensor accuracy down to very low current level, together with the benefits of high power efficiency of the DC-DC converter in PSK mode.

ACKNOWLEDGMENT

The author would like to thank Mr. Salvo Musumeci from STMicroelectronics Catania who developed the current sharing algorithm for the four-phase DC-DC converter, and also helped to improve the presented topic via long calls and face-to-face discussions at the Catania site. The author also would like to thank Bianca Michal for the paper checking and revising, and the anonymous reviewers for deep verification of various technical aspects in the paper.

REFERENCES

[1] H. P. Forghani-Zadeh and G. A. Rincón-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. 2002 Midwest Symp. Circuits and Systems (MWSCAS)*, pp. 577–580.

[2] R. Lenk, "Application bulletin AB-20 optimum current-sensing techniques in CPU converters," Fairchild Semiconductor, Application Note, 1999.

[3] "Current-Sharing Techniques for VRMs," Intersil Corp., Milpitas, CA, USA, Technical Brief TB385.1.

[4] X. Zhou, P. Xu, and F. C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," *IEEE Trans. Power Electronics*, vol. 15, no. 6, pp. 1153–1162, Nov. 2000.

[5] S. Yuvarajan and L. Wang, "Power conversion and control using a current-sensing MOSEFET," in *Proc. 1992 Midwest Symp. Circuits and Systems (MWSCAS)*, pp. 166–169.

[6] Y.-H. Lam, W.-H. Ki, C.-Y. Tsui, and D. Ma, "Integrated 0.9 V charge-control switching converter with self-biased current sensor," in *Proc. 47th Int. Midwest Symp. Circuits and Systems (MWSCAS)*, 2004, vol. 2, pp. II-305–II-308.

[7] J. Mihhailov and S. Strik, "A continuous output current measurement circuit for switching step down DCDC regulator with a single sensing FET," in *Proc. 13th Biennial Baltic Electronics Conf. (BEC2012)*, Tallinn, Estonia, Oct. 3–5, 2012.

[8] E. Dallago, M. Passoni, and G. Sassone, "Lossless current sensing in low-voltage high-current DC/DC modular supplies," *IEEE Trans. Ind. Electron.*, vol. 47, no. 6, pp. 1249–1252, Dec. 2000.

[9] H. P. Forghani-Zadeh and G. A. Rincón-Mora, "An accurate, continuous, and lossless self-learning CMOS current-sensing scheme for inductor-based DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 665–679, Mar. 2007.

[10] G. Eirea and S. R. Sanders, "High precision load current sensing using on-line calibration of trace resistance," *IEEE Trans. Power Electronics*, vol. 23, no. 2, pp. 907–914, Mar. 2008.

[11] R. P. Singh and A. M. Khambadkone, "Giant magneto resistive (GMR) effect based current sensing technique for DC/DC converters," in *Proc. 33rd Annual Conf. IEEE Industrial Electronics Society (IECON)*, 2007.

[12] K. Hajek and J. Sedlacek, *Kmitoctove Filtry* (in Czech). Prague, Czech Republic: B.E.N. Pub., 2002, (see table 3.6, pp. 131).

[13] J. B. Grimbleby, "The ideal averaging filter: Its application and realization," *Radio Electron. Eng.*, vol. 49, 1979.

[14] P. Drennan and C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE J. Solid State Circuits*, vol. 38, no. 3, pp. 450–459, Mar. 2003.

[15] S. Rao, Q. Khan, S. S. Bang, D. Swank, A. Rao, W. McIntyre, and P. K. Hanumolu, "A 1.2-A buck-boost led driver with on-chip error averaged SenseFET-based current sensing technique," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2772–2783, Dec. 2011.

[16] V. Michal, "Peak-efficiency detection and peak-efficiency tracking algorithm for switched-mode DC-DC power converters," *IEEE Trans. Power Electronics*, accepted for publication 01/2014, available online. DOI: 10.1109/TPEL.2014.2304491.

[17] M. Pastre and M. Kayal, *Methodology for the Digital Calibration of Analog Circuits and Systems*. New York: Springer, 2006, (see sec. 3.3, Fig. 77).

[18] K.-L. Wong and C. Yang, "Offset compensation in comparators with minimum input-referred supply noise," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 837–840, May 2004.

[19] K. B. Casper and E. J. Jaussi, "Differential amplifier offset adjustment," U.S. Patent 6,614,301, Sep. 3, 2003.

Vratislav Michal was born in Olomouc, Czech Republic, in 1980. He received the M.S. degree in electrical engineering and control from the Brno University of Technology, Czech Republic, in 2004, and the Ph.D. degree in microelectronics from Supélec, Université Pierre et Marie Curie, Paris, France, in 2009.

He joined ST-Ericsson (now STMicroelectronics) in Grenoble, France, in 2008 as a Postdoctoral Researcher and after as full-time research and IC Design Engineer. He is involved in the R&D of the integrated switched mode power converters for mobile phones and tablet platforms. He is also the author of several patents in this domain. Past and present research activities concern mainly the circuit theory, analog signal processing with a focus on the frequency filters, IC design, and activity on cryogenic electronic as the low temperature amplifiers or superconducting RSFQ logic.

Dr. Michal has received several awards as an early-stage researcher from the Czech government, Brno University of Technology, and Czech Radio Club.