Shengwen **Liang**

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22 Feb 1996, Huaibei, AnHui, China

Bio. I am a Ph.D. Student at State Key Laboratory of Computer Architecture in Institute of Computing Technology of Chinese Academy of Sciences under supervision of Professor Ying Wang and Professor Huawei Li.

Research interests. My Ph.D research work covers a range of issues : **Near-Data Processing, Storage, Accelerator, and Graph Compute**. Currently, I am interesting in Open-Channel SSDs and Graph Compute).

Education

Sep 2016 – Jun 2022 (expected)	**PhD Candidate** in Computer Architecture, *Institute of Computing Technology* (ICT), Beijing State Key Laboratory of Computer System and Architecture *Advisor : Prof. Huawei Li and Ying Wang*
Sep 2012 –Jun 2016	**Bachelor of Microelectronic**, *HeFei University of Technology* (HFUT), HeFei School of electronic science & applied physics (GPA :3.75, Rank 3/98)

Publications

- **Shengwen Liang**, Ying Wang, Youyou Lu, Zhe Yang, Huawei Li, and Xiaowei Li, "Cognitive SSD : A Deep Learning Engine for In-Storage Data Retrieval," In Proceedings of the 2019 USENIX Conference on Usenix Annual Technical Conference (USENIX ATC '19). USENIX Association, USA, 395–410. **(CCF-A)**
- **Shengwen Liang**, Ying Wang, Cheng Liu, Dawen Xu, Huawei Li, Xiaowei Li,"EnGN : An Energy-Efficient Accelerator for Large Graph Neural Networks," in IEEE Transactions on Computers (TC), 2020. **(CCF-A)**
- **Shengwen Liang**, Ying Wang, Cheng Liu, Huawei Li, Xiaowei Li. "InS-DLA : A Deep Learning Accelerator for Near-Data Processing," in IEEE Field-Programmable Logic and Applications (FPL'19), 2019. **(CCF-C)**
- **Shengwen Liang**, Ying Wang, Cheng Liu, Huawei Li, Xiaowei Li, "DeepBurning-GLAn Automated Framework for Generating Graph Neural Network Accelerators," in International Conference On Computer Aided Design (ICCAD'19), 2020.**(CCF-B)**
- Ying Wang, **Shengwen Liang**, Huawei Li, Xiaowei Li, "A None-Sparse Deep Learning Accelerator that Explores the Computation Redundancy in Neural Networks," to appear in IEEE/ACM Proceedings of Design, Automation Conference (DAC'19), 2019. **(CCF-A)**

Projects & Experiences

Dec 2020 – Dec 2020 — Bare-metal deployment solution for Xilinx DPU, ,

- I achieve the bare-metal deployment solution for Xilinx DPU by hacking the execution flow of DPU.
- Source code : github.com/shengwenLeong/Xilinx$_{D}PU_{B}aremetal$

Xilinx DPU | efficientnet-lite

Aug 2020 – Jul 2020 — Low Power Computer Vision Competition FPGA track, ,

- We win the third prize of FPGA track in 2020 Low-Power Computer Vision Challenge using customized efficientnet-lite0 model with tensorflow and Xilinx vitis tools on Ultra96-V2 platform.
- Source code : github.com/shengwenLeong/lpcvc2020_water

Xilinx DPU | efficientnet-lite

Apr 2020 – Jan 2019 — EnGN :An Energy-Efficient Accelerator for Large Graph Neural Networks, ,

- We design a high-throughput accelerator for large graph neural network, which is implemented based on the edge-centric paradigm and supports various large scale GNNs.
- We proposed a graph property aware and ring-edgereduce (RER) dataflow to enable the EnGN to handle a vertex with arbitrary dimension property and high throughput update operations.
- Cycle accurate simulator : github.com/shengwenLeong/Simulator

graph neural network | hardware accelerator

Dec 2016 – July 2018 | **Cognitive SSD : A Deep Learning Engine for In-Storage Data Retrieval, ,**

- We propose and implement Cognitive SSD on Cosmos plus OpenSSD platform (Xilinx Zynq 7045), to enable within-SSD deep learning and graph search by designing and integrating a specialized deep learning and graph search accelerator.
- We employ multi Cognitive SSDs to build a serverless image retrieval system. It can independently respond to data retrieval requests at real-time speed and low energy cost.
- : github.com/Cognitive-SSD/Cognitive-SSD

image retrieval | deep hashing | graph-based ANN search | hardware accelerator | web server

Skills

Programming Skills : **Verilog**, C/C++, Python, LaTeX.
Hardware architecture : *master in* **Solid State Drive architecture, Accelerator design and NVMe protocol**.
familiar with SmartNIC, RDMA and Open-Channel SSD.
Software : *have a certain understanding of* Hardware simulator design, Xilinx Vitis, and QEMU.
Hardware Platform : Zynq, ZynqMPSoC, Cosmos plus OpenSSD, Mellanox BlueField DPU, Bittware 250-SoC.
Software Tools : Gem5, QEMU, Vivado, Vitis, Xilinx PetaLinux.

Honors & Awards

Fall 2020 National Scholarship for Ph.D of University Chinese Academy of Sciences (¥30,000).
Aug 2020 The third prize of FPGA track in 2020 Low-Power Computer Vision Challenge @CVPR (3/19).
Fall 2019 Pacemaker to Merit Student of University Chinese Academy of Sciences.
Spring 2016 Outstanding undergraduate student of HeFei University of Technology.

(last update : 13 Apr. 2017)