SONY

Diagonal 8.92 mm (Type 1/1.8) CMOS Image Sensor with Square Pixel for Color Cameras

IMX178LQJ-C

Description

The IMX178LQJ-C is a diagonal 8.92 mm (Type 1/1.8) CMOS active pixel type image sensor with a square pixel array and 6.44 M effective pixels. This chip operates with analog 2.9 V, digital 1.2 V and interface 1.8 V triple power supply, and has low power consumption.
High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters.
This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Input frequency
  54 MHz or 27 MHz / 74.25 MHz or 37.125 MHz
- ◆Number of recommended recording pixels: 3072 (H) × 2048 (V) approx. 6.29M pixels
- ◆Readout mode

  6M pixels in all-pixel scan mode (3:2)
  5M pixels in each format (4:3 / 5:4 QSXGA / 16:9)
  Horizontal / Vertical 2 × 2 binning mode, Horizontal / Vertical arbitrary cropping mode
  1080p-Full HD readout
  720p-HD readout (2 × 2 binning)
  Vertical/Horizontal direction-normal/inverted readout
- ◆Readout rate

  Maximum frame rate in 5M-pixel readout mode: 12 bit 60 frame/s, 14 bit 30 frame/s
  Maximum frame rate in 6M-pixel all readout mode: 10 bit 59.94 frame/s, 12 bit 29.97 frame/s
- ◆Variable-speed shutter function (resolution 1H units)
- ◆10-bit / 12-bit / 14-bit A/D converter
- ◆CDS/PGA function
  High light Performance mode : 0 dB to 48 dB (step pitch 0.1 dB)
  0 dB to 24 dB:Analog Gain
  24.1 dB to 48 dB: Analog Gain + Digital Gain 0.1 dB to 24 dB
  Low light Performance mode : 3 dB to 51 dB (step pitch 0.1 dB)
  3 dB to 27 dB:Analog Gain
  27.1 dB to 51 dB: Analog Gain + Digital Gain 0.1 dB to 24 dB
- ◆Supports I/O switching

  Low voltage LVDS (150 mVp-p) serial (4 ch / 8 ch / 10 ch switching) DDR output
- ◆Recommended exit pupil distance: –30 mm to –∞

Exmor R

* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.

Device Structure

- ◆ CMOS image sensor
- ◆ Image size, format
  Diagonal 8.92 mm (Type 1/1.8) approx. 6.38 M pixels (3:2)
  Diagonal 7.83 mm (Type 1/2.0) approx. 5.11 M pixels (4:3)
  Diagonal 7.92 mm (Type 1/2.0) approx. 5.32 M pixels (5:4) QSXGA
  Diagonal 8.51 mm (Type 1/1.9) approx. 5.39 M pixels (16:9)
- ◆ Total number of pixels
  3096 (H) × 2094 (V) approx. 6.48 M pixels (3:2)
- ◆ Number of effective pixels
  3096 (H) × 2080 (V) approx. 6.44 M pixels (3:2)
  2616 (H) × 1976 (V) approx. 5.17 M pixels (4:3)
  2584 (H) × 2080 (V) approx. 5.37 M pixels (5:4) QSXGA
  3096 (H) × 1760 (V) approx. 5.45 M pixels (16:9)
- ◆ Number of active pixels
  3089 (H) × 2064 (V) approx. 6.38 M pixels (3:2)
  2609 (H) × 1960 (V) approx. 5.11 M pixels (4:3)
  2577 (H) × 2064 (V) approx. 5.32 M pixels (5:4) QSXGA
  3089 (H) × 1744 (V) approx. 5.39 M pixels (16:9)
- ◆ Number of recommended recording pixels
  3072 (H) × 2048 (V) approx. 6.29 M pixels (3:2)
  2592 (H) × 1944 (V) approx. 5.04 M pixels (4:3)
  2560 (H) × 2048 (V) approx. 5.24 M pixels (5:4) QSXGA
  3072 (H) × 1728 (V) approx. 5.31 M pixels (16:9)
- ◆ Unit cell size
  2.4 µm (H) × 2.4 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixel, rear 0 pixel
  Vertical (V) direction: Front 14 pixels, rear 0 pixel
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings			Unit	Remarks
Supply voltage (analog 2.9 V)	AV_{DD}	–0.3	to	+3.3	V	
Supply voltage (interface 1.8 V)	OV_{DD}	–0.3	to	+3.3	V	
Supply voltage (digital 1.2 V)	DV_{DD}	–0.3	to	+2.0	V	
Input voltage	VI	–0.3	to	OV_{DD} + 0.3	V	Not exceed 3.3 V.
Output voltage	VO	–0.3	to	OV_{DD} + 0.3	V	Not exceed 3.3 V.
Operating guarantee temperature	Topr	–30	to	+85	˚C	
Storage guarantee temperature	Tstg	–40	to	+85	˚C	
Performance guarantee temperature	Tspec	–10	to	+60	˚C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 2.9 V)	AV_{DD}	2.80	2.90	3.00	V
Supply voltage (interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V

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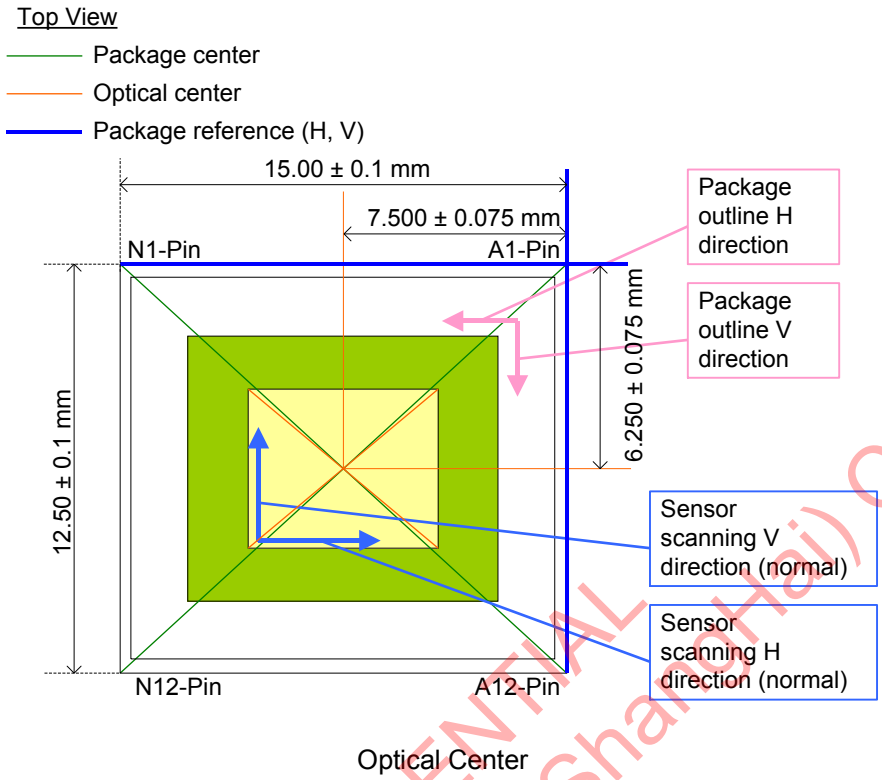
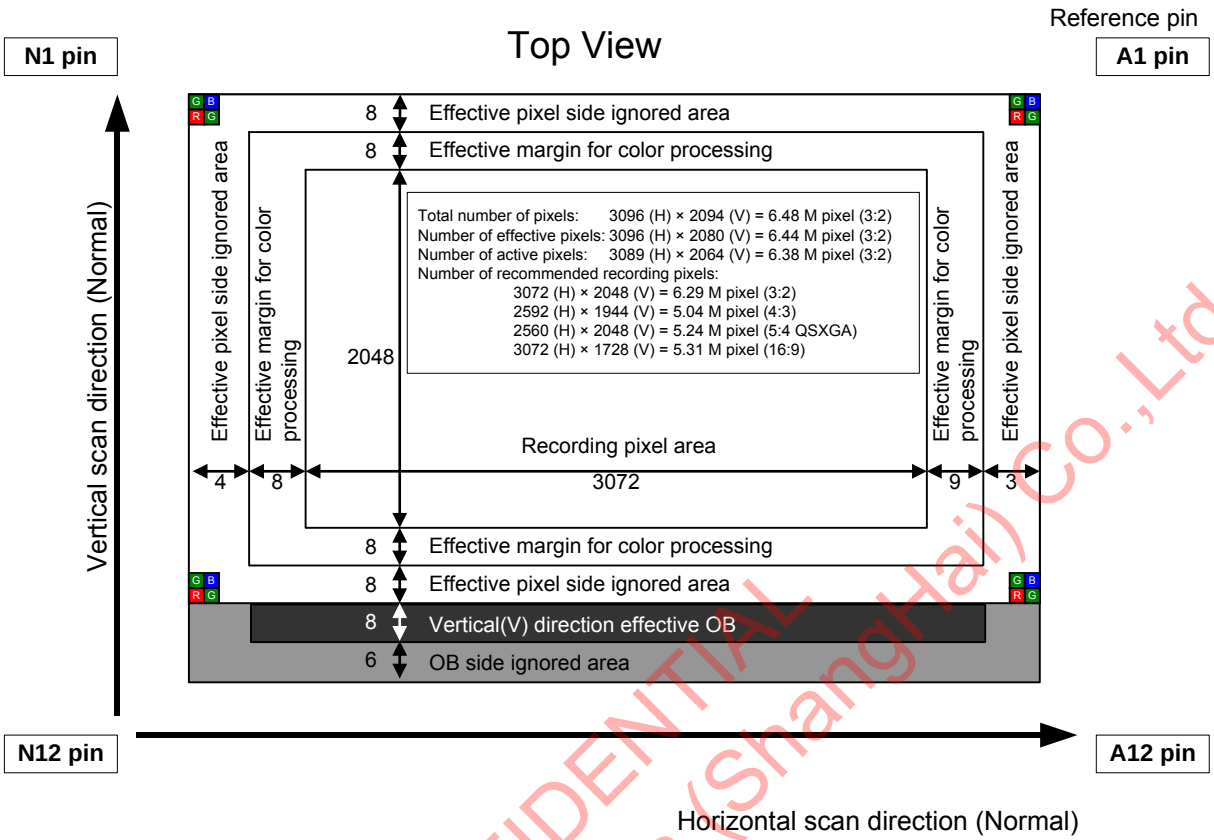
Contents

Chip Center and Optical Center

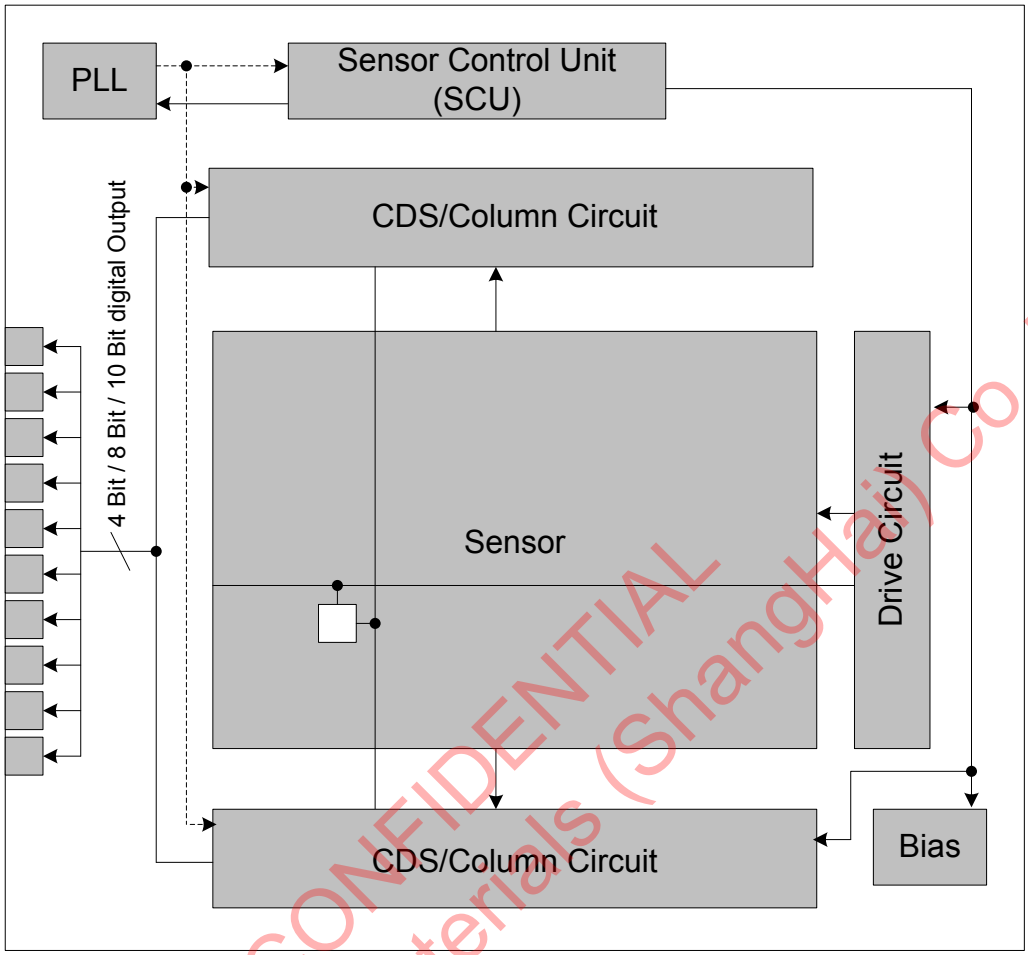


Pixel Array

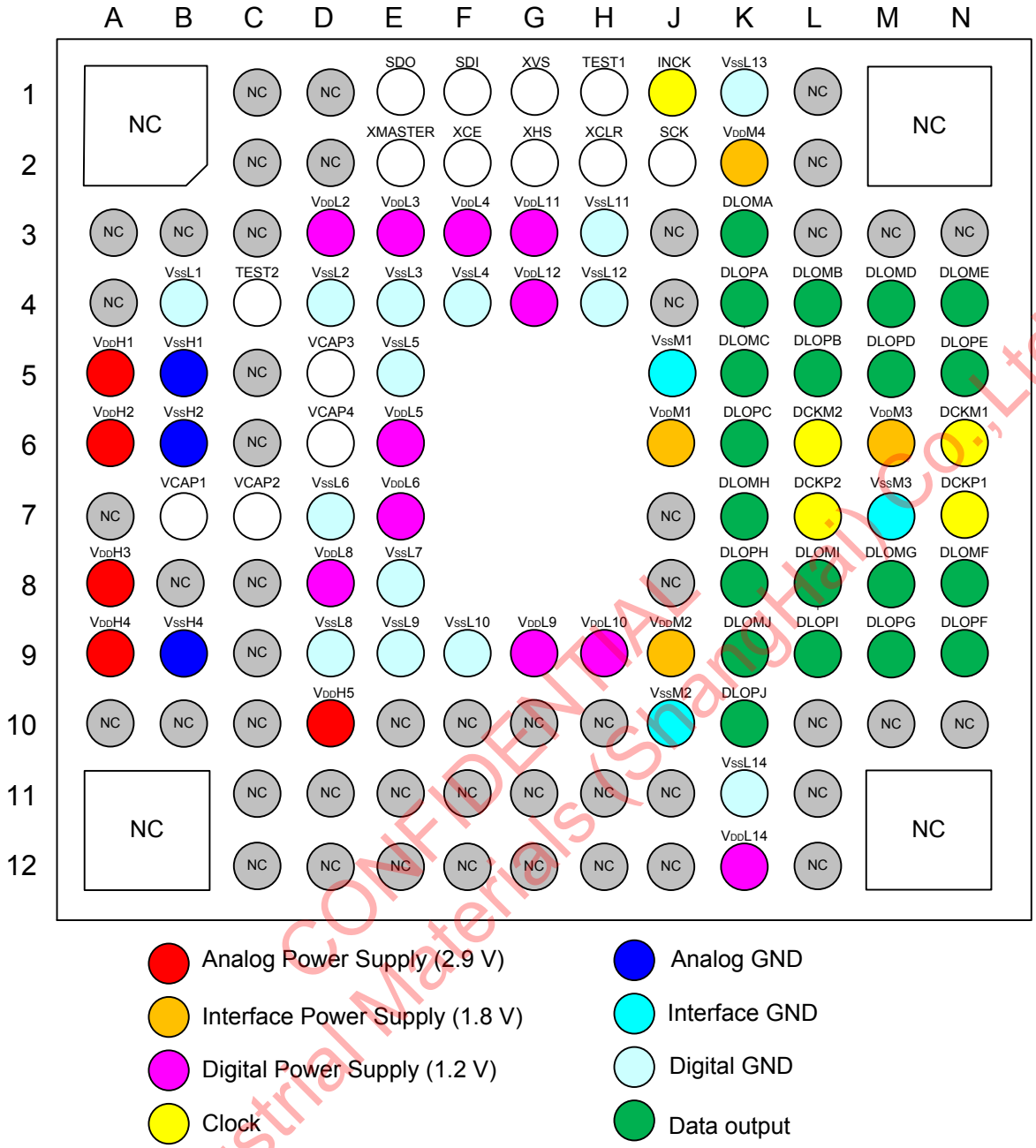


Block Diagram and Pin Configuration

(Top View)



Block Diagram



- Analog Power Supply (2.9 V)
- Interface Power Supply (1.8 V)
- Digital Power Supply (1.2 V)
- Clock
- Analog GND
- Interface GND
- Digital GND
- Data output

Bottom View

Pin Configuration

Pin Description

No.	Pin No.	I/O	Analog /Digital	Symbol	Description
1	A3	—	—	N.C.	—
2	A4	—	—	N.C.	—
3	A5	Power	A	VDDH1	2.9 V power supply
4	A6	Power	A	VDDH2	2.9 V power supply
5	A7	—	—	N.C.	—
6	A8	Power	A	VDDH3	2.9 V power supply
7	A9	Power	A	VDDH4	2.9 V power supply
8	A10	—	—	N.C.	—
9	B3	—	—	N.C.	—
10	B4	GND	D	VSSL1	1.2 V GND
11	B5	GND	A	VSSH1	2.9 V GND
12	B6	GND	A	VSSH2	2.9 V GND
13	B7	O	A	VCAP1	Reference pin (Connect to a 1 µF capacitor to GND)
14	B8	—	—	N.C.	—
15	B9	GND	A	VSSH4	2.9 V GND
16	B10	—	—	N.C.	—
17	C1	—	—	N.C.	—
18	C2	—	—	N.C.	—
19	C3	—	—	N.C.	—
20	C4	O	D	TEST2	Test output Leave open.
21	C5	—	—	N.C.	—
22	C6	—	—	N.C.	—
23	C7	O	A	VCAP2	Reference pin (Connect to a 0.1 µF capacitor to GND)
24	C8	—	—	N.C.	—
25	C9	—	—	N.C.	—
26	C10	—	—	N.C.	—
27	C11	—	—	N.C.	—
28	C12	—	—	N.C.	—
29	D1	—	—	N.C.	—
30	D2	—	—	N.C.	—
31	D3	Power	D	VDDL2	1.2 V power supply
32	D4	GND	D	VSSL2	1.2 V GND
33	D5	O	A	VCAP3	Reference pin (Connect to a 1 µF capacitor to GND)
34	D6	O	A	VCAP4	Reference pin (Connect to a 1 µF capacitor to GND)
35	D7	GND	D	VSSL6	1.2 V GND
36	D8	Power	D	VDDL8	1.2 V power supply
37	D9	GND	D	VSSL8	1.2 V GND
38	D10	Power	A	VDDH5	2.9 V power supply
39	D11	—	—	N.C.	—
40	D12	—	—	N.C.	—

No.	Pin No.	I/O	Analog /Digital	Symbol	Description
41	E1	O	D	SDO	4-wire serial interface SDO
42	E2	I	D	XMASTER	Master/slave mode switching (Slave Mode: High, Master Mode: Low)
43	E3	Power	D	VDDL3	1.2 V power supply
44	E4	GND	D	VSSL3	1.2 V GND
45	E5	GND	D	VSSL5	1.2 V GND
46	E6	Power	D	VDDL5	1.2 V power supply
47	E7	Power	D	VDDL6	1.2 V power supply
48	E8	GND	D	VSSL7	1.2 V GND
49	E9	GND	D	VSSL9	1.2 V GND
50	E10	—	—	N.C.	—
51	E11	—	—	N.C.	—
52	E12	—	—	N.C.	—
53	F1	I	D	SDI	4-wire serial interface SDI
54	F2	I	D	XCE	4-wire serial interface XCE
55	F3	Power	D	VDDL4	1.2 V power supply
56	F4	GND	D	VSSL4	1.2 V GND
57	F9	GND	D	VSSL10	1.2 V GND
58	F10	—	—	N.C.	—
59	F11	—	—	N.C.	—
60	F12	—	—	N.C.	—
61	G1	I/O	D	XVS	Vertical Sync pulse
62	G2	I/O	D	XHS	Horizontal Sync pulse
63	G3	Power	D	VDDL11	1.2 V power supply
64	G4	Power	D	VDDL12	1.2 V power supply
65	G9	Power	D	VDDL9	1.2 V power supply
66	G10	—	—	N.C.	—
67	G11	—	—	N.C.	—
68	G12	—	—	N.C.	—
69	H1	I	D	TEST1	Test input Connect to 1.8 V power supply.
70	H2	I	D	XCLR	(System clear: Normal: High, clear: Low)
71	H3	GND	D	VSSL11	1.2 V GND
72	H4	GND	D	VSSL12	1.2 V GND
73	H9	Power	D	VDDL10	1.2 V power supply
74	H10	—	—	N.C.	—
75	H11	—	—	N.C.	—
76	H12	—	—	N.C.	—
77	J1	I	D	INCK	Clock input
78	J2	I	D	SCK	4-wire serial interface SCK
79	J3	—	—	N.C.	—
80	J4	—	—	N.C.	—
81	J5	GND	D	VSSM1	1.8 V GND
82	J6	Power	D	VDDM1	1.8 V power supply
83	J7	—	—	N.C.	—
84	J8	—	—	N.C.	—
85	J9	Power	D	VDDM2	1.8 V power supply

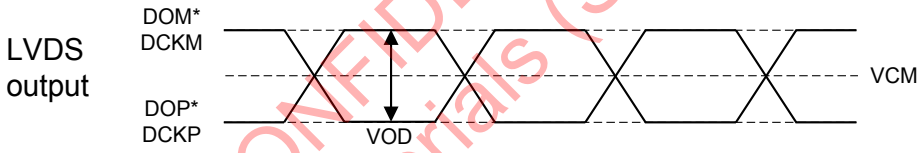
No.	Pin No.	I/O	Analog /Digital	Symbol	Description
86	J10	GND	D	VSSM2	1.8 V GND
87	J11	—	—	N.C.	—
88	J12	—	—	N.C.	—
89	K1	GND	D	VSSL13	1.2 V GND
90	K2	Power	D	VDDM4	1.8 V power supply
91	K3	O	D	DLOMA	Low voltage LVDS serial output (Data)
92	K4	O	D	DLOPA	
93	K5	O	D	DLOMC	Low voltage LVDS serial output (Data)
94	K6	O	D	DLOPC	
95	K7	O	D	DLOMH	Low voltage LVDS serial output (Data)
96	K8	O	D	DLOPH	
97	K9	O	D	DLOMJ	Low voltage LVDS serial output (Data)
98	K10	O	D	DLOPJ	
99	K11	GND	D	VSSL14	1.2 V GND
100	K12	Power	D	VDDL14	1.2 V power supply
101	L1	—	—	N.C.	—
102	L2	—	—	N.C.	—
103	L3	—	—	N.C.	—
104	L4	O	D	DLOMB	Low voltage LVDS serial output (Data)
105	L5	O	D	DLOPB	
106	L6	O	D	DCKM2	Low voltage LVDS serial output (Clock)
107	L7	O	D	DCKP2	Outputs the same clock signal as DCKM1/P1 by setting register STBDCK2 = 0d, DCK2EN = 1d.
108	L8	O	D	DLOMI	Low voltage LVDS serial output (Data)
109	L9	O	D	DLOPI	
110	L10	—	—	N.C.	—
111	L11	—	—	N.C.	—
112	L12	—	—	N.C.	—
113	M3	—	—	N.C.	—
114	M4	O	D	DLOMD	Low voltage LVDS serial output (Data)
115	M5	O	D	DLOPD	
116	M6	Power	D	VDDM3	1.8 V power supply
117	M7	GND	D	VSSM3	1.8 V GND
118	M8	O	D	DLOMG	Low voltage LVDS serial output (Data)
119	M9	O	D	DLOPG	
120	M10	—	—	N.C.	—
121	N3	—	—	N.C.	—
122	N4	O	D	DLOME	Low voltage LVDS serial output (Data)
123	N5	O	D	DLOPE	
124	N6	O	D	DCKM1	Low voltage LVDS serial output (Clock)
125	N7	O	D	DCKP1	
126	N8	O	D	DLOMF	Low voltage LVDS serial output (Data)
127	N9	O	D	DLOPF	
128	N10	—	—	N.C.	—

* N.C. pins in the table above should be left open on the board.

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx	AV_{DD}	—	2.80	2.90	3.00	V
	Interface	VDDMx	OV_{DD}	—	1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}	—	1.10	1.20	1.30	V
Interface Input voltage		XHS XVS XCLR INCK XMASTER SCK SDI XCE	VIH	XVS/XHS In slave mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Interface Output voltage		DLOPx DLOMx DCKPx DCKMx	VCM	Low-voltage LVDS (termination resistance: 100 Ω)	—	OV_{DD}/2	—	mV
			VOD		100	150	200	mV
		XHS XVS SDO	VOH	XVS/XHS In master mode	OV_{DD} - 0.4	—	—	V
			VOL		—	—	0.4	V



Power Consumption

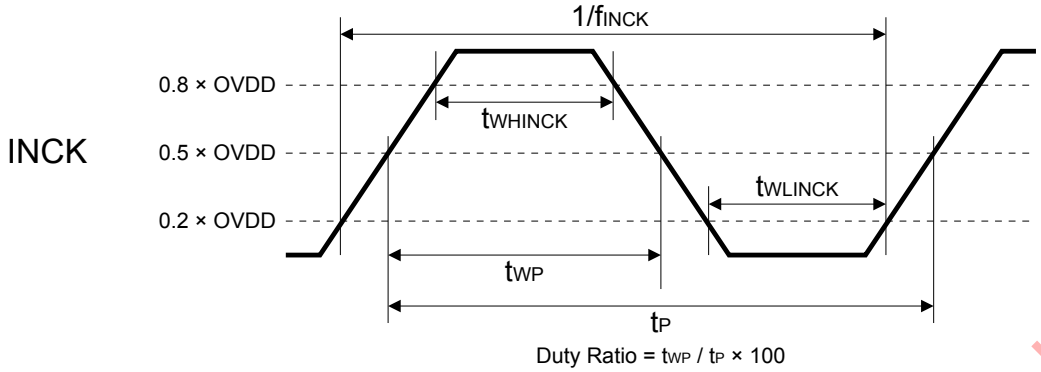
Item	Pin	Symbol	Typ.	Max.	Unit
Operating current (All Pixel Scan mode ADC = 14 bit LVDS = 10 ch)	VDDH	IAV_{DD}	91	121	mA
	VDDM	IOV_{DD}	21	26	mA
	VDDL	IDV_{DD}	137	197	mA
Standby current	VDDH	IAV_{DD}_STB	—	0.1	mA
	VDDM	IOV_{DD}_STB	—	0.1	mA
	VDDL	IDV_{DD}_STB	—	9.5	mA

Operating current:
(Typical value condition) : Supply voltage 2.9 V / 1.8 V / 1.2 V, Tj = 25 ˚C
(Typical value condition) : Supply voltage 3.0 V / 1.9 V / 1.3 V, Tj = 60 ˚C,
Worst state of internal circuit operating current consumption.

Standby: current:
(Maximum value condition) : Supply voltage 3.0 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK = 0 V,
In the light-obstructed state

AC Characteristics

Master clock (INCK)

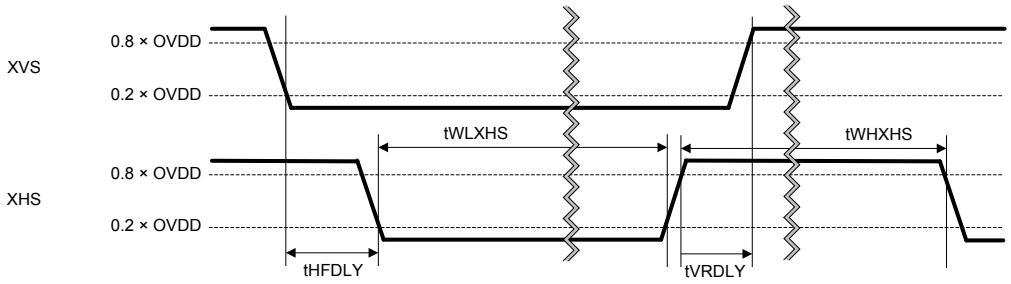


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK Low level width	t_{WLINCK}	4	—	—	ns	
INCK High level width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

* The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (XMASTER = High)

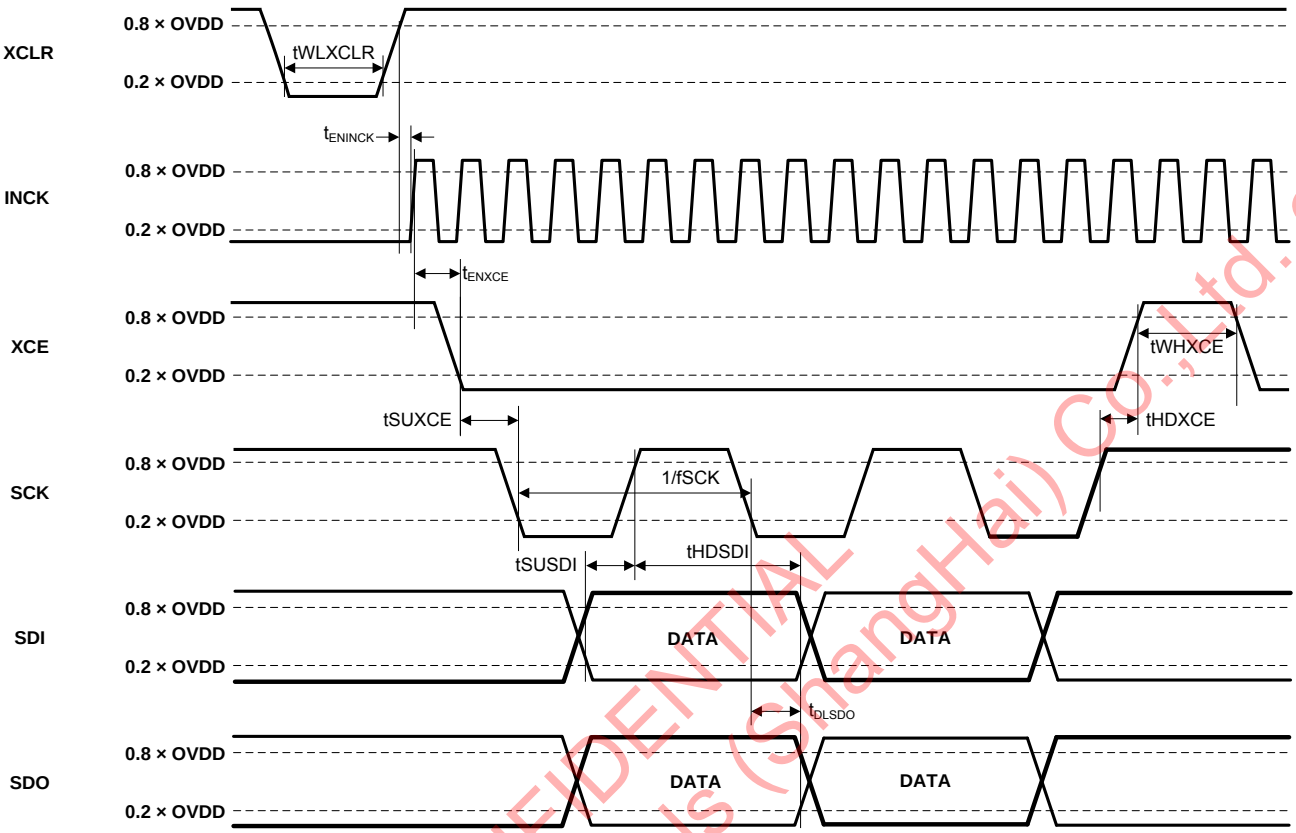


Item	Symbol	Min.	Typ.	Max.	Unit
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns
XVS-XHS fall width	t_{HFDLY}	0	—	—	ns
XHS-XVS rise width	t_{VRDLY}	0	—	—	ns

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

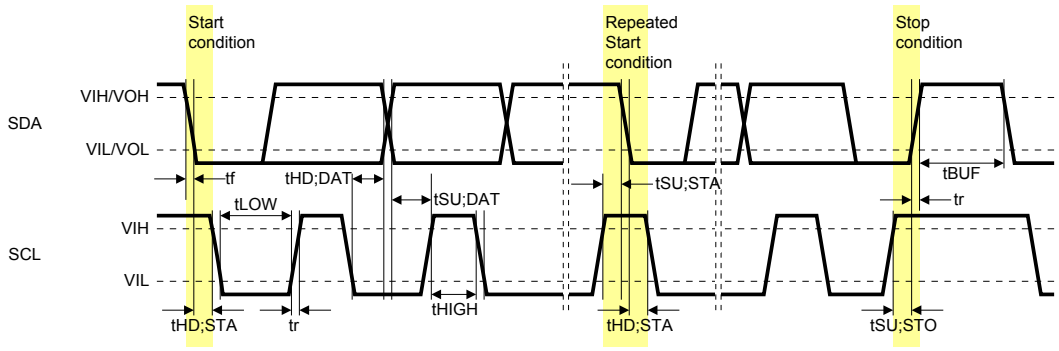
Serial Communication

4-wire serial



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
INCK effective margin	t_{ENINCK}	0	—	—	μs	
XCE effective margin	t_{ENXCE}	20	—	—	μs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output hold time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C serial communication operating specification

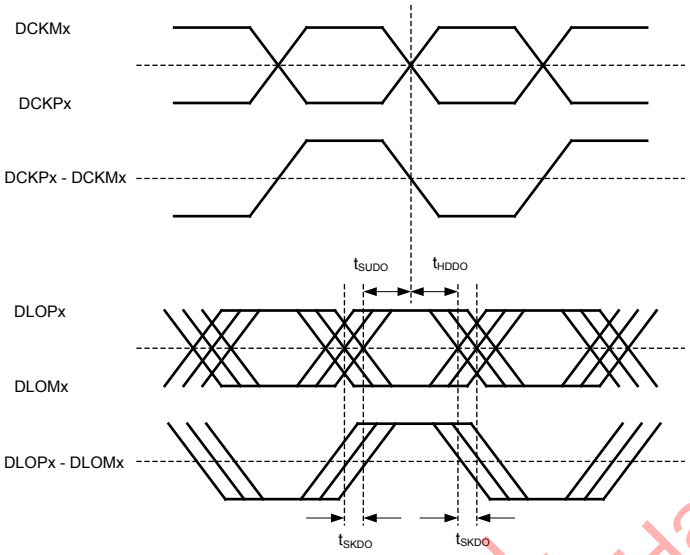
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	VIL	-0.3	—	0.3 × OVDD	V	
High level input voltage	VIH	0.7 × OVDD	—	1.9	V	
Low level output voltage	VOL2	0	—	0.2 × OVDD	V	OVDD < 2 V, Sink 3 mA
High level output voltage	VOH	0.8 × OVDD	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF 0.7 × OVDD – 0.3 × OVDD
Input current	Ii	-10	—	10	μA	0.1 × OVDD – 0.9 × OVDD
Capacitance for SCK (SCL) / SDI (SDA)	Ci	—	—	10	pF	

I²C serial communication AC timing

Item	Symbol	Min.	Typ.	Max.	Unit
SCLclock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs
SCLclockLowperiod	t_{LOW}	1.3	—	—	μs
SCLclockHighperiod	t_{HIGH}	0.6	—	—	μs
Setup time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs
Data setup time	$t_{SU;DAT}$	100	—	—	ns
SDA-SCLrise time	t_r	—	—	300	ns
SDA-SCLfall time	t_f	—	—	300	ns
Setup time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs

DCKPx/DCKMx, DLOPx/DLOMx

Low voltage LVDS DDR output



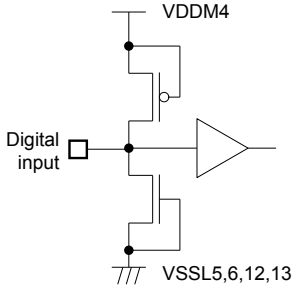
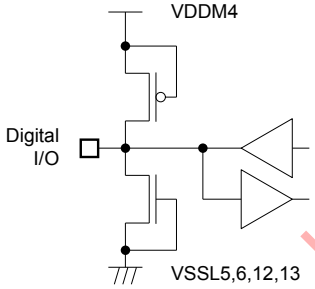
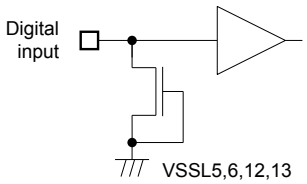
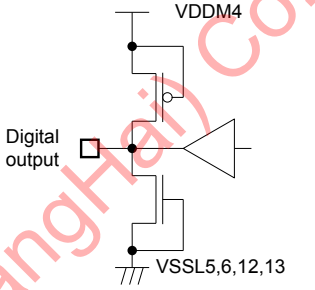
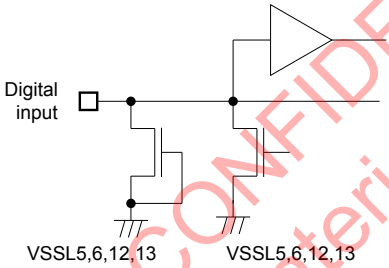
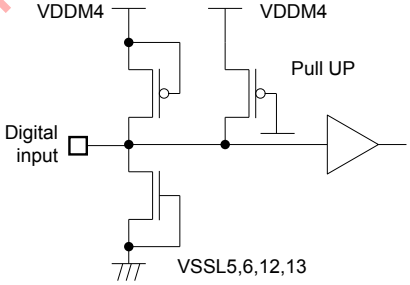
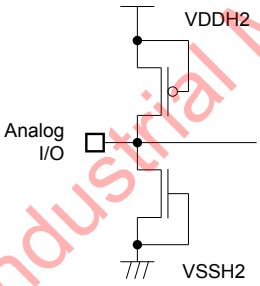
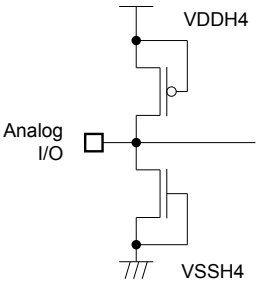
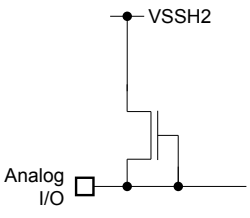
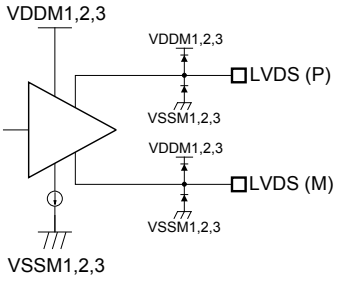
Serial Output

(Output load capacitance: 8 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCKPclock duty	—	40	50	60	%	DCK freq = 297 MHz (Max.)
DLOskew	t_{SKDO}	—	—	400	ps	Data Rate 297 MHz DDR
DLOsetup time	t_{SUDO}	400	—	—	ps	Data Rate 297 MHz DDR
DLOhold time	t_{HDDO}	400	—	—	ps	Data Rate 297 MHz DDR

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK XMASTER XCE		XVS XHS	
XCLR		SDO TEST2	
SDI SCK		TEST1	
VCAP1		VCAP2	
VCAP3 VCAP4		DLOPx DLOMx DCKPx DCKMx	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

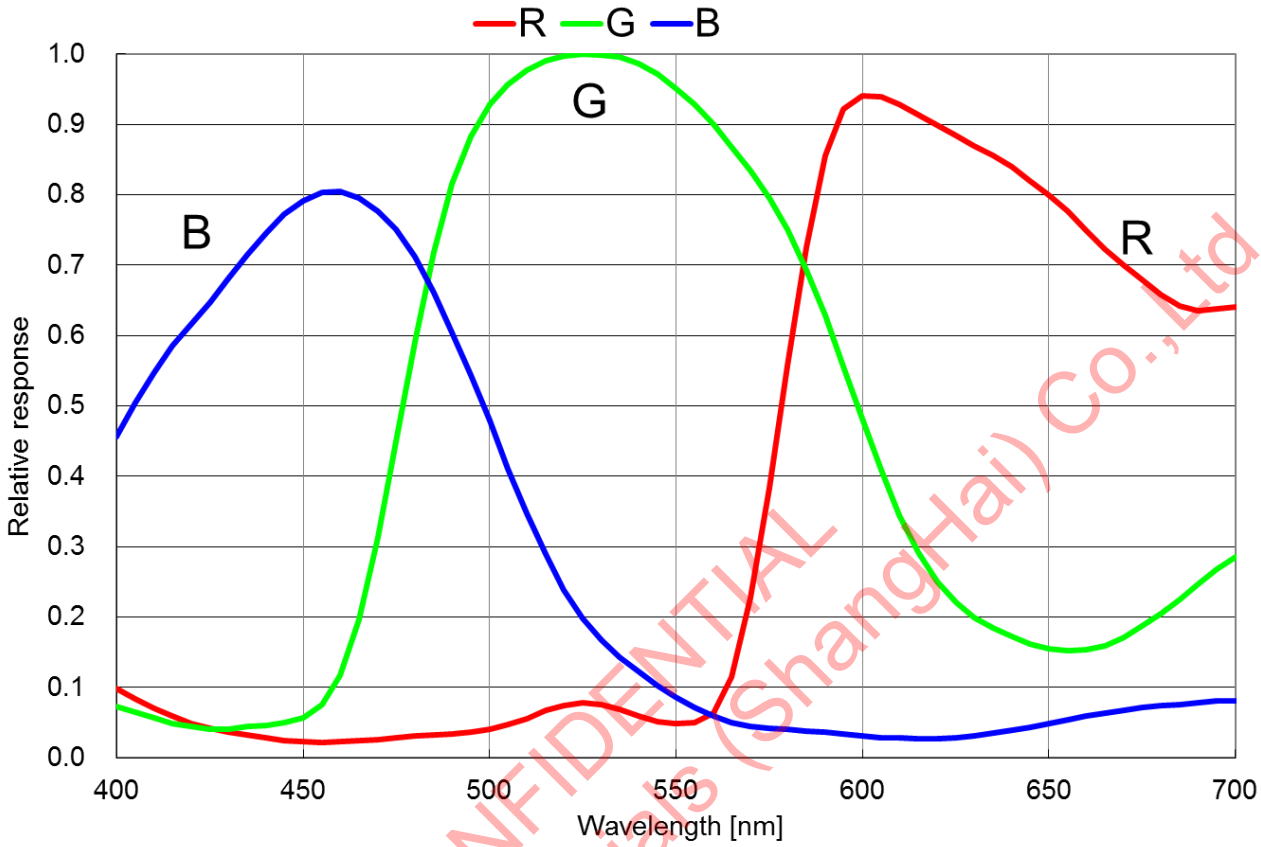


Image Sensor Characteristics

(AVDD = 2.9 V, OVDD = 1.8 V, DVDD = 1.2 V, All-pixel scan mode, AD: 12 bit, Tj = 60 ˚C, Gain = 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	1525 (370)	1751 (425)	—	Digit (mV)	1	1/30 s integration
Sensitivity ratio	R/G	RG	0.38	—	0.53	—	2	
	B/G	BG	0.35	—	0.50	—		
Saturation		Vsat2D	3895 (945)	—	—	Digit (mV)	3	Zone 0 to II'
Video signal shading		SH01	—	—	20	%	4	Zone 0, I
		SH2D	—	—	25	%		Zone 0 to II'
Dark signal		Vdt	—	—	0.61 (0.15)	Digit (mV)	5	1/30 s integration
Dark signal shading		ΔVdt	—	—	0.62 (0.15)	Digit (mV)	6	1/30 s integration
Line crawl R		Lcr	—	—	6	%	7	
Line crawl B		Lcb	—	—	6	%		
Lag		Lag	—	—	0.50	%	8	

Note) 1. Converted value into mV using 1Digit = 0.0607 mV for 14-bit output,
1Digit = 0.2426 mV for 12-bit output and
1Digit = 0.9704 mV for 10-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.

Zone Definition of Image Sensor Characteristics

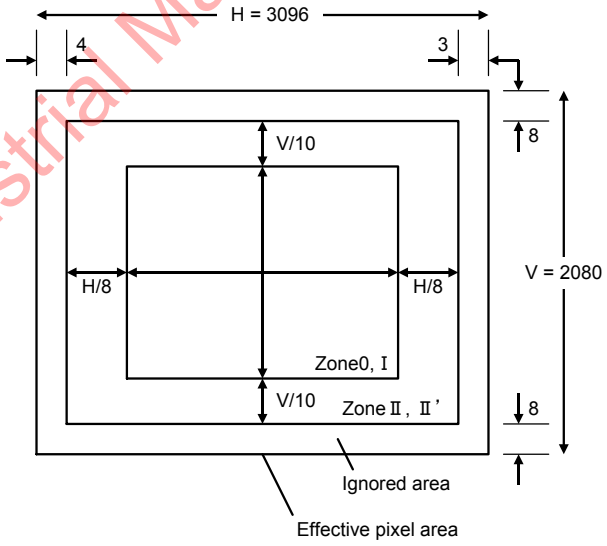


Image Sensor Characteristics Measurement Method

Measurement conditions

In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal
output of the measurement system.

Color coding of this image sensor and readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gb and Gr denote the G signals on the same line as the B signal and the R signal, respectively. Gb signal and B signal lines and R signal and Gr signal lines are output successively.

R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   S = (VGr + VGb) / 2 × 100 / 30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the value of the Gr and Gb signal outputs to 425 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 425 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 425 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 425 × 100 [%]

5. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

6. Dark signal shading
   After the measurement item 5, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

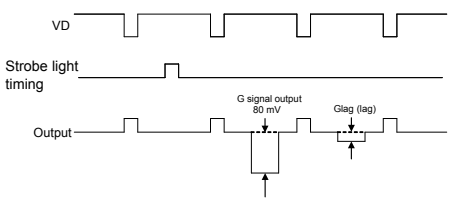
   ΔVdt = Vdmax – Vdmin [mV]

7. Line crawl
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Grsignal output to 425 mV, insert R and B filters and measure the difference between G signal lines (ΔGlr, ΔGlb [mV]) as well as the average values of the G signal outputs (Gar, Gab). Substitute the values into the following formula.

   Lci = (ΔGli / Gai) × 100 [%] (i = r,b)

8. Lag
   Adjust the G signal output value generated by strobe light to 80 mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Glag), and substitute the value into the following formula.

   Lag = (Glag / 80) × 100 [%]



Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

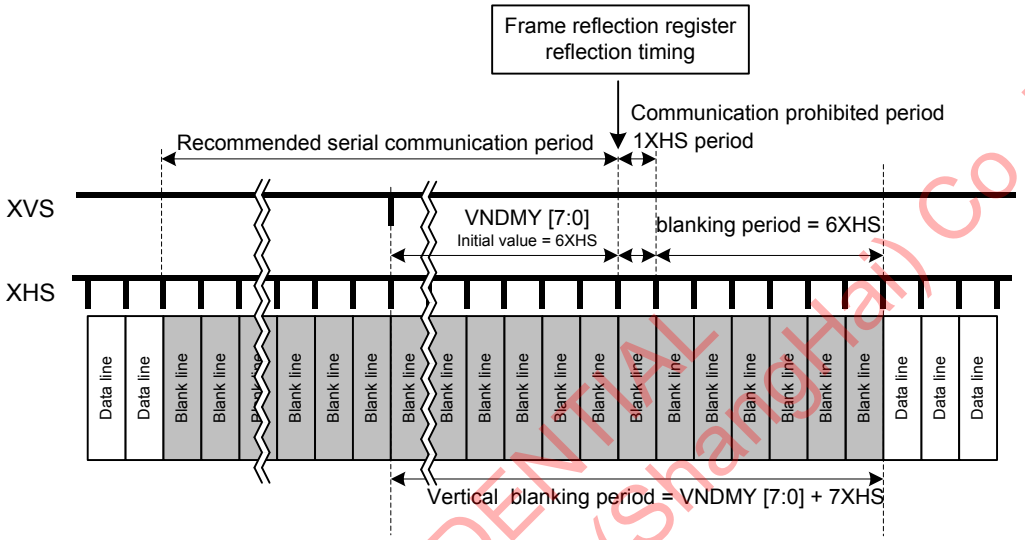
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	02h: Write to the CID = 02h register 03h: Write to the CID = 03h register 04h: Write to the CID = 04h register 05h: Write to the CID = 05h register 82h: Read from the CID = 02h register 83h: Read from the CID = 03h register 84h: Read from the CID = 04h register 85h: Read from the CID = 05h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing

Perform serial communication in sensor standby mode or within in the period which is set by VNDMY [7:0] period after the falling edge of XVS from the blanking line output start time after valid line of one frame is finished. The default value of VNDMY [7:0] is 6H. For the registers marked "V" in the item of Update timing, when the communication is performed in the communication period shown in the figure below they are updated by frame update timing.
For the registers noted Immediately in the item of Update timing, the settings are updated when the communication is performed. (For the immediate update registers other than STANDBY, STBEXPL,STBLOGIC, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.)



Register Write and Read

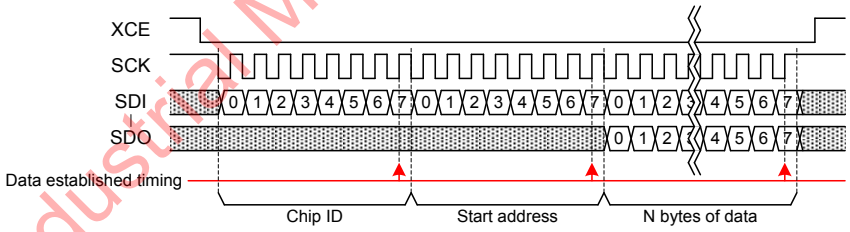
◆Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h or 03h or 04h or 05h) to the first byte. If the Chip ID differs, subsequent data is ignored. If the category ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

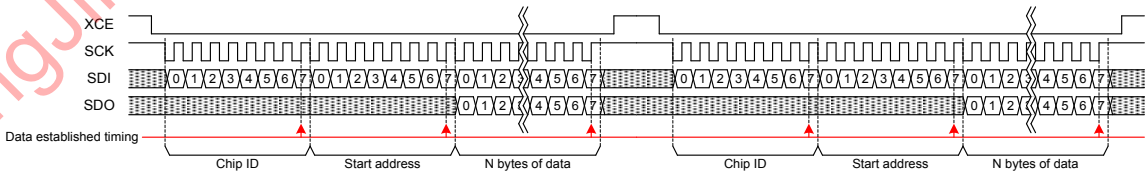
◆Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h or 83h or 84h or 85h) to the first byte. If the category ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. Input dummy data (SCK) in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



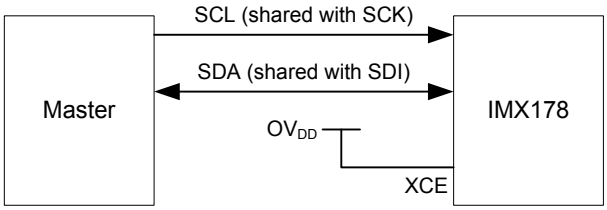
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

Description of Setting Registers (I^2C)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R/W

*R/W is data direction bit.

R/W

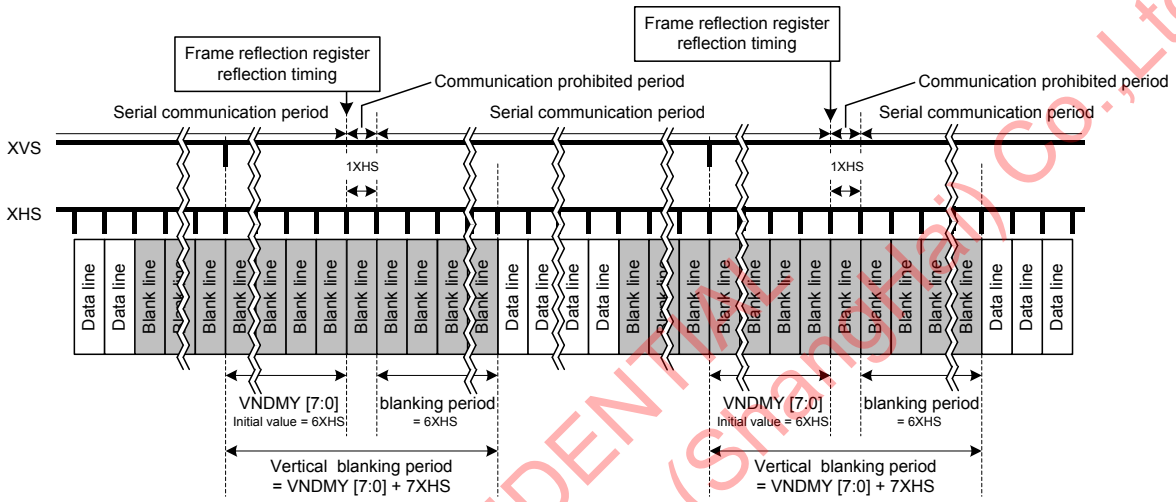
R/W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Description
SDA (common to SDI)	F1	Serial data communication
SCL (common to SCK)	J2	Serial clock input

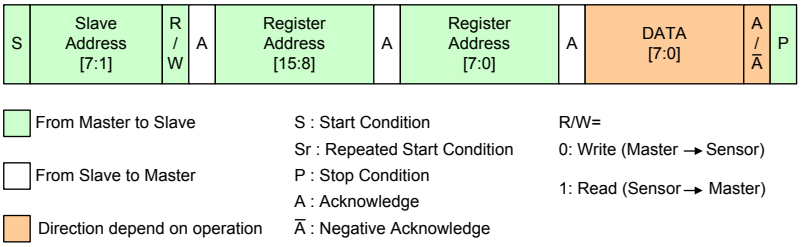
Register Communication Timing

In I^{2}C communication system, communication can be performed excluding during the oeriod when communication is prohibited from the falling edge of XVS to the period set by VNDMY [7:0] after (1H period). The default value of VNDMY [7:0] is 6H. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted Immediately in the item of Update timing, the settings are updated when the communication is performed. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, STBEXPL, STBLOGIC, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.)) Using REGHOLD function is recommended for register setting using I^{2}C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.



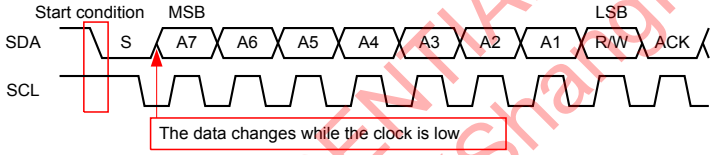
Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

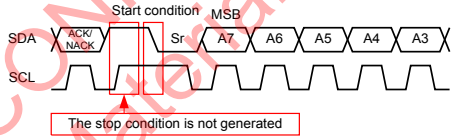


I²C Communication Protocol

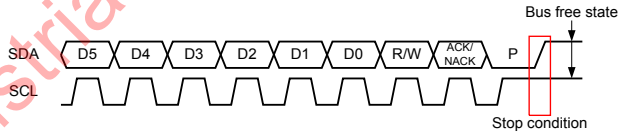
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / A (_) (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

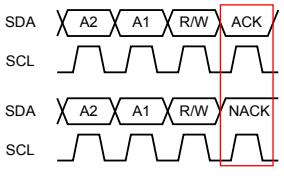


Repeated Start Condition



Stop Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.

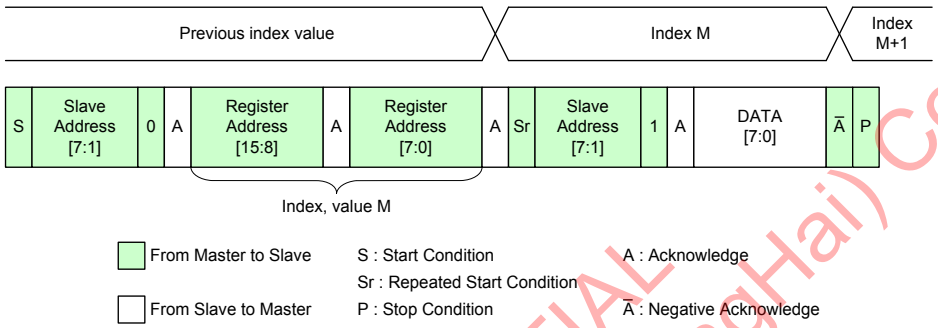


Acknowleadge and Negative Acknowledge

I²C Register Write and Read

Single Read from Random Location

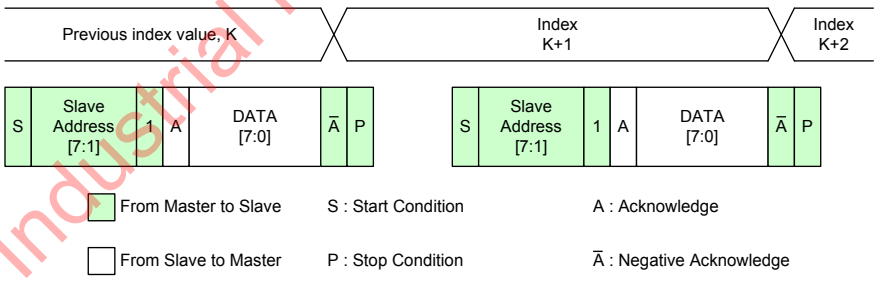
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

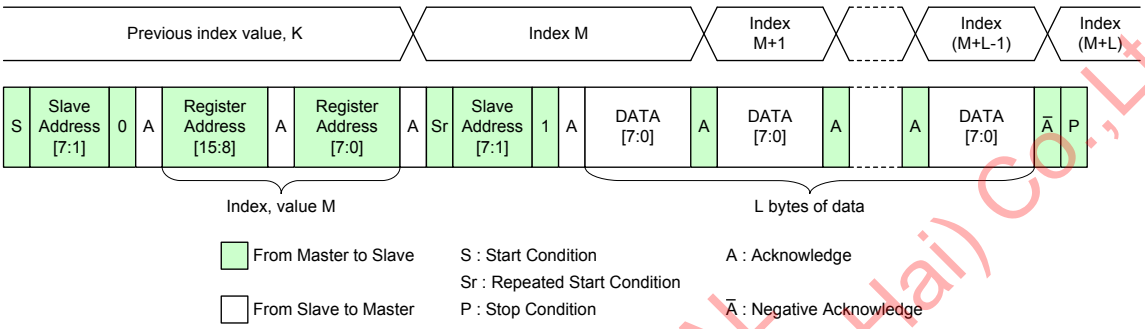
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge / Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

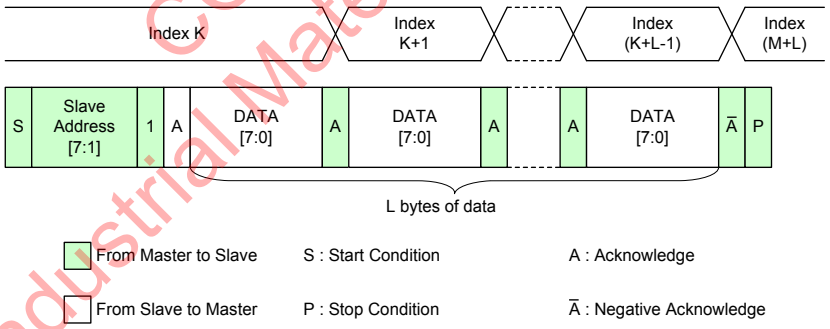
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

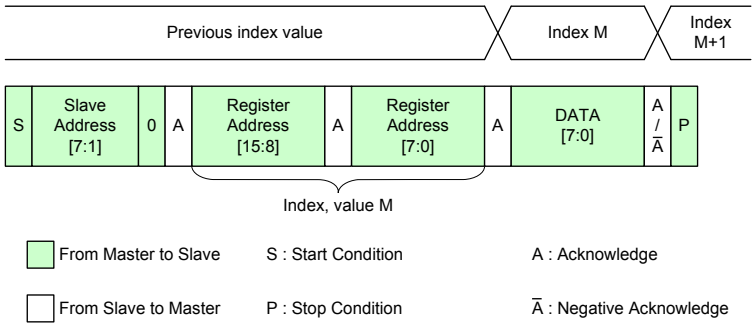
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

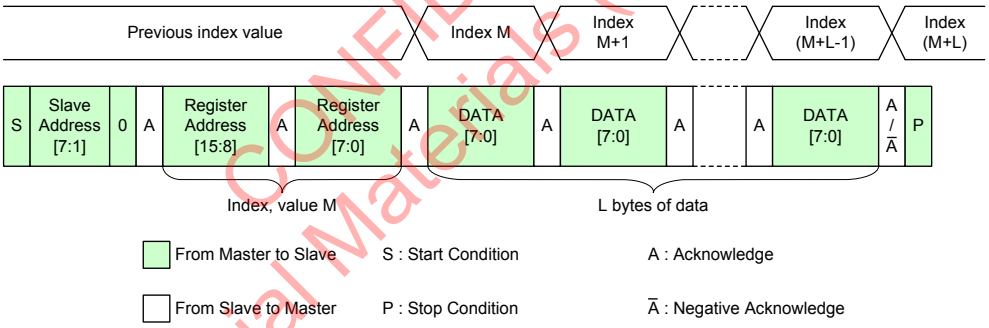
The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Read Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Register Map

This sensor has a total of 1024 bytes of registers, composed of registers with addresses 00h to FFh that correspond to Chip ID = 02h (write mode) / 82h (read mode), registers with addresses 00h to FFh that correspond to Chip ID = 03h (write mode) / 83h (read mode), registers with addresses 00h to FFh that correspond to Chip ID = 04h (write mode) / 84h (read mode), and registers with addresses 00h to FFh that correspond to Chip ID = 05h (write mode) / 85h (read mode). Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 1024 bytes.

Notice)
There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than STANDBY, STBEXPL, STBLOGIC, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.
Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h, 04h and 05h.

1) Registers corresponding to Chip ID = 02h in Write mode. (1/4) The register values can be read using Chip ID = 82h.

Address		Bit	Register name	Description	Default value after reset		Update timing
4-wire	I^2C				By Register	By address	
00h	3000h	0	STANDBY [0]	Standby control 0d: Operating 1d: Standby	1h	07h	Immediately
		1	STBEXPL [0]	Standby control 0d: Operating 1d: Standby	1h		Immediately
		2	STBLOGIC [0]	Standby control 0d: Operating 1d: Standby	1h		Immediately
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
03h	3003h	0		Fixed to "0".	0h	50h	—
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "1".	1h		—
		5		Fixed to "0".	0h		—
		6	STBDCK2	DCK2 standby control 0d : DCK2 active 1d : DCK2 Standby	1h		Immediately
		7		Fixed to "0".	0h		—
04h	3004h	0	STBLVDS [3:0]	LVDS standby control 0h : 10 ch All active 1h : 8 ch B,C,D,E,F,G,H,I,DCK1 active 3h : 4 ch D,E,F,G,DCK1 active 7h to Fh : All Standby Others:Setting prohibited	1h	01h	Immediately
		1					
		2					
		3					
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
07h	3007h	0	REGHOLD [0]	Register hold (Function not to update V reflection register) 0d: Invalid 1d: Valid	0h	00h	Immediately
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
08h	3008h	0	XMSTA [0]	Setting of master mode operation 0d: Master mode operation start 1d: Master mode operation stop	1h	01h	Immediately
		1		Fixed to "0".	0h		—
		2		Fixedd to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
09h	3009h	0	SW_RESET [0]	Software reset 0d: Operating 1d: Reset	0h	00h	Immediately
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
0Dh	300Dh	0	ADBIT [1:0]	ADconversion bits setting 0d: AD 10 bit 1d: AD 12 bit 2d: AD 14 bit 3d: Setting prohibited	1h	01h	V
		1					
		2	ADBITFREQ [1:0]	ADC mode setting 0d: AD14 bit AD10 bit (HD720p 2 × 2 Binning 120 fps is excluded) 1d: AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others: Setting prohibited	0h		V
		3					
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—

1) Registers corresponding to Chip ID = 02h in Write mode. (2/4)

Address		Bit	Register name	Description	Default value after reset		Update timing
4-wire	I^2C				By Register	By address	
0Eh	300Eh	0	MODE [5:0]	Drive mode setting 00h: All-pixel scan mode 01h: HD 1080p 23h: 2 × 2 binning 24h: HD 720p 2 × 2 binning Others: Setting prohibited	0h	00h	V
		1					
		2					
		3					
		4					
		5					
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
0Fh	300Fh	0	VREVERSE [0]	Vertical (V) direction readout inversion control 0d: Normal 1d: Inverted	0h	00h	V
		1	HREVERSE [0]	Horizontal (H) direction readout inversion control 0d: Normal 1d: Inverted	0h		V
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4	WINMODE [3:0]	0d: All pixel (6 M, HD 1080, HD 720) 1d : Windowcropping mode (4:3) 2d : Windowcropping mode (5:4) 3d : Windowcropping mode (16:9) 4d to 15 d : Setting prohibited	0h		V
		5					
		6					
		7					
10h	3010h	0	TCYCLE [1:0]	Vertical drive mode setting 0d: Normal 1d : 2binning Others: Setting prohibited	0h	00h	V
		1					
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
15h	3015h	0	BLKLEVEL [11:0]	LSB	03Ch	3Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
16h	3016h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
1Bh	301Bh	0	LP_MODE [7:0]	LSB Light performance mode setting 00h: High light performance mode 1Eh: Low light performance mode Others: Setting prohibited MSB	0Ch	0Ch	Immediately
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Fh	301Fh	0	GAIN [8:0]	LSB Gain setting High light Performance mode: 0.0 dB to 48.0 dB Low light Performance mode: 3.0 dB to 51.0 dB Step = 0.1 dB MSB	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
20h	3020h	0				00h	
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—

1) Registers corresponding to Chip ID = 02h in Write mode. (3/4)

Address		Bit	Register name	Description	Default value after reset		Update timing
4-wire	I²C				By Register	By address	
2Ch	302Ch	0	VMAX [16:0]	LSB	00FFFh	FFh	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
2Dh	302Dh	0		When sensor master mode vertical span setting (Number of operation lines count from 1)		0Fh	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
2Eh	302Eh	0		MSB		00h	
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
2Fh	302Fh	0	HMAX [15:0]	LSB	025Dh	5Dh	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
30h	3030h	0		When sensor master mode horizontal span setting (Number of operation clocks count from 1)		02h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
34h	3034h	0	SHS1 [16:0]	LSB	00008h	08h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
35h	3035h	0		Integration time adjustment Designated in line units		00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
36h	3036h	0		MSB		00h	
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—

1) Registers corresponding to Chip ID = 02h in Write mode. (4/4)

Address		Bit	Register name	Description	Default value after reset		Update timing
4-wire	I²C				By Register	By address	
41h	3041h	0	SVS [9:0]	LSB	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
42h	3042h	0				00h	
		1		MSB			
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
43h	3043h	0	SPL1 [9:0]	LSB	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
44h	3044h	0				00h	
		1		MSB			
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
59h	3059h	0	ODBIT [1:0]	Number of output bit setting 0d: 10 bit 1d: 12 bit 2d: 14 bit 3d: Setting prohibited	1h	11h	V
		1					
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4	OPORTSEL [2:0]	Serial output LVDS use number of channels select 0d: 10 ch 1d: 8 ch 3d: 4 ch Others: Setting prohibited	1h		V
		5					
		6					
		7		Fixed to "0".	0h		—
5Bh	305Bh	0		Fixed to "0".	0h	00h	—
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4	XVSLNG [1:0]	XVS pulse width setting in master mode 0d: 1H 1d: 2H 2d: 4H 3d: 8H	0h		Immediately
		5					
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
5Ch	305Ch	0		Fixed to "0".	0h	00h	—
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4	XHSLNG [1:0]	XHS pulse width setting in master mode 0d: 16 clock 1d: 32 clock 2d: 64 clock 3d: 128 clock	0h		Immediately
		5					
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
5Eh	305Eh	0	XVSOUTSEL [1:0]	XVS pin setting (in master mode) 0d: Output High setting 2d: VSYNC output 3d: External pulse output Others: Setting prohibited	0h	00h	Immediately
		1					
		2	XHSOUTSEL [1:0]	XHS pin setting (in master mode) 0d: Output High setting 2d: HSYNC output 3d: External pulse output Others: Setting prohibited	0h		Immediately
		3					
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
66h	3066h	0	VNDMY [7:0]	VSetting of the period from reflection register updated timing to read start timing VDesignated in XHS units counted from updated timing (1d to 255d) 0d: Setting prohibited	06h	06h	Immediately
		1					
		2					
		3					
		4					
		5					
		6					
		7					

2) Registers corresponding to Chip ID = 03h in Write mode. (1/2)
The register values can be read using Chip ID = 83h.

Address		Bit	Register name	Description	Default value after reset		Update timing
4-wire	I^2C				By Register	By address	
01h	3101h	0	FREQ [1:0]	LVDS output frequency setting	0h	30h	V
		1					
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "1".	1h		—
		5		Fixed to "1".	1h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
0Ch	310Ch	0		Fixed to "0".	0h	00h	—
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4	DCK2EN [0]	DCK2 output setting 0d: Lowfixed output 1d: Clock output	0h		Immediately
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
9Ch	319Ch	0	WINPH [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (Horizontal position) Set to become the multiple of four.	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
9Dh	319Dh	0		MSB		00h	
		1					
		2					
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
9Eh	319Eh	0	WINWH [11:0]	LSB In window cropping mode Cropping size designation (Horizontal direction) Set to become the multiple of four.	79Ch	9Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
9Fh	319Fh	0		MSB		07h	
		1					
		2					
		3					
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
A0h	31A0h	0	VWINPOS [11:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (Vertical position) Set to the even number.	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
A1h	31A1h	0		MSB		00h	
		1					
		2					
		3					
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—

2) Registers corresponding to Chip ID = 03h in Write mode. (2/2)

Address		Bit	Register name	Description	Default value after reset		Update timing
4-wire	I²C				By Register	By address	
A2h	31A2h	0	VWIDCUT [12:0]	LSB	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6		In window cropping mode Cropping size designation (Vertical direction)			
		7		Set to the even number.			
A3h	31A3h	0				00h	
		1					
		2					
		3					
		4		MSB			
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
A4h	31A4h	0	WINENH [0]	Arbitrary cropping (horizontal) enable 0d: Normal 1d: Arbitrary cropping in vertical direction	0h	00h	V
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—
A5h	31A5h	0	VWINSEL [0]	Arbitrary cropping (vertical) enable 0d: Normal 1d: Arbitrary cropping in vertical direction	0h	00h	V
		1		Fixed to "0".	0h		—
		2		Fixed to "0".	0h		—
		3		Fixed to "0".	0h		—
		4		Fixed to "0".	0h		—
		5		Fixed to "0".	0h		—
		6		Fixed to "0".	0h		—
		7		Fixed to "0".	0h		—

3) The register set up according to drive mode
These registers must be set to the value shown in the table below.
Depending on the INCK frequency and output data rate.And this setting must be done during standby mode.

4-wire		I²C	Default value after reset	Setting value					
				Data Rate [Mbps]					
Chip ID	Address	Address		594 / 297 / 148.5 / 74.25				432 / 216 108 / 54	
				INCK [MHz]				INCK [MHz]	
				74.25	54	37.125	27	54	27
03h	0Ch [0]	310Ch [0]	0h	0h	←	←	←	1h	←
05h	BEh	33BEh	0Ch	0Ch	21h	18h	21h	21h	←
05h	BFh	33BFh	10h	0Ch	21h	18h	21h	21h	←
05h	C0h	33C0h	10h	10h	2Ch	20h	2Ch	2Ch	←
05h	C1h	33C1h	10h	10h	2Ch	20h	2Ch	2Ch	←
05h	C2h	33C2h	0Ch	0Ch	21h	18h	21h	21h	←
05h	C3h	33C3h	10h	10h	2Ch	20h	2Ch	2Ch	←
05h	C4h	33C4h	10h	10h	16h	20h	2Ch	10h	20h
05h	C5h	33C5h	00h	00h	01h	00h	00h	01h	00h
03h	1Ch	311Ch	48h	34h	←	←	←	1Eh	←
03h	1Dh	311Dh	28h	28h	←	←	←	15h	←
03h	1Eh	311Eh	ABh	ABh	←	←	←	72h	←
03h	1Fh	311Fh	00h	00h	←	←	←	00h	←
03h	20h	3120h	A8h	95h	←	←	←	5Ch	←
03h	21h	3121h	00h	00h	←	←	←	00h	←
03h	22h	3122h	B3h	B4h	←	←	←	72h	←
03h	23h	3123h	00h	00h	←	←	←	00h	←
03h	24h	3124h	8Bh	8Ch	←	←	←	C7h	←
03h	25h	3125h	02h	02h	←	←	←	01h	←
03h	2Dh	312Dh	03h	03h	←	←	←	00h	←
03h	2Eh	312Eh	16h	0Ch	←	←	←	01h	←
03h	2Fh	312Fh	17h	28h	←	←	←	15h	←
03h	31h	3131h	36h	2Dh	←	←	←	10h	←
03h	32h	3132h	00h	00h	←	←	←	00h	←
03h	33h	3133h	77h	B4h	←	←	←	72h	←
03h	34h	3134h	00h	00h	←	←	←	00h	←
03h	37h	3137h	50h	50h	←	←	←	38h	←
03h	38h	3138h	08h	08h	←	←	←	00h	←
03h	39h	3139h	15h	00h	←	←	←	00h	←
03h	3Ah	313Ah	12h	07h	←	←	←	00h	←
03h	3Dh	313Dh	05h	05h	←	←	←	00h	←
03h	40h	3140h	06h	06h	←	←	←	00h	←
04h	20h	3220h	8Bh	8Bh	←	←	←	89h	←
04h	21h	3221h	00h	00h	←	←	←	00h	←
04h	22h	3222h	74h	74h	←	←	←	54h	←
04h	23h	3223h	00h	00h	←	←	←	00h	←
04h	26h	3226h	C2h	C2h	←	←	←	8Dh	←
04h	27h	3227h	00h	00h	←	←	←	00h	←
04h	A9h	32A9h	1Ah	1Bh	←	←	←	14h	←
04h	AAh	32AAh	00h	00h	←	←	←	00h	←
04h	B3h	32B3h	0Dh	0Eh	←	←	←	Ah	←
04h	B4h	32B4h	00h	00h	←	←	←	00h	←
05h	D6h	33D6h	18h	16h	←	←	←	10h	←
05h	D7h	33D7h	18h	15h	←	←	←	0Fh	←
05h	D8h	33D8h	16h	14h	←	←	←	0Eh	←
05h	D9h	33D9h	10h	10h	←	←	←	0Ch	←
05h	DAh	33DAh	08h	08h	←	←	←	06h	←

4) Registers which must be changed from the default value
Change the following registers from the default value after the reset.
And this setting must be done during standby mode.

4-wire		I^2C	Default value after reset	Setting value
Chip ID	Address	Address		
02h	11h	3011h	10h	00h
02h	1Bh	301Bh	0Ch	00h
02h	37h	3037h	07h	08h
02h	38h	3038h	00h	00h
02h	39h	3039h	00h	00h
02h	ADh	30ADh	05h	49h
02h	AFh	30AFh	14h	54h
02h	B0h	30B0h	23h	33h
02h	B3h	30B3h	00h	0Ah
02h	C4h	30C4h	10h	30h
03h	03h	3103h	00h	03h
03h	04h	3104h	1C	08h
03h	07h	3107h	11h	10h
03h	0Fh	310Fh	02h	01h
04h	E5h	32E5h	0Eh	06h
04h	E6h	32E6h	1Fh	00h
04h	E7h	32E7h	1Fh	1Fh
04h	E8h	32E8h	1Fh	00h
04h	E9h	32E9h	1Fh	00h
04h	EAh	32EAh	1Eh	00h
04h	EBh	32EBh	1Dh	00h
04h	ECh	32ECh	1Ah	00h
04h	EEh	32EEh	1Eh	00h
04h	F2h	32F2h	03h	02h
04h	F4h	32F4h	04h	00h
04h	F5h	32F5h	06h	00h
04h	F6h	32F6h	04h	00h
04h	F7h	32F7h	06h	00h
04h	F8h	32F8h	06h	00h
04h	FCh	32FCh	07h	02h
05h	10h	3310h	12h	11h
05h	38h	3338h	41h	81h
05h	3Dh	333Dh	01h	00h
05h	62h	3362h	01h	00h
05h	6Bh	336Bh	01h	02h
05h	6Eh	336Eh	21h	11h
05h	B4h	33B4h	96h	FEh
05h	B5h	33B5h	06h	06h
05h	B9h	33B9h	01h	00h

Readout Drive Modes

The table below lists the operating modes available with this sensor.

List of Operation Modes and Output Rates for Parallel Output (1/2)

Mode	Recording pixels		Total number of pixels		INCK	Frame Rate	ADC	Bit Width	Data Rate		
	H	V	H	V					LVDS 10 ch	LVDS 8 ch	LVDS 4 ch
	[pix]	[line]	[pix]	[line]	[MHz]	[fps]	[bit]	[bit]	[Mbps/ch]	[Mbps/ch]	[Mbps/ch]
All-Pixel Scan 6.3 M (3:2)	3072	2048	3096	2094	54 / 27	59.94	10	10	432	N/A	N/A
						29.97	14	14	432	432	N/A
							12	12	432	432	N/A
							10	10	432	432	N/A
					54 / 27 / 74.25 / 37.125		10	10	N/A	N/A	594
Window cropping 5.0 M (4:3)	2592	1944	2616	1990	54 / 27	59.94	12	12	432	N/A	N/A
							10	10	432	432	N/A
						29.97	14	14	432	432	N/A
							12	12	216	432	N/A
							10	10	216	432	432
					54 / 27 / 74.25 / 37.125		12	12	N/A	N/A	594
							10	10	N/A	N/A	594
Window cropping 5.2 M (5:4) QSXGA	2560	2048	2584	2094	54 / 27	59.94	12	12	432	N/A	N/A
							10	10	432	432	N/A
						29.97	14	14	432	432	N/A
							12	12	216	432	N/A
							10	10	216	432	432
					54 / 27 / 74.25 / 37.125		14	14	N/A	N/A	594
							12	12	N/A	N/A	594
							10	10	N/A	N/A	594
All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning	1536	1024	1548	1050	54 / 27	29.97	12	14	108	108	216
							10	12	108	108	216
Window cropping 1.3 M (4:3) 2 × 2 Binning	1296	972	1308	998	54 / 27	59.94	12	14	216	216	432
							10	12	216	216	432
						29.97	12	14	108	108	216
							10	12	108	108	216
Window cropping 1. 3 M (5:4) QSXGA 2 × 2 Binning	1280	1024	1292	1050	54 / 27	59.94	12	14	216	216	432
							10	12	216	216	432
						29.97	12	14	108	108	216
							10	12	108	108	216
Arbitrary cropping 6.3 M	3072	2048	3096	2094	54 / 27	59.94	10	10	432	N/A	N/A
						29.97	14	14	432	432	N/A
							12	12	432	432	N/A
							10	10	432	432	N/A
					54 / 27 / 74.25 / 37.125		10	10	N/A	N/A	594

N/A: Mode not supported

List of Operation Modes and Output Rates for Serial Output (2/2)

Mode	Recording pixels		Total number of pixels		INCK	Frame Rate	ADC	Bit Width	Data Rate		
	H	V	H	V					LVDS 10 ch	LVDS 8 ch	LVDS 4 ch
	[pix]	[line]	[pix]	[line]	[MHz]	[fps]	[bit]	[bit]	[Mbps/ch]	[Mbps/ch]	[Mbps/ch]
Window cropping 5.3 M (16:9)	3072	1728	3096	1774	54 / 27 74.25 / 37.125	60	12	12	594	594	N/A
							10	10	594	594	N/A
						30	14	14	297	594	594
							12	12	297	297	594
							10	10	297	297	594
HD 1080p	1920	1080	1944	1116	54 / 27 74.25 / 37.125	120	12	12	594	594	N/A
							10	10	594	594	N/A
						60	12	12	297	297	594
							10	10	297	297	594
						30	14	14	148.5	148.5	297
HD 720p 2 × 2 Binning	1280	720	1304	742	54 / 27 74.25 / 37.125	120	10	12	297	297	594
						60	12	14	148.5	148.5	297
							10	12	148.5	148.5	297
						30	12	14	74.25	74.25	148.5
							10	12	74.25	74.25	148.5

N/A: Mode not supported

Sync code

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The output timing is shown below. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)

Sync Code Output Timing

List of Sync Code

Sync code	1st code			2nd code			3rd code			4th code		
	10 bit	12 bit	14 bit	10 bit	12 bit	14 bit	10 bit	12 bit	14 bit	10 bit	12 bit	14 bit
SAV (Valid line)	3FFh	FFFh	3FFFh	000h	000h	0000h	000h	000h	0000h	200h	800h	2000h
EAV (Valid line)	3FFh	FFFh	3FFFh	000h	000h	0000h	000h	000h	0000h	274h	9D0h	2740h
SAV (Invalid line)	3FFh	FFFh	3FFFh	000h	000h	0000h	000h	000h	0000h	2ACh	AB0h	2AC0h
EAV (Invalid line)	3FFh	FFFh	3FFFh	000h	000h	0000h	000h	000h	0000h	2D8h	B60h	2D80h

(Note) They are output to each channel seriously in MSB first.
For details, see the item of "Signal output" and "Output pin setting".

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.

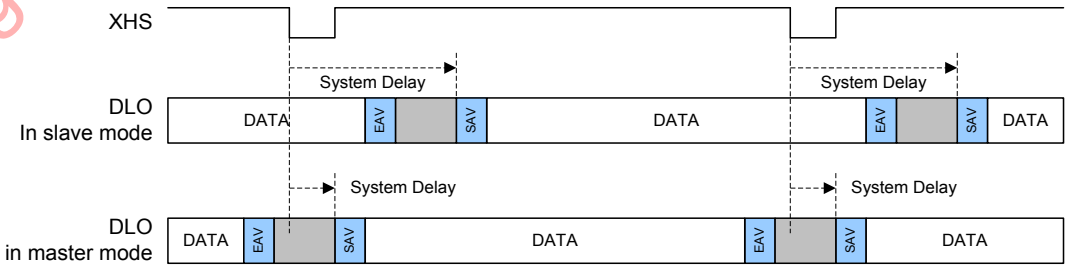


Image Data Output Format

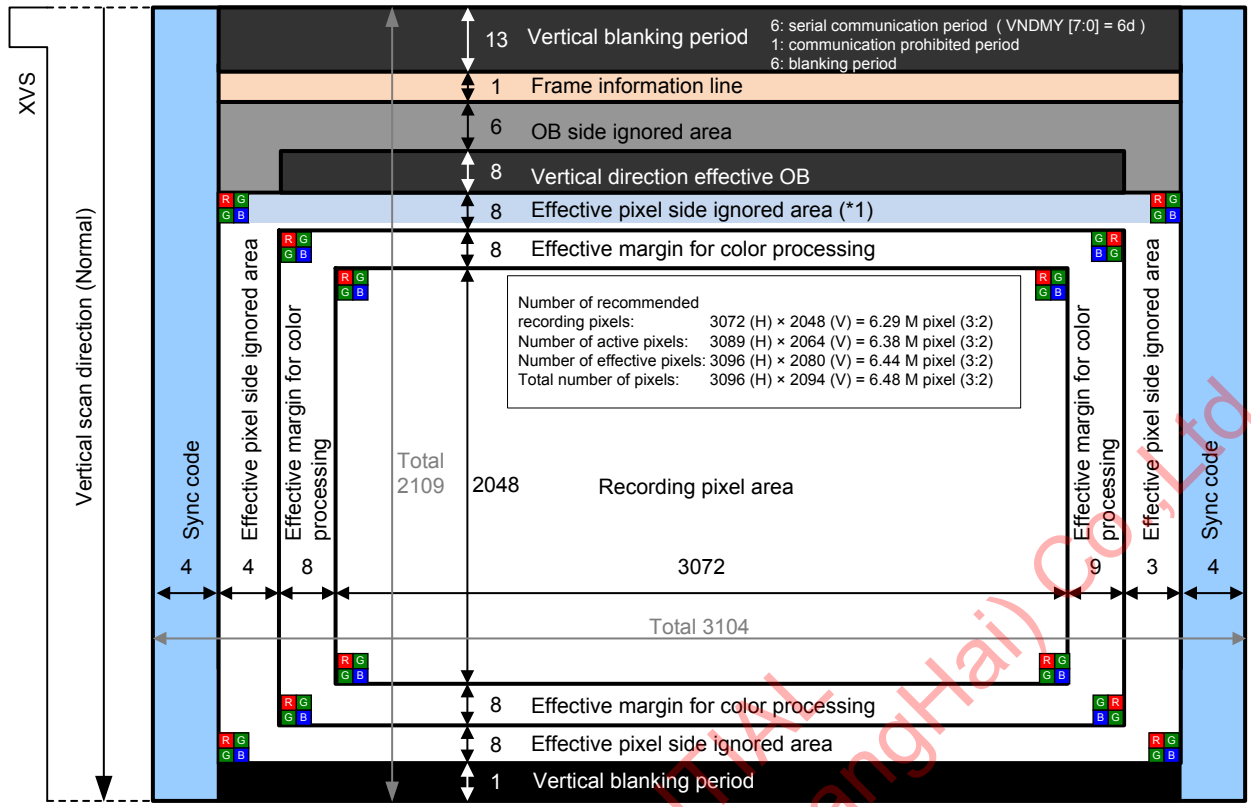
All-Pixel Scan 6.3 M (3:2)

Register List of All-Pixel Scan 6.3 M (3:2)

Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	00h	All-Pixel Scan 6.3M (3:2)
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	0h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	0h	Normal vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX [7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX [15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX [7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX [15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

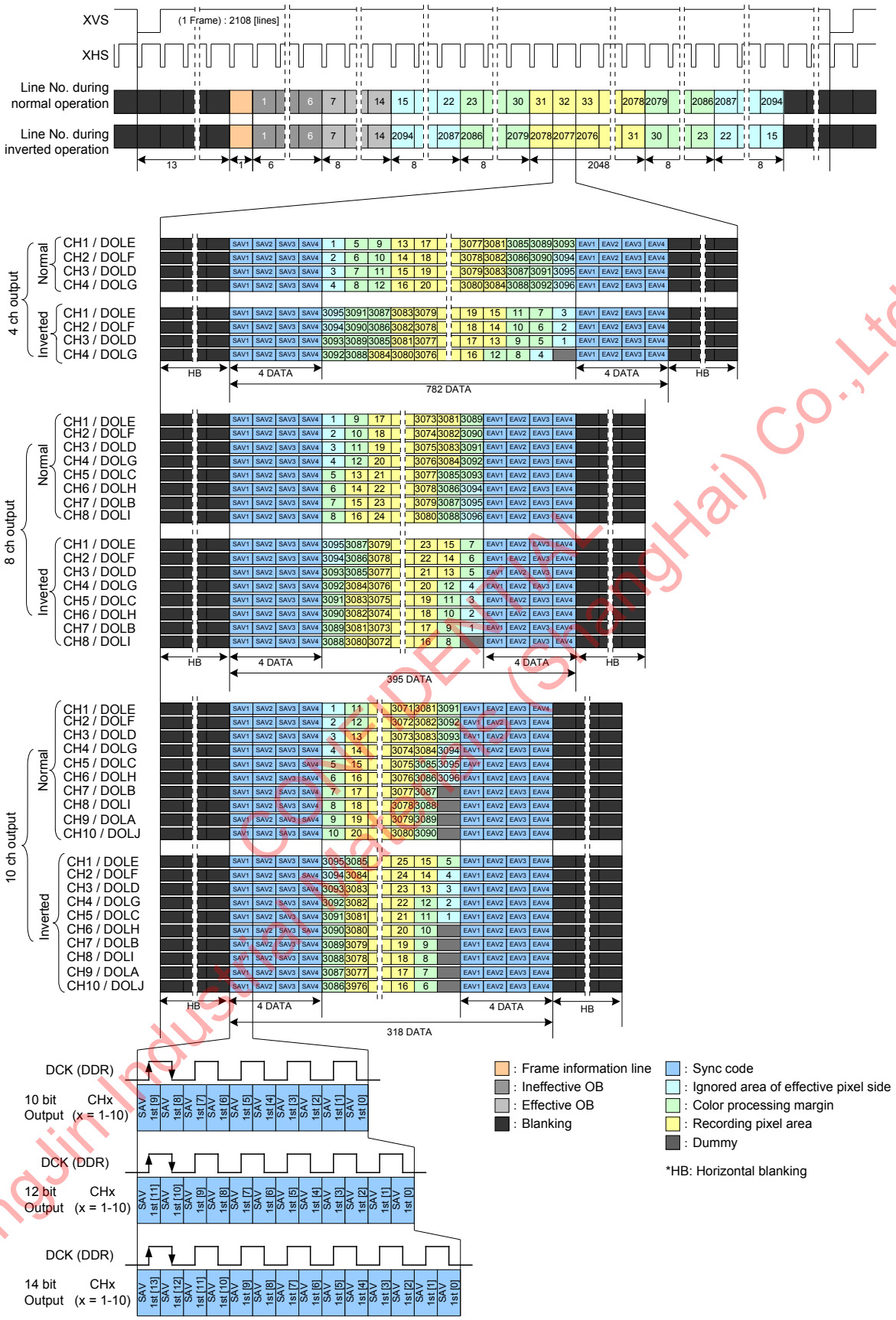
All-Pixel Scan 6.3 M (3:2) register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	59.94	10	10	432	3360	420	2145	01A4h	00861h	0h	0.36
		29.97	14	14	432	4800	840	2145	0348h	00861h	0h	0.28
			12	12	432	3300	495	3640	01EFh	00E38h	0h	0.29
			10	10	432	3360	420	4290	01A4h	010C2h	0h	0.36
	8 ch	29.97	14	14	432	3840	840	2145	0348h	00861h	0h	0.28
			12	12	432	3200	600	3003	0258h	00BBBh	0h	0.24
			10	10	432	3226	504	3575	01F8h	00DF7h	0h	0.30
54 / 27 / 74.25 / 37.125	4 ch	29.97	10	10	594	3203	728	2475	03E9h	009ABh	0h	0.15



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Pixel Array Image in All-Pixel Scan 6.3 M (3:2) Mode



Drive Timing Chart for All-Pixel Scan 6.3M (3:2) Mode

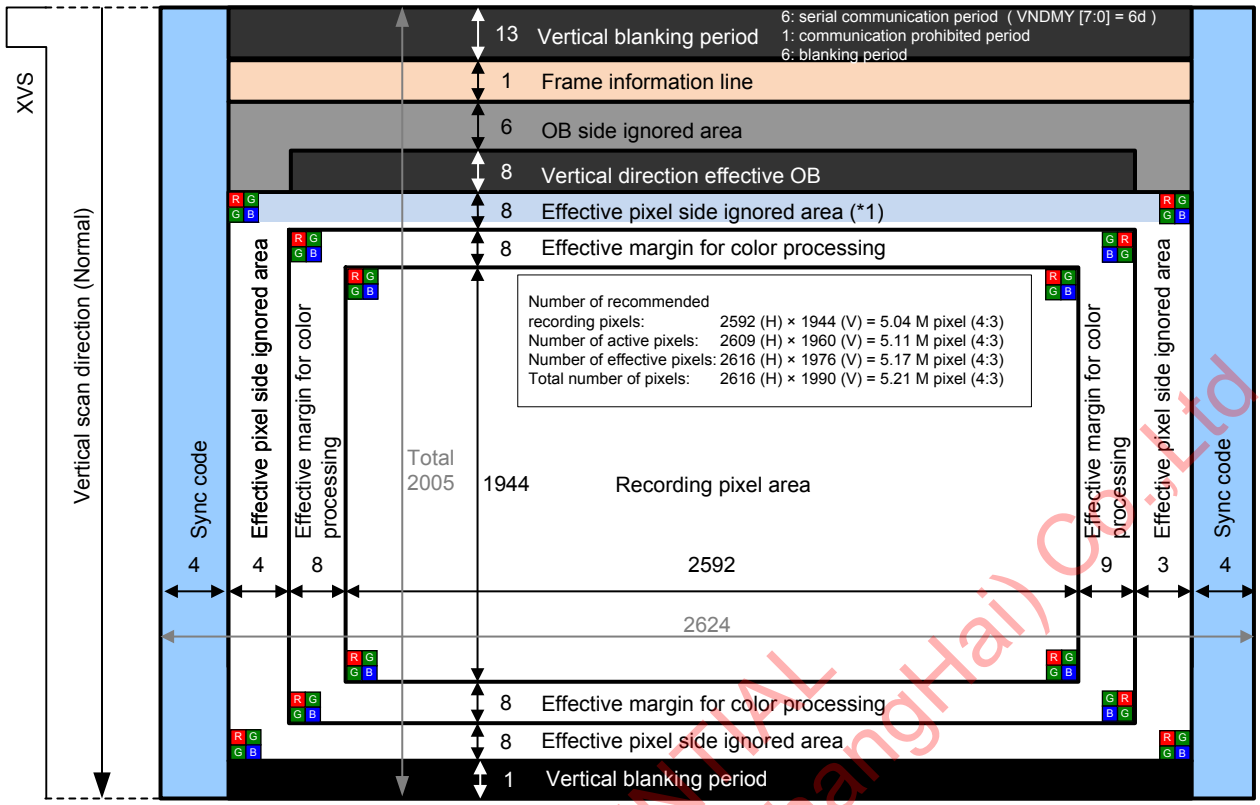
Window cropping 5.0 M (4:3)

Register List of Window cropping 5.0 M (4:3)

Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	00h	Window cropping 5.0M (4:3)
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	1h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	0h	Normal vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX [7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX [15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX [7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX [15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

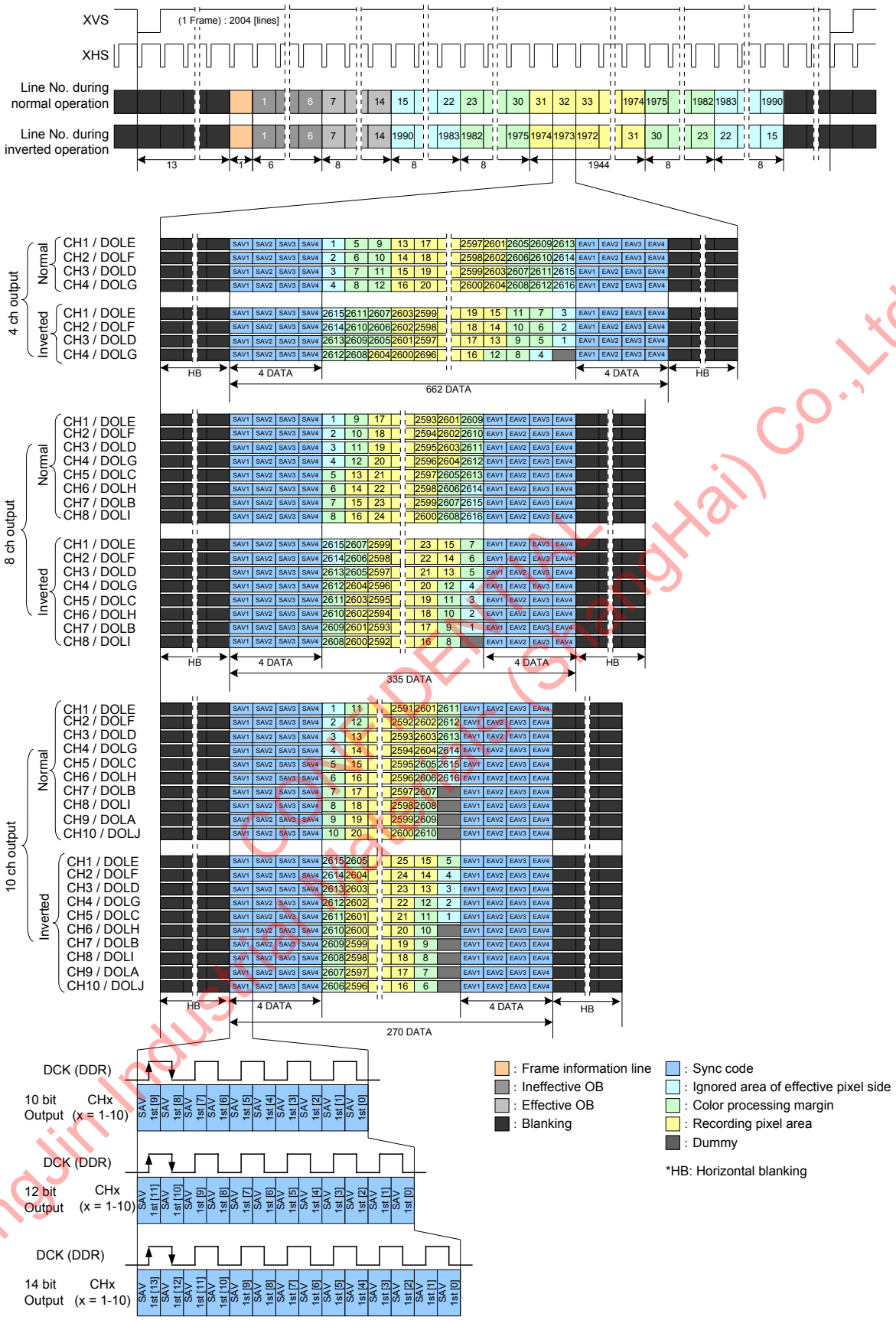
Window cropping 5.0 M (4:3) register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	59.94	12	12	432	2800	420	2145	01A4h	00861h	0h	0.34
			10	10	432	3360	420	2145	01A4h	00861h	0h	0.36
		29.97	14	14	432	4800	840	2145	0348h	00861h	0h	0.28
			12	12	216	2730	819	2200	0333h	00898h	1h	0.18
			10	10	216	2772	693	2600	02B5h	00A28h	1h	0.22
	8 ch	59.94	10	10	432	2746	429	2100	01ADh	00834h	0h	0.36
		29.97	14	14	432	3840	840	2145	0348h	00861h	0h	0.28
			12	12	432	2773	520	3465	0208h	00D89h	0h	0.28
			10	10	432	2746	429	4200	01ADh	01068h	0h	0.36
	4 ch	29.97	10	10	432	2688	840	2145	0348h	00861h	0h	0.18
54 / 27 74.25 / 37.125			12	12	594	2669	728	2475	03E9h	009ABh	0h	0.14
			10	10	594	2710	616	2925	034Fh	00B6Dh	0h	0.18



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Pixel Array Image in Window cropping 5.0 M (4:3) Mode



Drive Timing Chart for Window cropping 5.0 M (4:3) Mode

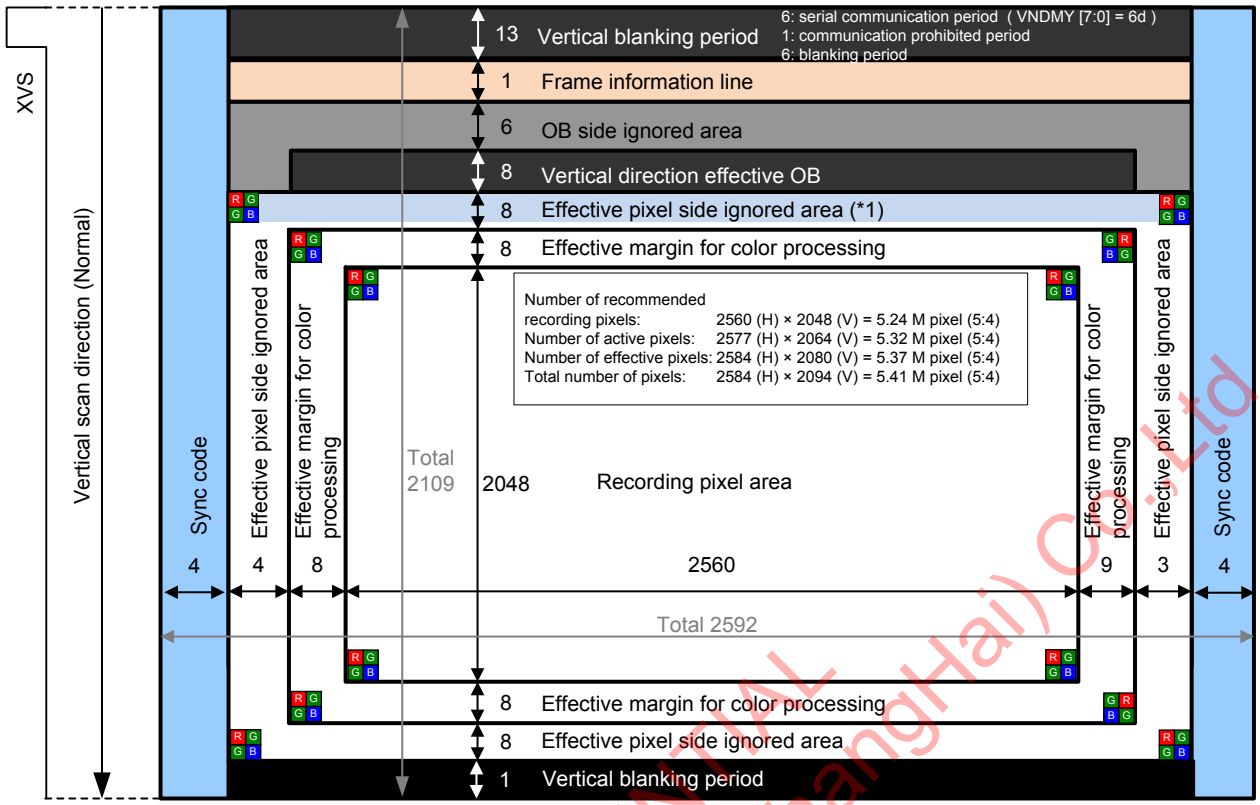
Window cropping 5.2 M (5:4) QSXGA

Register List of Window cropping 5.2 M (5:4) QSXGA

Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	00h	Window cropping 5.2 M (5:4) QSXGA
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	2h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	0h	Normal vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX [7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX [15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX [7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX [15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

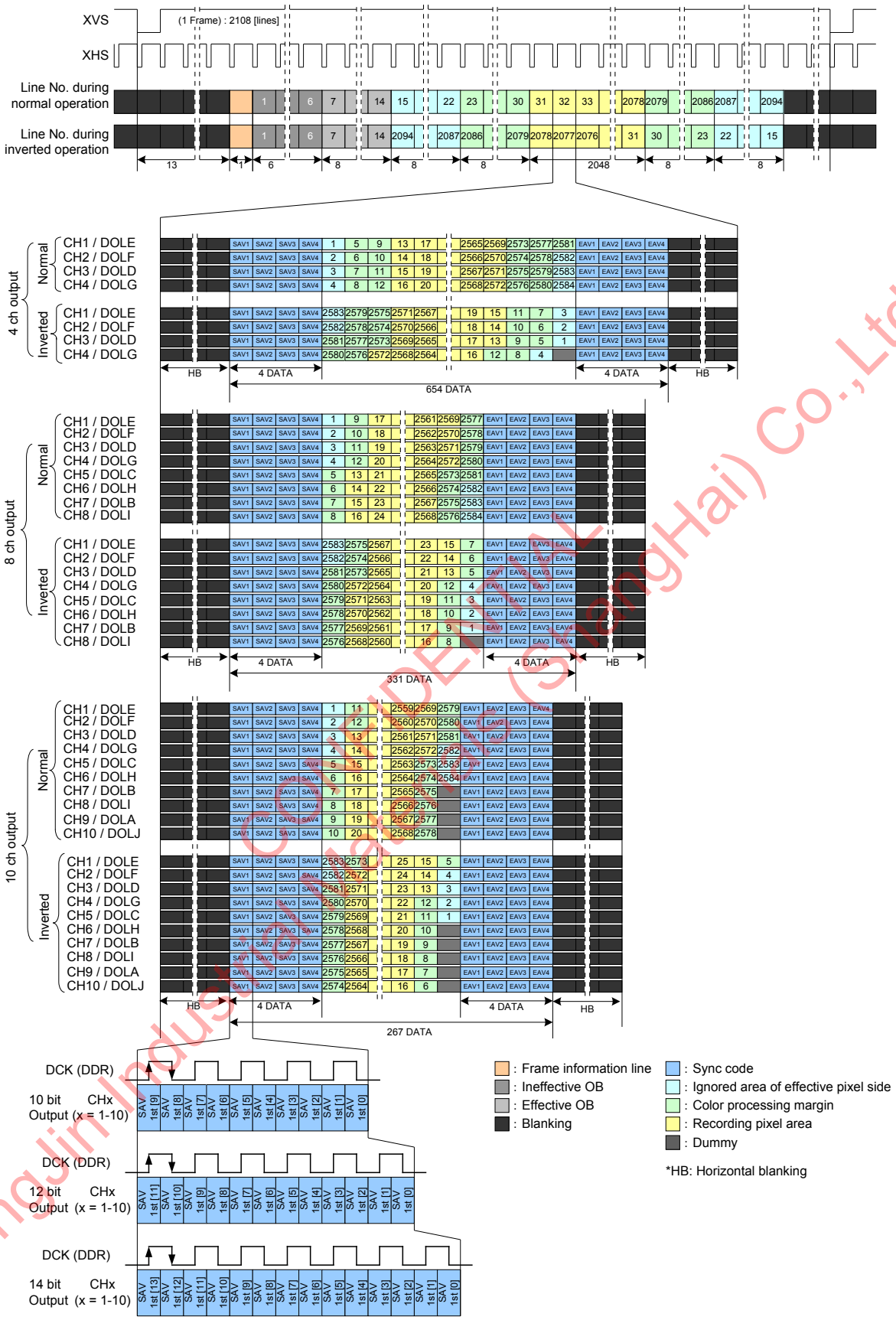
Window cropping 5.2 M (5:4) QSXGA register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	59.94	12	12	432	2800	420	2145	01A4h	00861h	0h	0.34
			10	10	432	3360	420	2145	01A4h	00861h	0h	0.36
		29.97	14	14	432	4800	840	2145	0348h	00861h	0h	0.28
			12	12	216	2730	819	2200	0333h	00898h	1h	0.18
			10	10	216	2772	693	2600	02B5h	00A28h	1h	0.22
	8 ch	59.94	10	10	432	2688	420	2145	01A4h	00861h	0h	0.36
		29.97	14	14	432	3840	840	2145	0348h	00861h	0h	0.28
			12	12	432	2688	504	3575	01F8h	00DF7h	0h	0.29
			10	10	432	2688	420	4290	01A4h	010C2h	0h	0.36
	4 ch	29.97	10	10	432	2688	840	2145	0348h	00861h	0h	0.18
54 / 27 74.25 / 37.145			14	14	594	2640	840	2145	0483h	00861h	0h	0.21
			12	12	594	2669	728	2475	03E9h	009ABh	0h	0.14
			10	10	594	2640	600	3003	0339h	00BBBh	0h	0.19



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Pixel Array Image in Window cropping 5.2 M (5:4) QSXGA Mode



Drive Timing Chart for Window cropping 5.2 M (5:4) QSXGA Mode

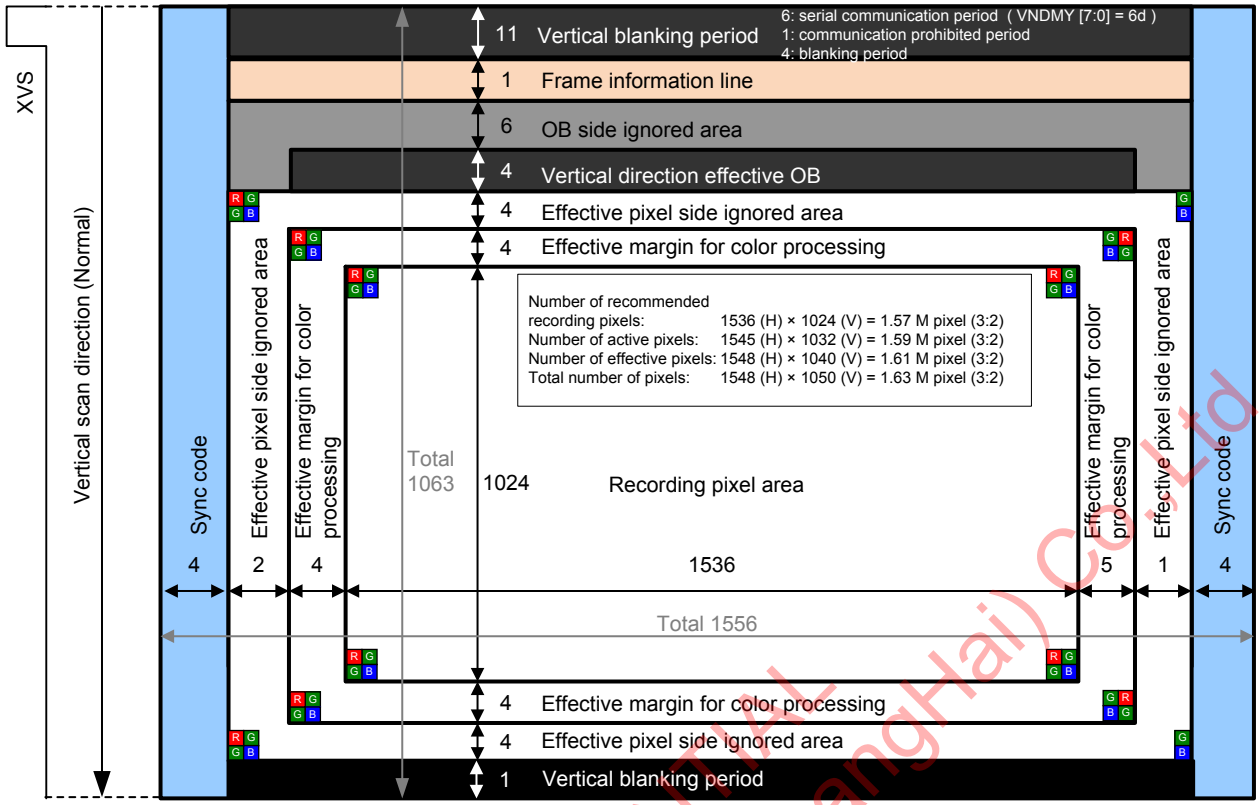
All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning

Register List of All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning

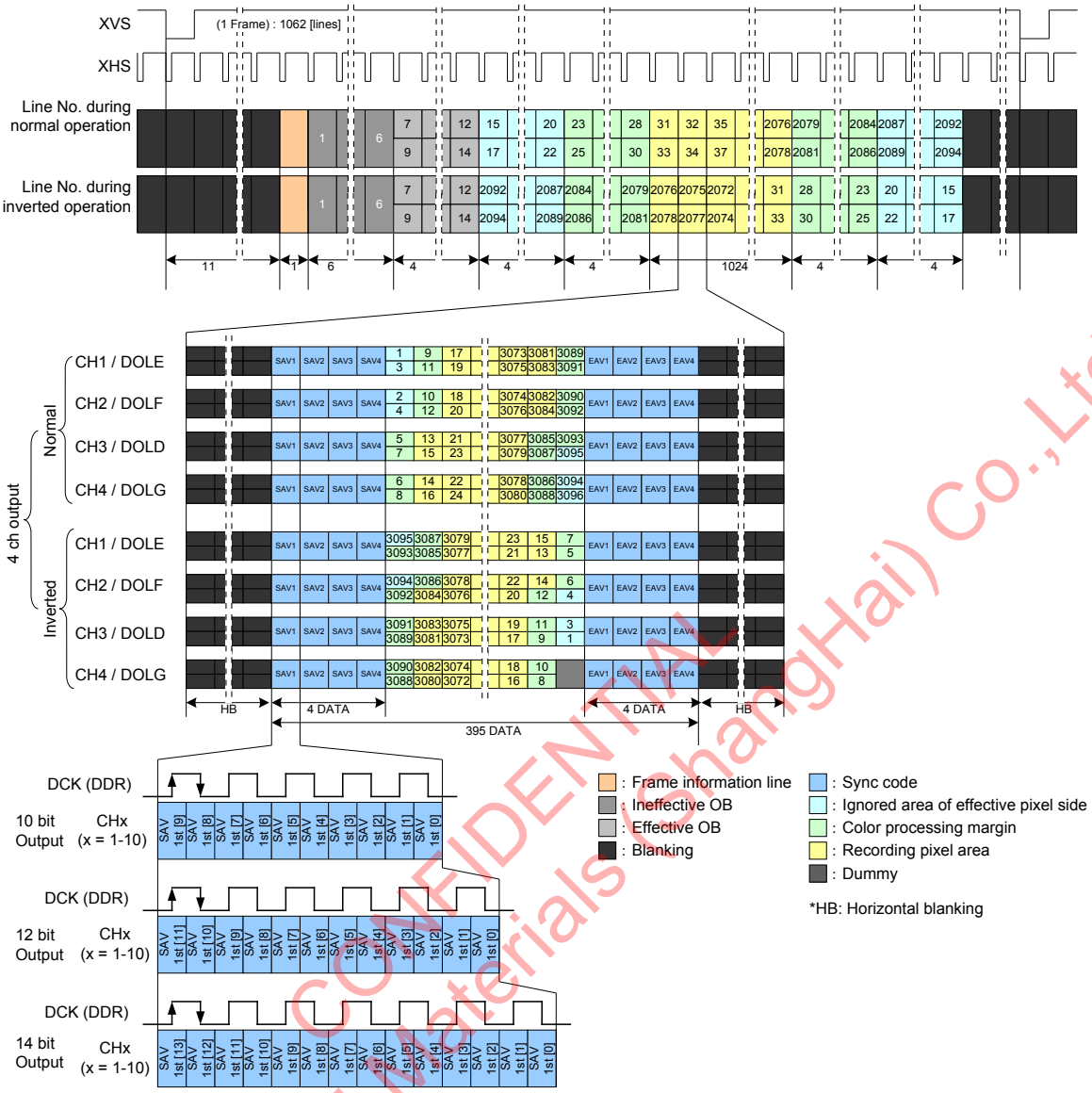
Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	23h	All-Pixel Scan 1.6M (3:2) 2 × 2 Binning
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	0h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	1h	2 binning vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX[7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX[15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX[7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX[15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	29.97	12	14	108	3343	585	3080	0249h	00C08h	2h	0.25
			10	12	108	3300	495	3640	01EFh	00E38h	2h	0.31
	8 ch	29.97	12	14	108	3269	715	2520	02CBh	009D8h	2h	0.20
			10	12	108	3285	616	2925	0268h	00B6Dh	2h	0.25
	4 ch	29.97	12	14	216	3200	700	2574	02BCh	00A0Eh	1h	0.21
			10	12	216	3200	600	3003	0258h	00BBBh	1h	0.26



Pixel Array Image in All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning Mode



Drive Timing Chart for All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning Mode

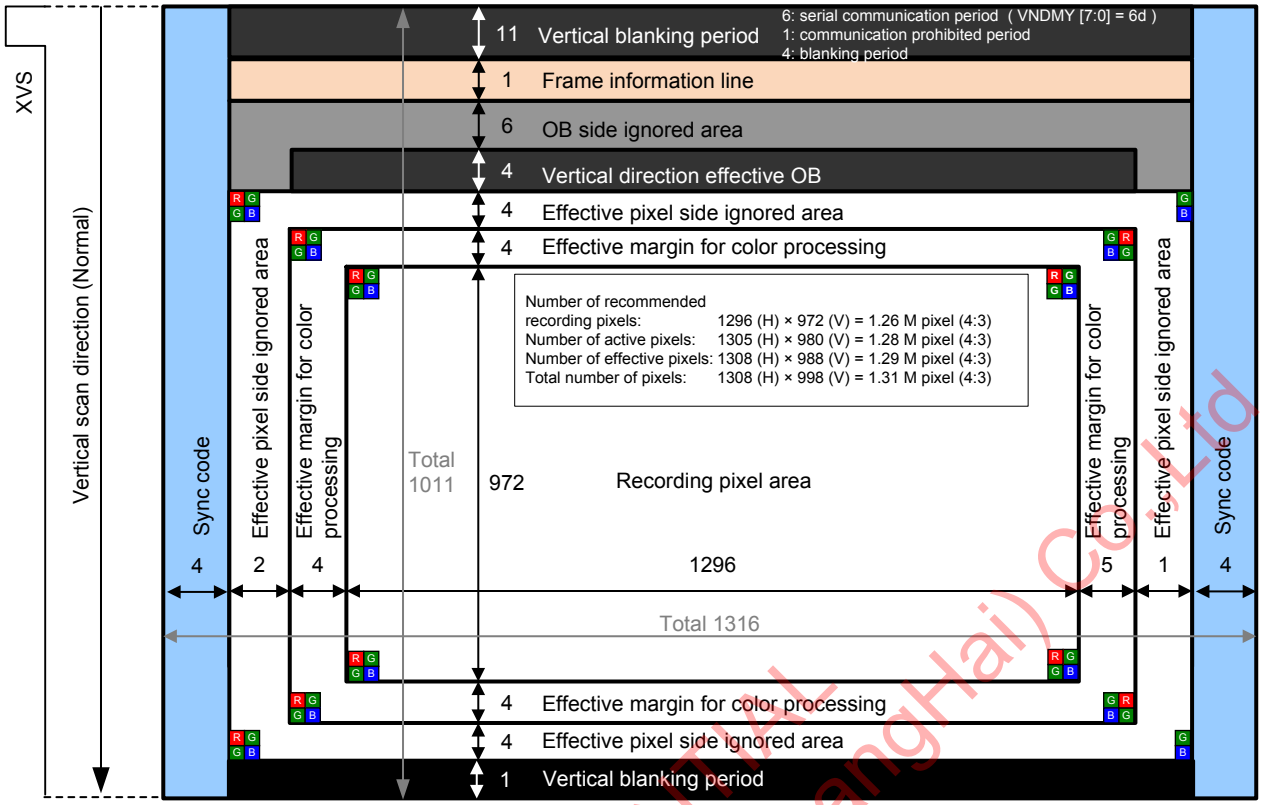
Window cropping 1.3 M (4:3) 2 × 2 Binning

Register List of Window cropping 1.3 M (4:3) 2 × 2 Binning

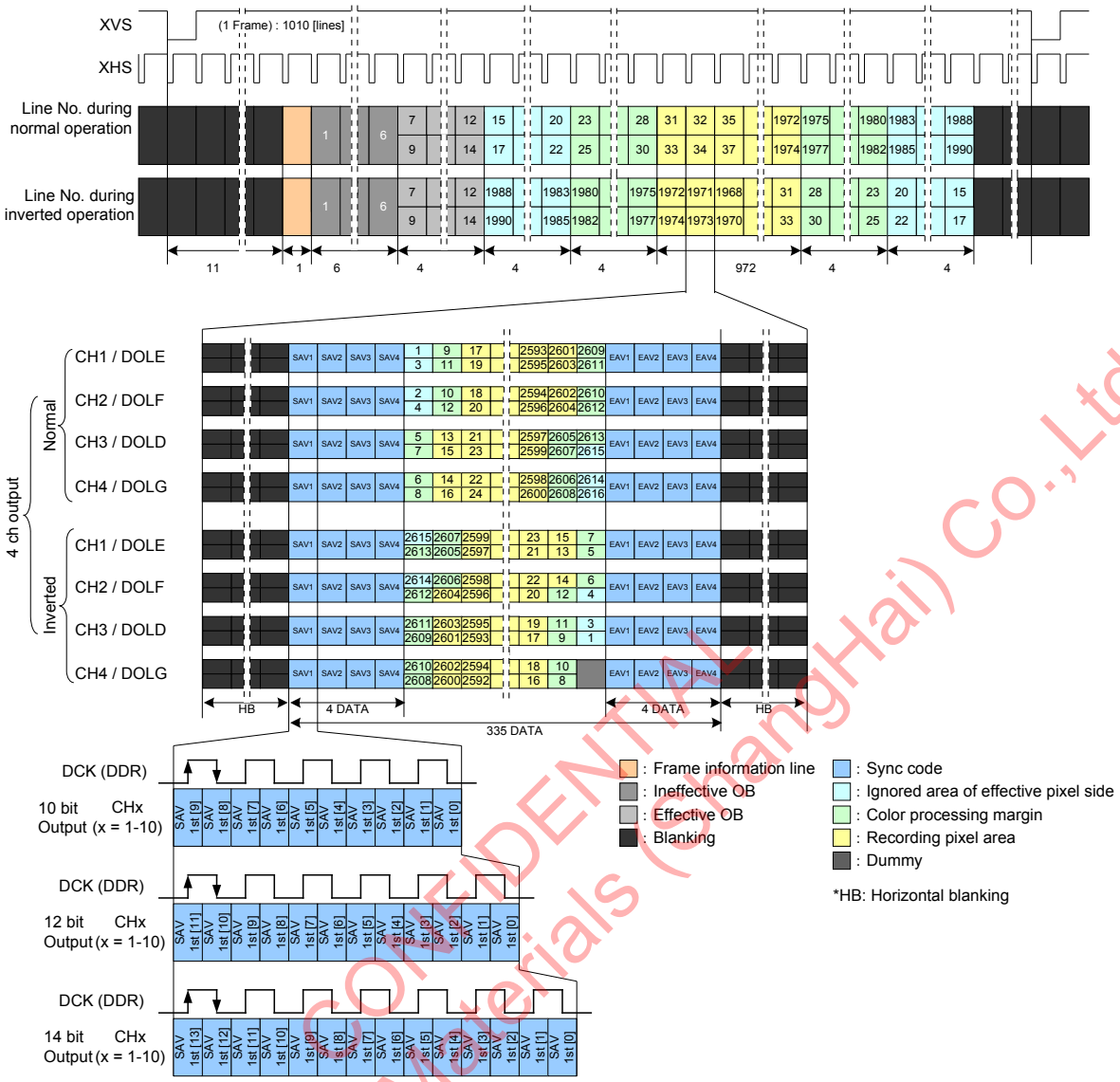
Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	23h	Window cropping 1.3 M (4:3) 2 × 2 Binning
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	1h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	1h	2 binning vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX [7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX [15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX [7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX [15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

Window cropping 1.3 M (4:3) 2 × 2 Binning register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	59.94	12	14	216	4800	420	2145	01A4h	00861h	1h	0.34
			10	12	216	5600	420	2145	01A4h	00861h	1h	0.36
		29.97	12	14	108	2829	495	3640	01EFh	00E38h	2h	0.29
			10	12	108	2933	440	4095	01B8h	00FFFh	2h	0.35
	8 ch	59.94	12	14	216	3840	420	2145	01A4h	00861h	1h	0.34
			10	12	216	4480	420	2145	01A4h	00861h	1h	0.36
		29.97	12	14	108	2816	616	2925	0268h	00B6Dh	2h	0.23
			10	12	108	2773	520	3465	0208h	00D89h	2h	0.29
	4 ch	59.94	12	14	432	3840	420	2145	01A4h	00861h	0h	0.34
			10	12	432	4480	420	2145	01A4h	00861h	0h	0.36
		29.97	12	14	216	2743	600	3003	0258h	00BBBh	1h	0.24
			10	12	216	2773	520	3465	0208h	00D89h	1h	0.29



Pixel Array Image in Window cropping 1.3 M (4:3) 2 × 2 Binning Mode



Drive Timing Chart for Window cropping 1.3 M (4:3) 2 × 2 Binning Mode

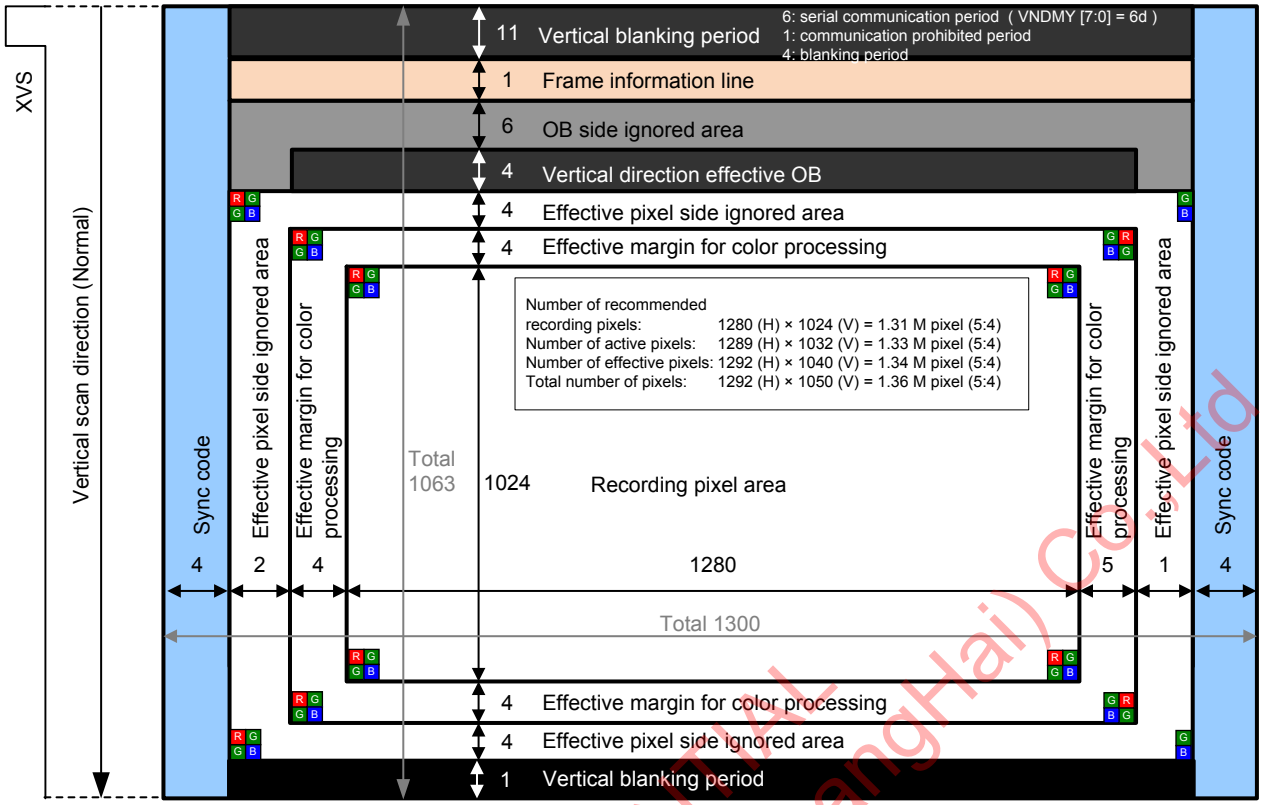
Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning

Register List of Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning

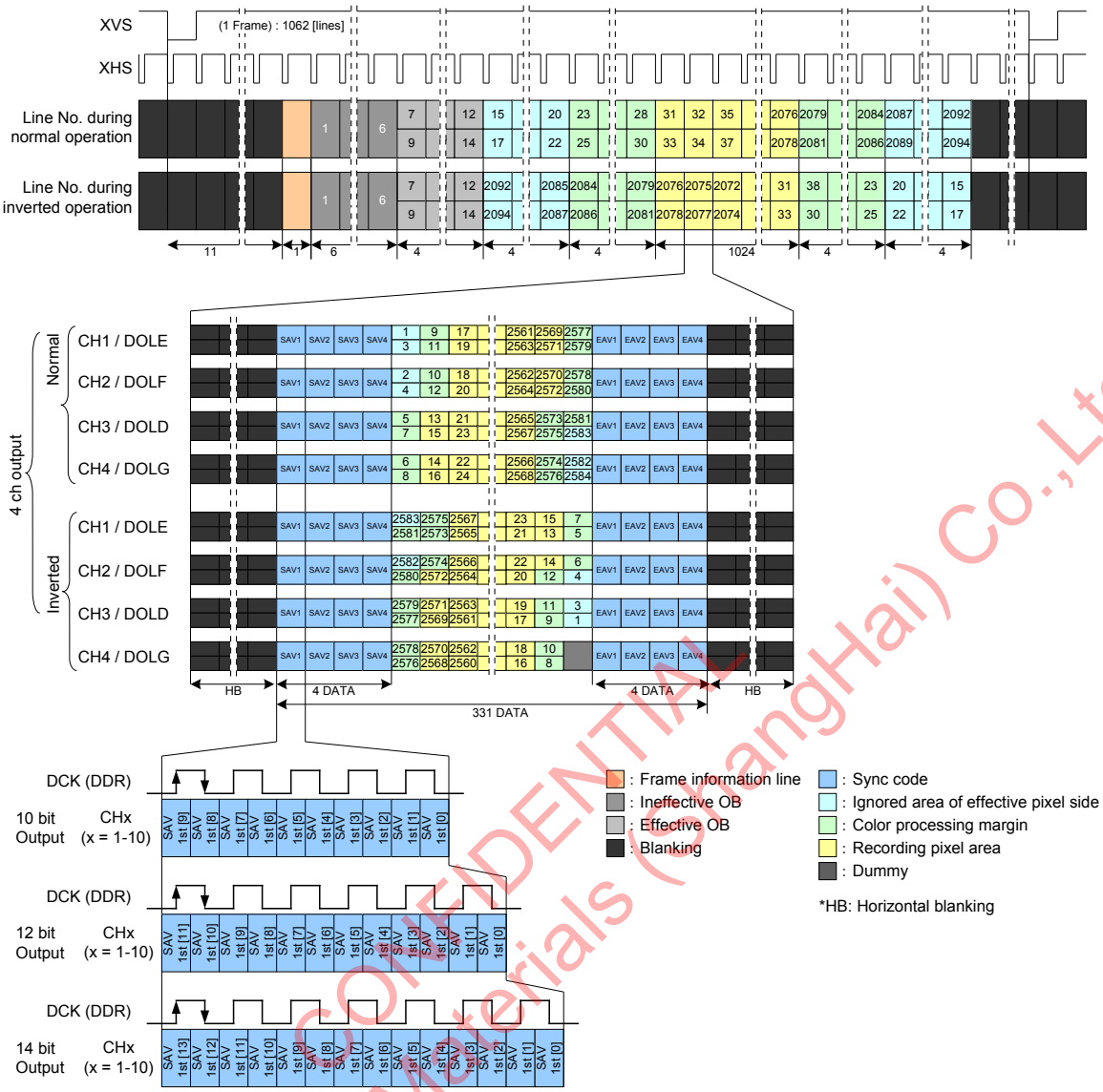
Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	23h	Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	2h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	1h	2 binning vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX [7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX [15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX [7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX [15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	59.94	12	14	216	4800	420	2145	01A4h	00861h	1h	0.34
			10	12	216	5600	420	2145	01A4h	00861h	1h	0.36
		29.97	12	14	108	2829	495	3640	01EFh	00E38h	2h	0.29
			10	12	108	2800	420	4290	01A4h	010C2h	2h	0.36
	8 ch	59.94	12	14	216	3840	420	2145	01A4h	00861h	1h	0.34
			10	12	216	4480	420	2145	01A4h	00861h	1h	0.36
		29.97	12	14	108	2816	616	2925	0268h	00B6Dh	2h	0.23
			10	12	108	2773	520	3465	0208h	00D89h	2h	0.29
	4 ch	59.94	12	14	432	3840	420	2145	01A4h	00861h	0h	0.34
			10	12	432	4480	420	2145	01A4h	00861h	0h	0.36
		29.97	12	14	216	2743	600	3003	0258h	00BBBh	1h	0.24
			10	12	216	2773	520	3465	0208h	00D89h	1h	0.29



Pixel Array Image in Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning Mode



Drive Timing Chart for Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning Mode

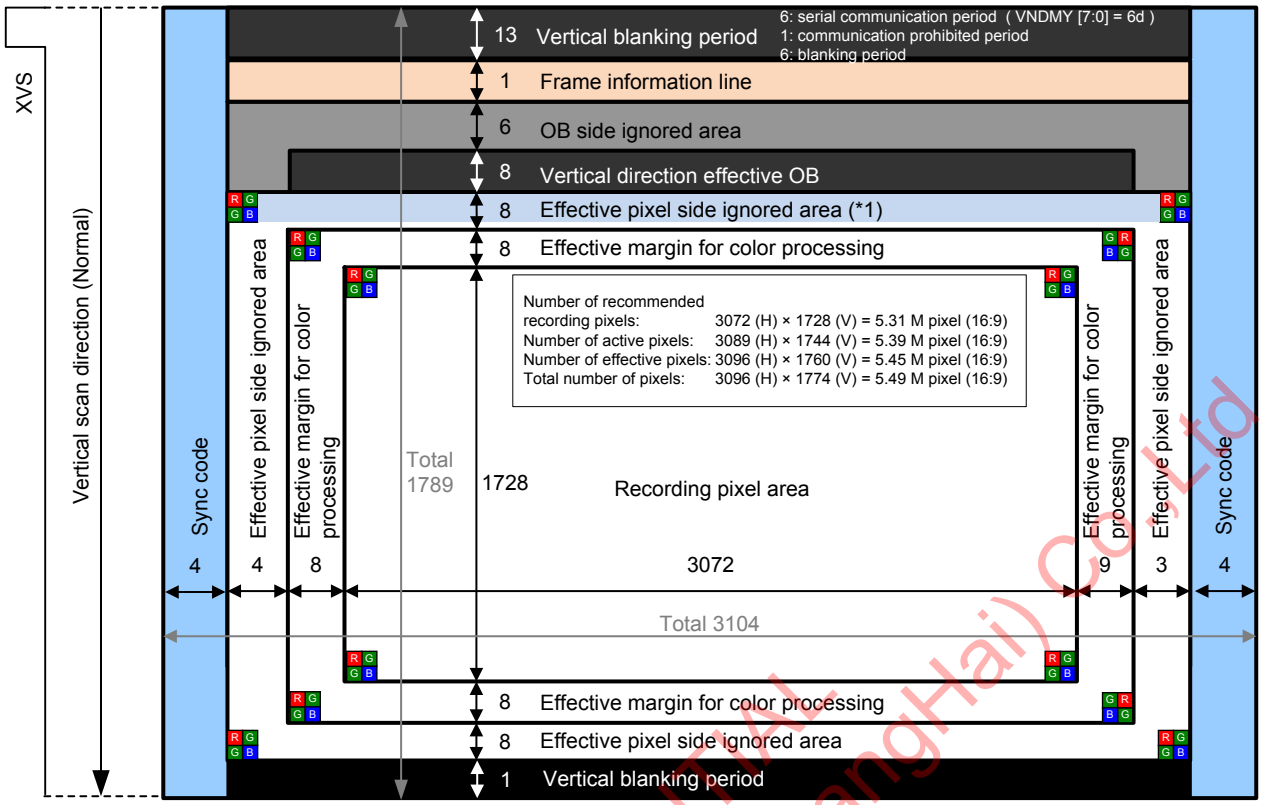
Window cropping 5.3 M (16:9)

Register List of Window cropping 5.3 M (16:9)

Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	00h	Window cropping 5.3 M (16:9)
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	3h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	0h	Normal vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX[7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX[15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX[7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX[15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

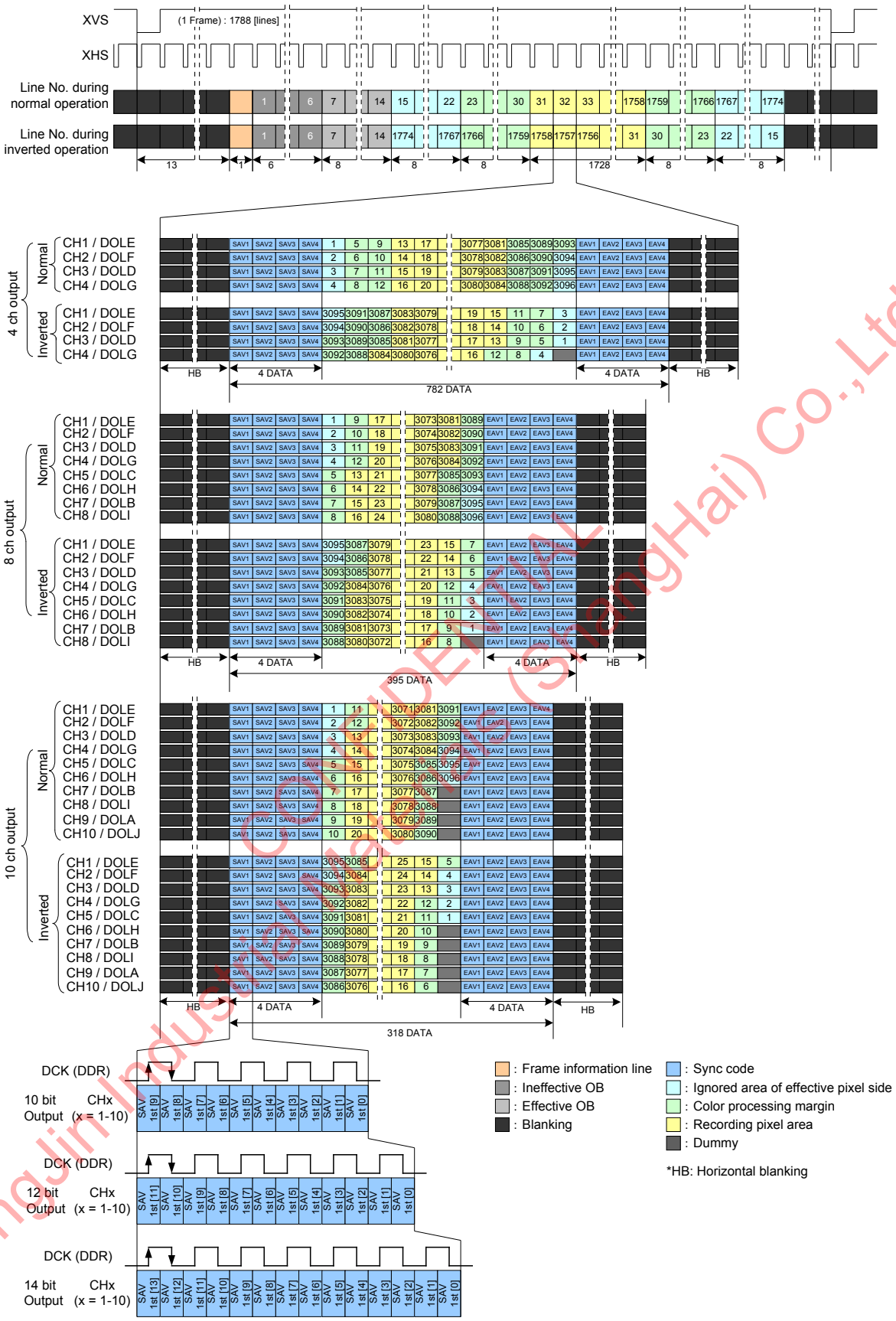
Window cropping 5.3 M (16:9) register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27 74.25 / 37.125	10 ch	60	12	12	594	4167	625	1980	0271h	07BCh	0h	0.29
			10	10	594	5000	625	1980	0271h	07BCh	0h	0.31
		30	14	14	297	3214	1125	2200	0465h	0898h	1h	0.28
			12	12	297	3300	990	2500	03DEh	09C4h	1h	0.18
			10	10	297	3300	825	3000	0339h	0BB8h	1h	0.23
	8 ch	60	12	12	594	3333	625	1980	0271h	07BCh	0h	0.29
			10	10	594	4000	625	1980	0271h	07BCh	0h	0.31
		30	14	14	594	5143	1125	2200	0465h	0898h	0h	0.28
			12	12	297	3333	1250	1980	04E2h	07BCh	1h	0.14
			10	10	297	3200	1000	2475	03E8h	09ABh	1h	0.19
	4 ch	30	14	14	594	3143	1375	1800	055Fh	0708h	0h	0.23
			12	12	594	3333	1250	1980	04E2h	07BCh	0h	0.14
			10	10	594	3168	990	2500	03DEh	09C4h	0h	0.19



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Pixel Array Image in Window cropping 5.3 M (16:9) Mode



Drive Timing Chart for Window cropping 5.3 M (16:9) Mode

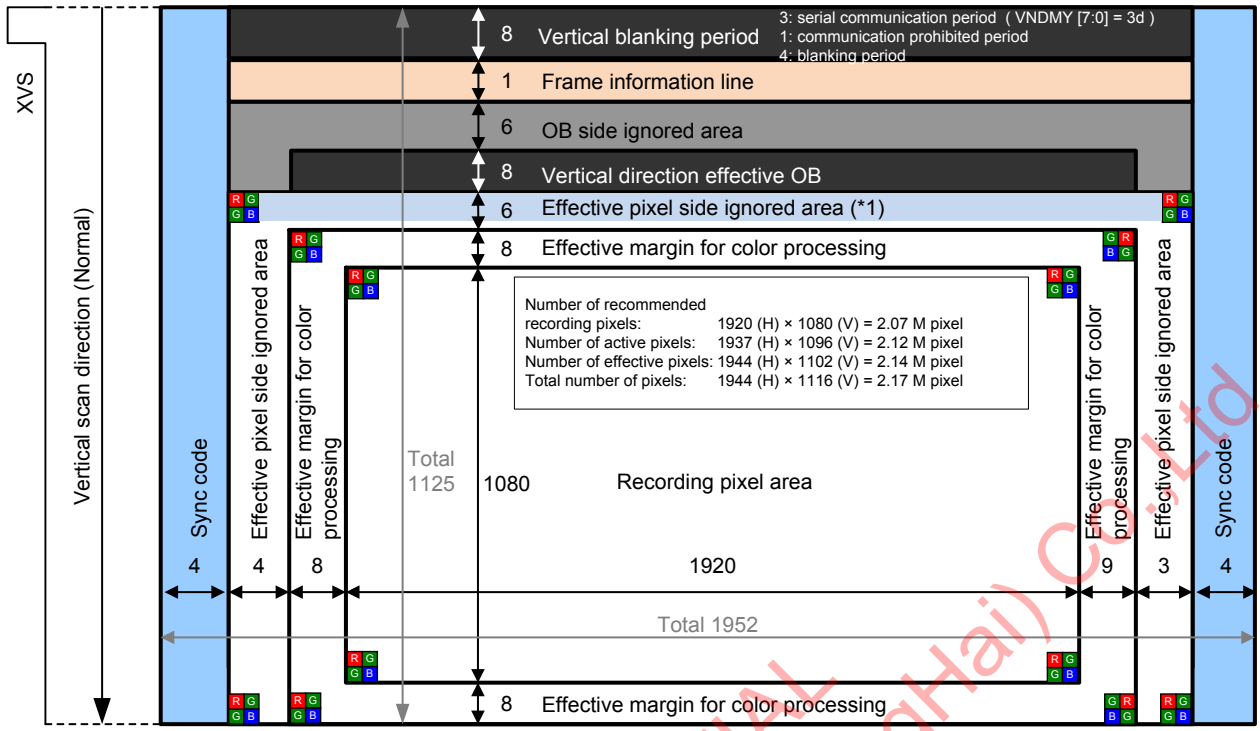
HD 1080p

Register List of HD 1080p

Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	01h	HD 1080p
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	0h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	0h	Normal vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	3h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX[7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX[15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX[7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX[15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

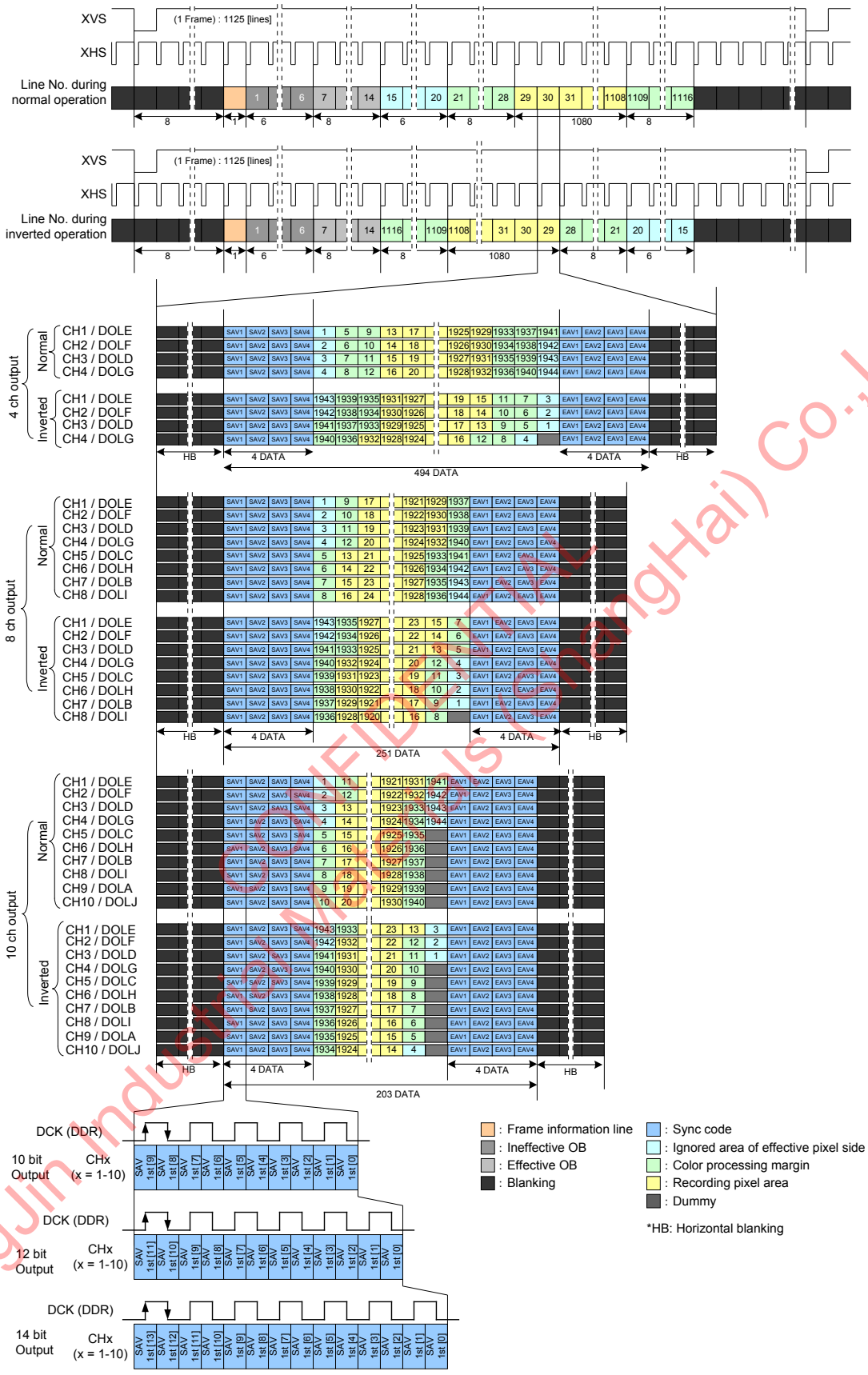
HD1080p register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27 74.25 / 37.125	10 ch	120	12	12	594	3667	550	1125	0226h	00465h	0h	0.33
			10	10	594	4400	550	1125	0226h	00465h	0h	0.35
		60	12	12	297	2083	625	1980	0271h	007BCh	1h	0.29
			10	10	297	2200	550	2250	0226h	008CAh	1h	0.35
		30	14	14	148.5	2143	1500	1650	05DCh	00672h	2h	0.21
	8 ch	120	12	12	594	2933	550	1125	0226h	00465h	0h	0.33
			10	10	594	3520	550	1125	0226h	00465h	0h	0.35
		60	12	12	297	2200	825	1500	0339h	005DCh	1h	0.22
			10	10	297	2112	660	1875	0294h	00753h	1h	0.29
		30	14	14	148.5	2057	1800	1375	0708h	0055Fh	2h	0.17
	4 ch	60	12	12	594	2000	750	1650	02EEh	00672h	0h	0.24
			10	10	594	2000	625	1980	0271h	007BCh	0h	0.31
		30	14	14	297	2057	1800	1375	0708h	0055Fh	1h	0.17



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Pixel Array Image in HD 1080p



Drive Timing in HD 1080p Mode

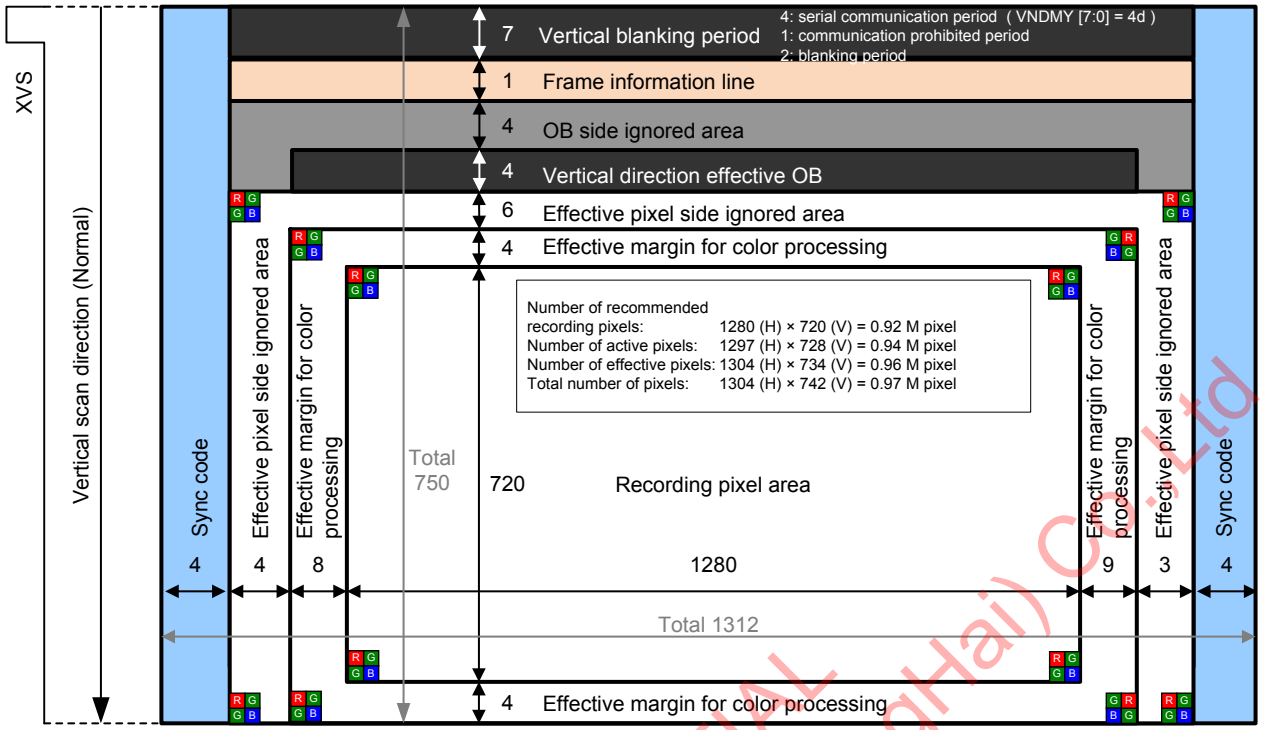
HD 720p 2 × 2 Binning

Register List of HD 720p 2 × 2 Binning

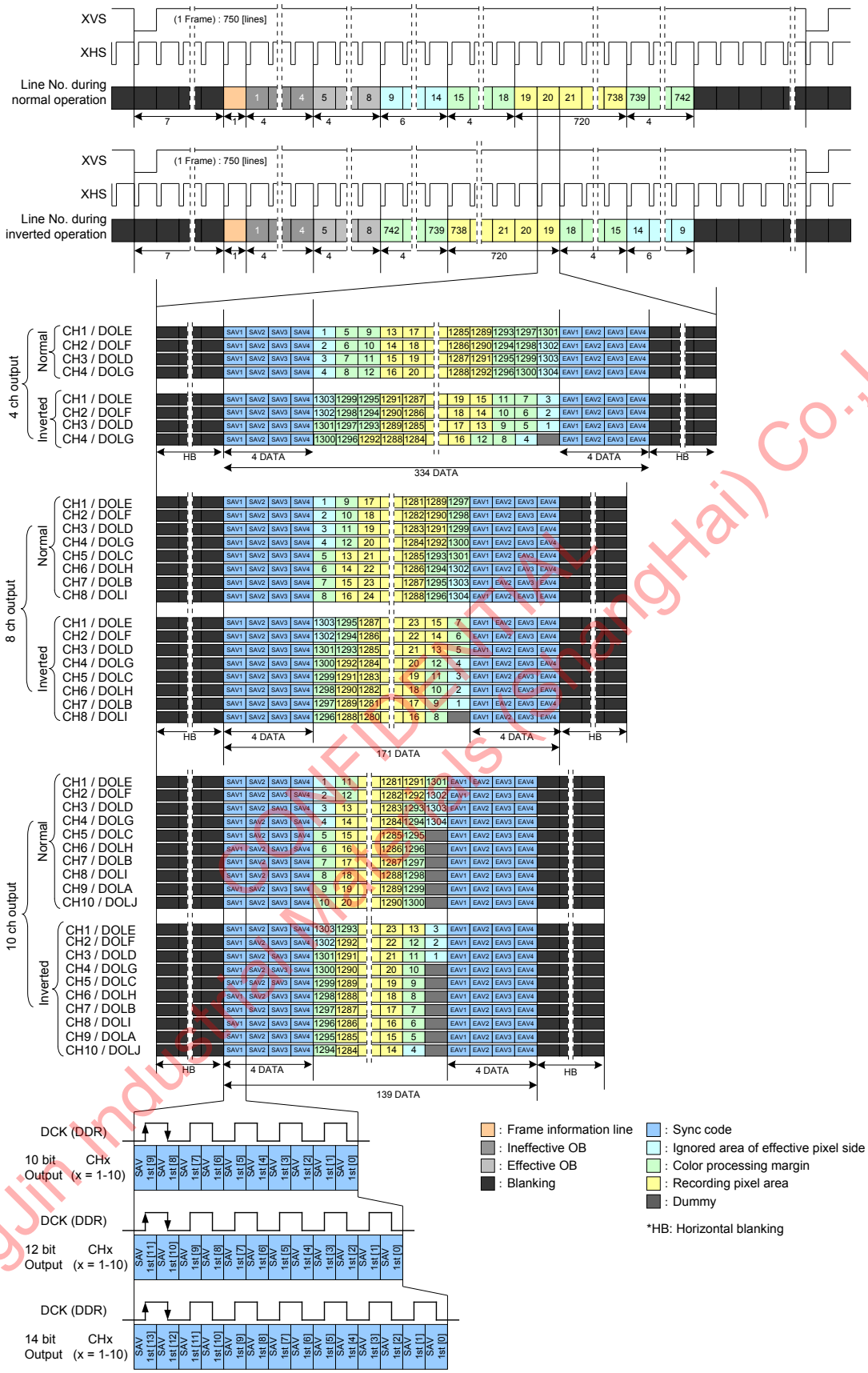
Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	24h	HD 720p 2 × 2 Binning
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	0h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	1h	2 binning vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	4h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX[7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX[15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX[7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX[15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting

HD720p 2 × 2 Binning register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27 74.25 / 37.125	10 ch	120	10	12	297	5000	375	1650	0177h	0672h	1h	0.41
		60	12	14	148.5	3143	550	2250	0226h	08CAh	2h	0.33
			10	12	148.5	3667	550	2250	0226h	08CAh	2h	0.28
		30	12	14	74.25	2829	990	2500	03DEh	09C4h	3h	0.18
			10	12	74.25	3667	1100	2250	044Ch	08CAh	3h	0.14
	8 ch	120	10	12	297	4000	375	1650	0177h	0672h	1h	0.41
		60	12	14	148.5	2857	625	1980	0271h	07BCh	2h	0.29
			10	12	148.5	2933	550	2250	0226h	08CAh	2h	0.28
		30	12	14	74.25	2857	1250	1980	04E2h	07BCh	3h	0.14
			10	12	74.25	2933	1100	2250	044Ch	08CAh	3h	0.14
	4 ch	120	10	12	594	4000	375	1650	0177h	0672h	0h	0.41
		60	12	14	297	2857	625	1980	0271h	07BCh	1h	0.29
			10	12	297	2933	550	2250	0226h	08CAh	1h	0.28
		30	12	14	148.5	2857	1250	1980	04E2h	07BCh	2h	0.14
			10	12	148.5	2933	1100	2250	044Ch	08CAh	2h	0.14



Pixel Array Image in HD 720p 2 × 2 Binning Mode

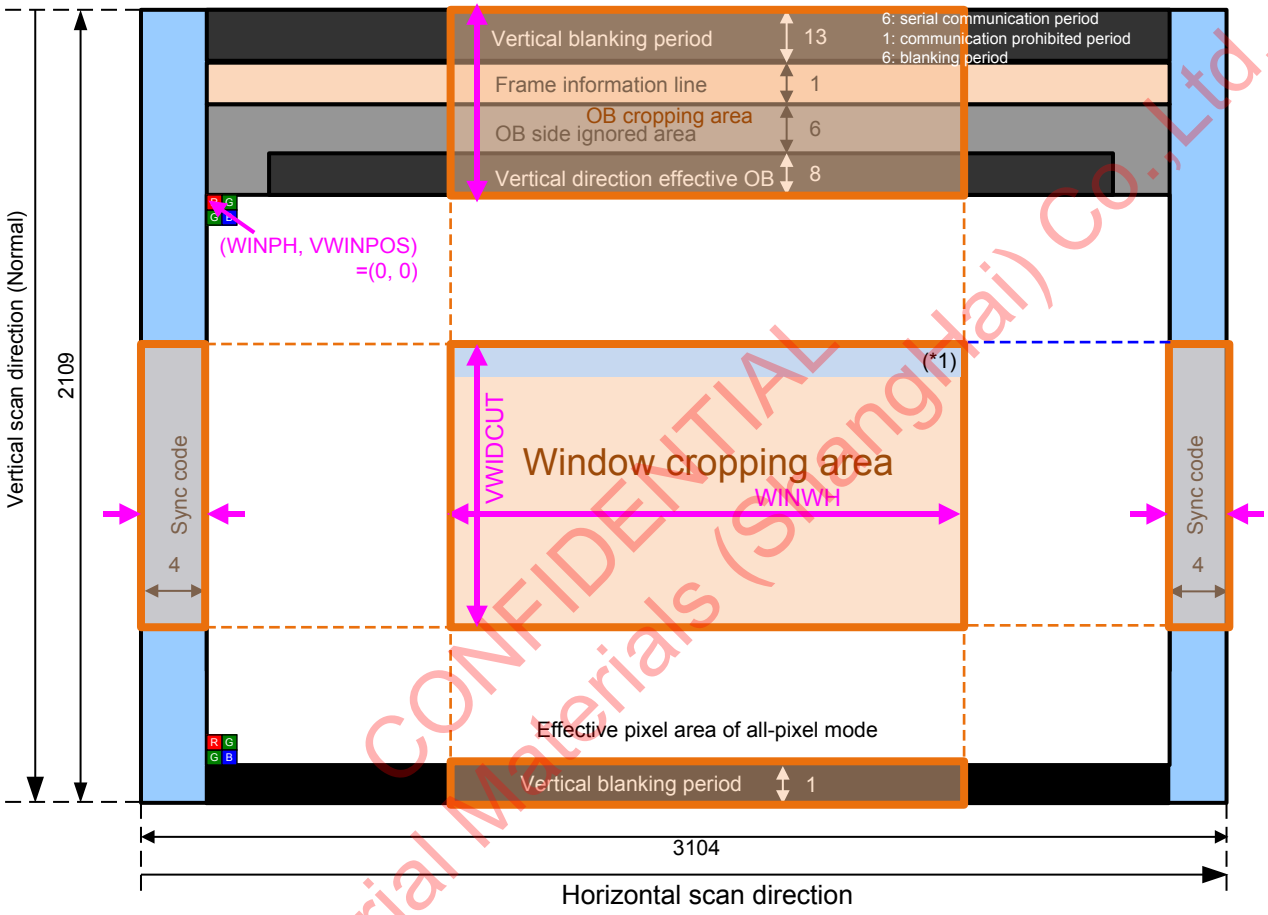


Drive Timing in HD 720p 2 × 2 Binning Mode

Arbitrary cropping

Sensor signals are cropped and read out in arbitrary positions.

Cropping position is set, regarding effective pixel start position as origin (0, 0).
Cropping is available from all-pixel scan mode and vertical, horizontal period and frame rate are fixed to the value for this mode.
Pixels cropped by horizontal cropping setting are output with left justified and that extends the horizontal blanking period. In vertical cropping, the number of image data is also output from cropping start line and that extends the vertical blanking period. Window cropping image is shown in the figure below.



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Image Drawing of Window Arbitrary Cropping Mode

Register List of Window Arbitrary Cropping Mode Setting

Setting item	Register details	Chip ID Address ( ) : I²C	bit	Initial value	Setting value	Remarks
MODE [5:0]	—	ID = 02h 0Eh (300Eh)	[5:0]	00h	00h	All-Pixel Scan 6.3 M (3:2)
WINMODE [3:0]	—	ID = 02h 0Fh (300Fh)	[7:4]	0h	0h	
TCYCLE [1:0]	—	ID = 02h 10h (3010h)	[1:0]	0h	0h	Normal vertical drive mode
VNDMY [7:0]	—	ID = 02h 66h (3066h)	[7:0]	6h	6h	Vertical setting of the period from reflection register updated timing to read start timing
VMAX [16:0]	VMAX [7:0]	ID = 02h 2Ch (302Ch)	[7:0]	00FFFh (4095d)	See table below.	Vertical (V) direction line number designation Designate by mode.
	VMAX [15:8]	ID = 02h 2Dh (302Dh)	[7:0]			
	VMAX [16]	ID = 02h 2Eh (302Eh)	[0]			
HMAX [15:0]	HMAX [7:0]	ID = 02h 2Fh (302Fh)	[7:0]	025Dh (605d)	See table below.	1H output pixel number designation Designate by mode.
	HMAX [15:8]	ID = 02h 30h (3030h)	[7:0]			
ADBIT [1:0]	—	ID = 02h 0Dh (300Dh)	[1:0]	1h	See remarks	ADC resolution designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
ADBITFREQ [1:0]	—	ID = 02h 0Dh (300Dh)	[3:2]	0h	See remarks	ADC mode setting 0d:AD14 bit AD10 bit HD720p 2 × 2 Binning 120 fps is excluded 1d:AD12 bit AD10 bit HD720p 2 × 2 Binning 120 fps Others:Setting prohibited
ODBIT [1:0]	—	ID = 02h 59h (3059h)	[1:0]	1h	See remarks	Output bit width designation 0h: 10 bit / 1h: 12 bit / 2h: 14 bit Setting prohibited other than above.
OPORTSEL [2:0]	—	ID = 02h 59h (3059h)	[6:4]	1h	See remarks	LVDS use channel number selection 0h: 10 ch / 1h: 8 ch / 3h: 4 ch Setting prohibited other than above.
STBLVDS [3:0]	—	ID = 02h 04h (3004h)	[3:0]	1h	See remarks	LVDS standby control 0h : 10 ch all active 1h : 8 ch active 3h : 4 ch active 7h to Fh : all standby Others:Setting prohibited
FREQ [1:0]	—	ID = 03h 01h (3101h)	[1:0]	0h	See table below.	LVDS output frequency setting
VWINSEL [0]	—	ID = 03h A5h (31A5h)	[0]	0h	1h	Arbitrary cropping (vertical) enable 0h: Normal 1h: Arbitrary cropping in vertical direction
VWINPOS [11:0]	VWINPOS [7:0]	ID = 03h A0h (30A0h)	[7:0]	000h	See next page.	Designation of upper left coordinate for cropping position (Vertical) Set by complement of 2. Settable range: - 2048d to +2047d
	VWINPOS [11:8]	ID = 03h A1h (31A1h)	[3:0]			
VWIDCUT [12:0]	VWIDCUT [7:0]	ID = 03h A2h (31A2h)	[7:0]	0000h	See next page.	Effective pixel window area width Settable range: 320d to 2080d
	VWIDCUT [12:8]	ID = 03h A3h (31A3h)	[4:0]			
WINENH [0]	—	ID = 03h A4h (31A4h)	[0]	0h	1h	Arbitrary cropping (horizontal) enable 0h: Normal 1h: Arbitrary cropping in horizontal direction
WINPH [10:0]	WINPH [7:0]	ID = 03h 9Ch (319Ch)	[7:0]	000h	See next page.	Designation of upper left coordinate for cropping position (Horizontal) Settable range: 0d to 3096d Set to become the multiple of four.
	WINPH [10:8]	ID = 03h 9Dh (319Dh)	[2:0]			
WINWH [11:0]	WINWH [7:0]	ID = 03h 9Eh (319Eh)	[7:0]	79Ch	See next page.	Effective pixel window area width Settable range: 376d to 3096d Set to become the multiple of four.
	WINWH [11:8]	ID = 03h 9Fh (319Fh)	[3:0]			

Restrictions on Window cropping mode

The register settings should satisfy the following conditions:

WINPH + WINWH ≤ 3096d
VWINPOS + VWIDCUT ≤ 2080d

376d ≤ WINWH ≤ 3096d
320d ≤ VWIDCUT ≤ 2080d

(Number of lines per frame) or VMAX ≥ VWIDCUT + 28

Set the WINPH and WINWH in 4-pixel units.

(Frame rate on Window cropping mode)

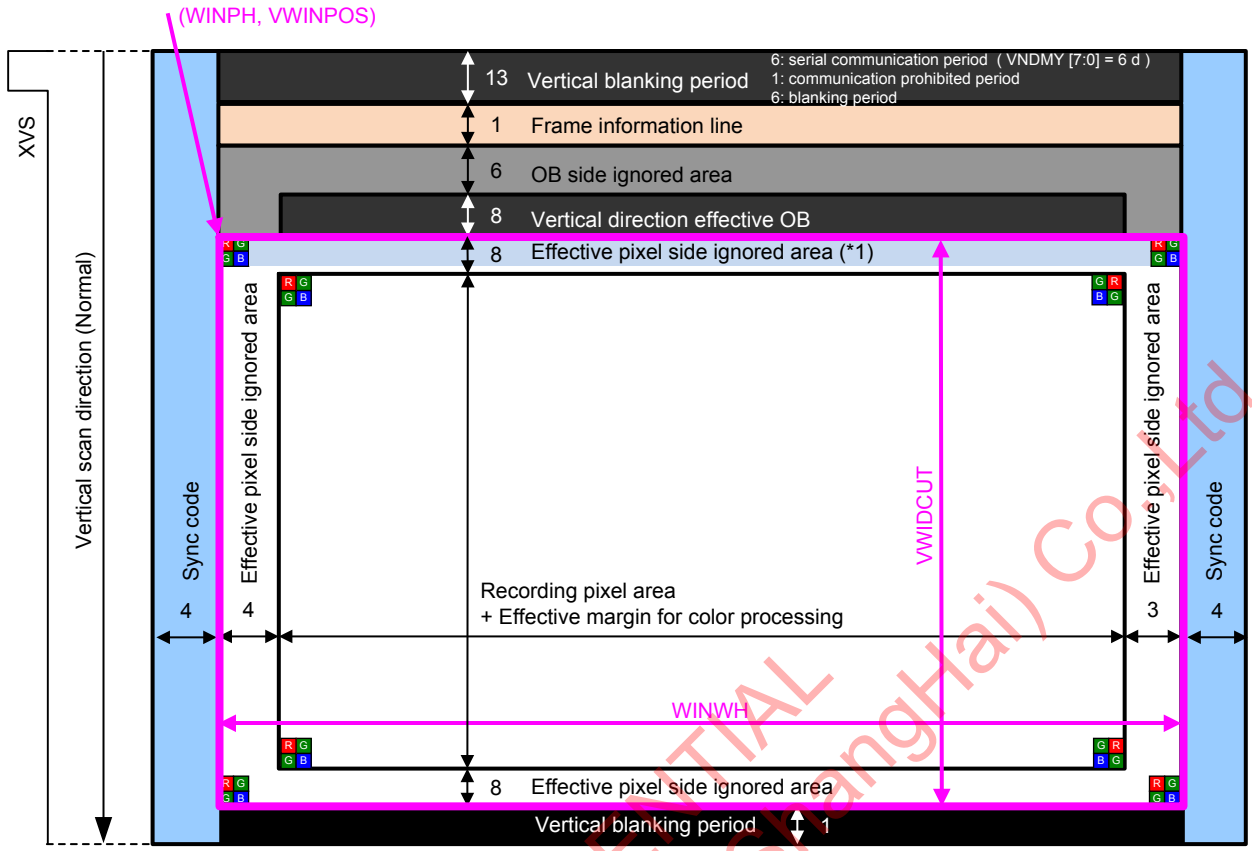
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1H period))

1H period (unit: [μs]) Fix 1H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".

The example of window cropping setting is shown below.
The frame rate is maximum setting as each image format. For adjustment of the frame rate, please adjust the VMAX or the number of lines per frame.
Number of lines per frame designated

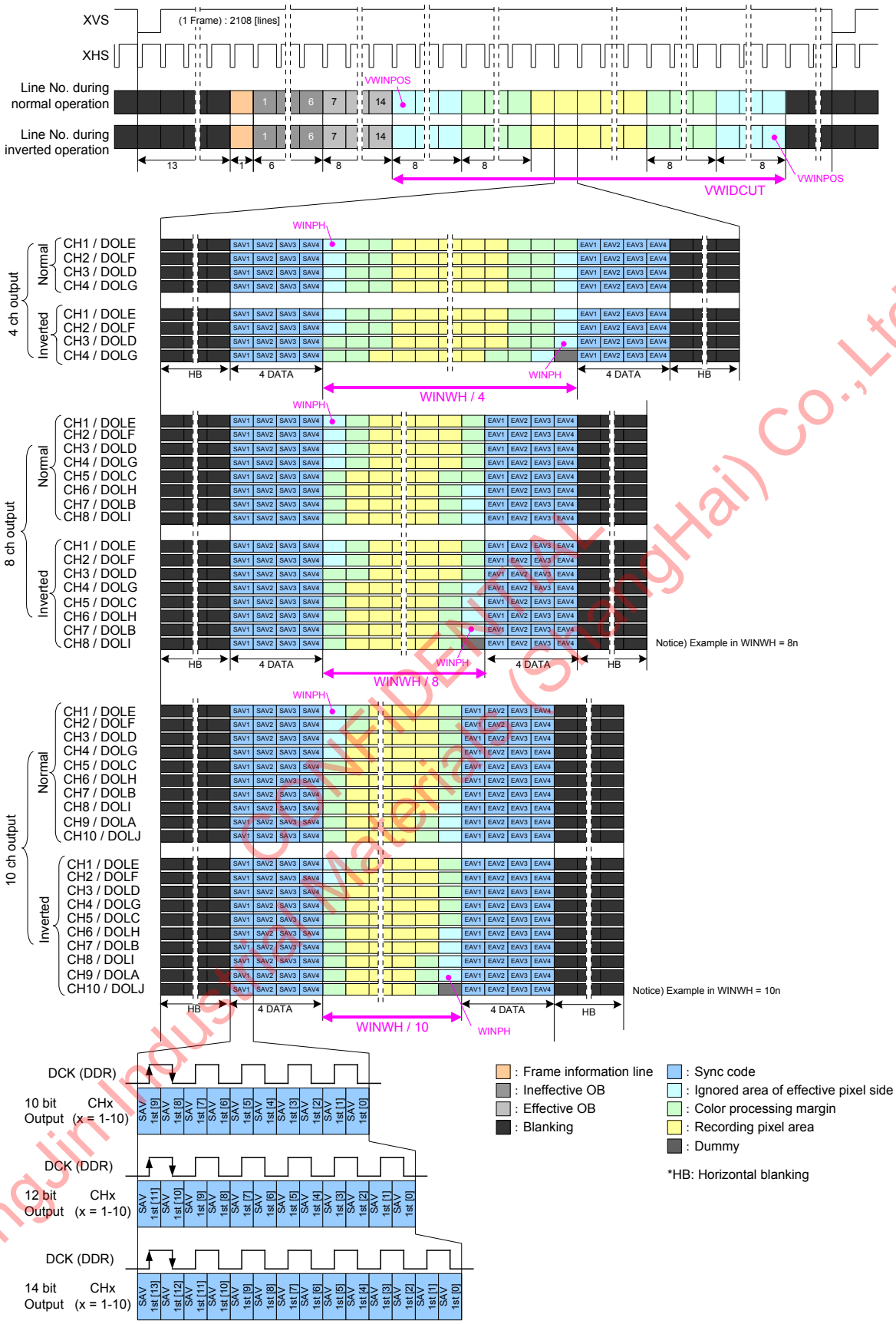
Window Arbitrary Cropping register setting details

INCK	Output	Frame Rate	ADC	Bit Width	Data Rate	H	H	V	HMAX [15:0]	VMAX [16:0]	FREQ [1:0]	t_{offset}
[MHz]	[ch]	[fps]	[bit]	[bit]	[Mbps/ch]	[pix]	[INCK]	[line]				[H]
54 / 27	10 ch	59.94	10	10	432	3360	420	2145	01A4h	00861h	0h	0.36
			14	14	432	4800	840	2145	0348h	00861h	0h	0.28
		29.97	12	12	432	3300	495	3640	01EFh	00E38h	0h	0.29
			10	10	432	3360	420	4290	01A4h	010C2h	0h	0.36
	8 ch	29.97	14	14	432	3840	840	2145	0348h	00861h	0h	0.28
			12	12	432	3200	600	3003	0258h	00BBBh	0h	0.24
			10	10	432	3226	504	3575	01F8h	00DF7h	0h	0.30
54 / 27 / 74.25 / 37.125	4 ch	29.97	10	10	594	3203	728	2475	03E9h	009ABh	0h	0.15



(*1) When vertical direction normal readout : The first line is shaded.
When vertical direction inverted readout : The first line is shaded. The next line is outputted only the blue pixel.

Pixel Array Image in Window Arbitrary Cropping



Drive Timing Chart for Window Arbitrary Cropping Mode

Description of Various Function

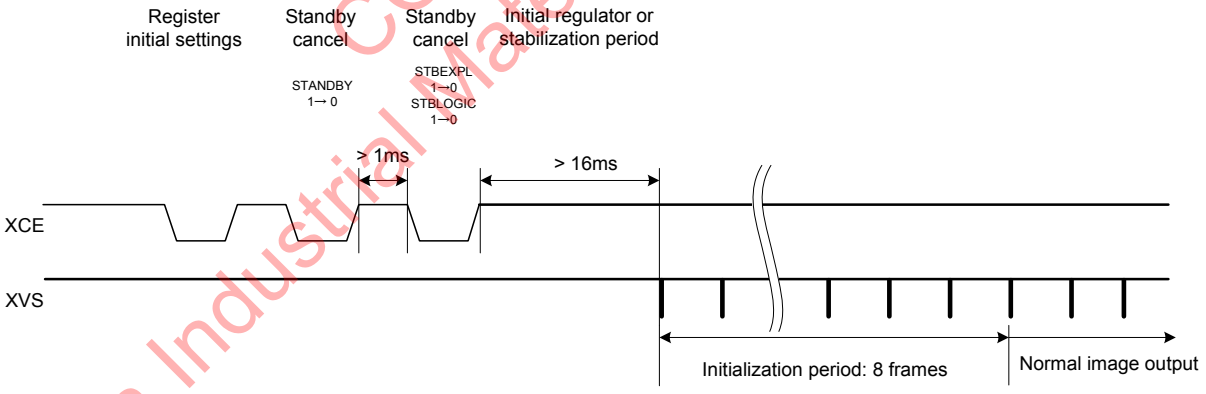
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY, STBLOGIC and STBEXPL.
Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Status	Remarks
	Register	Address ( ) : I^2C	bit				
STANDBY	—	00h (3000h)	[0]	1h	1h	Standby	Register communication is executed even in standby mode.
					0h	Normal operation	
STBEXPL	—	00h (3000h)	[1]	1h	1h	Standby	
					0h	Normal operation	
STBLOGIC	—	00h (3000h)	[2]	1h	1h	Standby	
					0h	Normal operation	

The serial communication registers hold the previous values. In addition, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY, STBLOGIC and STBEXPL register to “0”.
For details on the sequence of setting and cancel of standby mode, see the sensor setting flow after power on.
Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (16 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal.
See the section of "Operating mode" for the number of output data line and 1H period.

Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX[16:0] register, and the clock number in horizontal direction by the HMAX[15:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register details	Address ( ) : I^2C	Bit			
XMSTA	—	08h (3008h)	[0]	1h	1h: Master operation ready (initial value) 0h: Master operation start	The master operation starts by setting 0.
VMAX[16:0]	VMAX [7:0]	2Ch (302Ch)	[7:0]	00FFFh	See the item of each drive mode.	Master mode and slave mode common setting Number of lines per frame designated
	VMAX [15:8]	2Dh (302Dh)	[7:0]			
	VMAX [16]	2Eh (302Eh)	[0]			
HMAX[15:0]	HMAX [7:0]	2Fh (302Fh)	[7:0]	025D h	See the item of each drive mode.	Master mode and slave mode common setting Number of clocks per line designated
	HMAX [15:8]	30h (3030h)	[7:0]			
XVSLNG[1:0]	XVSLNG [1:0]	5Bh (305Bh)	[5:4]	0h	0h: 1H, 1h: 2H 2h: 4H, 3h: 8H	In master mode, XVS low level pulse width designated In slave mode, setting is invalid.
XHSLNG [1:0]	XHSLNG [1:0]	5Ch (305Ch)	[5:4]	0h	0h: 16 clock 1h : 32 clock 2h : 64 clock 3h : 128 clock (based on INCK)	In master mode XHS low level pulse width designated In slave mode, setting is invalid.
XVSOUTSEL [1:0]	—	5Eh (305Eh)	[1:0]	0h	0h: High level output 2h: VSYNC output Others: Setting prohibited	In master mode set to 2h. In slave mode set to 0h.
XHSOUTSEL [1:0]	—		[3:2]	0h	0h: High level output 2h: HSYNC output Others: Setting prohibited	In master mode set to 2h. In slave mode set to 0h.

Gain Adjustment Function

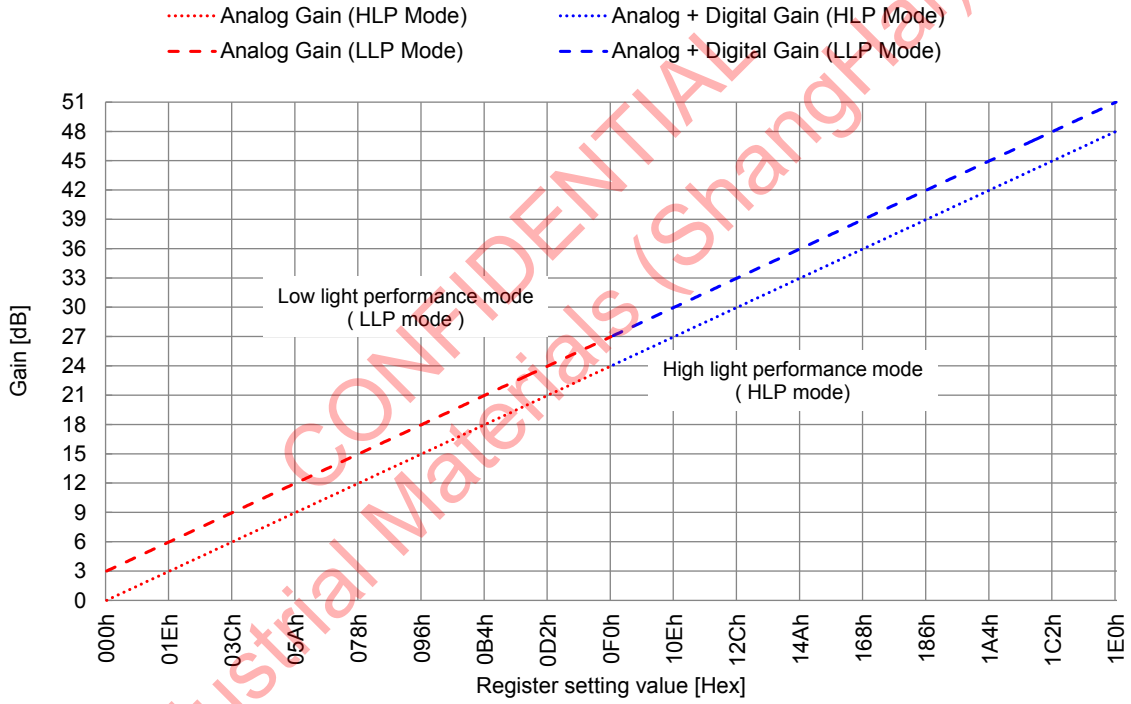
PGC Outline

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting. The same setting is applied in all colors.
In addition, the readout drive mode can be switched to High light performance mode to support imaging under high illumination or Low light performance mode to make much of visibility under low illumination to increase the sensor output level by setting the register LP_MODE [7:0]. In standard imaging, setting to Low light performance mode is recommended.

The value which is ten times the gain is set to register as hexadecimal number.

Example)
When set to 6 dB in High light performance mode:
6 × 10 = 60d, GAIN = 3Ch

When set to 6 dB in Low light performance mode:
(6 - 3) × 10 = 30 d, GAIN = 01 Eh



List of PGC Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value / Setting range	Remarks
	Register details	Address ( ) : I^2C	bit			
LP_MODE	—	1Bh (301Bh)	[7:0]	0Ch	00h	High light Performance mode
					1Eh	Low light Performance mode
GAIN	GAIN [7:0]	1Fh (301Fh)	[7:0]	000h	000h-1FEh (0d-480d)	Setting value: Low light performance mode (Gain [dB] - 3) × 10 High light Performance mode Gain [dB] × 10
	GAIN [8]	20h (3020h)	[0]			

Black Level Adjustment Function

The black level offset (offset variable range: 000h to FFFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [8:0] register. When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

*Use with values shown below is recommended.
10 bit output: 32h (50 d)
12 bit output: C8h (200 d)
14 bit output: 320h (800 d)

List of Black Level Adjustment Register

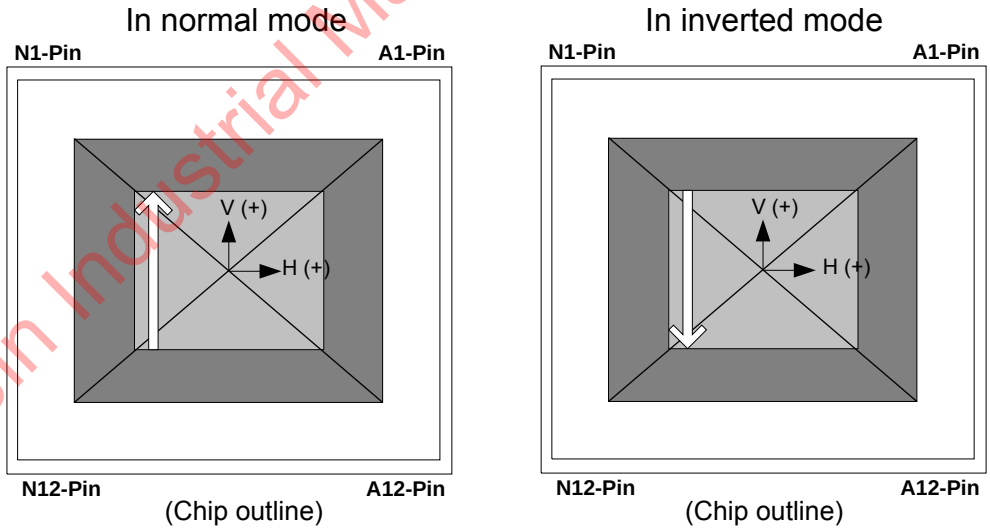
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
BLKLEVEL [11:0]	BLKLEVEL [7:0]	15h (3015h)	[7:0]	03Ch	000h to FFFh
	BLKLEVEL [11:8]	0Bh (3015h)	[3:0]		

Vertical Normal Operation and Inverted Drive

The sensor readout direction (normal/inverted) in vertical direction can be switched by the VREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Vertical Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
VREVERSE	—	0Fh (300Fh)	[0]	0h	0h: Normal (Initial value) 1h: Inverted



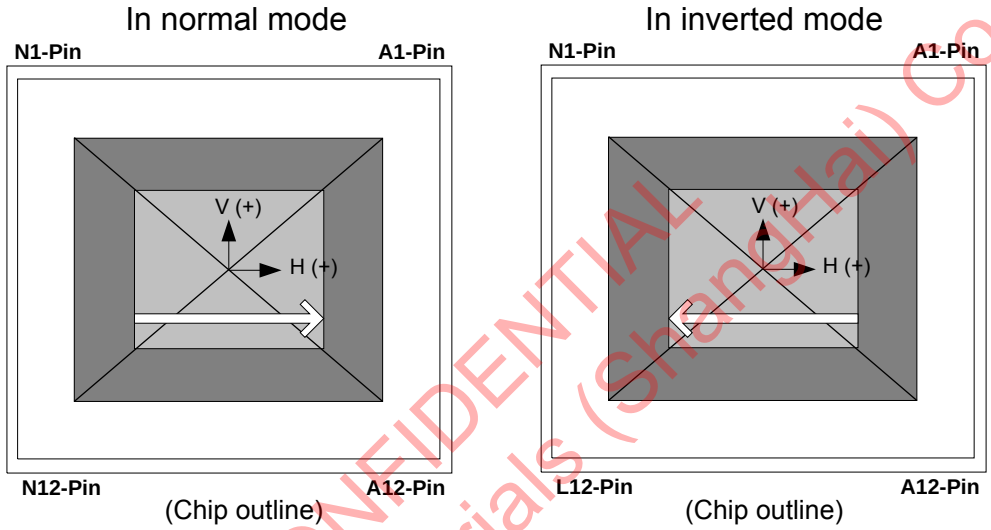
Normal and Inverted Drive Outline in Vertical Direction (Top View)

Horizontal Normal Operation and Inverted Drive

The sensor readout direction (normal/inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes.
One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Horizontal Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
HREVERSE	—	0Fh (300Fh)	[1]	0h	0h: Normal (Initial value) 1h: Inverted



Normal and Inverted Drive Outline in Horizontal Direction (Top View)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - (SHS1) × (1H period) + t_{OFFSET}

Note) 1. The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
2. See “Operating Modes” for the 1H period.
3. t_{OFFSET} is the integration time error. Please refer to the register setting table in each drive mode.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

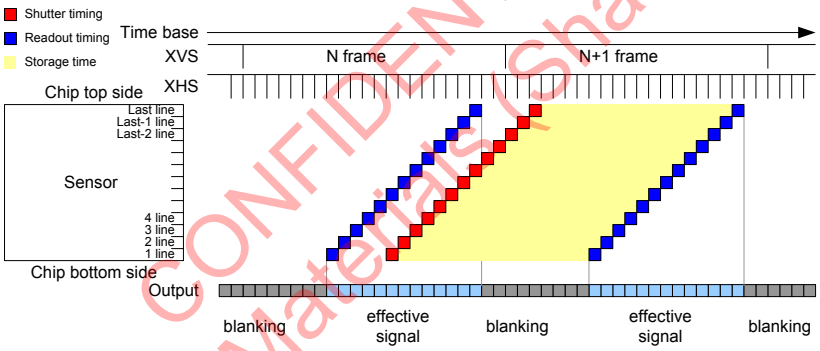


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 [16:0] register.
Set SHS1 [16:0] to a value between 0 and (Number of lines per frame - 1).
When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [16:0] register. The number of lines per frame differs according to the operating mode. See the item of drive mode.

Registers Used to Set the Integration Time in 1H Units

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
SHS1 [16:0]	SHS1 [7:0]	34h (3034h)	[7:0]	00008h	Sets the shutter sweep time. 0 to (Number of lines per frame - 1)
	SHS1 [15:8]	35h (3035h)	[7:0]		
	SHS1 [16]	36h (3036h)	[0]		
VMAX [16:0]	VMAX [7:0]	2Ch (302Ch)	[7:0]	00FFFh	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	2Dh (302Dh)	[7:0]		
	VMAX [16]	2Eh (302Eh)	[0]		

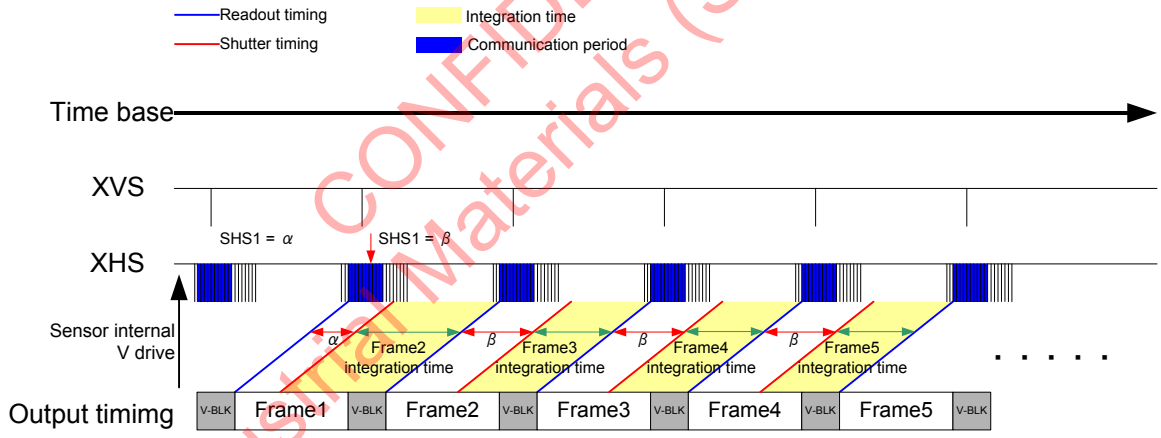


Image Drawing of Integration Time Control within a Frame

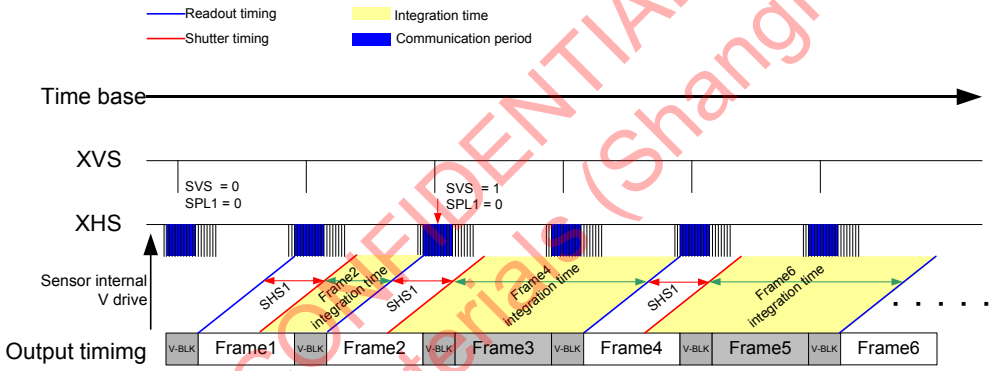
Long Exposure Operation

The vertical sync signal XVS can be subsampled inside the sensor according to the SVS register. The vertical sync signal period is treated as SVS + 1 inside the sensor. When setting the electronic shutter during the vertical sync signal subsampling period, the SPL1 register is available.

Register Name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I²C	bit		
SVS [9:0]	SVS [7:0]	41h (3041h)	[7:0]	000h	Specifies the integration shutdown vertical period. Integration time = Setting value + 1 frame
	SVS [9:8]	42h (3042h)	[1:0]		
SPL1 [9:0]	SPL1 [7:0]	43h (3043h)	[7:0]	000h	Designates the number of sweep frames.
	SPL1 [9:8]	44h (3044h)	[1:0]		

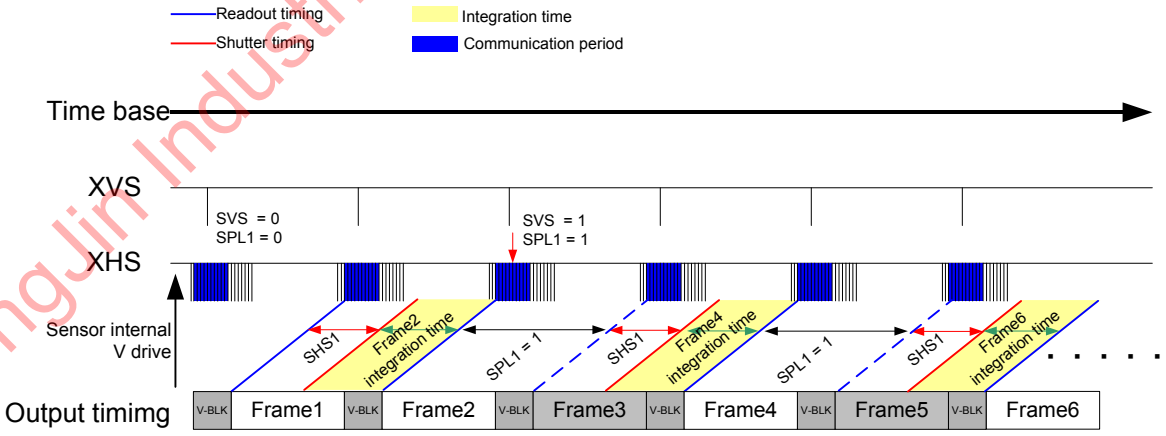
Note) The SVS and SPL1 register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.
Then the maximum of long time exposure is approximately 1 second.

Example of Electronic Shutter Operation 1



Example of SVR operation

Example of Electronic Shutter Operation 2



Example of SVR and SPL operation

Signal Output

Output Pin Settings

The output formats of this sensor support Low voltage LVDS serial (4 ch / 8 ch / 10 ch switching) DDR output. Each mode is set using the register OPORTSEL [2:0]. The table below shows the output format settings.

Settings for Output Format

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Description
	Register details	Address ( ) : I^2C	bit			
OPORTSEL [2:0]	—	59h (3059h)	[6:4]	1h	0h	Low voltage LVDS serial 10 ch DDR output
					1h	Low voltage LVDS serial 8 ch DDR output
					3h	Low voltage LVDS serial 4 ch DDR output
					Setting prohibited other than above.	

Each output pin is shown in the table below when setting low-voltage LVDS serial 4 ch/8 ch/10 ch output.

Output Pins for Low voltage LVDS Serial mode

DLOP / DLOM	Low voltage LVDS serial DDR output		
	4 ch output	8 ch output	10 ch output
DLOPA / DLOMA	Hi-Z	Hi-Z	CH9
DLOPB/ DLOMB	Hi-Z	CH7	CH7
DLOPC / DLOMC	Hi-Z	CH5	CH5
DLOPD / DLOMD	CH3	CH3	CH3
DLOPE / DLOME	CH1	CH1	CH1
DLOPF / DLOMF	CH2	CH2	CH2
DLOPG / DLOMG	CH4	CH4	CH4
DLOPH / DLOMH	Hi-Z	CH6	CH6
DLOPI / DLOMI	Hi-Z	CH8	CH8
DLOPJ / DLOMJ	Hi-Z	Hi-Z	CH10

Low-voltage LVDS serial 4 ch / 8 ch / 10 ch output format is shown in the figure below.

When setting 4 ch, after four data of SAV is output in the order of CH1, CH2, CH3 and CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1, CH2, CH3 and CH4 respectively.

When setting 8 ch, after four data of SAV is output in the order of CH1 to CH8 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH8 respectively.

When setting 10 ch, each pixel data is also output in the same order as well as the 4 ch and 8 ch setting.

Data is sent MSB first. For details, see drive timing in each mode in the section of "Operation Mode".

Low-voltage LVDS Serial 4 ch / 8 ch / 10 ch Output Format

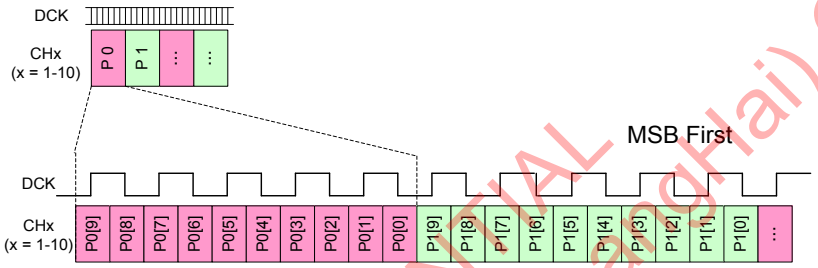
Output Pin Bit Width Selection

The output pin width can be selected from 10-bit, 12-bit or 14-bit output using the register ODBIT.
Sync code is also output according to the output bit width selected by the register ODBIT.

Output Pin Bit Width Selection Setting Register

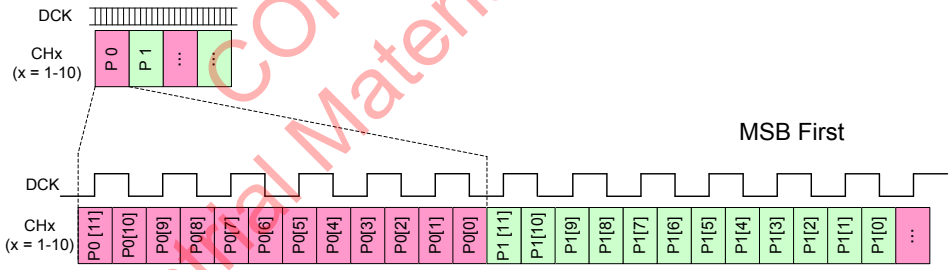
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
ODBIT [1:0]	—	59h (3059h)	[1:0]	1h	0h: 10 bit 1h: 12 bit 2h : 14 bit 3h : Setting prohibited

ODBIT = 0h (Low voltage LVDS serial 10 bit output)



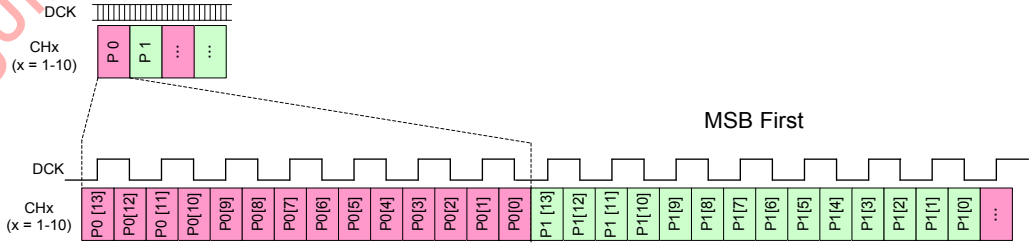
Example of format output when Low voltage LVDS serial 10 bit output

ODBIT = 1h (Low voltage LVDS serial 12 bit output)



Example of format output when Low voltage LVDS serial 12 bit output

ODBIT = 2h (Low voltage LVDS serial 14 bit output)



Example of format output when Low voltage LVDS serial 14 bit output

Internal A/D Conversion Bit Width Setting

The width of internal A/D conversion bits can be selected from 10 bits, 12 bits or 14 bits by the register ADBIT. Selectable conversion bit width is restricted according to operating mode.

Output Signal Resolution Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
ADBIT	—	0Dh (300Dh)	[1:0]	1h	A/D conversion bit width setting 0h: 10 bit 1h: 12 bit 2h : 14 bit 3h : Setting prohibited
ODBIT	—	59h (3059h)	[1:0]	1h	Output bit width setting 0h: 10 bit 1h: 12 bit 2h: 14 bit 3h: Setting prohibited

Output bit width setting

The set of output bit width is decided from A/D-conversion bit width and the operational mode. set up output bit width with reference to the following table.

A/D bit width setting ADBIT [1:0]		Output bit width setting ODBIT [1:0]		Normal operation	2 × 2 Binning
0h	10 bit	0h	10 bit	Recommended setting	Setting prohibited
		1h	12 bit	Setting prohibited	Recommended setting
		2h	14 bit	Setting prohibited	Setting prohibited
1h	12 bit	0h	10 bit	Setting prohibited	Setting prohibited
		1h	12 bit	Recommended setting	Setting prohibited
		2h	14 bit	Setting prohibited	Recommended setting
2h	14 bit	0h	10 bit	Setting prohibited	Setting prohibited
		1h	12 bit	Setting prohibited	Setting prohibited
		2h	14 bit	Recommended setting	Setting prohibited

Readout Viewing Angle

The registers related to readout viewing angle setting are shown in the table below.

Registers Related to Readout Viewing Angle

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
MODE [5:0]	—	0Eh (300Eh)	[5:0]	00h	00h: All-pixel cropping 01h: HD 1080p 23h: 2 × 2 binning 24h: HD 720p 2 × 2 binning Others: Setting prohibited
WINMODE [3:0]	—	0Fh (300Fh)	[7:4]	0h	0h: All pixel (6 M, HD 1080, HD 720) 1h: Window cropping (4:3) 2h: Window cropping (5:4) 3h: Window cropping (16:9) 4h to Fh: Setting prohibited

Output Signal Range

The sensor output has 10 bit, 12 bit or 14 bit gray scale according to the setting. The output is not performed at full range and the range is the values shown in the table below.
The gray scale at maximum level is output only in the sync code. See the item of "Operating Modes" and "Sync Code" for the sync code.

Output Gradation and Output Range

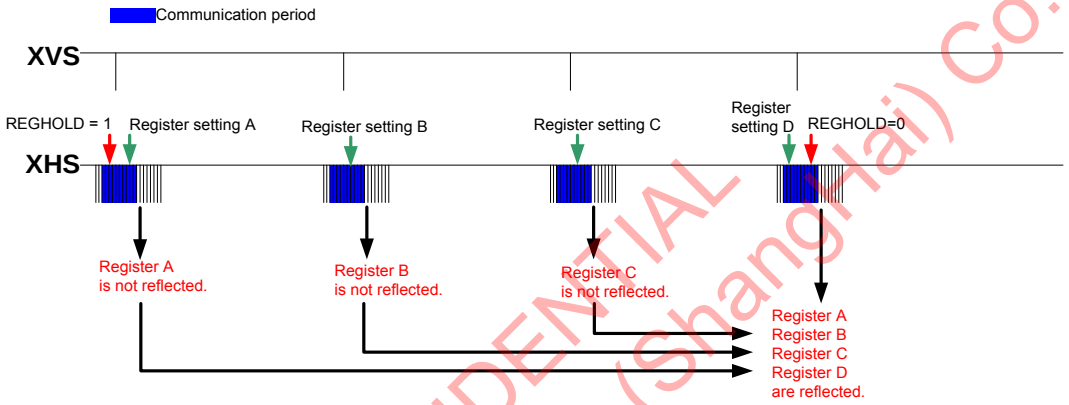
Output Gradation	Output value	
	Min.	Max.
10 bit	001h	3FEh
12 bit	001h	FFEh
14 bit	001h	3FFEh

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register Hold Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
REGHOLD	—	07h (3007h)	[0]	0h	0h: Invalid 1h: Valid (register hold)



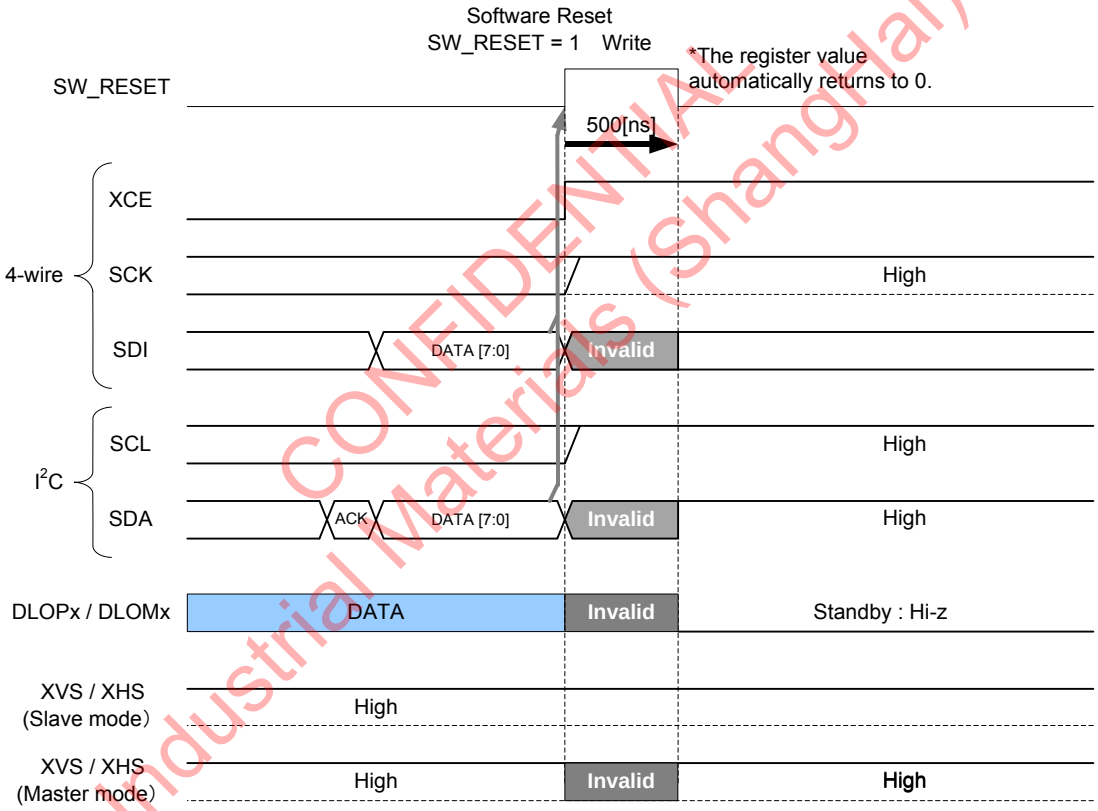
Register Hold Setting

Software Reset

Software reset can be performed by register setting using the register SW_RESET.
However, the communication to continuous address can not use. In I^2C communication, sensor not return ACK when SW_RESET is transferred.
Sensor reset is performed by setting SW_RESET = 1. The registers become initial state and standby 500 ns after setting SW_RESET = 1.
(The SW_RESET signal returns to "0" automatically.) DLOPx, DLOMx, DCKPx and DCKMx become standby (Hi-Z).
The XVS and XHS output High in master mode. Input High to the XVS and XHS before setting SW_RESET = 1 in slave mode. Follow the sequence in the item of "Standby Mode" to perform register initial setting and standby cancel from standby state.

Software Reset Register Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register details	Address ( ) : I^2C	bit		
SW_RESET	—	09h (3009h)	[0]	0h	0h: Normal operation 1h: Reset



Software Reset

Mode Transitions

When changing the operating mode during sensor drive operation, first set the sensor to all-pixel scan mode, and then it again to the desired operating mode. An invalid frame of one frame generates during mode transition. An invalid frame of one frame generates as well as when changing frame rate in the same operating mode. The table below shows the number of invalid frames generated by transition between the various modes. Data is output from sensor during the invalid frame period, but the output values may reflect the integration time or may not be uniform on the screen, or a partially saturated image may be output.

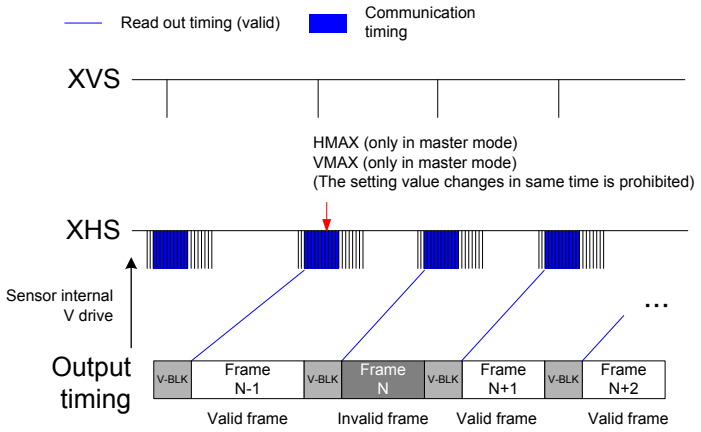
When changing input INCK frequency (register FREQ [1:0]) or when operating mode transition that changes output bit width (register ODBIT[1:0]) or number of output channels (register OPORTSEL [2:0]), always start the operation via sensor standby after changing mode during standby following the standby cancel sequence.

When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High/Low level width in front and behind of the INCK pulse at the frquency change.

Number of Invalid Frames Generated during Mode Transitions

Mode transition			Number of invalid frames
All-Pixel Scan 6.3 M (3:2)	→	Window cropping 5.0 M (4:3)	1
	→	Window cropping 5.2 M (5:4) QSXGA	
	→	All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning	
	→	Window cropping 1.3 M (4:3) 2 × 2 Binning	
	→	Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning	
Window cropping 5.0 M (4:3)	→	All-Pixel Scan 6.3 M (3:2)	
Window cropping 5.2 M (5:4) QSXGA	→		
All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning	→		
Window cropping 1.3 M (4:3) 2 × 2 Binning	→		
Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning	→		

Mode transition			Number of invalid frames
Window cropping 5.3 M (16:9)	→	HD 1080p	1
	→	HD 720p 2 × 2 Binning	
HD 1080p	→	Window cropping 5.3 M (16:9)	
HD 720p 2 × 2 Binning	→		
HD 1080p	→	HD 720p 2 × 2 Binning	
HD 720p 2 × 2 Binning	→	HD 1080p	2



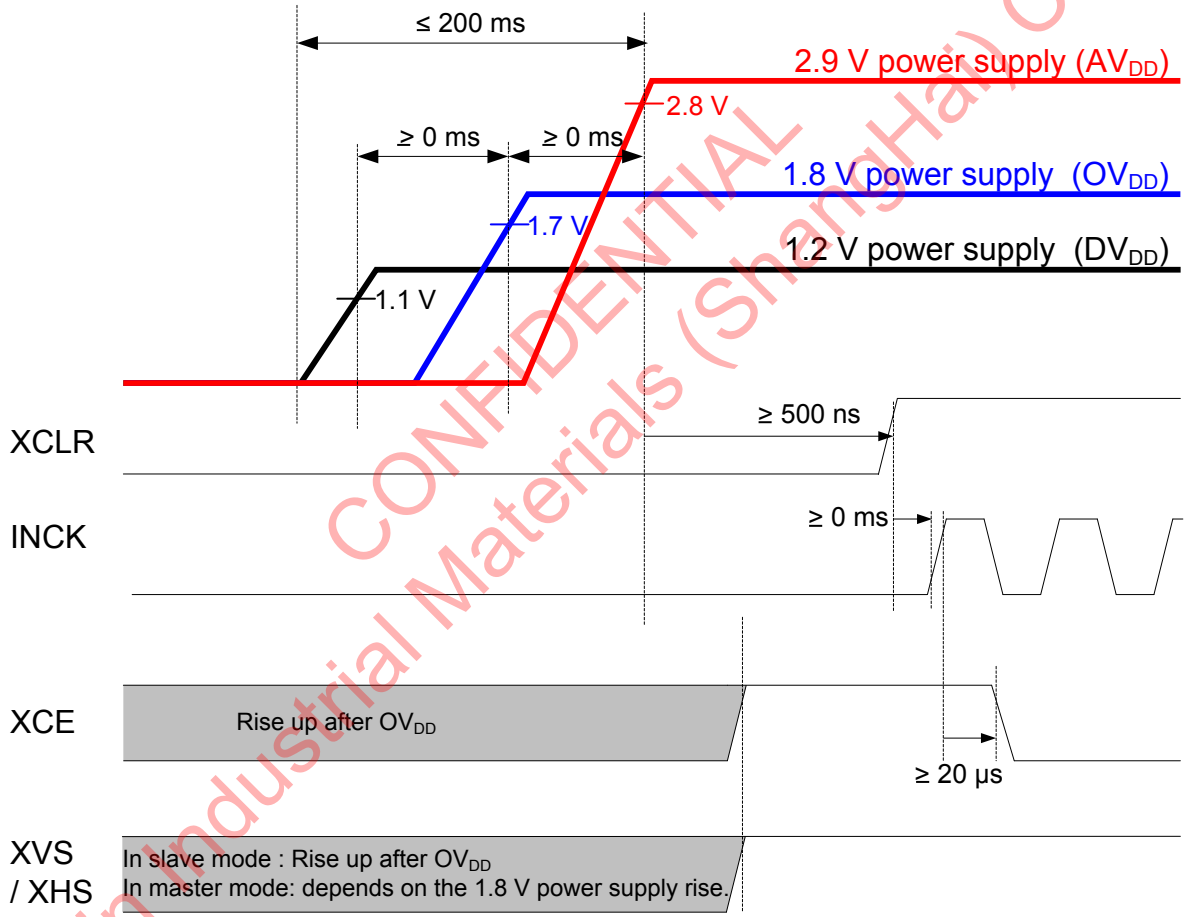
*When changing the drive mode also changes the frame period, the number of invalid frames is counted according to the frame period after the change.

Power-on / off Sequence

Power-on Sequence

Follow the sequence below to turn On the power supplies.

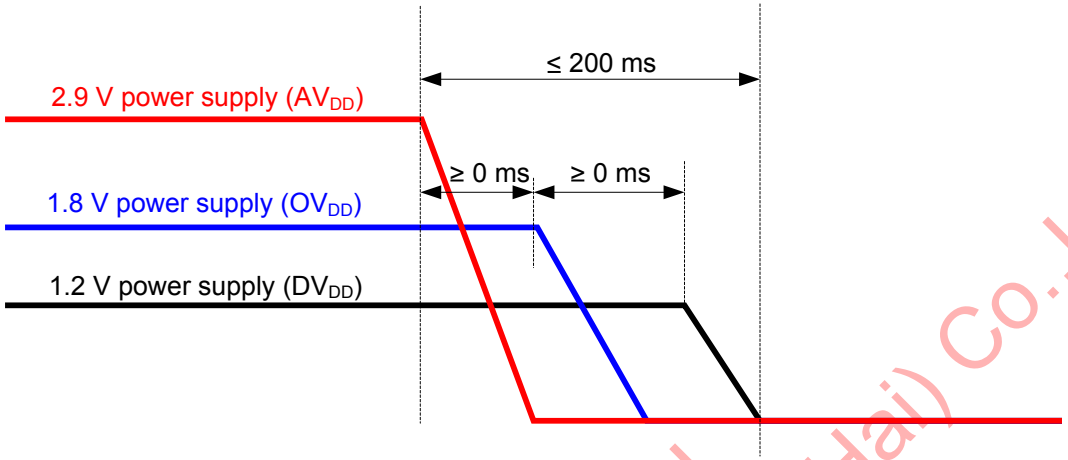
1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DVDD) →1.8 V power supply (OVDD) → 2.9 V power supply (AVDD). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.) In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OVDD).
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after stabilizing the input of the master clock (INCK). A period of 20 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In the I^2C communication, fix the level of XCE to the high.



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms.
Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.

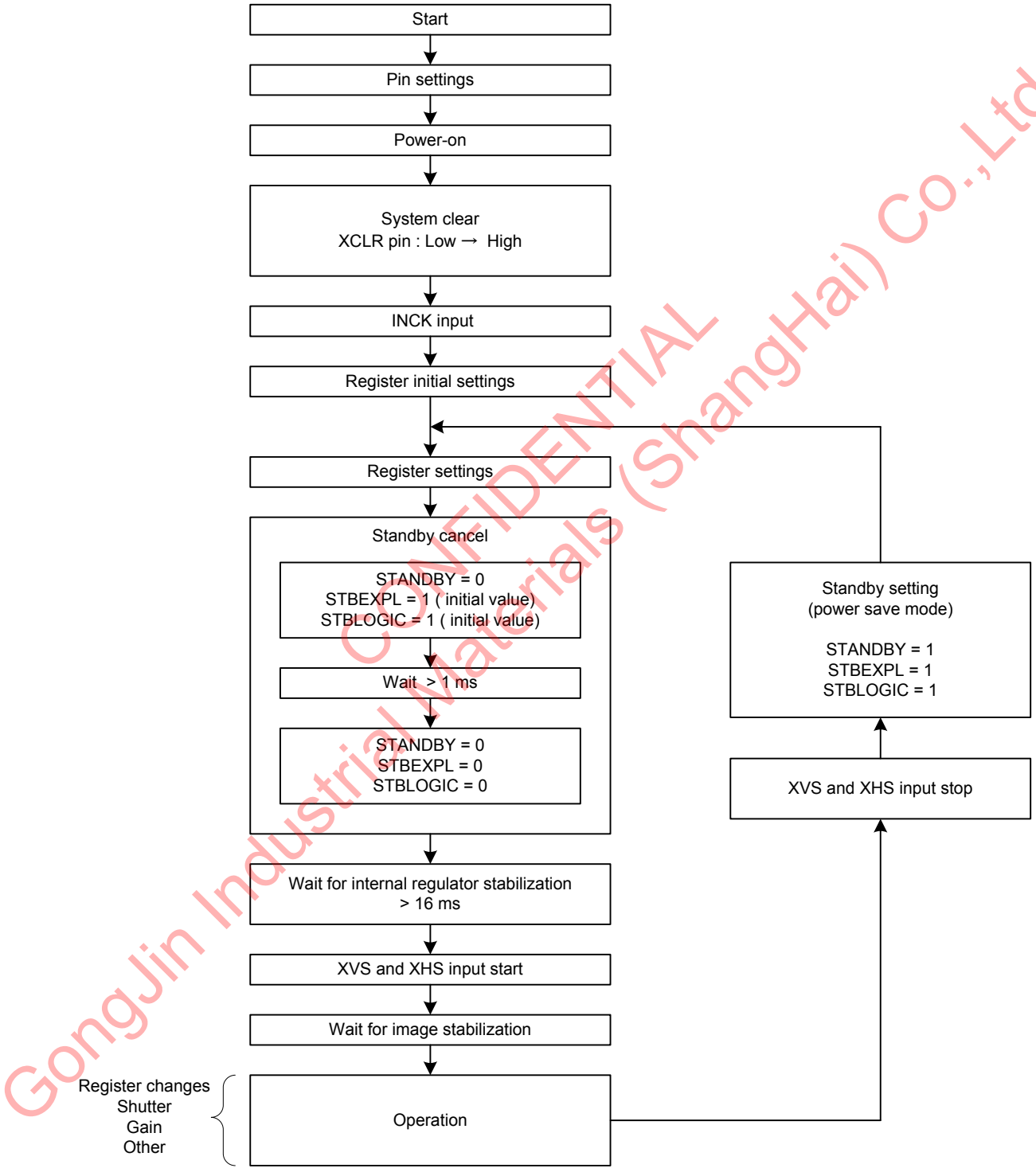


Power-off Sequence

Sensor Setting Flow after Power-on

Setting Flow in Sensor Slave Mode

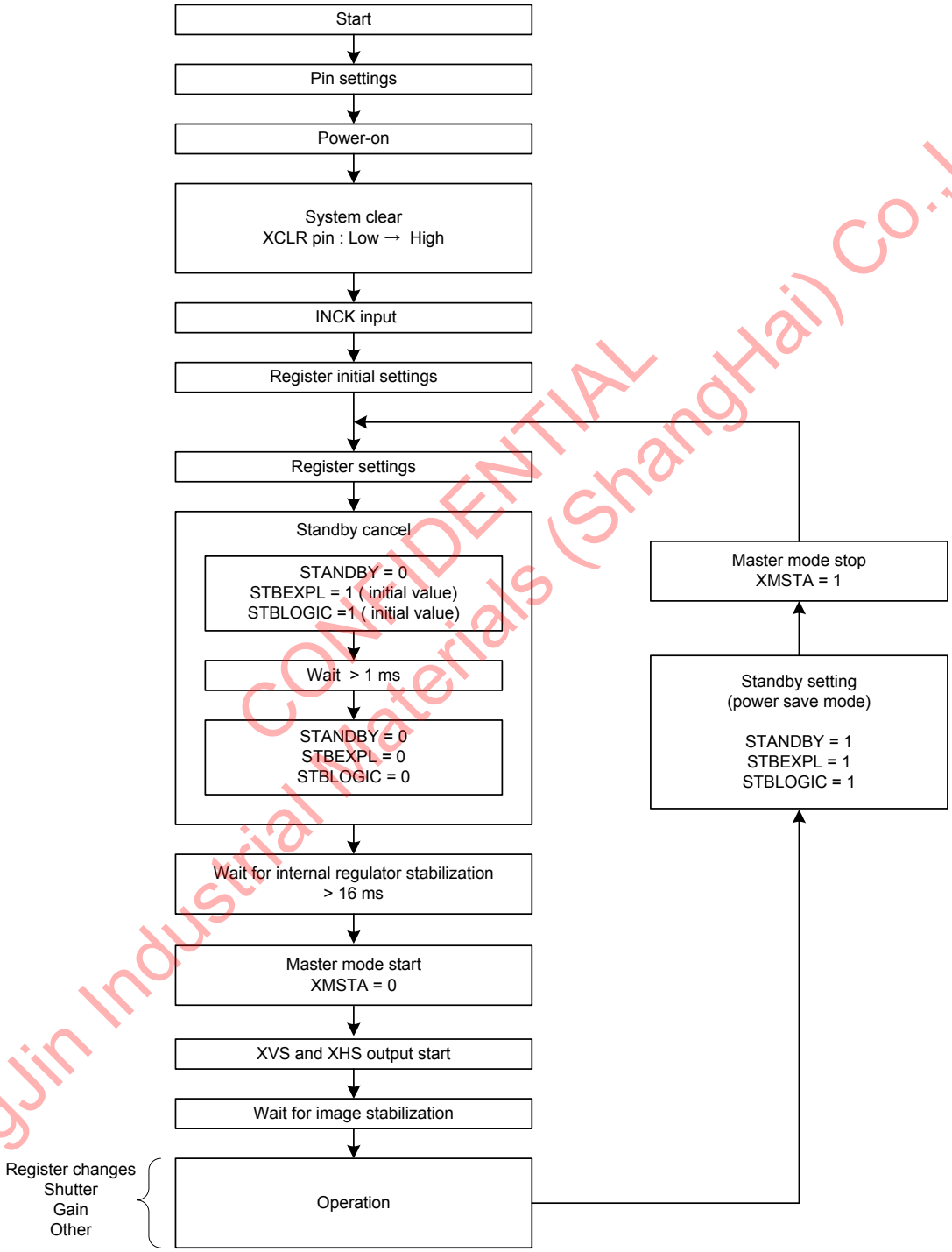
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "Reset cancel", see the item of "Power on sequence" in this section. For details after "Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".“Standby setting (power saving mode) can be made by setting the STANDBY, STBEXPL and STBLOGIC register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

Setting Flow in Sensor Master Mode

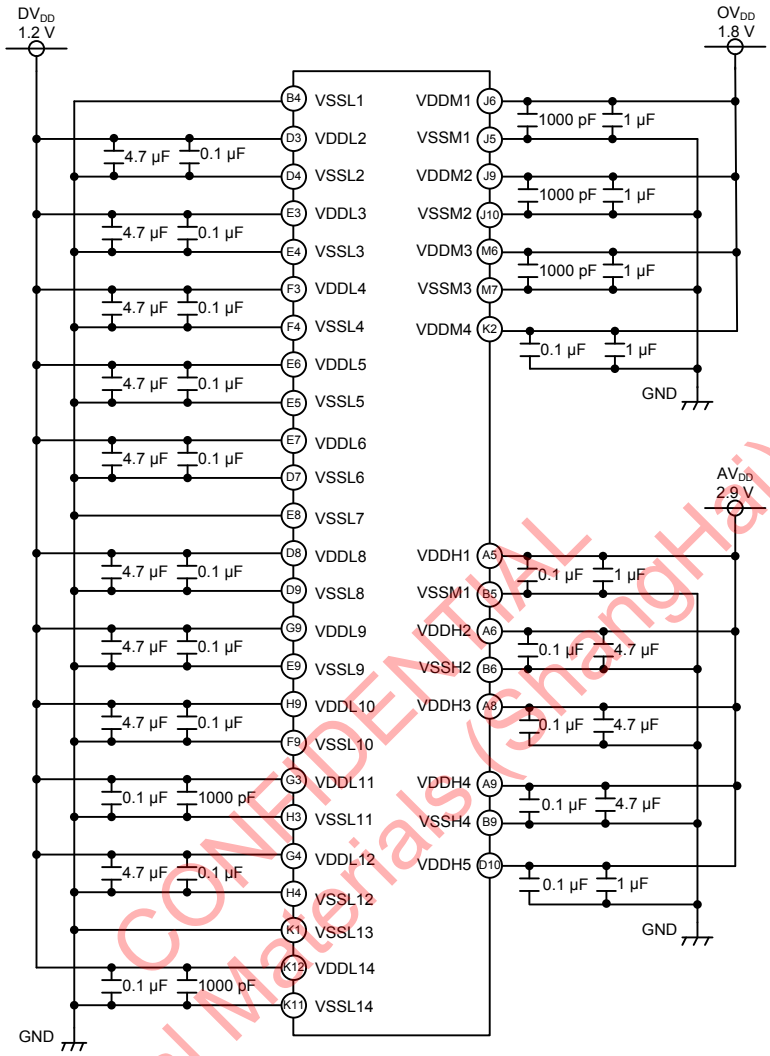
The figure below shows operating flow in sensor master mode.
For details of "Power on" to "Reset cancel", see the item of "Power on sequence" in this section. For details after "Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Waiting for internal regulator stabilization”.
“Standby setting (power saving mode) can be made by setting the STANDBY, STBEXPL and STBLOGIC register to “1” during “Operation”. This time, set "master mode stop" by setting the register XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

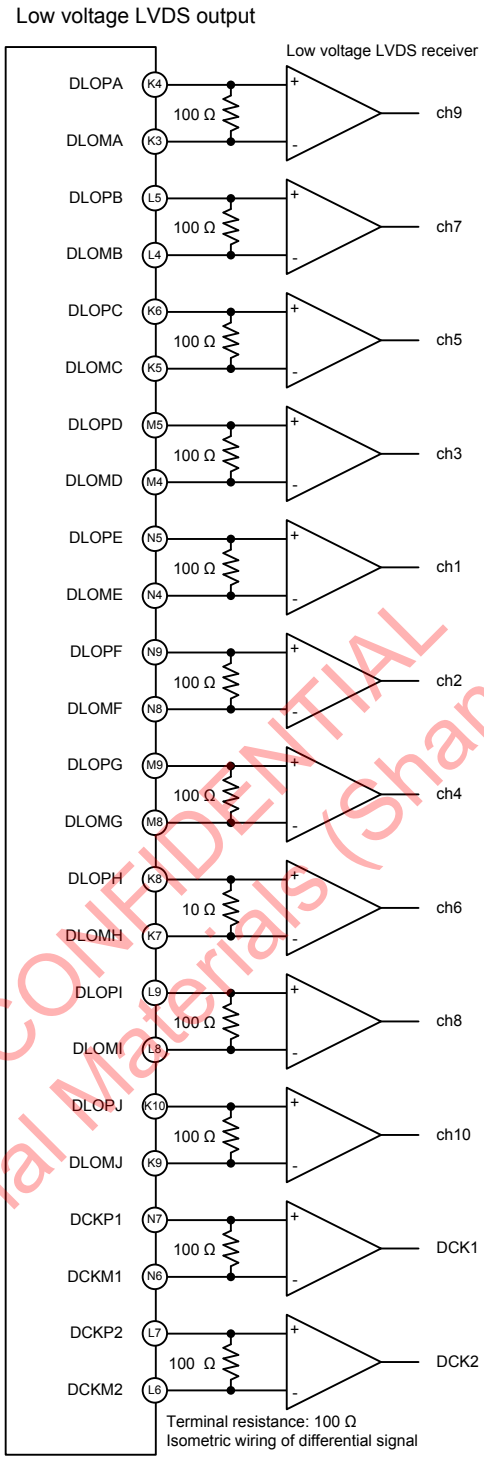
Peripheral Circuit

Power Pins



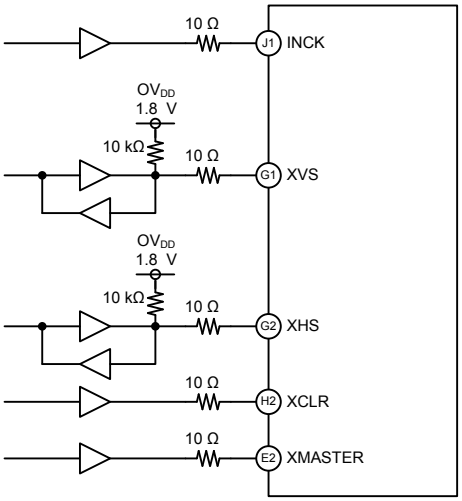
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

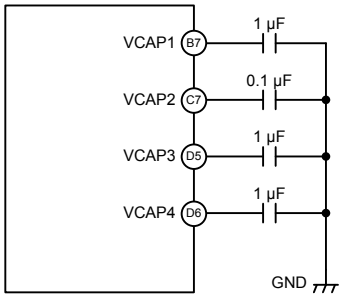
Output Pins



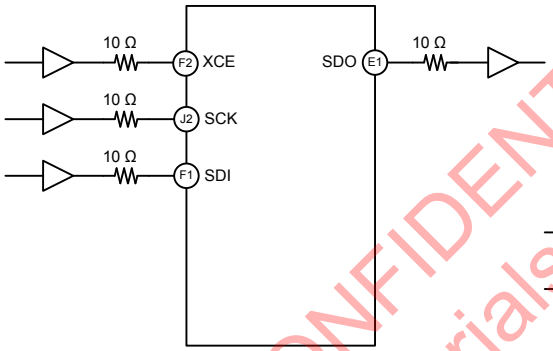
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Other Pins

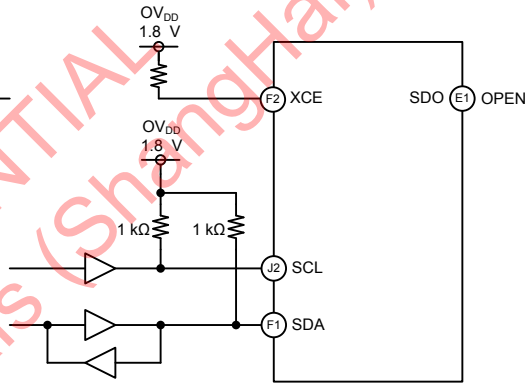




4-wire serial communication



I²C communication



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

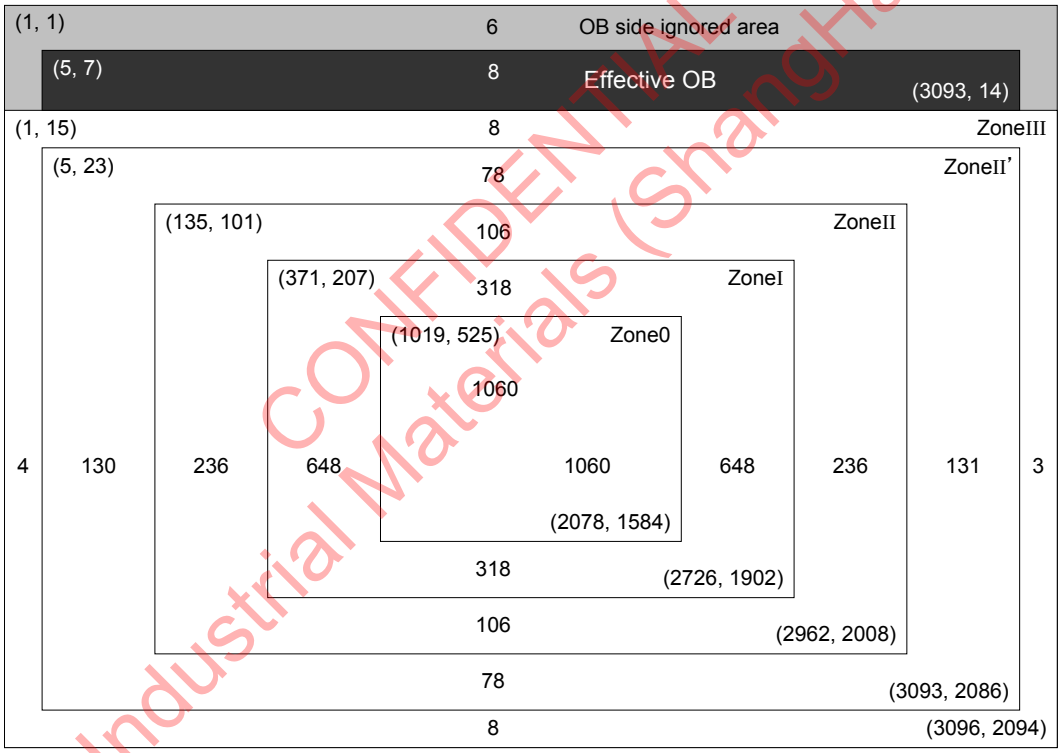
Spot Pixel Specifications

(Tj = 60 ˚C)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	46	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	560		No evaluation criteria applied		2	1/30 s integration
Black pixels at signal saturated	D ≤ 756 mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode.
2. D ... Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Spot Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	5.2 pcs
10.0 mV or higher	3.3 pcs
24.0 mV or higher	1.7 pcs
50.0 mV or higher	1.0 pcs
72.0 mV or higher	0.8 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

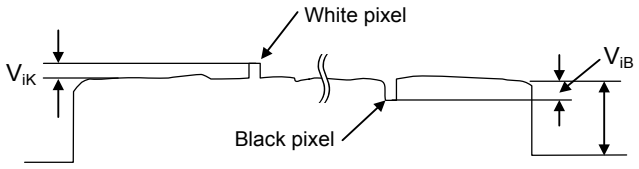
The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting the measurement condition to the standard imaging condition II, the device drive conditions should be within the bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 425 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

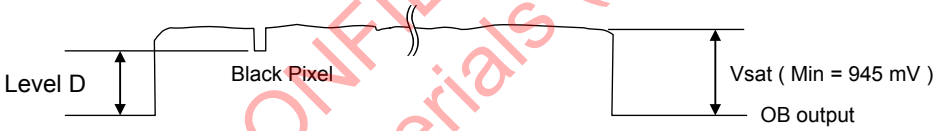
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R/G/B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

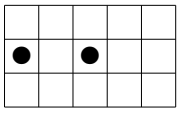
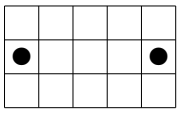
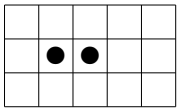
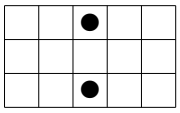
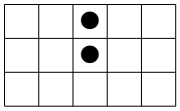


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specifications

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

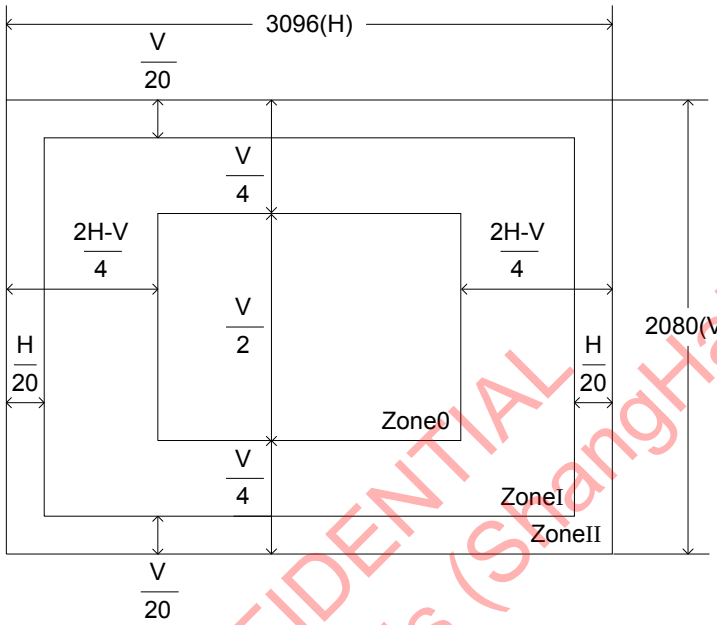
No.	Pattern (G B / R G) It provides by color filter array described in the left.	White pixel	Black pixel	Bright pixel
1	 Same color	Rejected	Rejected	Rejected
2	 Same color	Rejected	Rejected	Rejected
3	 Different color	Allowed	Allowed	Allowed
4	 Same color	Rejected	Allowed	Allowed
5	 Different color	Allowed	Allowed	Allowed

Note) 1. "● " shows the position of white pixel, black pixel and bright pixel. White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated "Rejected" is selected and removed.
3. Spot pixels indicated "Allowed" are not the subject of selected rejection. They are counted including the number of allowable spot pixels by zone.
4. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Stain Specifications

Zone	Allowable pixels	Size	Level	Lens aperture
0 to II	0	L ≥ 3	R ≥ 8 %	F = 16
Means no stain over three lines or more.				

Stain Zone Definition

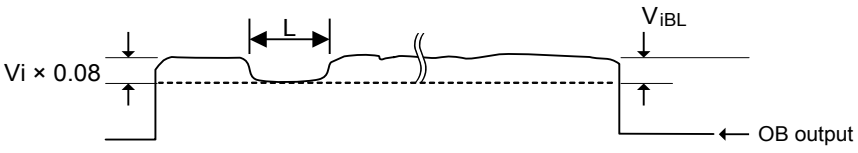


Stain Measurement Method

In the following measurement, set the measurement condition to the standard imaging condition II, set the lens diaphragm to F16, and adjust the luminous intensity so that the average value of the G channel signal output is 150 mV. Measure the local dip in the average value of the R / G / B channel signal output (Vi_{BL}), and then calculate the stain level (R) as the ratio of Vi_{BL} to the average value of the R / G / B channel signal output (Vi).

Stain level R = (Vi_{BL} / Vi) × 100 [%] (I = R, G, B)

At the same time, the size (L) of the area where the stain level is 8 % or more is determined by line number conversion.
The distance from one center of a stain to another is the stain interval, and is also determined in the same way by line number conversion.



Signal output waveform of R/G/B channel

Example of CRA Characteristics

(EPD = -30 mm)

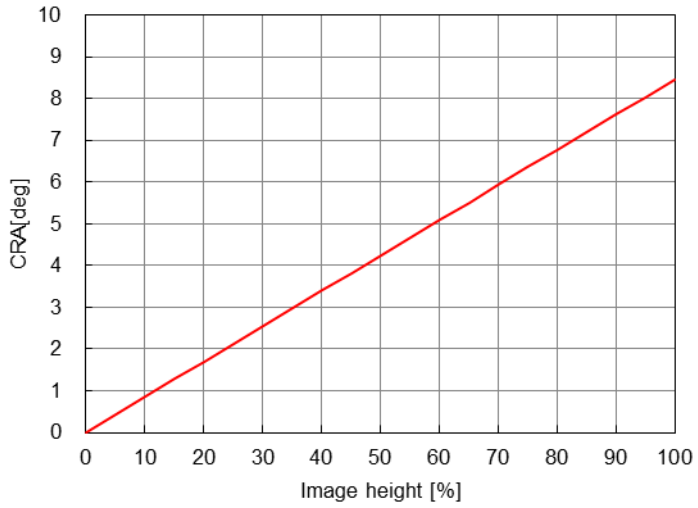
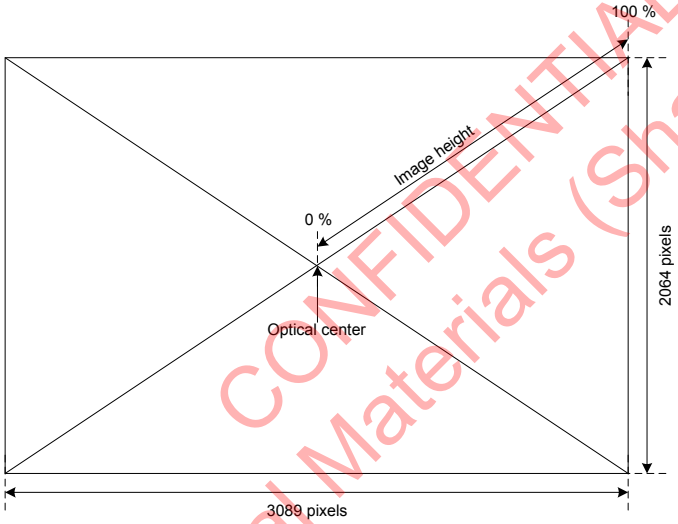
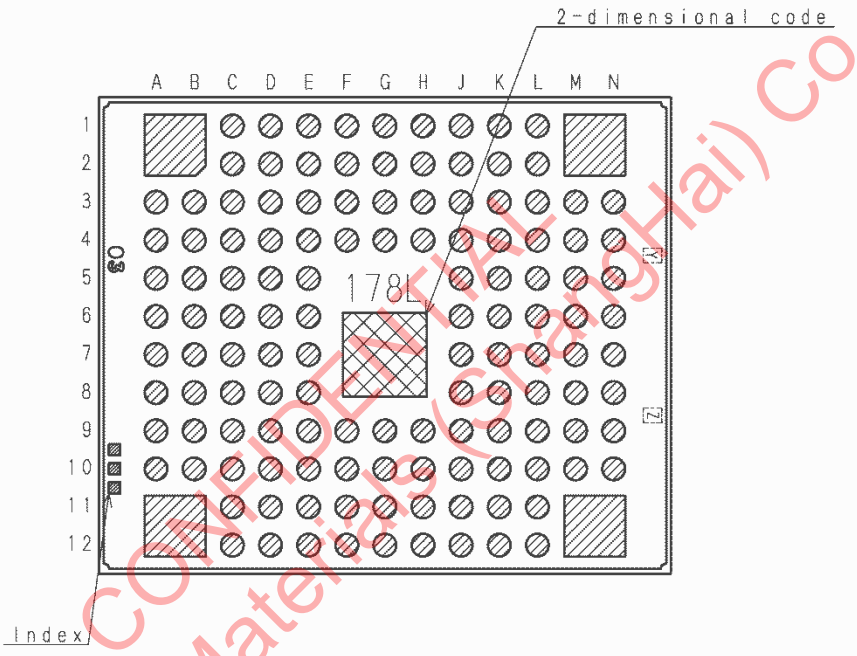


Image Height		CRA
(%)	(mm)	(deg)
0	0.0	0.00
5	0.2	0.43
10	0.4	0.85
15	0.7	1.28
20	0.9	1.70
25	1.1	2.13
30	1.3	2.55
35	1.6	2.98
40	1.8	3.40
45	2.0	3.83
50	2.2	4.25
55	2.5	4.67
60	2.7	5.10
65	2.9	5.52
70	3.1	5.94
75	3.3	6.36
80	3.6	6.78
85	3.8	7.20
90	4.0	7.62
95	4.2	8.04
100	4.5	8.45



Marking



Note:Following characters enter into "Y", and "Z". (No Au coat)
Y:In English upper case character. One character
Z:Number, single number

DRAWING No. AM-B178LQJC-01(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

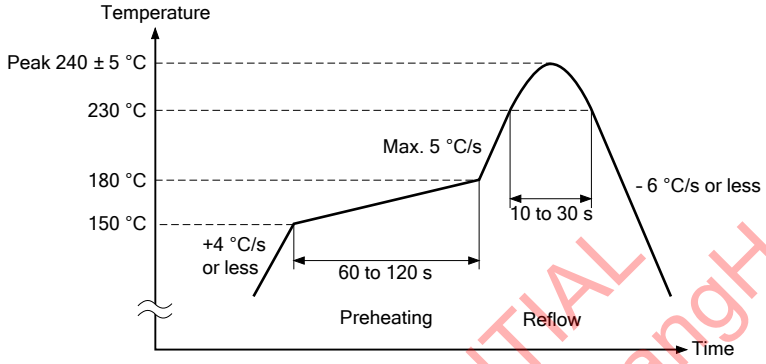
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

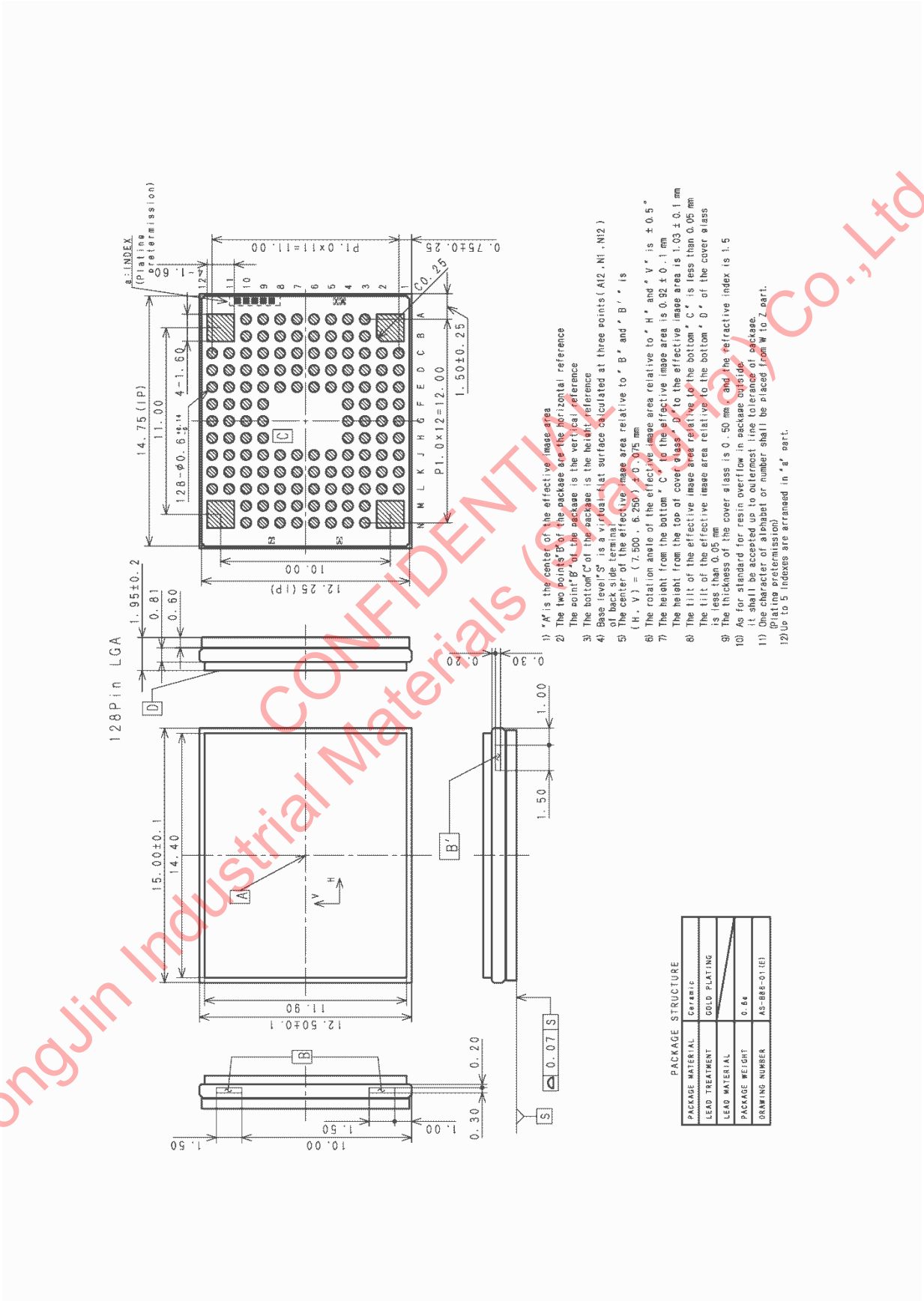
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

(Unit: mm)



Revision History

Date of change	Ver	Page	Contain of Change								
21-Nov-12	Rev1.0.0		First edition								
21-Nov-12	Rev1.0.1	100	AVDD 2.7V → AVDD2.9V								
27-Nov-12	Rev1.0.2	47	All-Pixel Scan 6.3M (3:2)	54MHz	10ch	29.97fps	14bit	HMAX =	0347h	→	0348h
			All-Pixel Scan 6.3M (3:2)	54MHz	10ch	29.97fps	12bit	HMAX =	01EEh	→	01EFh
			All-Pixel Scan 6.3M (3:2)	54MHz	8ch	29.97fps	12bit	HMAX =	0257h	→	0258h
			All-Pixel Scan 6.3M (3:2)	54MHz	8ch	29.97fps	10bit	HMAX =	01F7h	→	01F8h
		50	Window cropping 5.0M (4:3)	54MHz	10ch	29.97fps	14bit	HMAX =	0347h	→	0348h
			Window cropping 5.0M (4:3)	54MHz	10ch	29.97fps	12bit	HMAX =	0332h	→	0333h
			Window cropping 5.0M (4:3)	54MHz	10ch	29.97fps	10bit	HMAX =	02B4h	→	02B5h
			Window cropping 5.0M (4:3)	54MHz	8ch	59.94fps	10bit	HMAX =	01ACh	→	01ADh
			Window cropping 5.0M (4:3)	54MHz	8ch	29.97fps	10bit	HMAX =	01ACh	→	01ADh
			Window cropping 5.0M (4:3)	54MHz	4ch	29.97fps	12bit	HMAX =	03E8h	→	03E9h
			Window cropping 5.0M (4:3)	54MHz	4ch	29.97fps	10bit	HMAX =	034Eh	→	034Fh
		53	Window cropping 5.2M (5:4) QSXGA	54MHz	10ch	29.97fps	14bit	HMAX =	0347h	→	0348h
			Window cropping 5.2M (5:4) QSXGA	54MHz	10ch	29.97fps	12bit	HMAX =	0332h	→	0333h
			Window cropping 5.2M (5:4) QSXGA	54MHz	10ch	29.97fps	10bit	HMAX =	02B4h	→	02B5h
			Window cropping 5.2M (5:4) QSXGA	54MHz	8ch	29.97fps	12bit	HMAX =	01F7h	→	01F8h
			Window cropping 5.2M (5:4) QSXGA	54MHz	4ch	29.97fps	12bit	HMAX =	03E8h	→	03E9h
			Window cropping 5.2M (5:4) QSXGA	54MHz	4ch	29.97fps	10bit	HMAX =	0338h	→	0339h
		56	All-Pixel Scan 1.6M (3:2) 2x2 Binning	54MHz	10ch	29.97fps	12bit	HMAX =	0248h	→	0249h
			All-Pixel Scan 1.6M (3:2) 2x2 Binning	54MHz	10ch	29.97fps	10bit	HMAX =	01EEh	→	01EFh
			All-Pixel Scan 1.6M (3:2) 2x2 Binning	54MHz	8ch	29.97fps	12bit	HMAX =	02CAh	→	02CBh
			All-Pixel Scan 1.6M (3:2) 2x2 Binning	54MHz	4ch	29.97fps	10bit	HMAX =	0257h	→	0258h
		59	Window cropping 1.3M (4:3) 2x2 Binning	54MHz	10ch	59.94fps	12bit	HMAX =	01A3h	→	01A4h
			Window cropping 1.3M (4:3) 2x2 Binning	54MHz	10ch	29.97fps	12bit	HMAX =	01EEh	→	01EFh
			Window cropping 1.3M (4:3) 2x2 Binning	54MHz	10ch	29.97fps	10bit	HMAX =	01B7h	→	01B8h
		62	Window cropping 1.3M (5:4) QSXGA 2x2 Binning	54MHz	10ch	59.94fps	12bit	HMAX =	01A3h	→	01A4h
			Window cropping 1.3M (5:4) QSXGA 2x2 Binning	54MHz	10ch	29.97fps	12bit	HMAX =	01EEh	→	01EFh
		68	HD 1080p	74.25MHz	10ch	30.00fps	14bit	HMAX =	05DBh	→	05DCh
		47	Window Arbitrary Cropping	54MHz	10ch	29.97fps	14bit	HMAX =	0347h	→	0348h
			Window Arbitrary Cropping	54MHz	10ch	29.97fps	12bit	HMAX =	01EEh	→	01EFh
			Window Arbitrary Cropping	54MHz	8ch	29.97fps	12bit	HMAX =	0257h	→	0258h
			Window Arbitrary Cropping	54MHz	8ch	29.97fps	10bit	HMAX =	01F7h	→	01F8h

Date of change	Ver	Page	Contain of Change
5-Feb-13	Rev2.0.0	1	Updated “CDS/PGA function”
5-Feb-13	Rev2.0.0	3	Updated “Operating temperature”
5-Feb-13	Rev2.0.0	10	Updated “Pin Configuration”
5-Feb-13	Rev2.0.0	14	Updated Table “DC Characteristics”
5-Feb-13	Rev2.0.0	15	Updated Table “Power Consumption”
5-Feb-13	Rev2.0.0	22	Add Graph “Spectral Sensitivity Characteristics”
5-Feb-13	Rev2.0.0	23	Updated Table “Image Sensor Characteristics”
5-Feb-13	Rev2.0.0	25	Updated “Measurement method”
5-Feb-13	Rev2.0.0	27	Updated “Register Communication Timing”
5-Feb-13	Rev2.0.0	37	Add “LP_MODE [7:0] register”
5-Feb-13	Rev2.0.0	37	Updated “GAIN [8:0] register”
5-Feb-13	Rev2.0.0	39	Updated “XHSOUTSEL [1:0] register”
5-Feb-13	Rev2.0.0	40	Updated “ WINWH[11:0] register”
5-Feb-13	Rev2.0.0	42	Updated Table “The register set up according to drive mode”
5-Feb-13	Rev2.0.0	43	Updated Table “Registers which must be changed from the default value”
5-Feb-13	Rev2.0.0	46	Updated Table “List of Sync Code”
5-Feb-13	Rev2.0.0	47	Updated Table “All-Pixel Scan 6.3 M (3:2) register setting details”
5-Feb-13	Rev2.0.0	50	Updated Table “Window cropping 5.0 M (4:3) register setting details”
5-Feb-13	Rev2.0.0	53	Updated Table “Window cropping 5.2 M (5:4) QSXGA register setting details”
5-Feb-13	Rev2.0.0	56	Updated Table “All-Pixel Scan 1.6 M (3:2) 2 × 2 Binning register setting details”
5-Feb-13	Rev2.0.0	59	Updated Table “Window cropping 1.3 M (4:3) 2 × 2 Binning register setting details”
5-Feb-13	Rev2.0.0	62	Updated Table “Window cropping 1.3 M (5:4) QSXGA 2 × 2 Binning register setting details”
5-Feb-13	Rev2.0.0	65	Updated Table “Window cropping 5.3 M (16:9) register setting details”
5-Feb-13	Rev2.0.0	68	Updated Table “HD1080p register setting details”
5-Feb-13	Rev2.0.0	71	Updated Table “HD720p 2 × 2 Binning register setting details”
5-Feb-13	Rev2.0.0	76	Updated Table “Window Arbitrary Cropping register setting details”
5-Feb-13	Rev2.0.0	79	Updated “Standby Mode”
5-Feb-13	Rev2.0.0	81	Updated “Gain Adjustment Function”
5-Feb-13	Rev2.0.0	84	Updated “Shutter and Integration Time Settings”
5-Feb-13	Rev2.0.0	89	Updated Figure “ODBIT = 2h (Low voltage LVDS serial 14 bit output)”
5-Feb-13	Rev2.0.0	94	Updated Table “Number of Invalid Frames Generated during Mode Transitions”
5-Feb-13	Rev2.0.0	96	Updated “Power-on Sequence”
5-Feb-13	Rev2.0.0	98	Updated “Setting Flow in Sensor Slave Mode”
5-Feb-13	Rev2.0.0	99	Updated “Setting Flow in Sensor Master Mode”
5-Feb-13	Rev2.0.0	103	Updated “Spot Pixel Specifications”
5-Feb-13	Rev2.0.0	105	Updated “Measurement Method for Spot Pixels”
15-Mar-13	Rev2.0.1	42	Updated “The register set up according to drive mode”

Date of change	Ver	Page	Contain of Change
4-Jun-13	Rev3.0.0	1	Deleted “Recommend lens F number”
4-Jun-13	Rev3.0.0	8	Updated the title of the figure “Pixel Array”
4-Jun-13	Rev3.0.0	15	Updated “Power Consumption”
4-Jun-13	Rev3.0.0	18	Updated “AC Characteristics of Serial Communication”
4-Jun-13	Rev3.0.0	38	Updated “Register SHS1”
4-Jun-13	Rev3.0.0	44,45	Updated “Operation Modes”
4-Jun-13	Rev3.0.0	47,50,53 56,59,62,76	Updated “register setting details of each operation mode”
4-Jun-13	Rev3.0.0	80	Updated “Description of Slave Mode and Master Mode”
4-Jun-13	Rev3.0.0	93	Updated “Description of Software Reset”
4-Jun-13	Rev3.0.0	94,95	Updated “Description of Mode Transitions”
4-Jun-13	Rev3.0.0	96	Updated “Power-on Sequence”
28-Aug-13	E13819	3	Updated “Operating guarantee temperature and Storage guarantee temperature”
28-Aug-13	E13819	20	Updated “Output load capacitance”
28-Aug-13	E13819	22	Updated ”Spectral Sensitivity Characteristics”
28-Aug-13	E13819	48,51,54,57 , 60,63,66,69 74,77	Updated “Pixel Array Image”
28-Aug-13	E13819	86	Updated Notice of Long Exposure Operation
28-Aug-13	E13819	109	Updated “Marking”
28-Aug-13	E13819	112	Updated “Package Outline”
6-Sep-13	E13819A39	74	Updated “Image Drawing of Window Arbitrary Cropping Mode”
25-Oct-13	E13819B3X	3	Update “Storage guarantee temperature”