SONY

Diagonal 9.33 mm (Type 1/1.7) CMOS Image Sensor with Square Pixel for Color Cameras

IMX226CQJ-C

Description

The IMX226CQJ-C is a diagonal 9.33 mm (Type 1/1.7) CMOS image sensor with a color square pixel array and approximately 12.4M effective pixels. The image sensor can output effective approximately 9.03M pixels signal for high-definition (4K2K: 4096 × 2160) moving picture at 59.94 frame/s in 10-bit-digital output format.
In addition, sensor supporting horizontal/vertical addition, this is capable of outputting a 12 bit digital for HD1080 (2048 × 1080) -60p moving picture. For still picture imaging, this sensor can output approximately 12.4 M effective pixels signal in a high-definition 12-bit digital output format. Realizing high-sensitivity, low dark current, this sensor also has an electronic shutter function with variable storage time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- ◆CMOS active pixel type pixels
- ◆Input clock frequency 72 MHz
- ◆Number of effective pixels (12M) : 4072 (H) × 3046 (V) approx 12.4M pixels
- ◆Number of effective pixels (4K2K) : 4152 (H) × 2174 (V) approx 9.03M pixels
- ◆Readout mode
  All-pixel scan mode (12 M, 4K2K)
  Horizontal/vertical 2/2-line binning mode (4K2K)
- ◆High-sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- ◆Variable-speed shutter function (minimum unit: 1 horizontal sync signal period (1XHS))
- ◆Low power consumption
- ◆H driver, V driver and serial communication circuit on chip
- ◆CDS/PGA on chip. Gain + 27 dB (step pitch < 0.1 dB)
- ◆10-bit/12-bit A/D conversion on chip
- ◆R, G, B primary color mosaic filters on chip

Exmor R

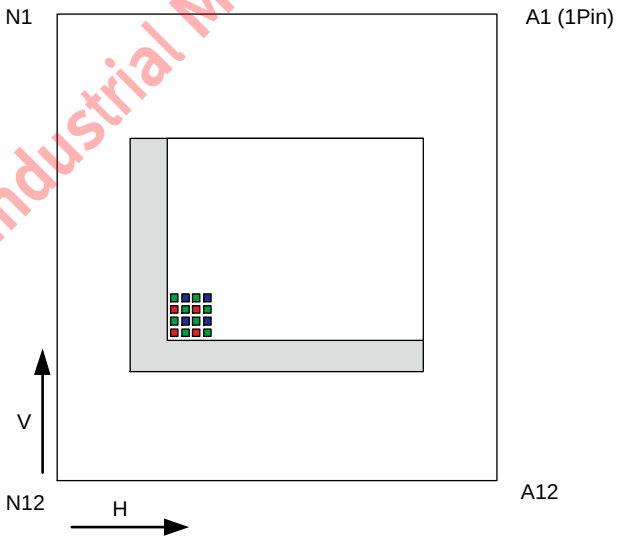
* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.

Device Structure

- ◆CMOS image sensor
- ◆Image size
  Diagonal 9.33 mm (Type 1/1.7)
- ◆Total number of pixels
  4168 (H) × 3062 (V) approx. 12.76 M pixels
- ◆Number of effective pixels
  - Type 1/1.7 (12 M) : 4072 (H) × 3046 (V) approx. 12.40 M pixels
  - Type 1/1.9 (4K2K) : 4152 (H) × 2174 (V) approx. 9.03 M pixels
- ◆Number of active pixels
  - Type 1/1.7 (12M) : 4024 (H) × 3036 (V) approx. 12.22 M pixels diagonal 9.33 mm
  - Type 1/1.9 (4K2K) : 4120 (H) × 2168 (V) approx. 8.93 M pixels diagonal 8.61 mm
- ◆Number of recommended recording pixels
  - Type 1/1.7 (12M) : 4000 (H) × 3000 (V) 12.00 M pixels aspect ratio 4:3
  - Type 1/1.9 (4K2K) : 4096 (H) × 2160 (V) approx. 8.85 M pixels aspect ratio approx. 17:9
- ◆Unit cell size
  1.85 µm (H) × 1.85 µm (V)
- ◆Optical black
  Horizontal (H) direction : Front 96 pixels, rear 0 pixels
  Vertical (V) direction : Front 16 pixels, rear 0 pixels
- ◆Substrate material
  Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during normal readout in the vertical direction.

Absolute Maximum Ratings

◆ Supply voltage 1	V_{ADD} *1	–0.3 to +3.3	V
◆ Supply voltage 2	V_{DDD1} *2	–0.5 to +2.0	V
◆ Supply voltage 3	V_{DDD2} *3	–0.5 to +3.3	V
◆ Input voltage (digital)	V_I	–0.3 to V_{DDD2} + 0.3	V
◆ Output voltage (digital)	V_O	–0.3 to V_{DDD2} + 0.3	V
◆ Guaranteed operating temperature	T_{OPR}	–30 to +75	˚C
◆ Storage guarantee temperature	T_{STG}	–40 to +80	˚C
◆ Performance guarantee temperature	T_{SPEC}	–10 to +60	˚C

Recommended Operating Conditions

◆ Supply voltage 1	V_{ADD} *1	2.9 ± 0.1	V
◆ Supply voltage 2	V_{DDD1} *2	1.2 ± 0.1	V
◆ Supply voltage 3	V_{DDD2} *3	1.8 ± 0.1	V
◆ Input voltage (digital)	V_I	–0.1 to V_{DDD2} + 0.1	V
◆ Output voltage (digital)	V_O	–0.1 to V_{DDD2} + 0.1	V

*1 V_{ADD} : V_{DD}SUB, V_{DD}HCM, V_{DD}HVS, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP (2.9 V power supply)
*2 V_{DDD1} : V_{DD}LCN1 and V_{DD}LCN2, V_{DD}LSC1 and V_{DD}LSC2, V_{DD}LPL (1.2 V power supply)
*3 V_{DDD2} : V_{DD}MIO, V_{DD}MLV1 and V_{DD}MLV2 (1.8 V power supply)

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Contents

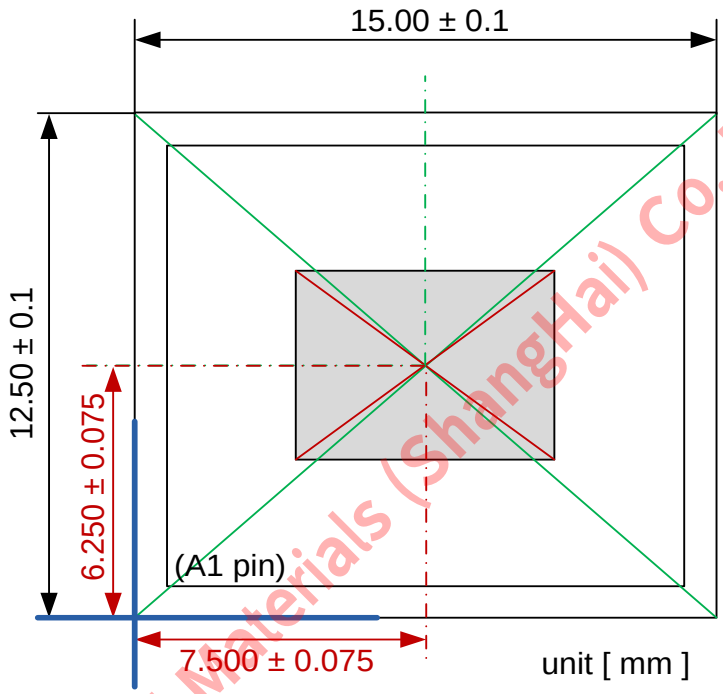
Package Center and Optical Center

Top View

Package center

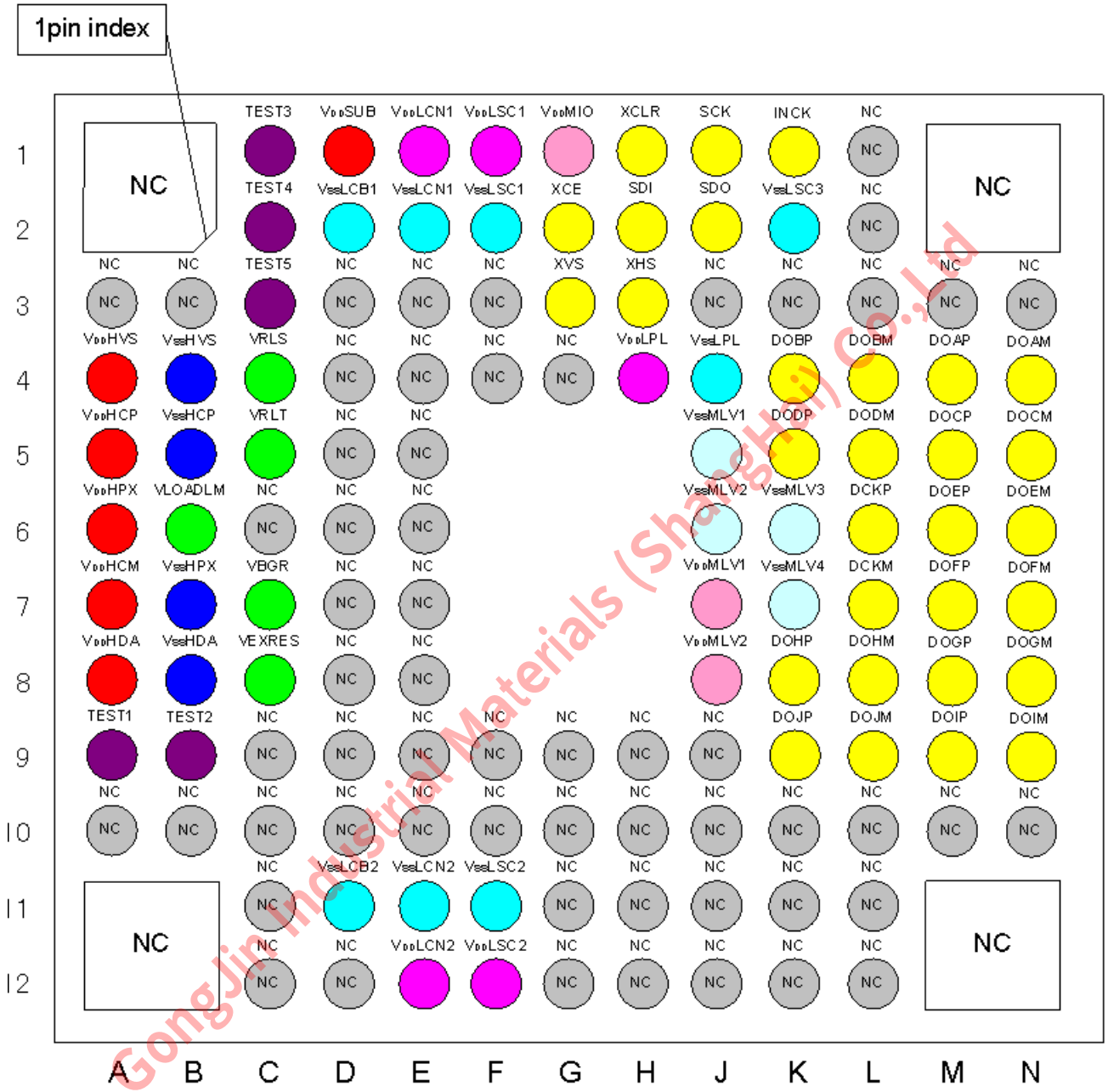
Optical center

Package reference (H,V)



Pin Configuration

(Bottom View)



Pin Description

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
A4	V_{DD}HVS	Power	A	Analog power supply (2.9 V)	—	
A5	V_{DD}HCP	Power	A	Analog power supply (2.9 V)	—	
A6	V_{DD}HPX	Power	A	Analog power supply (2.9 V)	—	
A7	V_{DD}HCM	Power	A	Analog power supply (2.9 V)	—	
A8	V_{DD}HDA	Power	A	Analog power supply (2.9 V)	—	
A9	TEST1	O	A	Test	Hi-Z	Leave open. (No connection)
B4	V_{SS}HVS	GND	A	Analog GND (2.9 V)	—	
B5	V_{SS}HCP	GND	A	Analog GND (2.9 V)	—	
B6	VLOADLM	O	A	Capacitor connection	Pull-down	
B7	V_{SS}HPX	GND	A	Analog GND (2.9 V)	—	
B8	V_{SS}HDA	GND	A	Analog GND (2.9 V)	—	
B9	TEST2	O	A	Test	Hi-Z	Leave open. (No connection)
C1	TEST3	I	D	Test	—	Leave open. (No connection)
C2	TEST4	I	D	Test	—	Leave open. (No connection)
C3	TEST5	O	D	Test	Low Level	Leave open. (No connection)
C4	VRLS	O	A	Capacitor connection	Pull-down	
C5	VRLT	O	A	Capacitor connection	Pull-down	
C7	VBGR	O	A	Capacitor connection	Hi-Z	
C8	VEXRES	O	A	Resistor connection	Hi-Z	
D1	V_{DD}SUB	Power	A	Analog power supply (2.9 V)	—	
D2	V_{SS}LCB1	GND	D	Digital GND (1.2 V)	—	
D11	V_{SS}LCB2	GND	D	Digital GND (1.2 V)	—	
E1	V_{DD}LCN1	Power	D	Digital power supply (1.2 V)	—	
E2	V_{SS}LCN1	GND	D	Digital GND (1.2 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
E11	V_{SS}LCN2	GND	D	Digital GND (1.2 V)	—	
E12	V_{DD}LCN2	Power	D	Digital power supply (1.2 V)	—	
F1	V_{DD}LSC1	Power	D	Digital power supply (1.2 V)	—	
F2	V_{SS}LSC1	GND	D	Digital GND (1.2 V)	—	
F11	V_{SS}LSC2	GND	D	Digital GND (1.2 V)	—	
F12	V_{DD}LSC2	Power	D	Digital power supply (1.2 V)	—	
G1	V_{DD}MIO	Power	D	Digital power supply (1.8 V)	—	
G2	XCE	I	D	Serial communication enable input	—	
G3	XVS	I	D	Vertical sync signal input	—	
H1	XCLR	I	D	Reset pulse input	—	
H2	SDI	I	D	Serial communication data input	—	
H3	XHS	I	D	Horizontal sync signal input	—	
H4	V_{DD}LPL	Power	D	Digital power supply (1.2 V)	—	
J1	SCK	I	D	Serial communication clock input	—	
J2	SDO	O	D	Test output	Low Level	Leave open. (No connection)
J4	V_{SS}LPL	GND	D	Digital GND (1.2 V)	—	
J5	V_{SS}MLV1	GND	D	Digital GND (1.8 V)	—	
J6	V_{SS}MLV2	GND	D	Digital GND (1.8 V)	—	
J7	V_{DD}MLV1	Power	D	Digital power supply (1.8 V)	—	
J8	V_{DD}MLV2	Power	D	Digital power supply (1.8 V)	—	
K1	INCK	I	D	Input clock	—	
K2	V_{SS}LSC3	GND	D	Digital GND (1.2 V)	—	
K4	DOBP	O	D	Digital LVDS output	Hi-Z	
K5	DODP	O	D	Digital LVDS output	Hi-Z	
K6	V_{SS}MLV3	GND	D	Digital GND (1.8 V)	—	
K7	V_{SS}MLV4	GND	D	Digital GND (1.8 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description	State in Standby mode	Remarks
K8	DOHP	O	D	Digital LVDS output	Hi-Z	
K9	DOJP	O	D	Digital LVDS output	Hi-Z	
L4	DOBM	O	D	Digital LVDS output	Hi-Z	
L5	DODM	O	D	Digital LVDS output	Hi-Z	
L6	DCKP	O	D	Digital LVDS output	Hi-Z	
L7	DCKM	O	D	Digital LVDS output	Hi-Z	
L8	DOHM	O	D	Digital LVDS output	Hi-Z	
L9	DOJM	O	D	Digital LVDS output	Hi-Z	
M4	DOAP	O	D	Digital LVDS output	Hi-Z	
M5	DOCP	O	D	Digital LVDS output	Hi-Z	
M6	DOEP	O	D	Digital LVDS output	Hi-Z	
M7	DOFP	O	D	Digital LVDS output	Hi-Z	
M8	DOGP	O	D	Digital LVDS output	Hi-Z	
M9	DOIP	O	D	Digital LVDS output	Hi-Z	
N4	DOAM	O	D	Digital LVDS output	Hi-Z	
N5	DOCM	O	D	Digital LVDS output	Hi-Z	
N6	DOEM	O	D	Digital LVDS output	Hi-Z	
N7	DOFM	O	D	Digital LVDS output	Hi-Z	
N8	DOGM	O	D	Digital LVDS output	Hi-Z	
N9	DOIM	O	D	Digital LVDS output	Hi-Z	

All the pins that do not have description in this table are the N.C. pins. Leave open. (No connection)

Electrical Characteristics

Electrical characteristics of the IMX226CQJ are shown below.

1. DC Characteristics

Current Consumption and Gain Variable Range

(V_{ADD} = 3.0 V, V_{DDD1} = 1.3 V, V_{DDD2} = 1.9 V, Tj = 60 ˚C, Reference Gain (0 dB), approximately 12.40 M pixels readout (MODE0), 34.97 frame/s)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	101	mA	
Current consumption (Digital)	I_{DDD1}	—	—	181	mA	
Current consumption (I/O)	I_{DDD2}	—	—	26	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	150	µA	In the dark
Standby current (Digital)	$I_{DDD1STB}$	—	—	5200	µA	In the dark
Standby current (I/O)	$I_{DDD2STB}$	—	—	50	µA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage

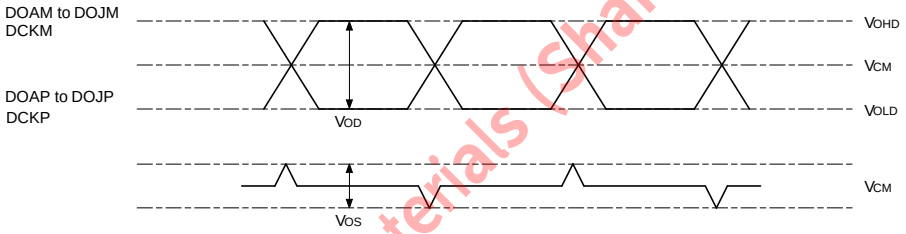
Item		Pins	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	Analog	V_{DD}SUB, V_{DD}HCM, V_{DD}HVS, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP	V_{ADD}	2.80	2.90	3.00	V	
	Digital	V_{DD}LCN1, V_{DD}LCN2, V_{DD}LSC1, V_{DD}LSC2, V_{DD}LPL	V_{DDD1}	1.10	1.20	1.30	V	
	I/O	V_{DD}MIO, V_{DD}MLV1, V_{DD}MLV2	V_{DDD2}	1.70	1.80	1.90	V	
Digital input voltage		XCLR, INCK, SCK, SDI, XCE, XHS, XVS	V_{IH}	0.8 × V_{DDD2}	—	V_{DDD2} + 0.1	V	
			V_{IL}	–0.1	—	0.2 × V_{DDD2}	V	
Digital input leakage current			I_{LI}	–1.0	—	1.0	µA	(V1 = –0.1 to V_{DDD2} + 0.1 V)

LVDS Output DC Characteristics

(Termination resistance : 100 Ω, LVDS current : 1.5 mA)

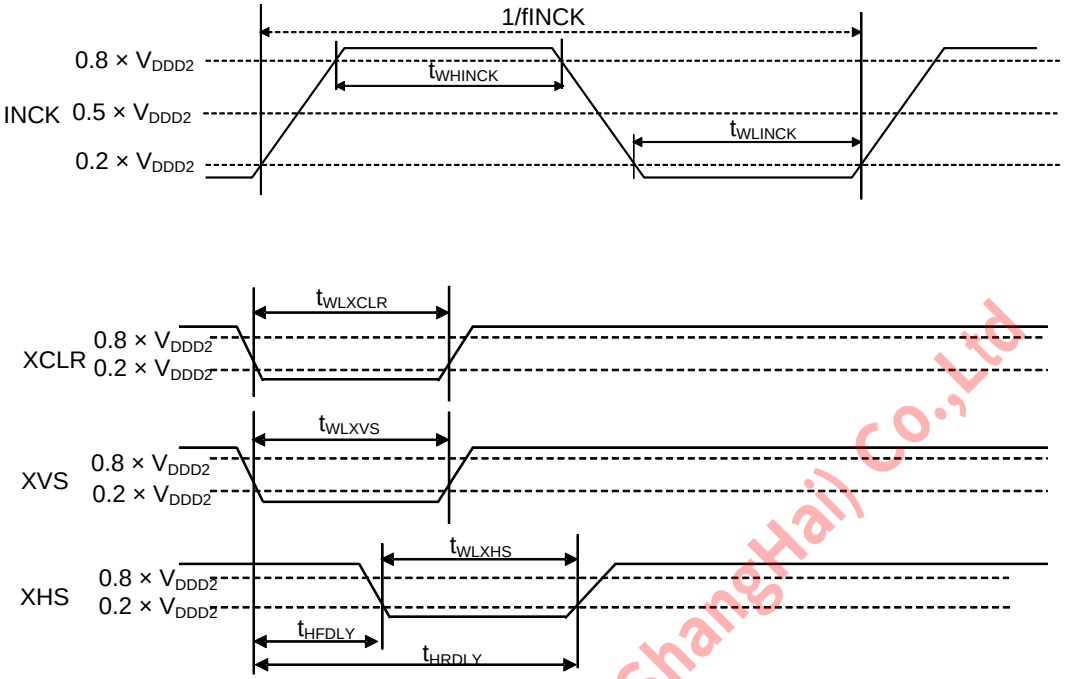
Item	Pins	Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Digital output voltage	DOAP to DOJP, DOAM to DOJM, DCKP, DCKM	Amplitude voltage	V_{OD}	100	150	200	mV	
		Common voltage	V_{CM}	$V_{DDD2}/2$ - 100	$V_{DDD2}/2$	$V_{DDD2}/2$ + 100	mV	
		Common voltage fluctuation	V_{OS}	—	20	—	mV	
		High level output voltage	V_{OHD}	V_{CM} + 50	V_{CM} + 75	V_{CM} + 100	mV	
		Low level output voltage	V_{OLD}	V_{CM} – 100	V_{CM} – 75	V_{CM} – 50	mV	
		Difference between amplitude voltage channels	V_{ODP}	—	—	50	mV	
		Difference between common voltage channels	V_{OSP}	—	—	50	mV	

LVDS output



2. AC Characteristics

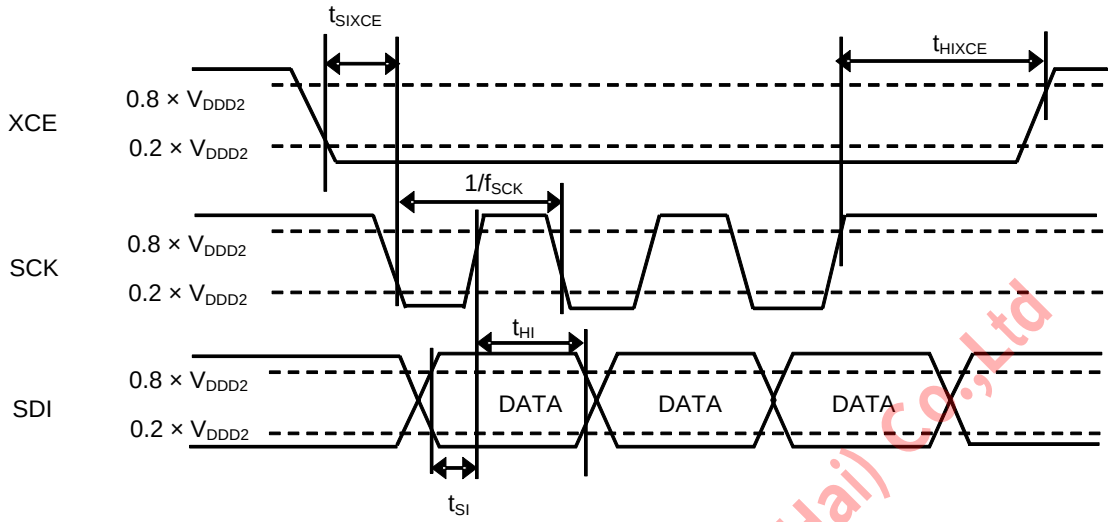
INCK, XVS, XHS, XCLR



Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{INCK}	71.0	72.0	73.0	MHz
INCK Low level pulse width	t_{WLINCK}	5	—	—	ns
INCK High level pulse width	t_{WHOMCK}	5	—	—	ns
Clock duty	—	40	50	60	%
XVS Low level pulse width	t_{WLXVS}	$4/f_{INCK}$	—	$12/f_{INCK}$	µs
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	$12/f_{INCK}$	µs
XVS fall – XHS fall width	t_{HFDLY}	0	—	—	µs
XVS fall – XHS rise width	t_{HRDLY}	$4/f_{INCK}$	—	$12/f_{INCK}$	µs
XCLR Low level pulse width	t_{WLXCLR}	100	—	—	ns

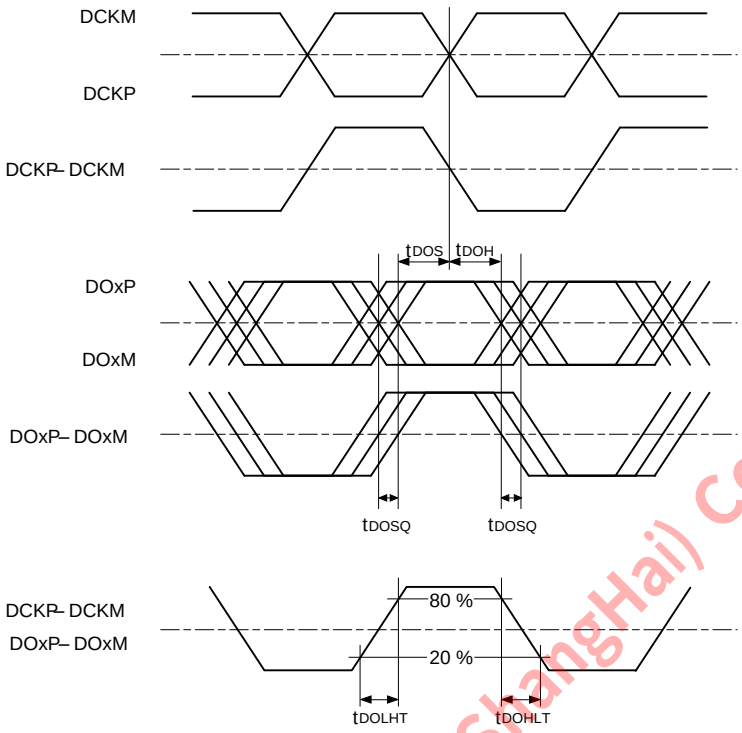
Serial Communication

Serial Control Interface Timing



Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	—	—	36	MHz
SDI input setup time	t_{SI}	7	—	—	ns
SDI input hold time	t_{HI}	7	—	—	ns
XCE input setup time	t_{SIXCE}	10	—	—	ns
XCE input hold time	t_{HIXCE}	10	—	—	ns

3. LVDS output

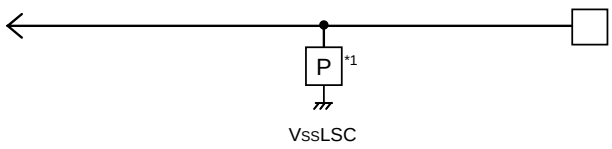
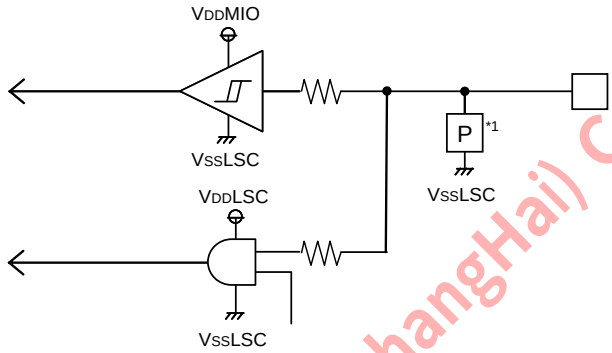
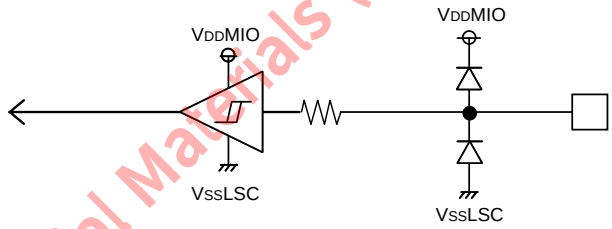
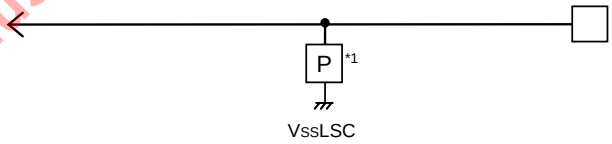
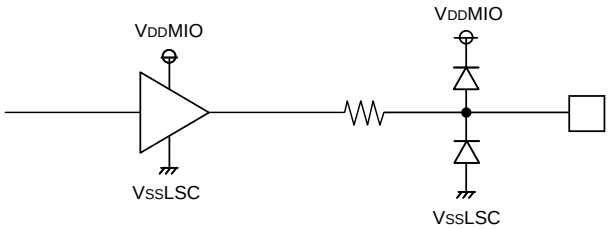


Note) "x" stands for the alphabets of A to J and the time chart is specified for all output channels.

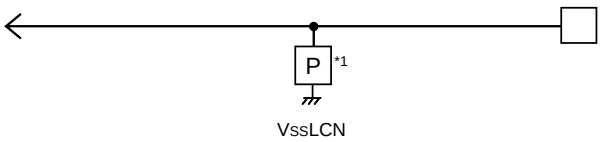
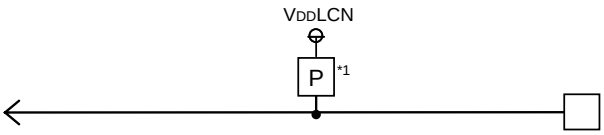
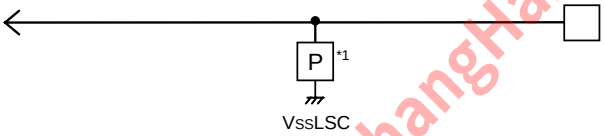
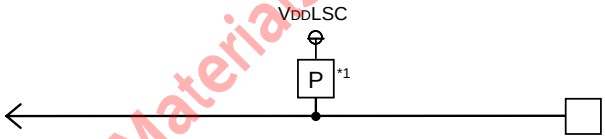
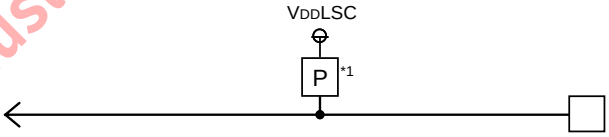
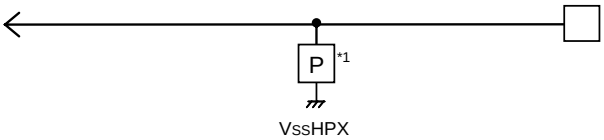
(Termination resistance : 100 Ω, load capacitance : 0 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DO skew time (including jitter)	t_{DOSQ}	—	—	361	ps	Data rate 288 MHz DDR
DO setup time	t_{DOS}	420	—	—	ps	Data rate 288 MHz DDR
DO hold time	t_{DOH}	420	—	—	ps	Data rate 288 MHz DDR
DO rise time	t_{DOLHT}	—	500	—	ps	Simulated value with load capacitance (4 pF)
DO fall time	t_{DOHLT}	—	500	—	ps	Simulated value with load capacitance (4 pF)
DCK duty cycle	D_{DCDCK}	45	50	55	%	

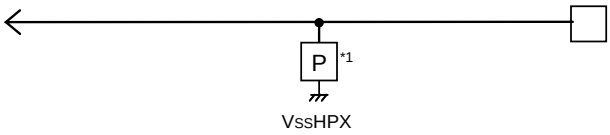
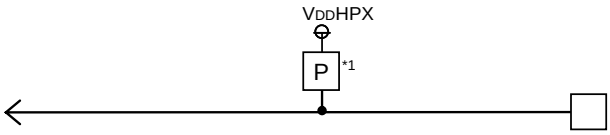
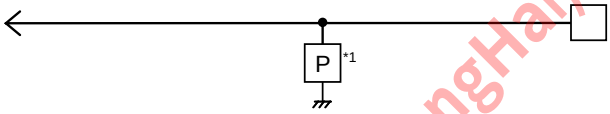
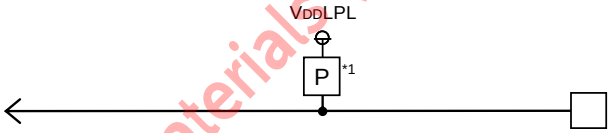
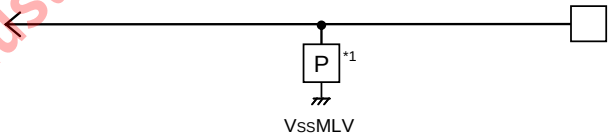
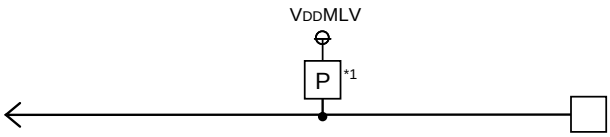
I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit
VDDSUB	
XCLR	
XCE SCK SDI XHS XVS INCK	
VDDMIO	
SDO	

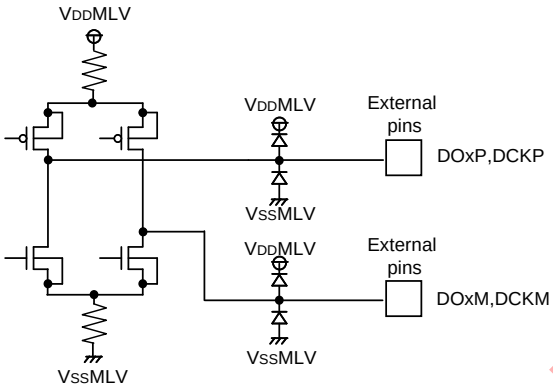
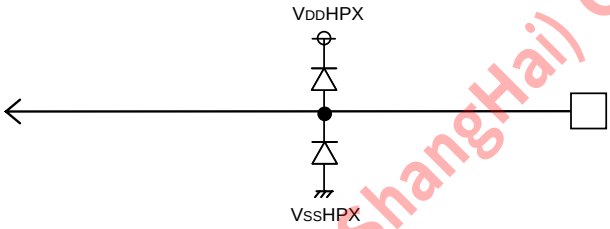
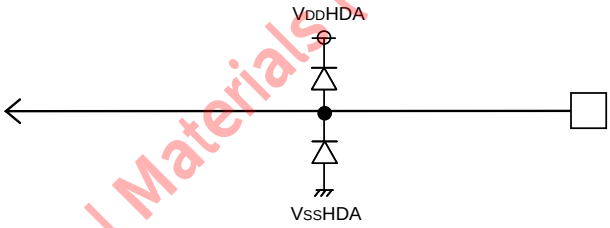
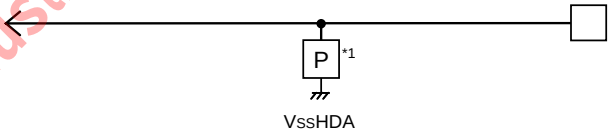
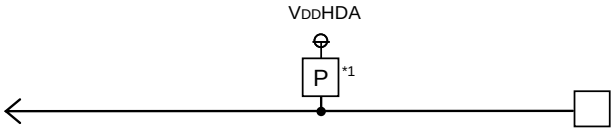
□ : External pins

Symbol	Equivalent circuit
V_{DD}LCN1 V_{DD}LCN2	
VSSLCN1 VSSLCN2	VSSLCN1 and VSSLCN2 are internally connected. 
V_{DD}LSC1 V_{DD}LSC2	V_{DD}LSC1 and V_{DD}LSC2 are internally connected. 
VSSLSC1 VSSLSC2 VSSLSC3	VSSLSC1, VSSLSC2 and VSSLSC3 are internally connected. 
VSSLCB1 VSSLCB2	VSSLCB1 and VSSLCB2 are internally connected. 
V_{DD}HCM	

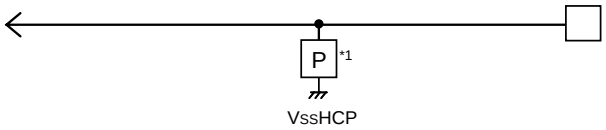
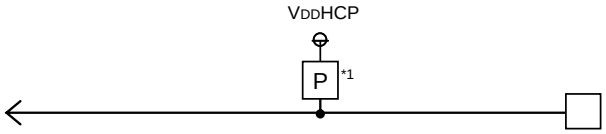
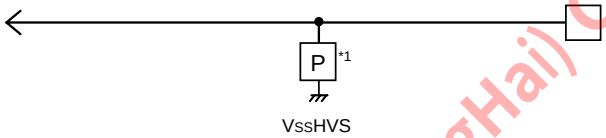
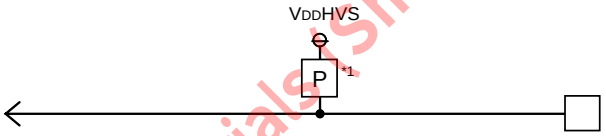
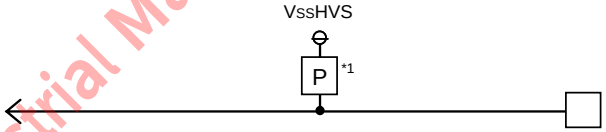
□ : External pins

Symbol	Equivalent circuit
$V_{DD}HPX$	
$V_{SS}HPX$	
$V_{DD}LPL$	
$V_{SS}LPL$	
$V_{DD}MLV1$ $V_{DD}MLV2$	$V_{DD}MLV1$ and $V_{DD}MLV2$ are internally connected. 
$V_{SS}MLV1$ $V_{SS}MLV2$ $V_{SS}MLV3$ $V_{SS}MLV4$	$V_{SS}MLV1$, $V_{SS}MLV2$, $V_{SS}MLV3$ and $V_{SS}MLV4$ are internally connected. 

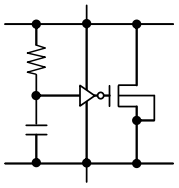
□ : External pins

Symbol	Equivalent circuit
DOxP(x=A to J) DOxM(x=A to J) DCKP DCKM	
VLOADLM	
VEXRES VBGR	
VDDHDA	
VSSHDA	

□ : External pins

Symbol	Equivalent circuit
$V_{DD}HCP$	
$V_{SS}HCP$	
$V_{DD}HVS$	
$V_{SS}HVS$	
VRLS VRLT	

Description of special symbol

Symbol	Equivalent circuit
	

□ : External pins

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics)

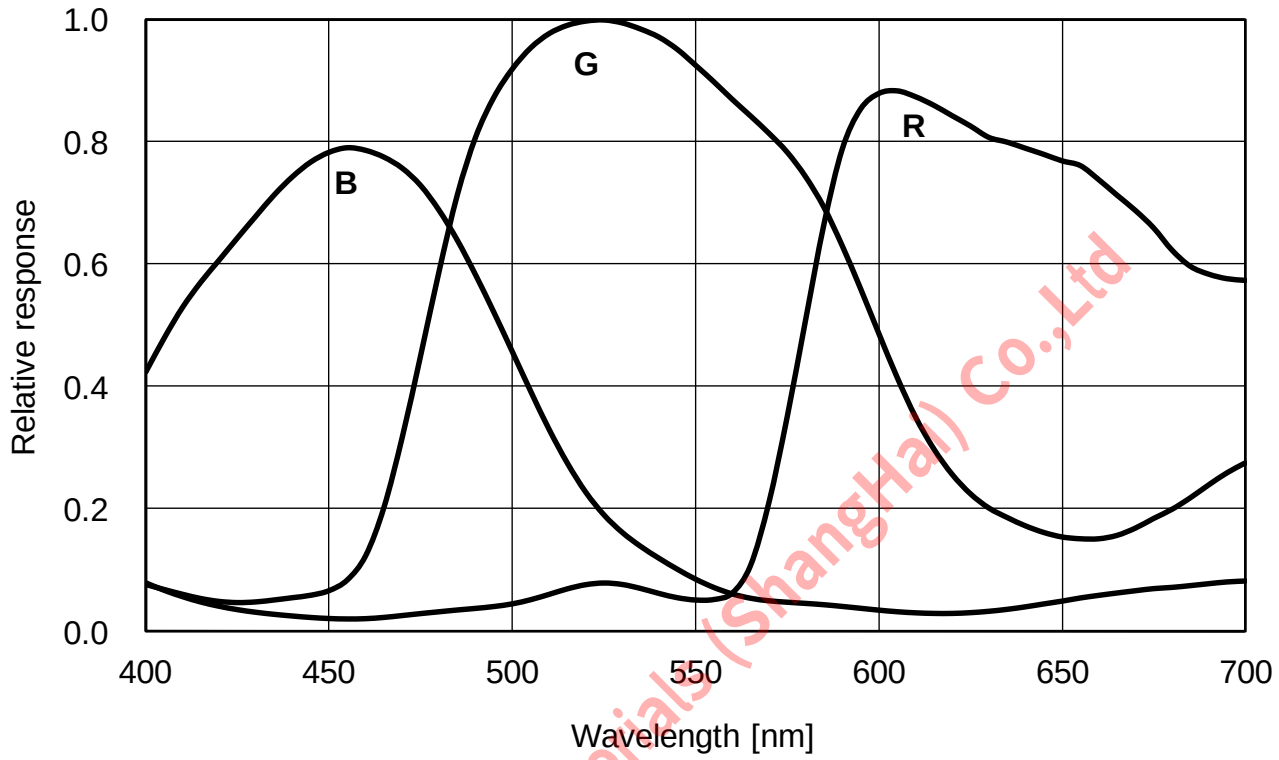


Image Sensor Characteristics

(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, Reference Gain (0 dB))

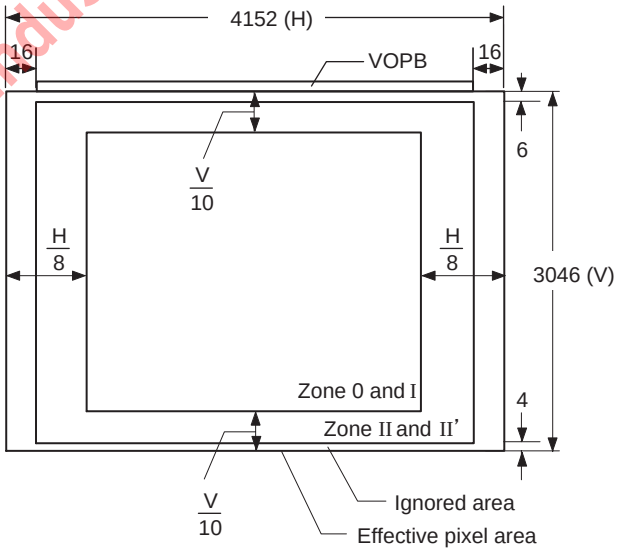
Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	1052 (209)	1405 (280)	—	digit (mV)	1	1/30 s integration conversion value 12-bit output
Sensitivity ratio	R	Rr	0.36	—	0.62		1	
	B	Rb	0.35	—	0.55		1	
Saturation signal		Vsat	4066 (810)	—	—	digit (mV)	2	12-bit output
Video signal shading		SHg	—	—	20	%	3	Zone 0 and zone I (the figure below)
			—	—	25			Zone 0, zone I, zone II and zone II' (the figure below)
Dark signal		Vdt	—	—	0.5 (0.1)	digit (mV)	4	1/30 s integration conversion value 12-bit output
Dark signal shading		ΔVdt	—	—	0.75 (0.15)	digit (mV)	5	1/30 s integration conversion value 12-bit output

Note)

1. Example of digit conversion: 1 digit ≈ 0.7967 mV when 10-bit output, 1 digit ≈ 0.1992 mV when 12-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.

1. Zone Definition of Video Signal Shading

Zone definition of video signal shading and reference position during dark signal measurement are shown below.



Zone Definition of Video Signal Shading and Reference Position during Dark Signal Measurement

Image Sensor Characteristics Measurement Method

1. Measurement Conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
(2) In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

2. Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

3. Definition of Standard Imaging Conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, Sensitivity ratio
Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr, Gb, R and B signal outputs (VGr, VGb, VR and VB) at the center of the screen, and substitute the values into the following formula.

VG = (VGr + VGb) /2
Sg = VG × 100/30 [mV]
Rr = VR/VG
Rb = VB/VG

2. Saturation signal
Set the measurement condition to the standard imaging condition II. Adjust the luminous intensity to 20 times the intensity with the average value of the G (= (Gr + Gb) / 2) signal output, 280 [mV] .
Measure the minimum values of the Gr, Gb, R and B signals when shooting in rolling shutter mode.

3. Video signal shading
   Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the G signal output is 280 [mV] .
   Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the G signal output, and substitute the values into the following formula.

   SHg = (Gmax – Gmin) / 280 × 100 [%]

4. Dark signal
   Measure the average value (Vdt [mV]) of the signal output in zone 0 to zone II' in the light-obstructed state.
   Define the average value of the signal output accumulated in 1 frame period (t1v) as Vdt1V and the average value of the signal output accumulated in the shortest period (1H period: t1h) as Vdt1H, and then substitute the values into the following formula.

   Vdt = (Vdt1V – Vdt1H) / (t1v – t1h) / 30 [mV]

5. Dark signal shading
   Following the item 4, measure the maximum value (Vdmax [mV]) and minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [mV]

Setting Registers by Serial Communication

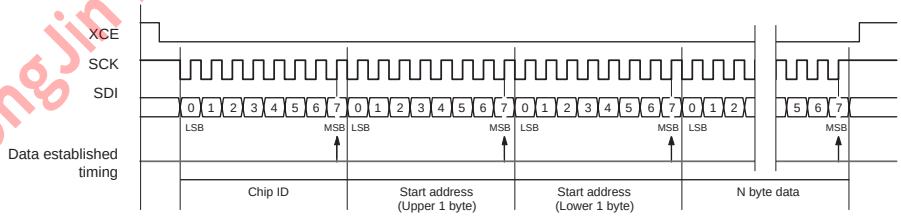
Sensor operation is controlled by the register settings. Follow the procedure below and make the register settings by serial communication.

1. Set XCE Low to enable the chip's serial communication function.
2. Transmit serial data (SDI) synchronized with SCK 1 bit at a time from the lower bits.
3. Transmit the Chip ID (fixed value : 81h) in the first byte.
4. Transmit the address value of the register to be set in the second and third bytes.
5. Transmit the register setting value to the address designated by the second and third bytes in the fourth byte.
6. Transmit the register setting value to the address following the address designated by the second and third bytes in the fifth byte.
7. Transmit the register setting values to subsequent addresses in order thereafter.
8. Set XCE High to end serial communication.

The IMX226CQJ clears the Chip ID and address setting data by setting XCE High.
Therefore, the Chip ID and address settings must also be made when the next serial communication is performed.
Continuous write across upper bytes is prohibited. When writing across upper bytes, first complete the above sequence, and then perform communication again. In addition, when jumping to a discontinuous address, also first complete the above sequence, and then perform communication again.
Perform serial communication within the 6XHS period (recommended serial communication period) after the fall of XVS to avoid affecting the image quality.
Settings made by serial communication are basically updated immediately each time 1 byte of setting values is transmitted. However, in some exceptional cases (electronic shutter setting, etc.), register setting values are updated immediately before the start of readout immediately after the recommended serial communication period (7th XHS).
For details, see “Register Map” on pages 27 to 30 and “1. Register Value Reflection Timing to Output Data” on page 31.

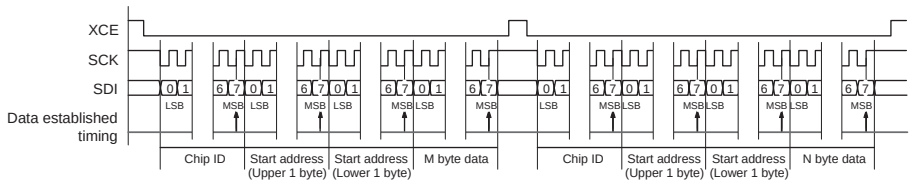
Note) 1. Communication is always accepted.
2. Communication should be completed within the recommended serial communication period to prevent noise. However, this restriction does not apply during the readout period of non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), so register communication can be performed other than during the communication period of those frames.
3. Communications with the following registers should always be performed within the same recommended serial communication period. Do not communicate with the 3 registers other than during communication period, even in non-picture frames in which noise is ignored.
   - PGC register (address 0009h, bit [7:0] and address 000Ah, bit [2:0])
   - APGC01 register (address 0352h, bit [7:0] and address 0353h, bit [0])
   - APGC02 register (address 0356h, bit [7:0] and address 0357h, bit [0])

Example of Serial Communication Timing 1



Example of Serial Communication 1

Example of Serial Communication Timing 2



Example of Serial Communication 2

Register Map

The register map is given below.

Address	Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
0000h	[0]	1h	Immediately	STANDBY	0h : Normal operation 1h : Overall standby	Setting range: 0h to 1h
	[1]	1h	Immediately	STBLOGIC	0h: Normal operation 1h: Digital circuit standby other than serial communications block	Setting range: 0h to 1h
	[7:2]	01h			—	Set the default value.
0001h	[0]	0h	Immediately	DCKRST	When changed from 0h to 1h: Fixes the LVDS clock output phase	Setting range: 0h to 1h After fixing the LVDS clock output phase, the value is automatically returned to 0h.
	[3:1]	0h			—	Set the default value.
	[4]	0h	Communication end frame *1	CLPSQRST	When changed from 0h to 1h: Resets the internal clamp circuit operation mode	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
	[7:5]	0h			—	Set the default value.
0002h	[0]	0h	*1	SSBRK	When changed from 0h to 1h: Interrupt enable	Setting range: 0h to 1h After the interrupt, the value is automatically returned to 0h.
	[7:1]	00h			—	Set the default value.
0003h	[3:0]	0h	*1	STBLVDS	0h : 10 ch 1h : 8 ch 3h : 4 ch Fh : All channel standby	Allowable setting values are 0h, 1h, 3h, and Fh.
	[6:4]	4h	*1	CHSEL	Number of LVDS output channels selection 0h : 10 ch 1h : 8 ch 3h : 4 ch	Allowable setting values are 0h, 1h, and 3h.
	[7]	0h			—	Set the default value.
0004h	[7:0]	2Ah	*1	MDSEL1		Set the value according to each readout mode register setting.
0005h	[7:0]	1Ch	*1	MDSEL2		Set the value according to each readout mode register setting.
0006h	[7:0]	00h	*1	MDSEL3		Set the value according to each readout mode register setting.
0007h	[7:0]	00h	*1	MDSEL4		Set the value according to each readout mode register setting.
0008h	[7:0]	0h			—	Set the default value.
0009h	[7:0]	000h	Immediately	PGC	Analog gain setting	Setting range: 0h to 7A5h
000Ah	[2:0]					
	[7:3]	00h			—	Set the default value.
000Bh	[7:0]	0007h	Next frame after communication end *2	SHR	Specifies the integration start horizontal period	Setting range is shown in ”Description of Registers”
000Ch	[7:0]					
000Dh	[7:0]	0000h	*2	SVR	Specifies the integration shutdown vertical period	Setting range: 0h to FFFFh
000Eh	[7:0]					
000Fh	[7:0]	0000h	*2	SPL	Specifies the integration start vertical period	Setting range: 0h to FFFFh
0010h	[7:0]					

Address	Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
0011h	[1:0]	0h	*1	DGAIN	Digital gain setting 0h : 0 dB gain setting value 1h : +6 dB gain setting value 2h : +12 dB gain setting value 3h : +18 dB gain setting value	Setting range: 0h to 3h
	[7:2]	00h			—	Set the default value.
0012h	[0]	0h	*1	FREQ	0h: (INCK × 4) MHz-DDR output 1h: (INCK × 2) MHz-DDR output	Setting range: 0h to 1h
	[7:1]	00h				
001Ah	[0]	0h	*1	MDVREV	0h : Vertical direction normal readout 1h : Vertical direction inversion readout	Setting range: 0h to 1h
	[7:1]	00h			—	Set the default value.
0026h	[7:0]	74h	*1	MDSEL13		Set the value according to each readout mode register setting.
0027h	[7:0]	74h	*1	MDSEL14		Set the value according to each readout mode register setting.
0028h	[7:0]	74h	*1	MDSEL15		Set the value according to each readout mode register setting.
0045h	[7:0]	32h	Immediately	BLKLEVEL	Digital black level offset setting	Setting range: 0h to FFh 10-bit readout mode : 1digit/1h 12-bit readout mode : 4digit/1h
004Dh	[3:0]	0h				Set the default value.
	[5:4]	0h	Immediately	PLSTMG01	Drive pulse timing setting 01	Set to 1h.
	[7:6]	0h				Set the default value.
0054h	[7:0]	05h	Immediately	PLSTMG02	Drive pulse timing setting 02	Set to 04h.
0057h	[7:0]	25h	Immediately	PLSTMG03	Drive pulse timing setting 03	Set to 24h.
007Eh	[7:0]	0000h	*1	MDSEL5		Set the value according to each readout mode register setting.
007Fh	[7:0]					
0080h	[7:0]	00h	Immediately	MDPLS01		Set the value according to each readout mode register setting.
0081h	[7:0]	00h	Immediately	MDPLS02		Set the value according to each readout mode register setting.
0082h	[7:0]	00h	Immediately	MDPLS03		Set the value according to each readout mode register setting.
0083h	[7:0]	00h	Immediately	MDPLS04		Set the value according to each readout mode register setting.
0084h	[7:0]	00h	Immediately	MDPLS05		Set the value according to each readout mode register setting.
0085h	[7:0]	00h	Immediately	MDPLS06		Set the value according to each readout mode register setting.
0086h	[7:0]	00h	Immediately	MDPLS07		Set the value according to each readout mode register setting.
0087h	[7:0]	00h	Immediately	MDPLS08		Set the value according to each readout mode register setting.
0095h	[7:0]	00h	Immediately	MDPLS09		Set the value according to each readout mode register setting.
0096h	[7:0]	00h	Immediately	MDPLS10		Set the value according to each readout mode register setting.
0097h	[7:0]	00h	Immediately	MDPLS11		Set the value according to each readout mode register setting.
0098h	[7:0]	00h	Immediately	MDPLS12		Set the value according to each readout mode register setting.
0099h	[7:0]	00h	Immediately	MDPLS13		Set the value according to each readout mode register setting.
009Ah	[7:0]	00h	Immediately	MDPLS14		Set the value according to each readout mode register setting.
009Bh	[7:0]	00h	Immediately	MDPLS15		Set the value according to each readout mode register setting.
009Ch	[7:0]	00h	Immediately	MDPLS16		Set the value according to each readout mode register setting.
00B6h	[7:0]	00h	Immediately	MDSEL6		Set the value according to each readout mode register setting.
00B7h	[7:0]	00h	Immediately	MDSEL7		Set the value according to each readout mode register setting.
00B8h	[7:0]	00h	Immediately	MDSEL8		Set the value according to each readout mode register setting.
00B9h	[7:0]	00h	Immediately	MDSEL9		Set the value according to each readout mode register setting.
00BAh	[7:0]	00h	Immediately	MDSEL10		Set the value according to each readout mode register setting.

Address	Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
00BBh	[7:0]	00h	Immediately	MDSEL11		Set the value according to each readout mode register setting.
00BCh	[7:0]	00h	Immediately	MDPLS17		Set the value according to each readout mode register setting.
00BDh	[7:0]	00h	Immediately	MDPLS18		Set the value according to each readout mode register setting.
00BEh	[7:0]	00h	Immediately	MDPLS19		Set the value according to each readout mode register setting.
00BFh	[7:0]	00h	Immediately	MDPLS20		Set the value according to each readout mode register setting.
00C0h	[7:0]	00h	Immediately	MDPLS21		Set the value according to each readout mode register setting.
00C1h	[7:0]	00h	Immediately	MDPLS22		Set the value according to each readout mode register setting.
00C2h	[7:0]	00h	Immediately	MDPLS23		Set the value according to each readout mode register setting.
00C3h	[7:0]	00h	Immediately	MDPLS24		Set the value according to each readout mode register setting.
00C4h	[7:0]	00h	Immediately	MDPLS25		Set the value according to each readout mode register setting.
00C5h	[7:0]	00h	Immediately	MDPLS26		Set the value according to each readout mode register setting.
00C6h	[7:0]	00h	Immediately	MDPLS27		Set the value according to each readout mode register setting.
00C7h	[7:0]	00h	Immediately	MDPLS28		Set the value according to each readout mode register setting.
00C8h	[7:0]	00h	Immediately	MDPLS29		Set the value according to each readout mode register setting.
00C9h	[7:0]	00h	Immediately	MDPLS30		Set the value according to each readout mode register setting.
00CAh	[7:0]	00h	Immediately	MDPLS31		Set the value according to each readout mode register setting.
00CBh	[7:0]	00h	Immediately	MDPLS32		Set the value according to each readout mode register setting.
00CCh	[7:0]	00h	Immediately	MDPLS33		Set the value according to each readout mode register setting.
00CEh	[7:0]	00h	*1	MDSEL12		Set the value according to each readout mode register setting.
0210h	[7:0]	000h	Immediately	PLSTMG04	Drive pulse timing setting 04	Set to 00Ah.
0211h	[0]					
	[7:1]	00h			—	Set the default value.
0212h	[7:0]	1FFh	Immediately	PLSTMG05	Drive pulse timing setting 05	Set to 131h.
0213h	[0]					
	[7:1]	00h			—	Set the default value.
021Ch	[7:0]	08Bh	Immediately	PLSTMG22	Drive pulse timing setting 22	Set to 064h.
021Dh	[0]					
	[7:1]	00h				Set the default value.
021Eh	[7:0]	12Bh	Immediately	PLSTMG06	Drive pulse timing setting 06	Set to 0EFh.
021Fh	[0]					
	[7:1]	00h			—	Set the default value.
0222h	[7:0]	12Ch	Immediately	PLSTMG23	Drive pulse timing setting 23	Set to 130h.
0223h	[0]					
	[7:1]	00h			—	Set the default value.
0313h	[4:0]	00h	Immediately	PLSTMG07	Drive pulse timing setting 07	Set to 10h.
	[7:5]	0h			—	Set the default value.
0352h	[7:0]	03Ch	Immediately	APGC01	Analog gain setting 01	Setting value is shown in “Description of register”.
0353h	[0]					
	[7:1]	00h			—	Set the default value.
0356h	[7:0]	03Bh	Immediately	APGC02	Analog gain setting 02	Setting value is shown in “Description of register”.
0357h	[0]					
	[7:1]	00h			—	Set the default value.
0366h	[0]	0h	Immediately	PLSTMG08	Drive pulse timing setting 08	Set to 1h.
	[7:1]	00h			—	Set the default value.
0371h	[1:0]	2h	Immediately	PLSTMG09	Drive pulse timing setting 09	Set to 1h.
	[7:2]	00h			—	Set the default value.
0528h	[4:0]	11h	Immediately	PLSTMG 10	Drive pulse timing setting 10	Set to 0Fh.
	[7:5]	0h			—	Set the default value.
0529h	[4:0]	11h	Immediately	PLSTMG 11	Drive pulse timing setting 11	Set to 0Fh.
	[7:5]	0h			—	Set the default value.

Address	Bit assignment	Default value	Reflection timing	Register name	Function	Remarks
052Ch	[4:0]	00h	Immediately	PLSTMG 12	Drive pulse timing setting 12	Set to 1Fh.
	[7:5]	0h			—	Set the default value.
052Dh	[7:0]	259h	Immediately	PLSTMG13	Drive pulse timing setting 13	Set to 401h.
052Eh	[2:0]					
	[7:3]	00h			—	Set the default value.
0534h	[7:0]	00h	Immediately	PLSTMG24	Drive pulse timing setting 24	Set to 10h.
057Ah	[7:0]	005h	Immediately	PLSTMG14	Drive pulse timing setting 14	Set to 00Bh.
057Bh	[0]					
	[7:1]	00h			—	Set the default value.
057Dh	[4:0]	10h	Immediately	PLSTMG15	Drive pulse timing setting 15	Set to 0Ah.
	[7:5]	0h			—	Set the default value.
057Eh	[3:0]	3h	Immediately	PLSTMG16	Drive pulse timing setting 16	Set to 0h.
	[7:4]	0h			—	Set the default value.
0582h	[2:0]	1h	Immediately	PLSTMG17	Drive pulse timing setting 17	Set to 7h.
	[7:3]	00h			—	Set the default value.
0617h	[3:0]	0h			—	Set the default value.
	[4]	0h	Immediately	PLSTMG18	Drive pulse timing setting 18	Set to 1h.
	[7:5]	0h			—	Set the default value.
0650h	[0]	1h	Immediately	PLSTMG19	Drive pulse timing setting 19	Set to 0h.
	[7:1]	00h			—	Set the default value.
065Ch	[4:0]	03h	Immediately	PLSTMG20	Drive pulse timing setting 20	Set to 07h.
	[7:5]	0h			—	Set the default value.
0700h	[7:0]	1918h	Immediately	PLSTMG21	Drive pulse timing setting 21	Set to 1919h.
0701h	[4:0]					
	[7:5]	0h			—	Set the default value.

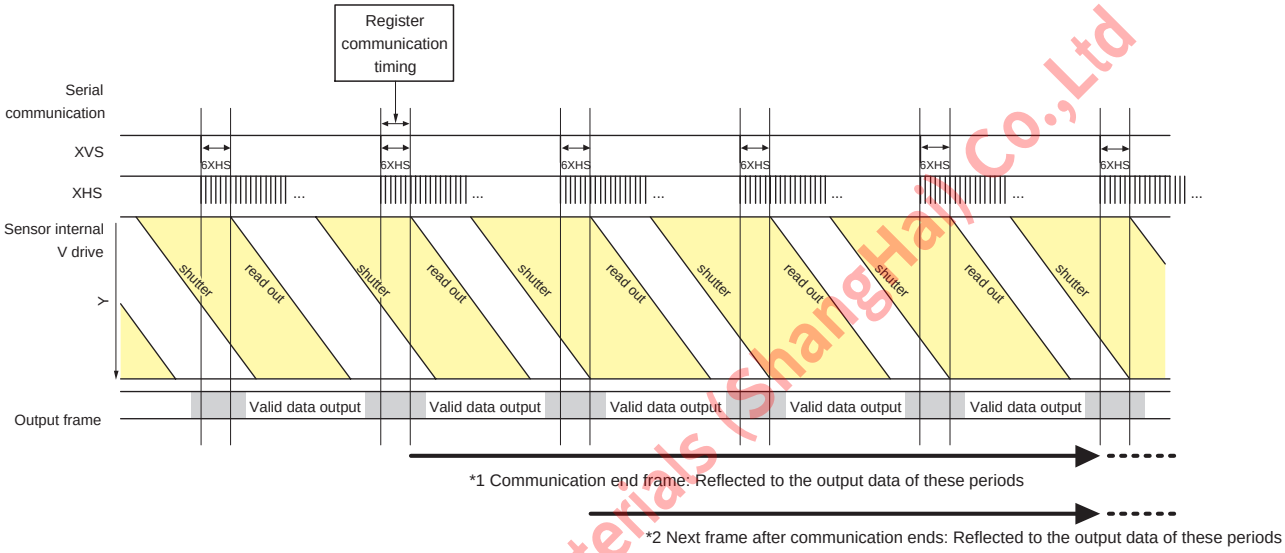
Note) • The “Default value” column indicates the initial value set in each register in the status before register communication is performed after start-up or after the reset signal XCLR is set to Low to reset the sensor.
• Operation is not guaranteed when using register settings other than noted in these specifications. Do not access addresses not noted in the table above, and do not set register values other than those noted in “2. Description of Registers” on pages 32 to 39
• When changing the mode, the address set designated in “3. Register Settings for Each Readout Drive Mode” on pages 40 to 41 must be written.
• For the detailed reflection timing, see “1. Register Value Reflection Timing to Output Data” on page 31.

1. Register Value Reflection Timing to Output Data

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Explanation
*1. Communication end frame	The communication contents are reflected to the output data from the V period during which communication was performed.
*2. Next frame after communication end	The communication contents are reflected to the output data from the next V period after the V period during which communication was performed.

For which reflection timing of each register, see “Register Map” on pages 27 to 30.



2. Description of Register

Total Standby Control

All sensor operation is stopped and the standby mode that reduces power consumption is established by setting the overall standby control register STANDBY (address 0000h, bit [0]) to “1h”.
(Standby mode is established immediately after reset.)
The serial communication block operates even in standby mode, so standby mode can be canceled by setting “0h” in the STANDBY register.

STANDBY Setting

Register value	Function
0h	Normal operation
1h	Overall standby

Digital Circuit Standby Control

Sensor digital circuit operation other than the serial communication block is stopped by setting the digital circuit standby control register STBLOGIC (address 0000h, bit [1]) to "1h". This register is valid only when STANDBY = 0h.
(Standby mode is established according to the STANDBY register initial value immediately after a reset.)
Set this register according to the recommended sequence during power-on or when canceling standby mode.

STBLOGIC Setting

Register value	Function
0h	Normal operation
1h	Digital circuit standby other than serial communications block

LVDS Clock Output Phase Fixed

The clock phase relative to the sync code start data in the LVDS data output is fixed by the LVDS clock output phase fixing register DCKRST (address 0001h, bit [0]). Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the phase fixing process, so there is no need to write “0h”.

DCKRST Operation Setting

Register value	Function
Changed from 0h to 1h	Fixes the LVDS clock output phase

Clamp Reset

The internal clamp circuit operation status is reset by the clamp reset register CLPSQRST (address 0001h, bit [4]). Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the reset process, so there is no need to write “0h”.

CLPSQRST Operation Setting

Register value	Function
Changed from 0h to 1h	Resets the internal clamp circuit operation status

Break Mode

XVS can be subsampled according to SVR. This XVS subsampling operation can be stopped and then restarted from the start of the exposure period using the break mode register SSBRK (address 0002h, bit [0]). This register automatically returns to “0h” after the break process, so there is no need to write “0h”.

SSBRK Setting

Register value	Function
Changed from 0h to 1h	Interrupt enable

subLVDS Standby Control

This sensor can set the subLVDS to standby mode according to the setting value by setting the subLVDS standby control register STBLVDS (address 0003h, bit [3:0]).

STBLVDS Setting

Register value	Function
0h	10 ch
1h	8 ch
3h	4 ch
Fh	All channel standby

subLVDS standby control is shown below.

dec	bin	hex	Function	A	B	C	D	E	DCK	F	G	H	I	J
STBLVDS [3:0]														
0d	0000b	0h	10 ch	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
1d	0001b	1h	8 ch	Active	Active	Active	STBY	Active	Active	Active	STBY	Active	Active	Active
3d	0011b	3h	4 ch	STBY	STBY	Active	STBY	Active	Active	Active	STBY	Active	STBY	STBY
15d	1111b	Fh	All Standby	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY

Number of LVDS Output Channels Selection

This sensor can set the number of output channels according to the setting value by setting the number of LVDS output channels selection register CHSEL (address 0003h, bit [6:4]).

CHSEL Setting

Register value	Function
0h	10 ch
1h	8 ch
3h	4 ch

Number of LVDS channels control is shown below.

dec	bin	hex	Function	A	B	C	D	E	DCK	F	G	H	I	J
CHSEL [2:0]														
0d	0000b	0h	10 ch	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
1d	0001b	1h	8 ch	Active	Active	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Active	Active
3d	0011b	3h	4 ch	Fixed Low	Fixed Low	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Fixed Low	Fixed Low

Electronic Shutter Timing

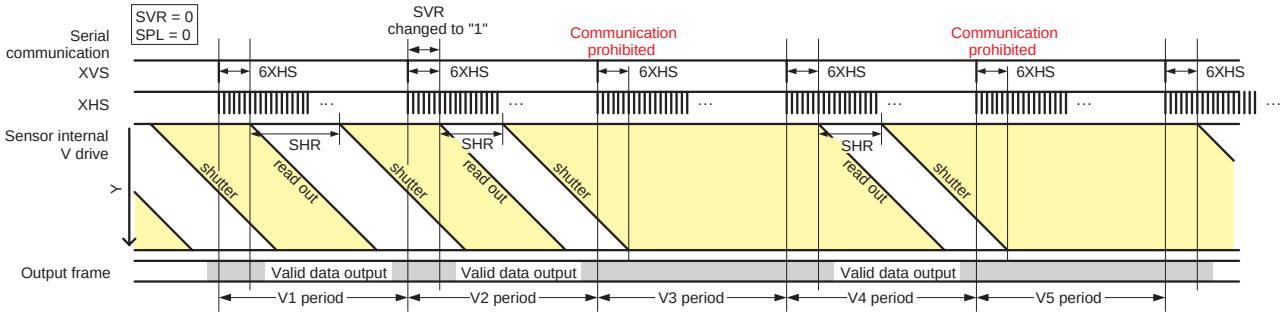
The exposure start timing can be designated by setting the electronic shutter timing register SHR (address 000Bh, bit [7:0] and address 000Ch, bit [7:0]). Designate the lower 8 bits in address 000Bh and the upper 8 bits in address 000Ch, for a total of 16 bits.
Note that this setting value unit is 1XHS period regardless of the readout drive mode. In addition, the vertical sync signal XVS can be subsampled inside the sensor according to the SVR register (address 000Dh, bit [7:0] and address 000Eh, bit [7:0]). The vertical sync signal period is treated as SVR + 1 inside the sensor.
When setting the electronic shutter during the vertical sync signal subsampling period, the SPL register (address 000Fh, bit [7:0] and address 0010h, bit [7:0]) is available.

Shutter Setting

Register	Register value		Function
SHR	8 to {(SVR + 1) × Number of XHS pulses per frame – 4}	Readout mode No.0, 1, 2, 3, 4 All-pixel scan mode (12 bits/10 bits)	Specifies the integration start horizontal period
	10 to {(SVR + 1) × Number of XHS pulses per frame – 4}	Readout mode No.5, Horizontal/vertical 2/2-line binning mode	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period
SPL	0h to FFFFh *Note 2.		Specifies the integration start vertical period

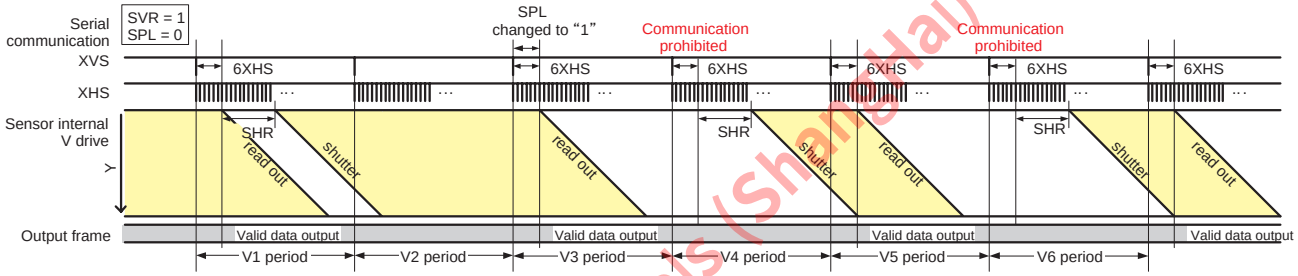
Note) 1. See “Integration Time in Each Readout Drive Mode” on page 55 for the integration time calculation formula.
2. The SVR and SPL register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.

Example of Electronic Shutter Operation 1



Example of SVR operation

Example of Electronic Shutter Operation 2



Example of SVR and SPL operation

Note) In vertical sync signal subsampling periods (Electronic Shutter Operation Example 1: V3 and V5 periods, Electronic Shutter Operation Example 2: V4 and V6 periods), communication is prohibited during the normal communication period (the 6XHS period after the vertical sync signal XVS is input), except in the following case.

- When stopping vertical sync signal subsampling using the break mode register SSBRK.

Analog Gain

The analog gain value can be set by setting the analog gain register PGC (address 0009h, bit [7:0] and address 000Ah, bit [2:0]). Set the lower 8 bits in address 0009h and the upper 3 bits in address 000Ah, for a total of 11 bits. In addition, change APGC01 (address 0352h, bit [7:0] and address 0353h, bit [0]) and APGC02 (address 0356h, bit [7:0] and address 0357h, bit [0]) linked with the analog gain register PGC. Communications with PGC, APGC01 and APGC02 should always be performed within the same recommended serial communication period. Do not communicate with the 3 registers other than during communication period, even in non-picture frames in which noise is ignored.
The values to be written are different with PGC setting and readout drive mode. See the following "APGC01 and APGC02 setting"for the detailed specifications.

PGC Setting

Register value	Function
0h to 7A5h (0d to 1957d)	Analog gain setting

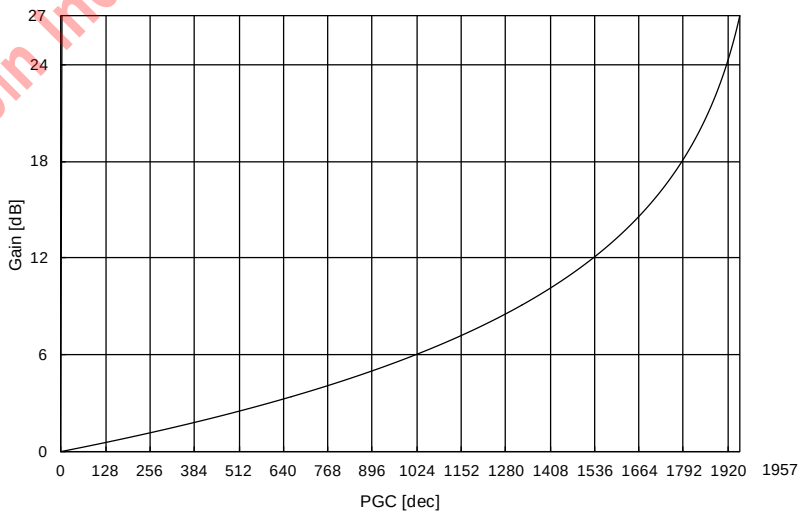
APGC01 and APGC02 Setting

PGC setting	Modes other than readout drive mode No.0,2,3 *1		Readout drive mode No.0,2,3 *1	
	APGC01 setting	APGC02 setting	APGC01 setting	APGC02 setting
0h to 146h	1Eh	1Dh	3Ch	3Bh
147h to 400h	20h	1Fh		
401h to 52Ch	25h	24h		
52Dh to 696h	27h	26h		
697h to 74Bh	2Bh	2Ah		
74Ch to 7A5h	2Fh	2Eh		

*1. See “1. Readout Drive Modes” on pages 42 for details of readout mode No.
In addition, the figure below shows the relationship between the register setting value and the set gain value. When the register setting value is “0h (0d) ”, the gain value is 0 dB (minimum settable value), and when “7A5h (1957d) ”, the gain value is approximately 27 dB (maximum settable value).

Relational Formula

Gain [dB] = –20log {(2048 – PGC [10:0]) /2048}



Relationship between Register Setting Value and Set Gain Value

Digital Gain

The digital gain applied to the data after pixel binning can be set by the digital gain setting register DGAIN (address 0011h, bit [1:0]).

DGAIN Setting

Register value	Function
0h	Digital gain setting value = 0 dB
1h	Digital gain setting value = +6 dB
2h	Digital gain setting value = +12 dB
3h	Digital gain setting value = +18 dB

Output Format

The LVDS-I/F output frequency can be set by the output format setting register, FREQ (address 0012h, bit [0]).
The readout drive mode in this data sheet is specified under the condition of FREQ = 0h. The data rate and the frame frequency are the half of the described values when set to FREQ = 1h.

FREQ Setting

Register value	Function
0h	(INCK × 4) MHz-DDR output
1h	(INCK × 2) MHz-DDR output

Vertical Direction Readout Inversion

The direction of vertical readout order can be set by the vertical direction readout inversion register MDVREV (address 001Ah, bit [0]).

MDVREV Setting

Register value	Function
0h	Vertical direction normal readout
1h	Vertical direction inversion readout

Digital Black Level Offset

The black level offset applied to the data after digital gain processing by the DGAIN register is set by the digital black level offset setting register BLKLEVEL (address 0045h, bit [7:0]).
Note that the offset unit changes according to the readout drive mode. When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 digit. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 digits.

BLKLEVEL Setting

Register value	Function
0h to FFh	Digital black level offset setting

*Use with values shown below is recommended.
10 bit output: 32h (50 digit)
12 bit output: 32h (200 digit)

Readout Drive Mode

The readout drive mode of this sensor can be switched by setting the readout drive mode register MDSEL1 to MDSEL15 and MDPLS01 to MDPLS33. When changing the mode, make the setting according to “3. Register Settings for Each Readout Drive Mode” on pages 40 to 41.

Readout Drive Pulse Timing

The drive pulse timing is set by readout drive pulse timing registers PLSTMG01 to PLSTMG24.

PLSTMG01 to PLSTMG24 Setting

Address	Bit assignment	Default value	Register name	Register Value
004Dh	[3:0]	0h		Set the default value.
	[5:4]	0h	PLSTMG01	1h
	[7:6]	0h		Set the default value.
0054h	[7:0]	05h	PLSTMG02	04h
0057h	[7:0]	25h	PLSTMG03	24h
0210h	[7:0]	000h	PLSTMG04	00Ah
0211h	[0]			
	[7:1]	00h		Set the default value.
0212h	[7:0]	1FFh	PLSTMG05	131h
0213h	[0]			
	[7:1]	00h		Set the default value.
021Ch	[7:0]	08Bh	PLSTMG22	064h
021Dh	[0]			
	[7:1]	00h		Set the default value
021Eh	[7:0]	12Bh	PLSTMG06	0EFh
021Fh	[0]			
	[7:1]	00h		Set the default value.
0222h	[7:0]	12Ch	PLSTMG23	130h
0223h	[0]			
	[7:1]	00h		Set the default value.
0313h	[4:0]	00h	PLSTMG07	10h
	[7:5]	0h		Set the default value.
0366h	[0]	0h	PLSTMG08	1h
	[7:1]	00h		Set the default value.
0371h	[1:0]	2h	PLSTMG09	1h
	[7:2]	00h		Set the default value.
0528h	[4:0]	11h	PLSTMG10	0Fh
	[7:5]	0h		Set the default value.
0529h	[4:0]	11h	PLSTMG11	0Fh
	[7:5]	0h		Set the default value.
052Ch	[4:0]	00h	PLSTMG12	1Fh
	[7:5]	0h		Set the default value.
052Dh	[7:0]	259h	PLSTMG13	401h
052Eh	[2:0]			
	[7:3]	00h		Set the default value.
0534h	[7:0]	00h	PLSTMG24	10h
057Ah	[7:0]	005h	PLSTMG14	00Bh
057Bh	[0]			
	[7:1]	00h		Set the default value.
057Dh	[4:0]	10h	PLSTMG15	0Ah
	[7:5]	0h		Set the default value.
057Eh	[3:0]	3h	PLSTMG16	0h
	[7:4]	0h		Set the default value.
0582h	[2:0]	1h	PLSTMG17	7h
	[7:3]	00h		Set the default value.
0617h	[3:0]	0h		Set the default value.
	[4]	0h	PLSTMG18	1h
	[7:5]	0h		Set the default value.
0650h	[0]	1h	PLSTMG19	0h
	[7:1]	00h		Set the default value.
065Ch	[4:0]	03h	PLSTMG20	07h
	[7:5]	0h		Set the default value.
0700h	[7:0]	1918h	PLSTMG21	1919h
0701h	[4:0]			
	[7:5]	0h		Set the default value.

3. Register Setting for Each Readout Drive Mode

The register setting for each readout drive mode available with this sensor is shown in the table below.

Address	Bit assignment	Register name	Readout mode No.*1					
			0	1	2	3	4	5
0000h	[0]	STANDBY	0h					
	[1]	STBLOGIC	0h					
	[7:2]		01h					
0003h	[3:0]	STBLVDS	0h	0h	1h	3h	0h	3h
	[6:4]	CHSEL	0h	0h	1h	3h	0h	3h
	[7]		0h					
0004h	[7:0]	MDSEL1	00h	00h	80h	80h	80h	89h
0005h	[7:0]	MDSEL2	07h	01h	47h	47h	41h	4Dh
0006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	00h
0007h	[7:0]	MDSEL4	00h	00h	00h	00h	00h	00h
000Dh	[7:0]	SVR	According to exposure time					
000Eh	[7:0]							
001Ah	[0]	MDVREV	0h: vertical direction normal/1h:inverted					
	[7:1]		00h					
0026h	[7:0]	MDSEL13	74h	74h	74h	74h	74h	74h
0027h	[7:0]	MDSEL14	74h	74h	74h	74h	74h	74h
0028h	[7:0]	MDSEL15	74h	74h	74h	74h	74h	74h
007Eh	[7:0]	MDSEL5	0120h	0120h	0120h	0120h	0120h	0120h
007Fh	[7:0]							
0080h	[7:0]	MDPLS01	00h	00h	00h	00h	00h	00h
0081h	[7:0]	MDPLS02	00h	00h	00h	00h	00h	00h
0082h	[7:0]	MDPLS03	00h	00h	00h	00h	00h	00h
0083h	[7:0]	MDPLS04	00h	00h	00h	00h	00h	00h
0084h	[7:0]	MDPLS05	00h	00h	00h	00h	00h	00h
0085h	[7:0]	MDPLS06	00h	00h	00h	00h	00h	00h
0086h	[7:0]	MDPLS07	00h	00h	00h	00h	00h	00h
0087h	[7:0]	MDPLS08	00h	00h	00h	00h	00h	00h
0095h	[7:0]	MDPLS09	00h	00h	00h	00h	00h	00h
0096h	[7:0]	MDPLS10	00h	00h	00h	00h	00h	00h
0097h	[7:0]	MDPLS11	00h	00h	00h	00h	00h	00h
0098h	[7:0]	MDPLS12	00h	00h	00h	00h	00h	00h
0099h	[7:0]	MDPLS13	00h	00h	00h	00h	00h	00h
009Ah	[7:0]	MDPLS14	00h	00h	00h	00h	00h	00h
009Bh	[7:0]	MDPLS15	00h	00h	00h	00h	00h	00h
009Ch	[7:0]	MDPLS16	00h	00h	00h	00h	00h	00h
00B6h	[7:0]	MDSEL6	47h	47h	47h	47h	47h	67h
00B7h	[7:0]	MDSEL7	00h	00h	00h	00h	00h	00h
00B8h	[7:0]	MDSEL8	00h	00h	00h	00h	00h	00h
00B9h	[7:0]	MDSEL9	00h	00h	00h	00h	00h	00h

Address	Bit assignment	Register name	Readout mode No.*1					
			0	1	2	3	4	5
00BAh	[7:0]	MDSEL10	00h	00h	00h	00h	00h	00h
00BBh	[7:0]	MDSEL11	00h	00h	00h	00h	00h	00h
00BCh	[7:0]	MDPLS17	00h	00h	00h	00h	00h	00h
00BDh	[7:0]	MDPLS18	00h	00h	00h	00h	00h	00h
00BEh	[7:0]	MDPLS19	00h	00h	00h	00h	00h	00h
00BFh	[7:0]	MDPLS20	00h	00h	00h	00h	00h	00h
00C0h	[7:0]	MDPLS21	00h	00h	00h	00h	00h	00h
00C1h	[7:0]	MDPLS22	00h	00h	00h	00h	00h	00h
00C2h	[7:0]	MDPLS23	00h	00h	00h	00h	00h	00h
00C3h	[7:0]	MDPLS24	00h	00h	00h	00h	00h	00h
00C4h	[7:0]	MDPLS25	00h	00h	00h	00h	00h	00h
00C5h	[7:0]	MDPLS26	00h	00h	00h	00h	00h	00h
00C6h	[7:0]	MDPLS27	00h	00h	00h	00h	00h	00h
00C7h	[7:0]	MDPLS28	00h	00h	00h	00h	00h	00h
00C8h	[7:0]	MDPLS29	00h	00h	00h	00h	00h	00h
00C9h	[7:0]	MDPLS30	00h	00h	00h	00h	00h	00h
00CAh	[7:0]	MDPLS31	00h	00h	00h	00h	00h	00h
00CBh	[7:0]	MDPLS32	00h	00h	00h	00h	00h	00h
00CCh	[7:0]	MDPLS33	00h	00h	00h	00h	00h	00h
00CEh	[7:0]	MDSEL12	0Eh	0Eh	0Eh	0Eh	0Eh	0Eh

*1 See “1. Readout Drive Modes” on pages 42 for details of readout mode No.

Readout Drive Modes

1. Readout Drive Modes

The table below describes the readout drive modes that can be used to operate this sensor.
All of the modes listed in the table below support vertical direction inversion operation (MDVREV = 0h/1h).
Note that some readout drive modes need different (1) register settings and (2) vertical front blanking when vertical readout direction is normal and inverted.
See “3. Register Setting for Each Readout Drive Mode” on pages 40 to 41 for the register setting, and “Minimum Vertical Operation Period in Each Readout Drive Mode” on pages 47, and “Image Data Output Format” on pages 49 to 54 for the vertical front blanking.

1-1. Description of Readout Drive Modes

Readout mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (12M, A/D12 bit, 10 ch output)	All pixels are readout with 12-bit output.
1	All-pixel scan mode (12M, A/D10 bit, 10 ch output)	All pixels are readout with 10-bit output.
2	All-pixel scan mode (4K2K, A/D12 bit, 8 ch output)	All pixels are readout with 12-bit output.
3	All-pixel scan mode (4K2K, A/D12 bit, 4 ch output)	All pixels are readout with 12-bit output.
4	All-pixel scan mode (4K2K, A/D10 bit, 10 ch output)	All pixels are readout with 10-bit output.
5	Horizontal/vertical 2/2-line binning (4K2K, A/D10 bit, 4 ch output)	Horizontal and vertical direction 2-line binning readout of pixels of the same color (See the image of binning on page 43)

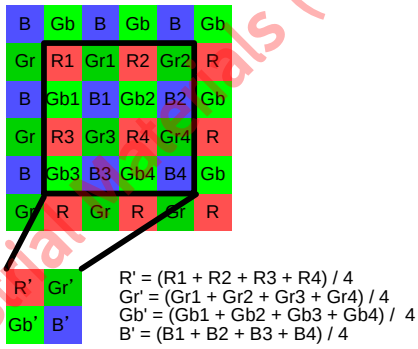
1-2. Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

The table below shows the relationship between the A/D conversion resolution, number of binning pixels, internal arithmetic processing, and number of output bits in each readout mode.
Note that the number of output bits differs in each mode. In addition the number of output bits is 10 bits, so the weight of 1 digit is 4 times greater than that during 12-bit output.

Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

Readout mode No.	A/D conversion resolution	Horizontal pixel processing	Vertical pixel processing	Total number of binning pixels	Internal arithmetic processing	Number of output bits
0	12 bits	—	—	—	—	12 bits
1	10 bits	—	—	—	—	10 bits
2	12 bits	—	—	—	—	12 bits
3	12 bits	—	—	—	—	12 bits
4	10 bits	—	—	—	—	10 bits
5	10 bits	2 binning	2 binning	4 pixels	1/4	10 bits + 2 bits *1

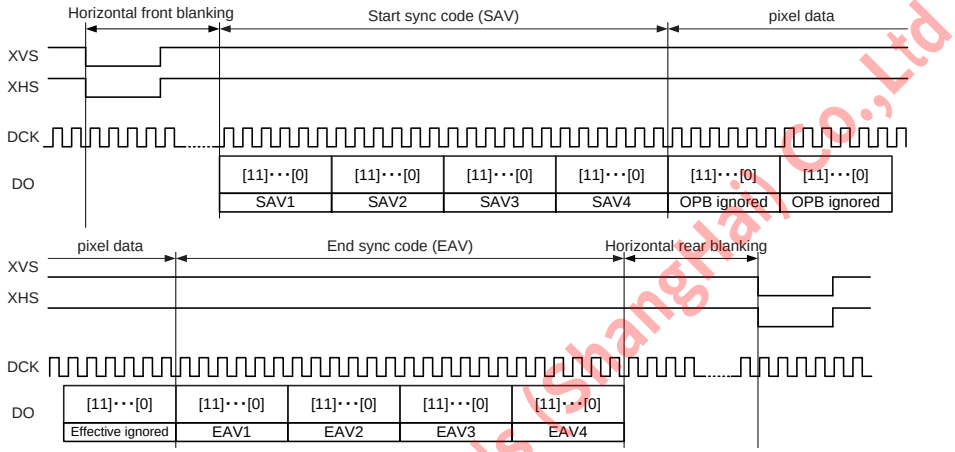
*1 Division is performed by internal arithmetic processing, then the results are output in 12 bits with the integer item in the upper 10 bits and the decimal item in the lower 2 bits.



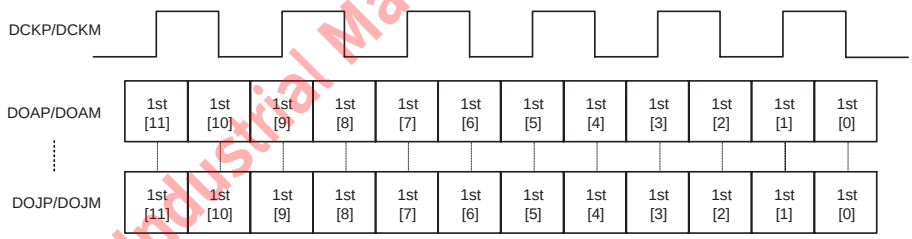
Horizontal/Vertical 2/2-line Binning Image

2. Sync Signals and Data Output Timing

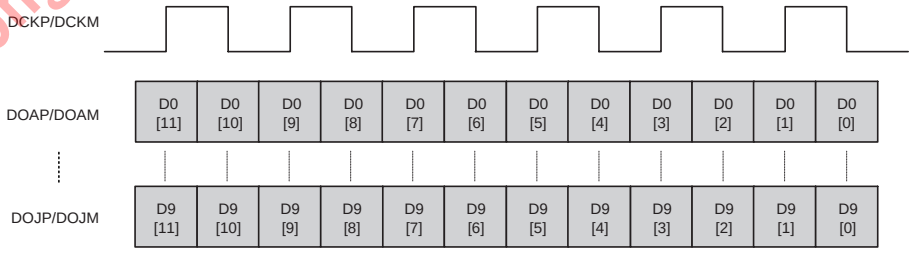
The figure below shows the sync signal and data output timing during 12-bit length serial output for this sensor.
The horizontal and vertical timing of the output data are controlled by the XVS and XHS sync signals. Timing control is performed at the falling edge of both the XVS and XHS signals. The data is output in order from the start sync code (SAV) after the horizontal front blanking period after the falling edge.
See “Minimum Horizontal Operation Period in Each Readout Drive Mode” on pages 47 for the detailed blanking length and number of OPB pixels. The length of horizontal front blanking pixels varies greatly according to the mode as described in “Minimum Horizontal Operation Period in Each Readout Drive Mode” on pages 47, so using the sync code as the trigger is recommended for the recording pixel start timing.
The sync code details are shown below.
In addition, the length of horizontal rear blanking changes when the XHS period is changed.



Sync Signal and Data Output Timing



Sync Signal and Data Output Timing



Serial Data Details (Sync Code Block)

Sync code details

LVDS output bit No.		Sync code (4 words)				
12-bit output	10-bit output	1st word	2nd word	3rd word	4th word	
11	9	1	0	0	1	
10	8	1	0	0	0	
9	7	1	0	0	V	1: Blanking line 0: Except blanking line
8	6	1	0	0	H	1: End sync code 0: Start sync code
7	5	1	0	0	P3	Protection bits
6	4	1	0	0	P2	
5	3	1	0	0	P1	
4	2	1	0	0	P0	
3	1	1	0	0	0	
2	0	1	0	0	0	
1	—	1	0	0	0	
0	—	1	0	0	0	

		Protection bits			
V	H	P3	P2	P1	P0
0	0	0	0	0	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

Sync code details (hexadecimal notation) 12-bit output

		1st word	2nd word	3rd word	4th word
Blanking line	Start sync code (SAV)	FFFh	000h	000h	AB0h
	End sync code (EAV)				B60h
Except blanking line	Start sync code (SAV)				800h
	End sync code (EAV)				9D0h

Sync code details (hexadecimal notation) 10-bit output

		1st word	2nd word	3rd word	4th word
Blanking line	Start sync code (SAV)	3FFh	000h	000h	2 ACh
	End sync code (EAV)				2D8h
Except blanking line	Start sync code (SAV)				200h
	End sync code (EAV)				274h

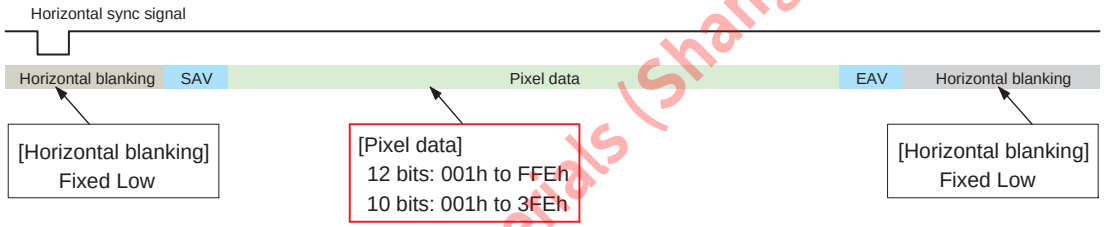
3. Output Range of LVDS Output Data

The table below shows the decimal point position, output bit length and output range of the output data in each readout mode. Note that the value of the first word of the sync code (3FFh, FFFh) and the maximum data value do not overlap in any readout mode.

Data output range in each readout mode

Readout mode No.	LVDS output		
	Decimal point position	Output bit length [bit]	Output range [hex]
0	2	12	001h to FFEh
1	0	10	001h to 3FEh
2	2	12	001h to FFEh
3	2	12	001h to FFEh
4	0	10	001h to 3FEh
5	2	12	001h to FFEh

Output value during horizontal blanking period is fixed to Low (all 0).



Readout Drive Timing

4. Detailed Specification of Each Mode

(1) Minimum Horizontal/Vertical Operation Period in Each Readout Drive Mode

Minimum Horizontal Operation Period in Each Readout Drive Mode

Readout mode No.	Data rate [MHz]	Horizontal front blanking [DCK] *2 *3	Minimum horizontal operation period (Number of pixels conversion)					XHS minimum period [INCK] *2
			Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
0	576 (288DDR *1)	348 to 353	96	36	4000	36	0	644
1	576 (288DDR *1)	348 to 353	96	36	4000	36	0	536
2	576 (288DDR *1)	348 to 353	96	28	4096	28	0	811
3	576 (288DDR *1)	348 to 353	96	28	4096	28	0	1608
4	576 (288DDR *1)	348 to 353	96	28	4096	28	0	546
5	576 (288DDR *1)	354 to 359	48	14	2048	14	0	407

*1 DDR : Double Data Rate

*2 If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.

*3 Number of LVDS output signal DCK clock

Minimum Vertical Operation Period in Each Readout Drive Mode

Readout mode No.	Number of lines per minimum vertical operation period (output data 1H conversion)						XVS minimum period [XHS]
	Vertical front blanking	Front OPB	Front effective pixel margin	Recommended recording pixels	Rear effective pixel margin	Rear OPB	
0	17 *1 16 *2	16	24	3000	22	0	3079
1	17 *1 16 *2	16	24	3000	22	0	3079
2	17 *1 16 *2	8	10	2160	4	0	2199
3	17 *1 16 *2	8	10	2160	4	0	2199
4	17 *1 16 *2	8	10	2160	4	0	2199
5	9 (20XHS)	4	10	1080	4	0	2216

*1 When vertical direction normal readout

*2 When vertical direction inverted readout

(2) Recommended Horizontal/Vertical Operation Period in Each Readout Drive Mode

Recommended H Period and V Periods

Readout mode No.	XHS period (INCK) *1	H period (number of XHS pulses) *2	V period (number of XHS pulses)	Frame frequency [frame/s]
0	660	1	3120	34.97
1	585	1	3080	39.96
2	1092	1	2200	29.97
3	2184	1	2200	14.99
4	546	1	2200	59.94
5	528	2	2275	59.94

*1 Number of INCK conversion clocks
*2 Number of XHS pulses required to output the data for one sensor line

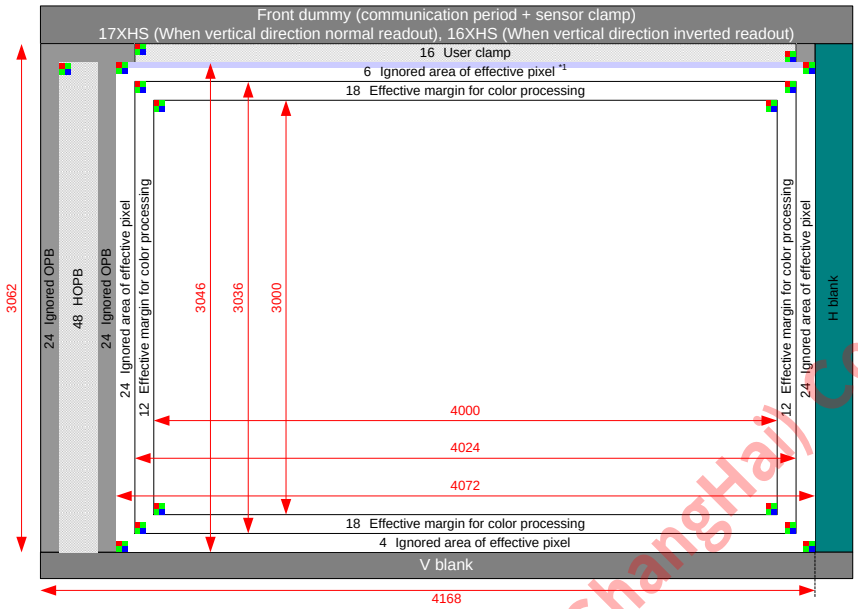
Imaging Conditions in Each Readout Drive Mode

Readout mode No.	Imaging conditions						
	Data rate [MHz]	Number of LVDS output channels [ch]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	576 (288DDR)	10	12	12	4000	3000	12.00 M pixels
1	576 (288DDR)	10	10	10	4000	3000	12.00 M pixels
2	576 (288DDR)	8	12	12	4096	2160	8.85 M pixels
3	576 (288DDR)	4	12	12	4096	2160	8.85 M pixels
4	576 (288DDR)	10	10	10	4096	2160	8.85 M pixels
5	576 (288DDR)	4	10	12	2048	1080	2.21 M pixels

5. Image Data Output Format

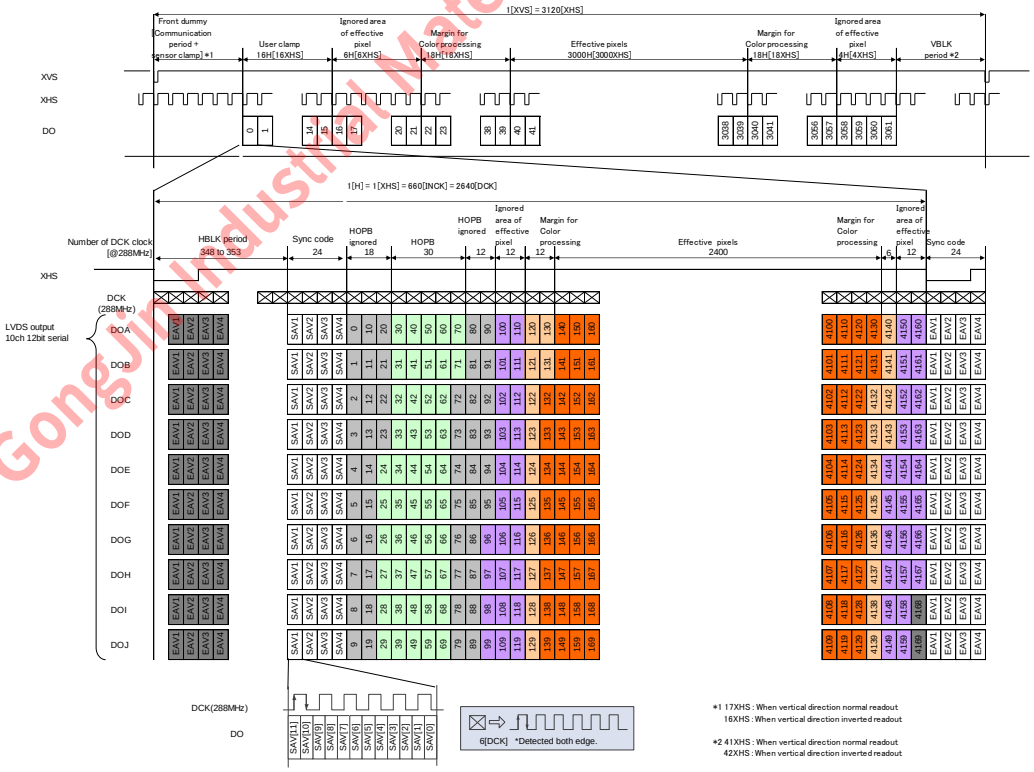
The output format in each readout drive mode is as follows.

MODE0 : All-pixel scan mode
(12M, 34.97 frame/s, 12-bit A/D conversion, 12-bit length output, 10 ch output)



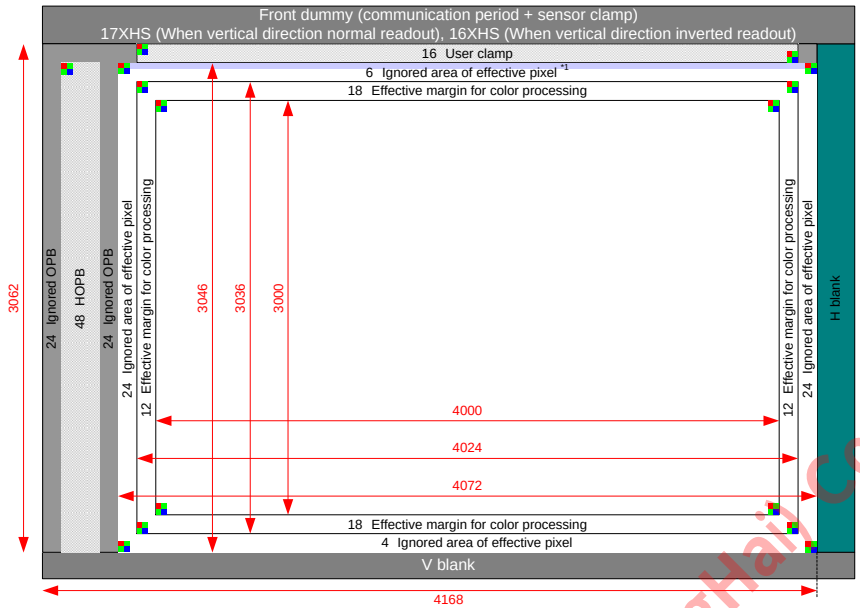
*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

Readout Pixel Image Diagram (4000 × 3000)



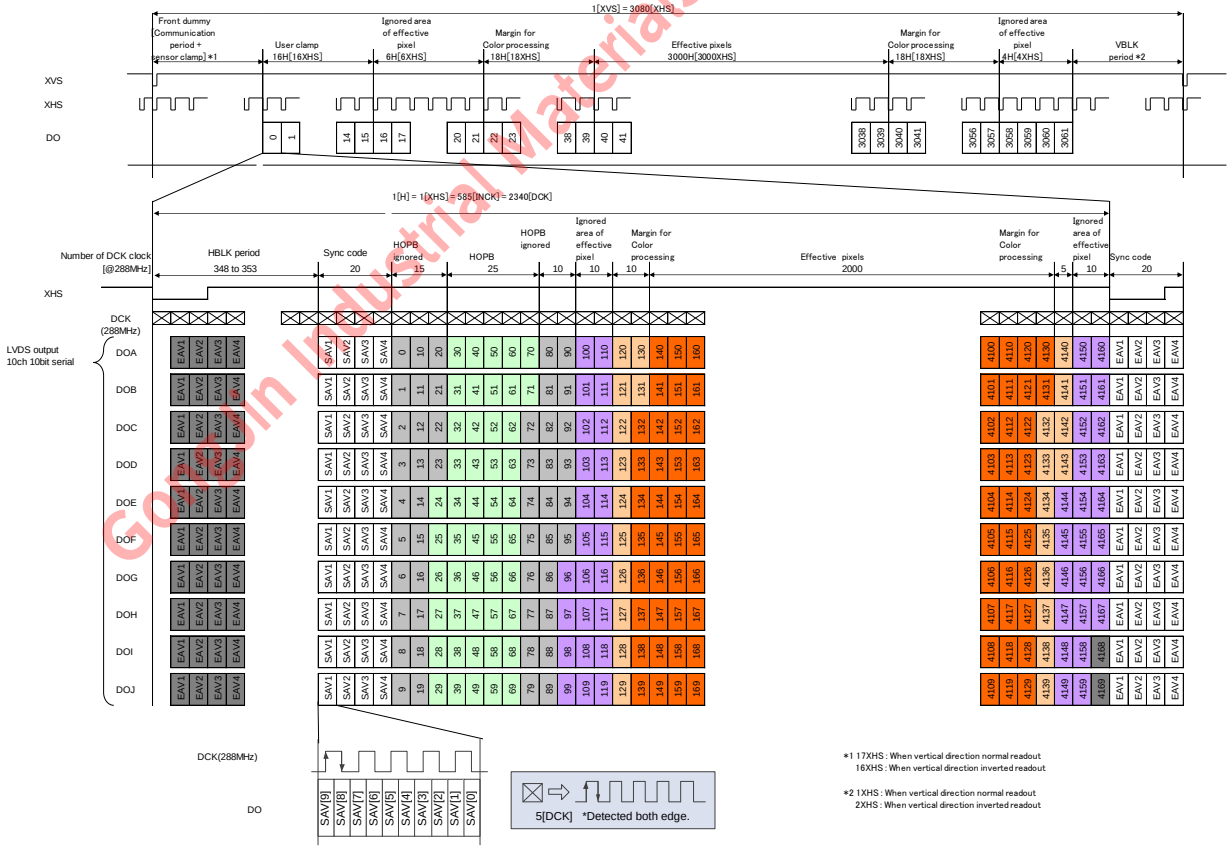
Readout Drive Timing

MODE1 : All-pixel scan mode
(12M, 39.96 frame/s, 10-bit A/D conversion, 10-bit length output, 10 ch output)



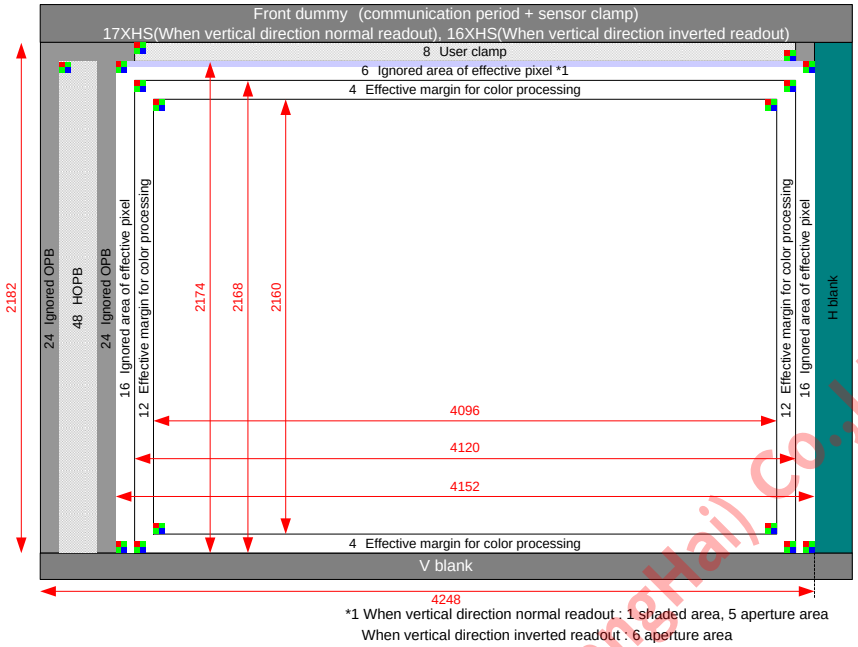
*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

Readout Pixel Image Diagram (4000 × 3000)

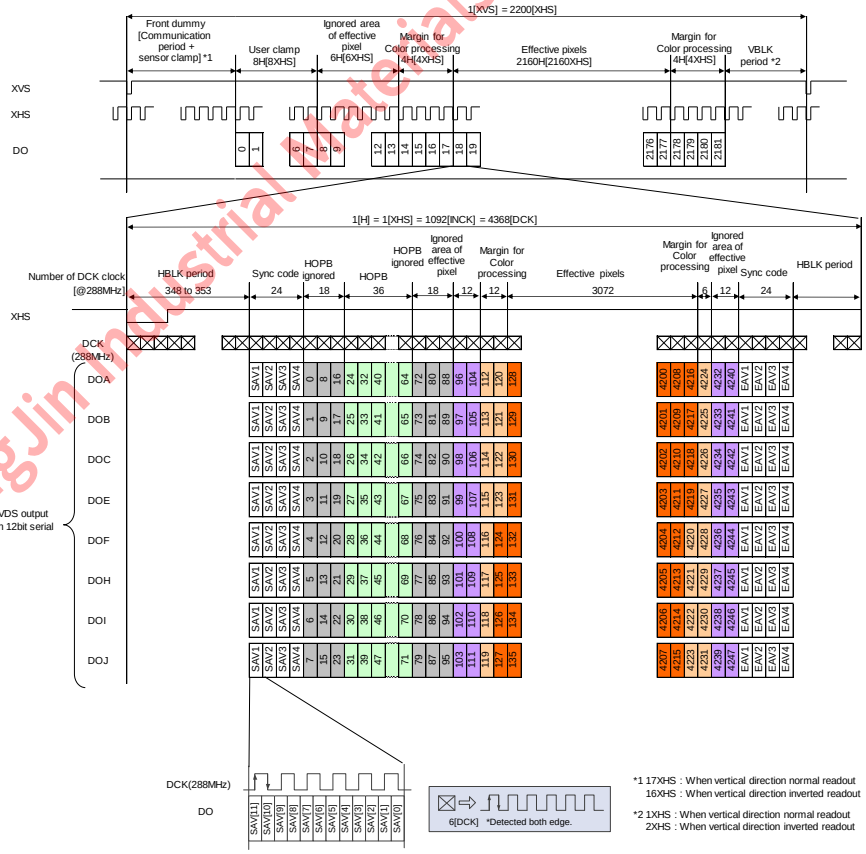


Readout Drive Timing

MODE2 : All-pixel scan mode
(4K2K, 29.97 frame/s, 12-bit A/D conversion, 12-bit length output, 8 ch output)

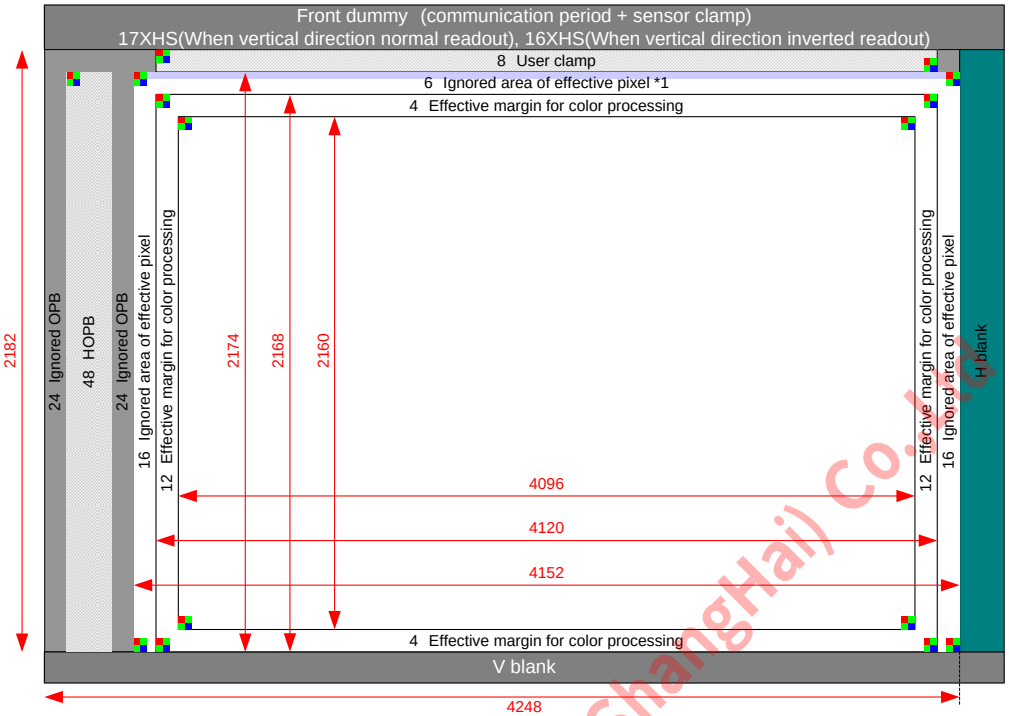


Readout Pixel Image Diagram (4096 × 2160)



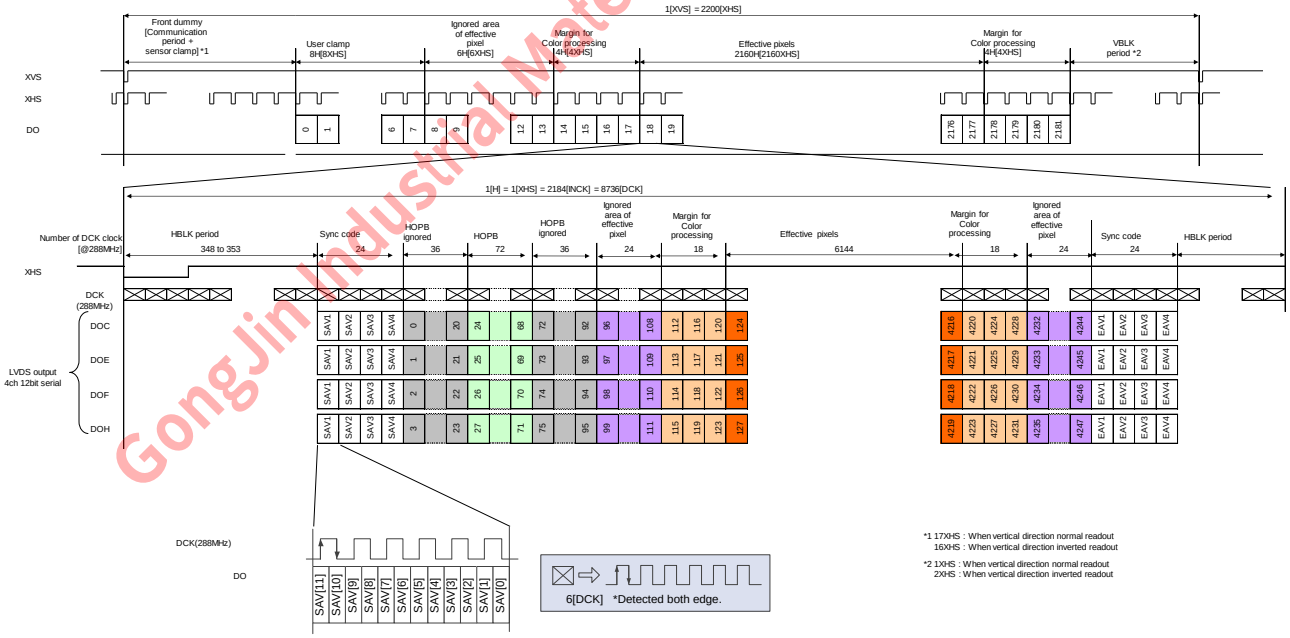
Readout Drive Timing

MODE3: All-pixel scan mode
(4K2K, 14.99 frame/s, 12-bit A/D conversion, 12-bit length output, 4 ch output)



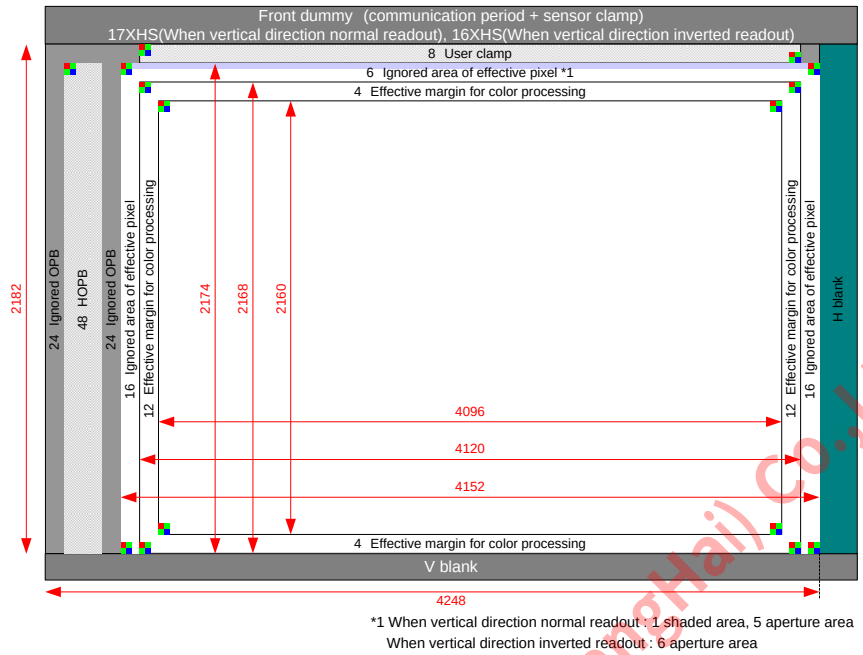
*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

Readout Pixel Image Diagram (4096 × 2160)



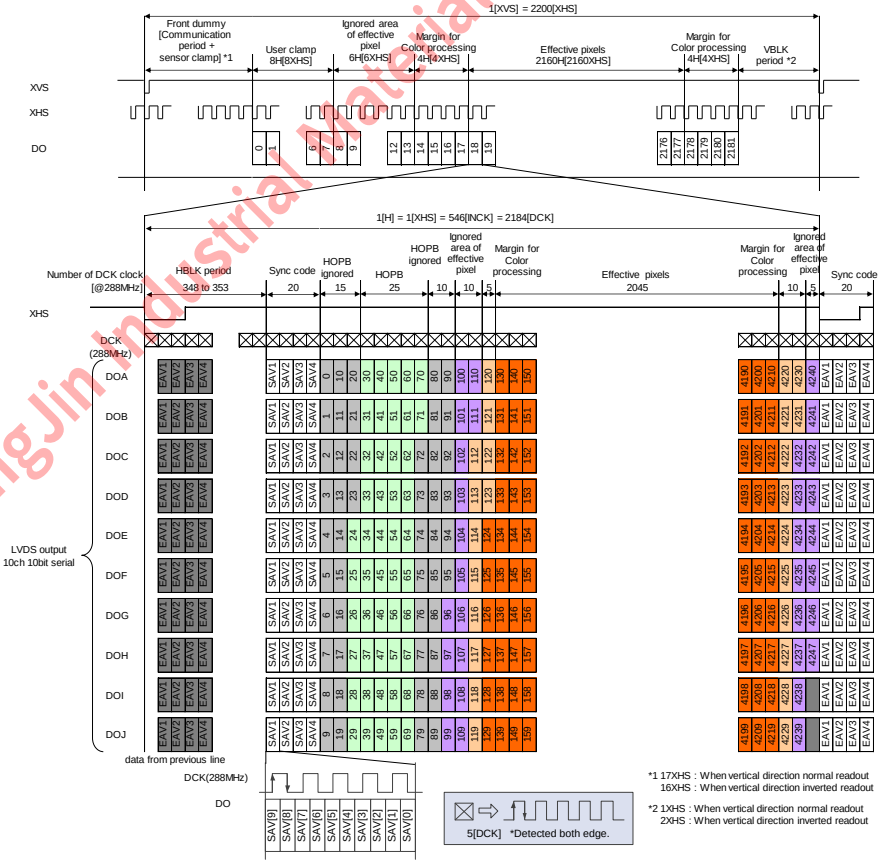
Readout Drive Timing

MODE4: All-pixel scan mode
(4K2K, 59.94 frame/s, 10-bit A/D conversion, 10-bit length output, 10 ch output)



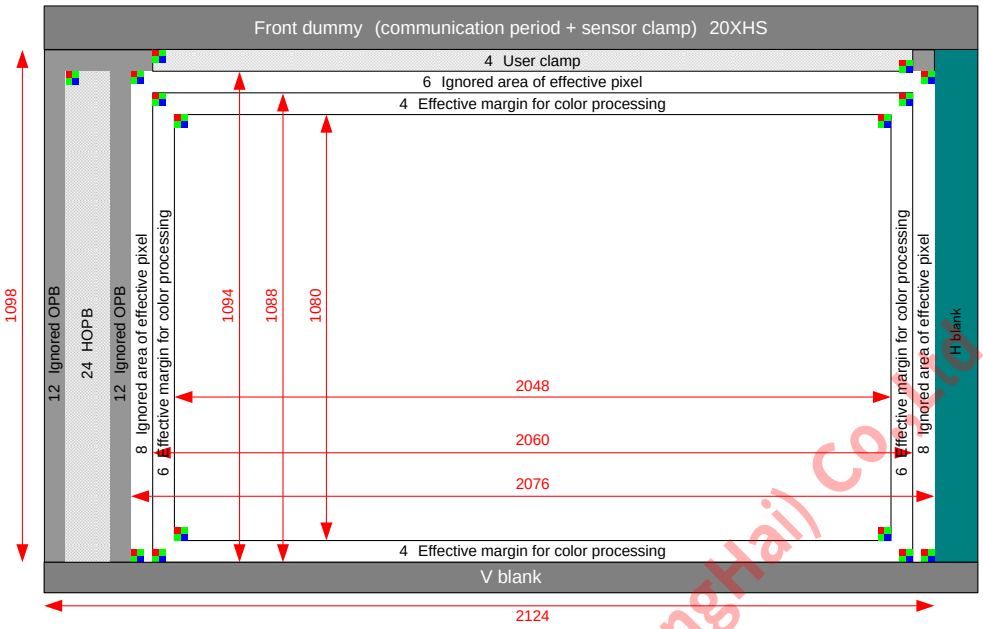
*1 When vertical direction normal readout : 1 shaded area, 5 aperture area
When vertical direction inverted readout : 6 aperture area

Readout Pixel Image Diagram (4096 × 2160)

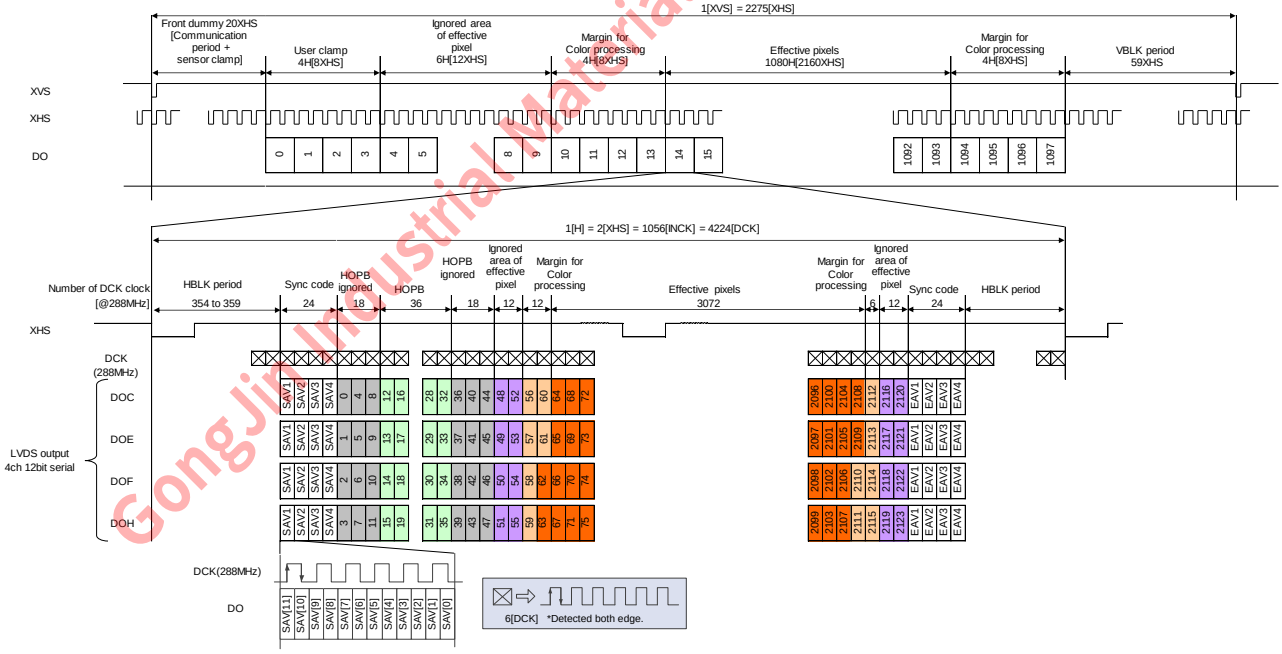


Readout Drive Timing

MODE5 : Horizontal/vertical 2/2-line binning mode
(4K2K, 59.94 frame/s, 10-bit A/D conversion, 12-bit length output, 4 ch output)



Readout Pixel Image Diagram (2048 × 1080)



Readout Drive Timing

Integration Time in Each Readout Drive Mode and Mode Changes

1. Integration Time in Each Readout Drive Mode

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR, SVR and SPL. The formulas and constants used to calculate the integration time are shown below.
In addition, the frame rate can be reduced by setting the SVR register to “1” or more.

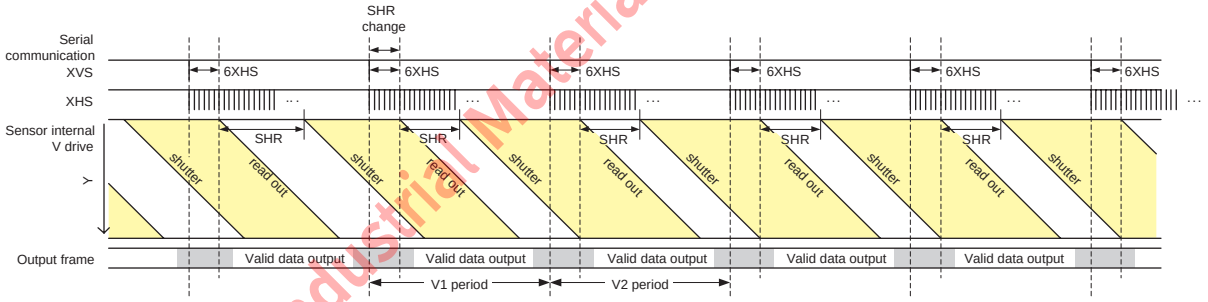
Integration Time [s] = [{Number of XHS per XVS period × (SVR value – SPL value + 1) – (SHR value)} × Number of clock per XHS Period + Number of clocks per internal offset period] /INCK frequency [Hz]

* See the following table for the numbers of clocks per internal offset period.
* See “Electronic Shutter Timing” on page 35 for the SHR register setting range.

Constants Used to Calculate the Integration Time

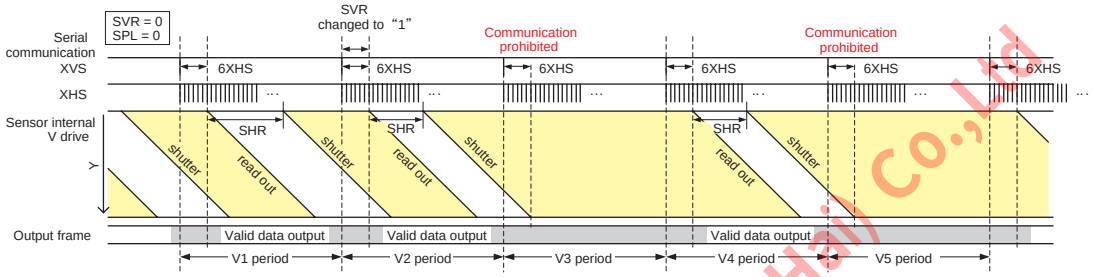
Readout mode No.	0	1	2	3	4	5
Number of clocks per internal offset period	201	149	201	201	149	149

The figure below shows operation when changing SHR. The V1 and V2 periods in the figure below are two continuous XVS periods. The SHR value set within the first 6XHS periods (recommended serial communication period) of V1 is updated internally at the end of the 6XHS periods, and then output data which reflect the new setting is output in the V2 period. Note that the SHR setting and output are offset by 1XVS period.



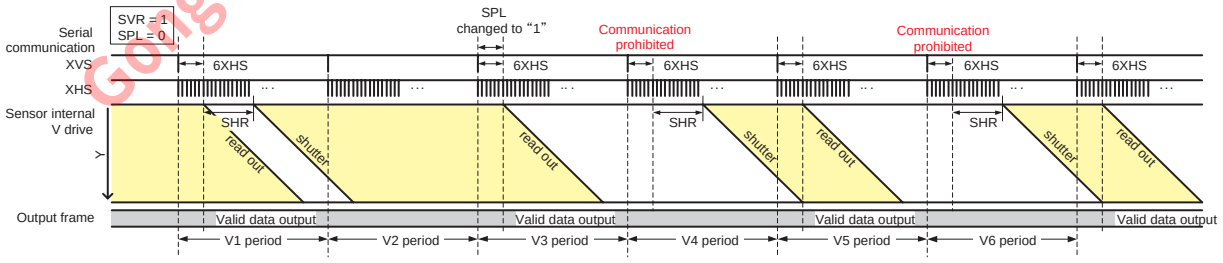
SHR Change Sequence

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. The vertical sync signal cycle is treated as (SVR value + 1) inside the sensor. In addition, the frame rate changes to 1/ (SVR value + 1) according to the SVR value.
The figure below shows the operation when changing the SVR register. The example in the figure below shows the update timing when SPL = 0 and the SVR value is changed from “0” to “1”. The SVR value set within the first 6XHS periods (recommended serial communication period) of V2 is updated internally at the end of the 6XHS periods, and then applied from the shutter operation in the V2 period. Readout operation is not performed in the V3 period, and output data which reflect the changing of SVR is output in the V4 period.
The image data of the V1 period before the SVR value is changed is output as valid data in the V2 period.
In addition, note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V3 period (the frame during which readout operation is not performed).



SVR Change Sequence

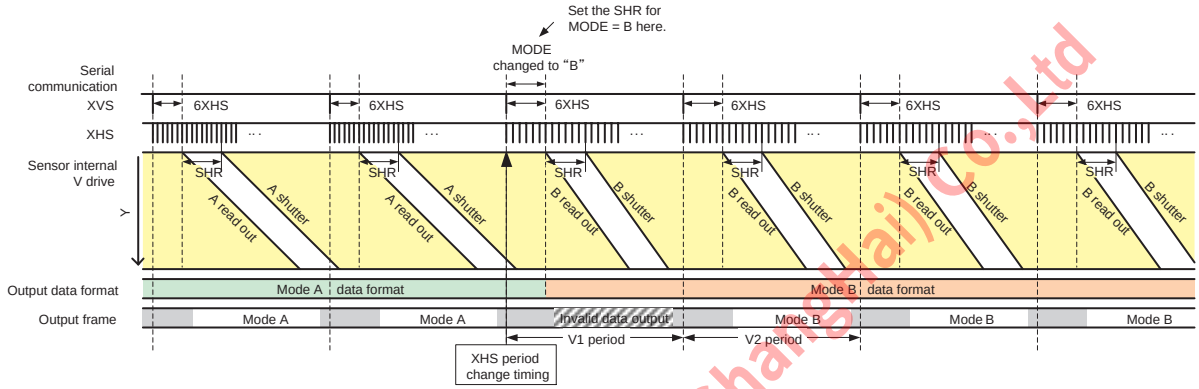
When the internal vertical sync signal is subsampled by the SVR register, the SPL register can be used to set the shutter in the vertical sync signal subsampling periods (the V2, V4 and V6 periods in the figure below).
The figure below shows the operation when changing the SPL register. The example in the figure below shows the update timing when SVR = 1 and SPL is changed from “0” to “1”. SVR = 1 and SPL = 0 in the continuous frames of the V1 and V2 periods, so shutter operation is performed in the V1 period and the corresponding data is output in the V3 period. (See the aforementioned description of operation when SVR ≥ 1.)
The SPL value set within the first 6XHS periods (recommended serial communication period) of V3 is updated internally at the end of the 6XHS periods, and then applied from the shutter operation in the V3 and V4 periods.
Readout operation is not performed in the V4 period, and output data which reflect the SPL change is output in the V5 period. The image data of the V1 and V2 periods before the SPL value is changed is output as valid data in the V3 period.
In addition, note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V4 period (the frame during which readout operation is not performed).
The SPL register cannot be used in readout mode No.6: Vertical 2/9 subsampling binning mode (low power consumption drive), so use the SHR register when setting the shutter in the vertical sync signal subsampling period.



SPL Change Sequence

2. Operation when Changing the Readout Drive Mode

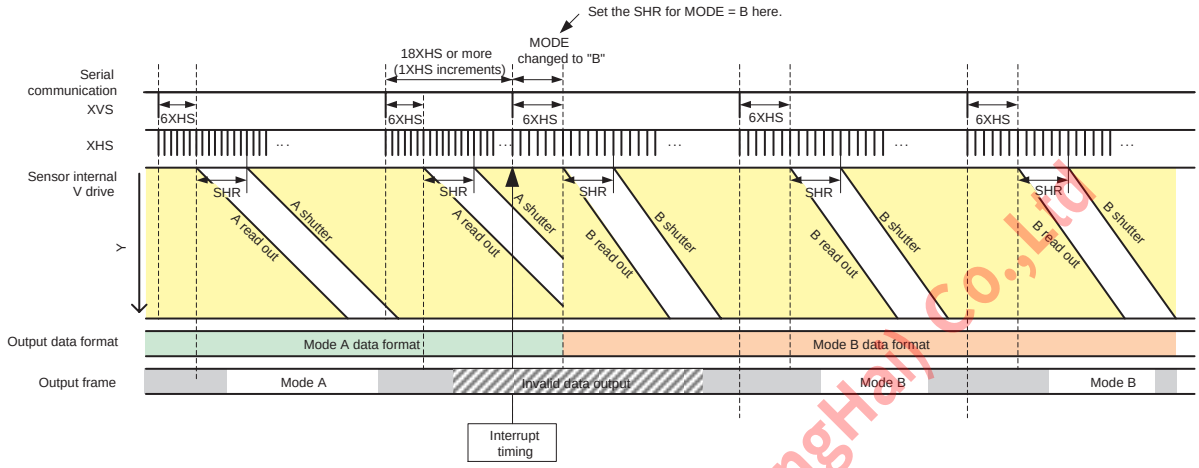
One frame of invalid data is always generated when changing the readout drive mode.
In addition to when changing the readout mode setting, this same sequence also results when the vertical direction readout inversion setting is changed.
The figure below shows the mode transition sequence (Mode A to Mode B). The output data is invalid in the frame (V1 period) in which the setting is changed to Mode B. Valid data which reflect the new setting is output from the next frame (V2 period). If the XHS period for Mode A and Mode B differs, change XHS period at the timing shown in the figure below (V1 head).
In addition, note that when the output data length or the output data rate differ in Mode A and Mode B, the new data format is output from the start of the 7th XHS of the frame (V1 period) in which the setting is changed to Mode B.



Mode Transition

3. Interrupt Mode Change

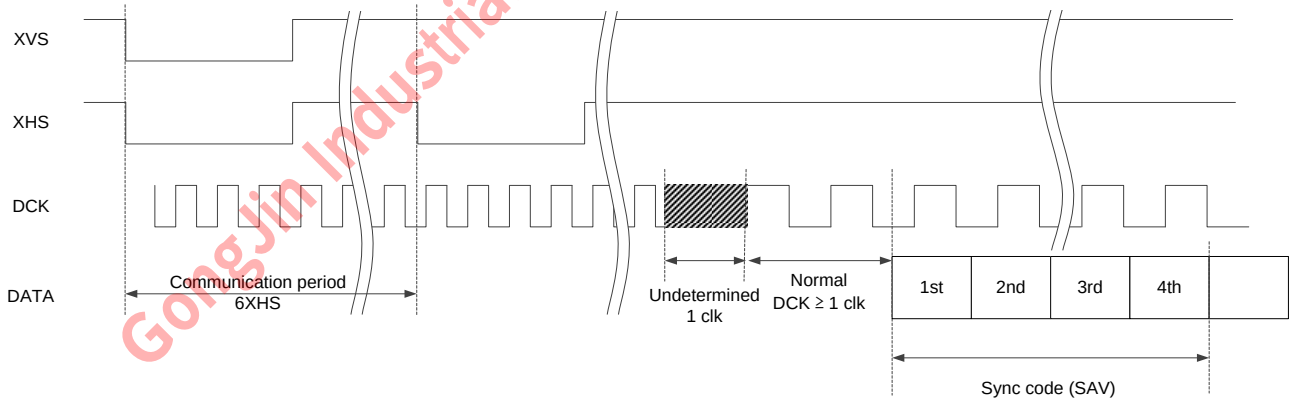
The sensor mode can be changed using interrupts in all modes.
When changing the mode using an interrupt, the mode can be changed by inputting XVS in sync with XHS after 18XHS periods or more[*1] have elapsed from the start of the frame, and transmitting the mode setting register value within the communication period. In addition, the data output before the interrupt mode change is cut off at the timing of the interrupt mode change.



Interrupt Mode Change

4. Data Clock (DCK) Change Timing

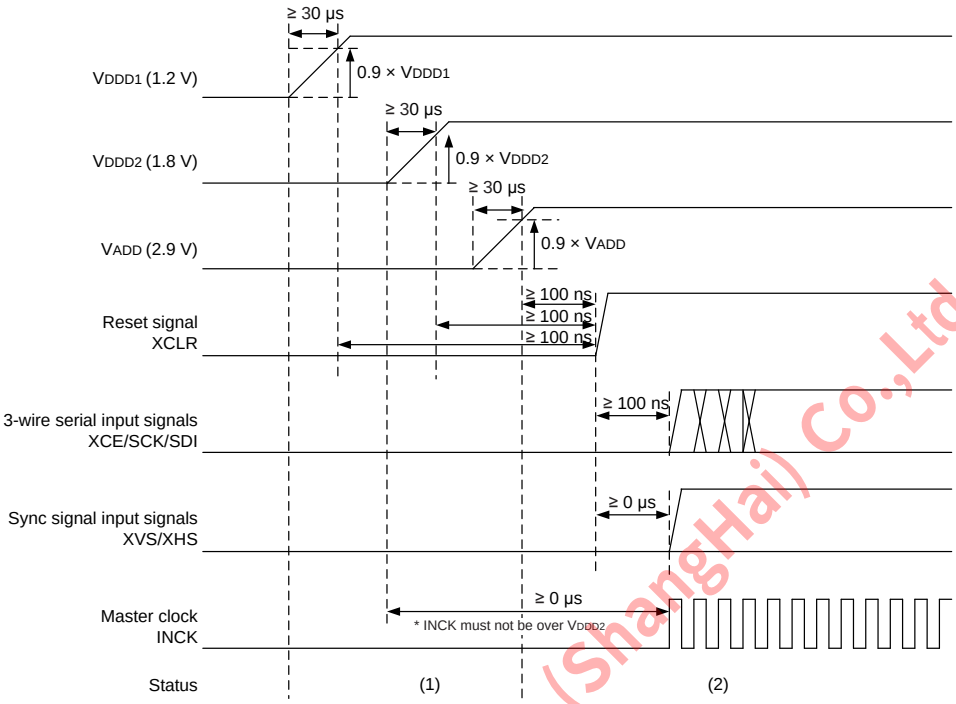
When switching the data clock (DCK) frequency by the output format setting register FREQ, hazard may occur in the 1 clock immediately after it.
Do not use the DCK immediately after the change. Note that normal DCK is output one or before the data start sync code.



DCK Change Period

Power-on/off Sequence

1. Power-on Sequence

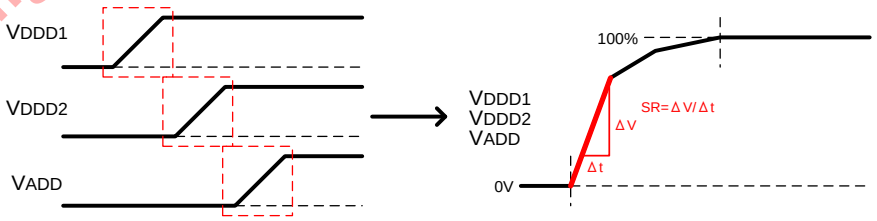


Power-on Sequence

Period name	Remarks
(1) Power stabilization time	All input signals are at Low level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1}, V_{DDD2}.
(2) Standby cancel register communication	Start the standby cancel sequence after the last power supply in V_{ADD}, V_{DDD1}, V_{DDD2}.

2. Slew Rate Limitation of Power-on Sequence

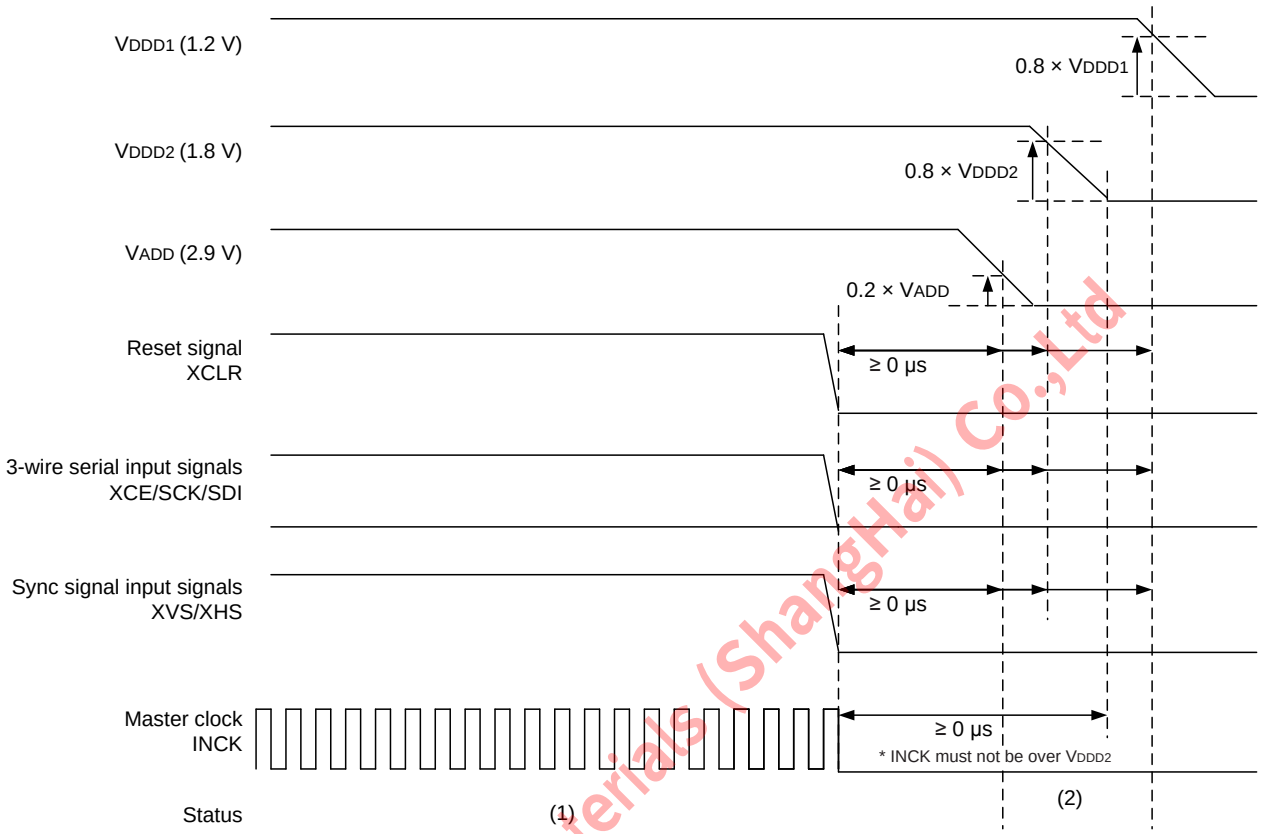
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit
Slew rate	SR	VDDD1 (1.2 V)	—	25	mV/µs
		VDDD2 (1.8 V)	—	25	mV/µs
		VADD (2.9 V)	—	25	mV/µs

3. Power-off Sequence

Make sure that all input signals for the 3-wire serial interface and other signals are at Low level in the area of (2).



Power-off Sequence

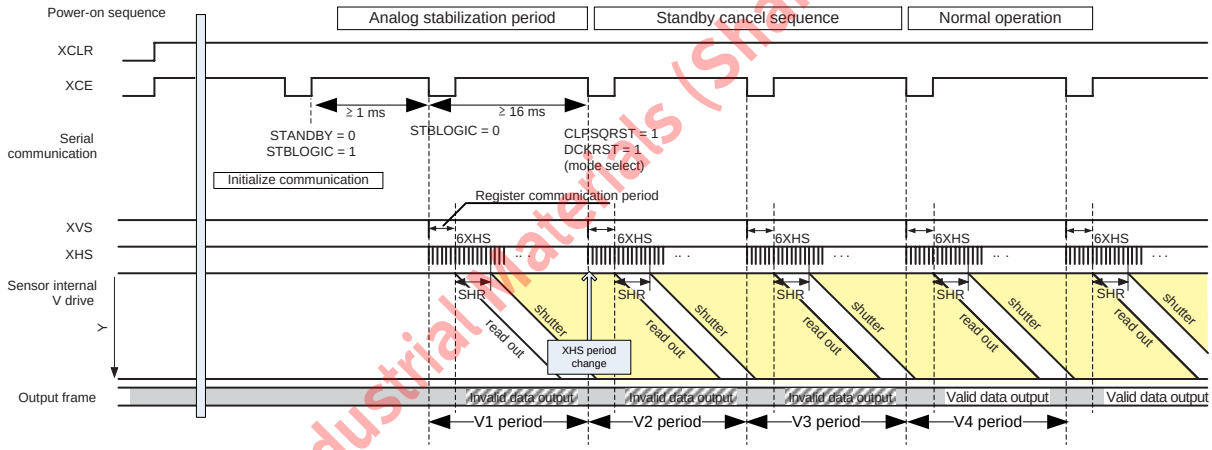
Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off time	Turn the power supplies off after "L" level is set to all input signals. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, V_{DDD2}.

Standby Cancel Sequence

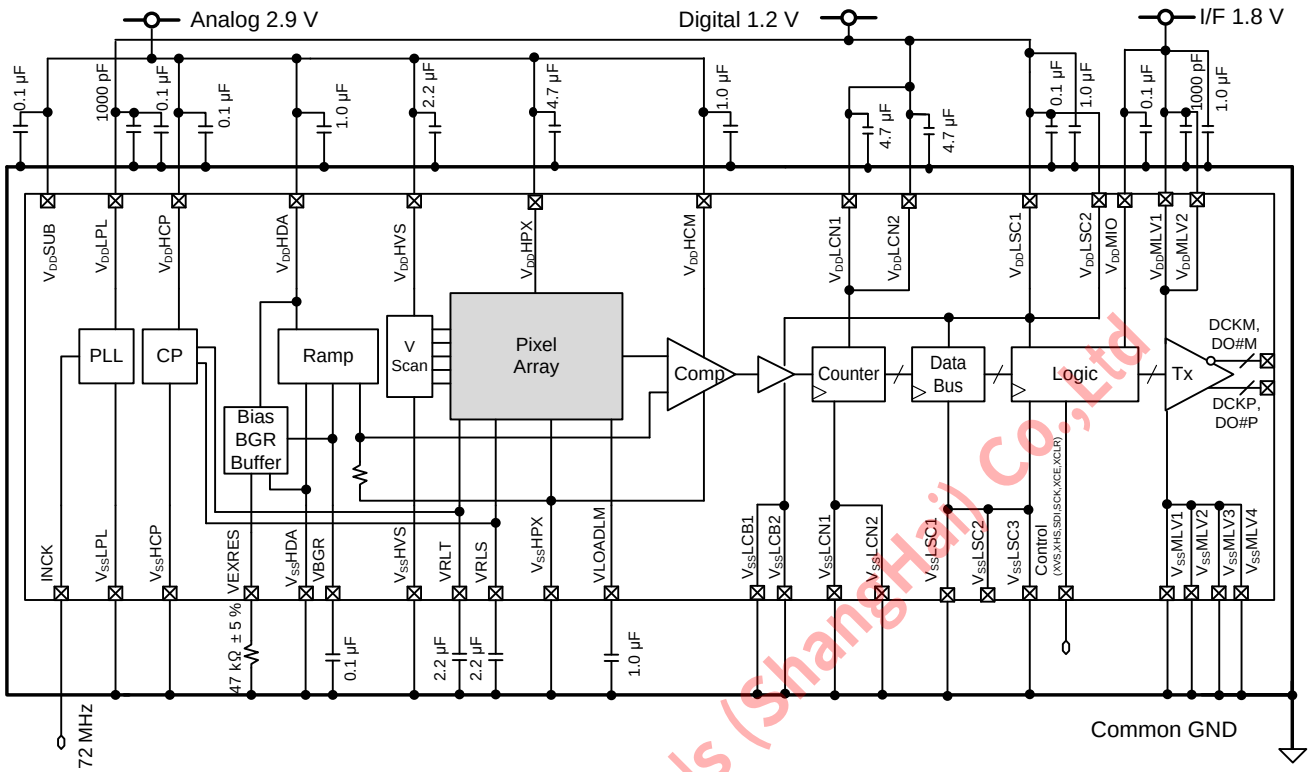
After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancel sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

1. After performing the power-on start-up sequence, set address 0000h, bit [1:0] to "2h" (STANDBY register = 0h, STBLOGIC register = 1h). When initialize communication is performed before the register communication period in the V1 period, there are no restrictions on the communication order. Register communication can be performed even when STANDBY = 1h.
2. After a stabilization period of 1 ms or more, set address 0000h, bit [1:0] to “0h” (STANDBY register = 0h, STBLOGIC register = 0h).
   In addition, when using the V4 period data after canceling standby mode, transmit the mode select register required for normal operation during the communication period of V2 period. Transmit the shutter setting and other settings during the communication period of V1 or V2 period.
3. After an analog stabilization period of 16 ms or more, set "1h" in the LVDS clock output phase locking register DCKRST (address 0001h, bit [0]) and “1h” in the clamp reset register CLPSQRST (address 0001h, bit [4]) during the register communication period of the next frame (the V2 period).

Note) 1. Vertical and horizontal sync signal can be input during initialize communication.
2. The V1 period requires a time of 16 ms or more.



Peripheral Circuit Diagram



Note) Locate a bypass capacitor for each pin. Note that even when pins have the same voltage, connecting the power supply wiring before these capacitors produces common impedance and may result in unexpected trouble.

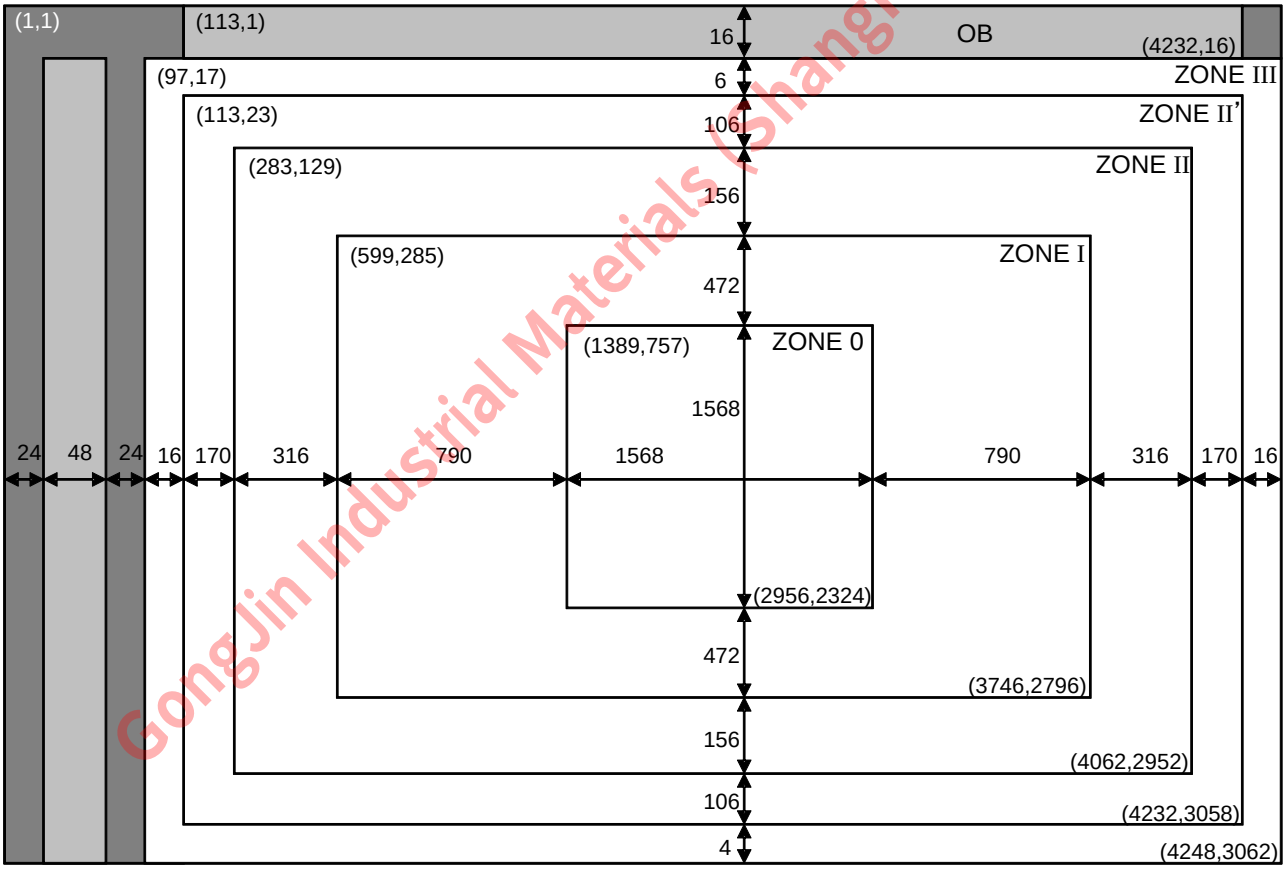
Spot Pixel Specifications

(V_{ADD} = 2.9 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, reference gain 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone						Measure-ment method	Remarks
		0	I	II	II'	OB	III		
Black pixels at high light	30 % ≤ D	60				No evaluation criteria applied		1	
White pixels at high light	30 % ≤ D					No evaluation criteria applied		1	
White pixels in the dark	5.6 mV ≤ D	950					No evaluation criteria applied	2	1/30 s integration
Black pixels at signal saturated	D ≤ 648 mV	0				No evaluation criteria applied		3	

Note) 1. D...Spot pixel level. Black pixels at signal saturated are prescribed at the signal output in spot pixel part.
2. Zone definition is illustrated in the figure below.

Spot Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	5.5 pcs
10.0 mV or higher	3.6 pcs
24.0 mV or higher	1.9 pcs
50.0 mV or higher	1.1 pcs
72.0 mV or higher	0.8 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

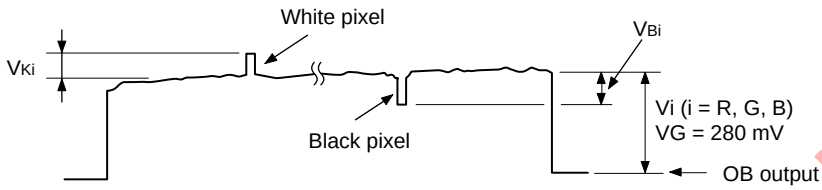
For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value of the G channel signal output is 280 [mV], measure the local dip point (black pixel at high light, V_{BR}, V_{BG} and V_{BB}) and peak point (white pixel at high light, V_{KR}, V_{KG} and V_{KB}) in each channel signal output. Substitute the values into the following formula.

   Spot pixel level = (V_{Ki} (or) V_{Bi}) / Vi × 100 [%] (i = R, G, B)



Signal output waveform of R/G/B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

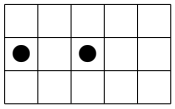
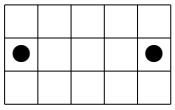
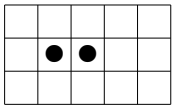
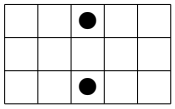
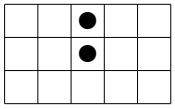
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point in each of the R, G and B channels using the OB output with sensor as a reference.

Signal output waveform of R/G/B channel

Spot Pixel Pattern Specifications

The white pixel and the black pixel are counted as follows

List of Spot Pixel Pattern

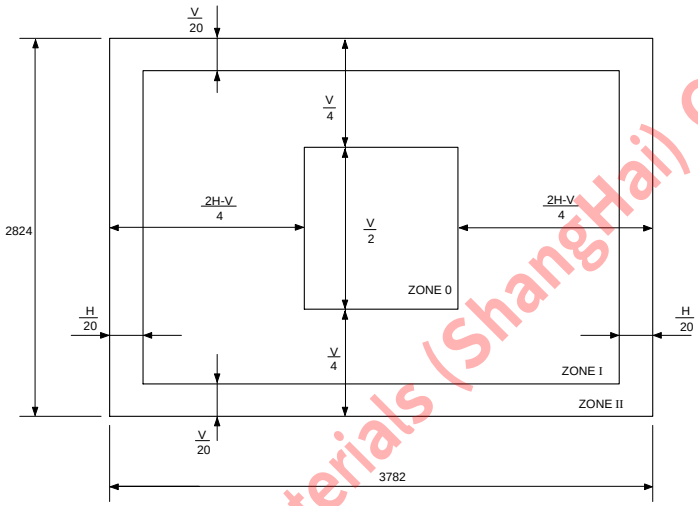
No.	Pattern (G B / R G) It provides by color filter array described in the left.	White pixel	Black pixel	Bright pixel
1	 Same color	Rejected	Rejected	Rejected
2	 Same color	Allowed	Allowed	Allowed
3	 Different color	Allowed	Allowed	Allowed
4	 Same color	Rejected	Allowed	Allowed
5	 Different color	Allowed	Allowed	Allowed

Note) 1. ●:It shows the position of black pixels and white pixels. Black pixels and white pixels are separately counted.
(Example: Even if black pixel is adjacent to white pixel like No. 1, it is not counted as a pattern. They are not rejected.)
2. “Rejected” means that it is rejected as a sensor with 1 piece of spot pixel to select.
3. “Allowed” means that it is not selected to be rejected. It is included in the number of allowable spot pixels by zone and is counted.
4. All spot pixels of the pattern other than the described above is included in the number allowable spot pixels by zone.

Stain Specifications

Zone	Allowable pixels	Total allowable pixels	Size	Level	Remarks
0	1	3	3 ≤ L ≤ 10 lines	4 ≤ R ≤ 8 %	≥ 200 lines
I	2				
II	3		4 ≤ L ≤ 20 lines	4 ≤ R ≤ 8 %	Overlap permitted
For a stain extending over two or more zones, the largest zone is applied to count.					

Stain Zone Definition

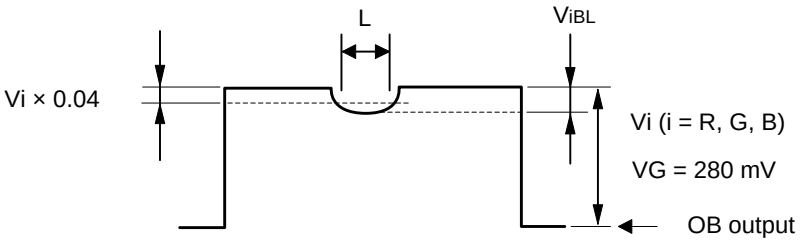


Stain Measurement Method

In the following measurements, set the measurement condition to the standard imaging condition II, set the lens diaphragm to F16, and adjust the luminous intensity so that the average value of the G channel signal output is 280 [mV]. Measure the local dip in the average value of the R, G and B channel signal output (V_{iBL}), and then calculate the stain level (R) as the ratio of V_{iBL} to the average value of the R, G and B channel signal output (Vi).

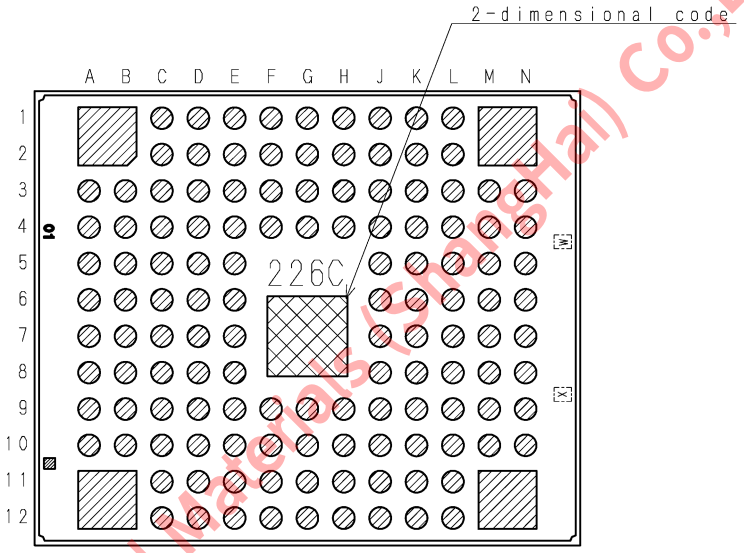
$$R = V_{iBL} / Vi \times 100 [\%] \ (i = R, G, B)$$

At the same time, the size (L) of the area where the stain level is 4 % or more is determined by line number conversion.
The distance from one center of a stain to another is the stain interval, and is also determined in the same way by line number conversion.



Signal output waveform of R/G/B channel

Marking



Note:Following characters enter into "W", and "X". (No Au coat)
W:In English upper case character, One character
X:Number, single number

DRAWING No. AM-B226CQJC(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

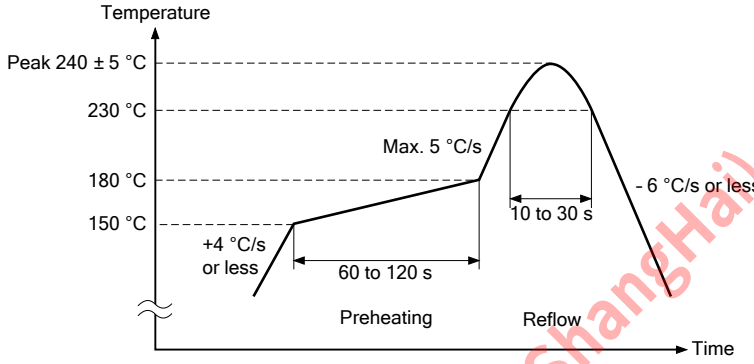
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

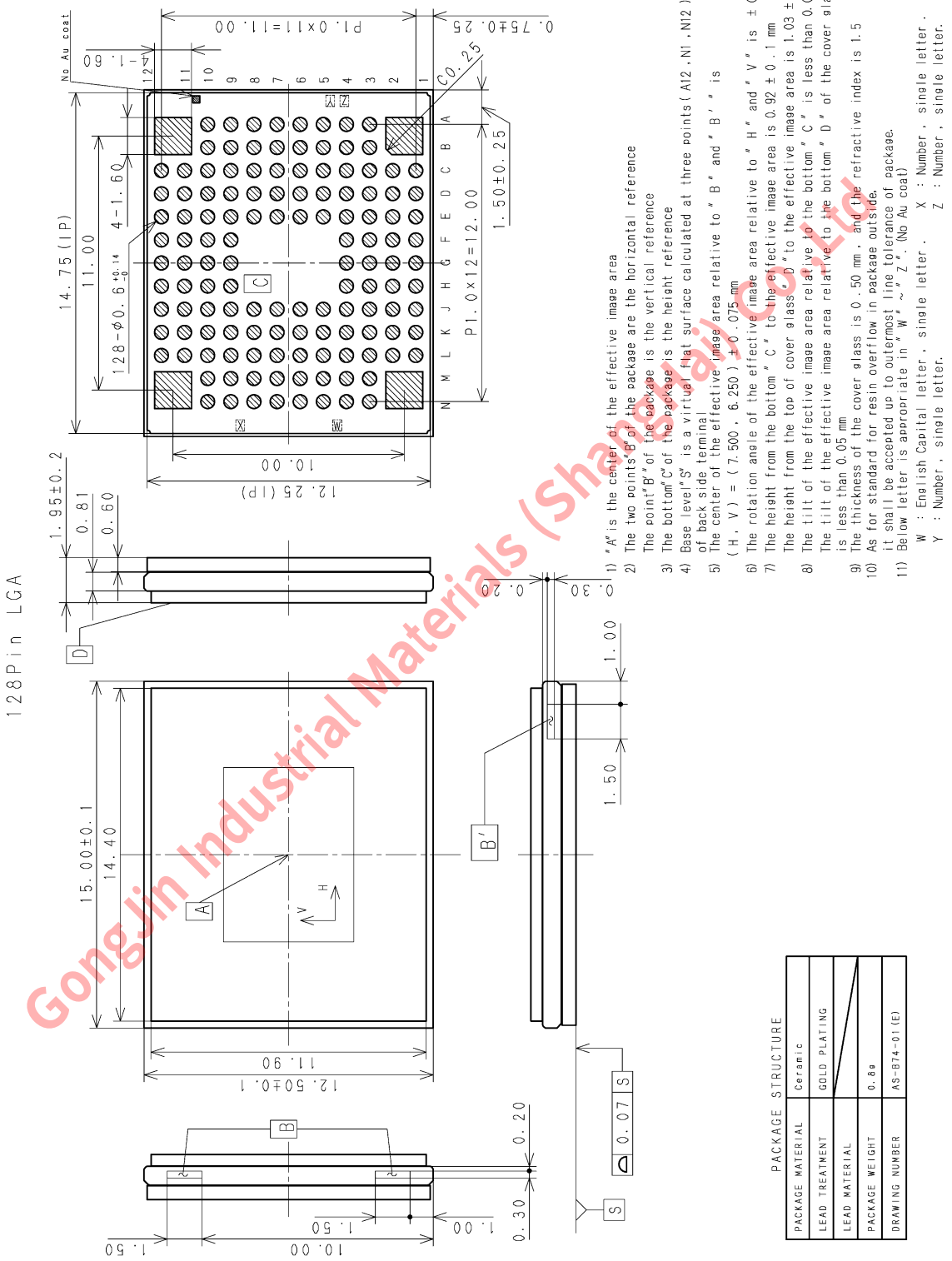
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

(Unit : mm)



SONY

Revision History

Version	Date	Page	Contain of Change
Rev.0.2.0	2013/09/27	ALL	First edition
Rev.0.3.2	2013/12/10	1	Update “Description”
Rev.0.3.2	2013/12/10	33	Update “Break Mode”
Rev.0.3.2	2013/12/10	38	Update “BLKLEVEL Setting”
Rev.0.3.2	2013/12/10	26,30,31, 35,37,38, 41,42,44, 55	Update of the reference page
Rev.0.4.0	2013/12/18	40,41	Update “Register Setting for Each Readout Drive Mode”
Rev.0.4.0	2013/12/18	63	Update “Spot Pixel Specifications”
Rev.0.5.0	2014/02/03	7	Update of the title “Package Center and Optical Center”
Rev.0.5.0	2014/02/03	23	Update “Image Sensor Characteristics”
Rev.0.5.0	2014/02/03	24, 25	Update “Definition of Standard Imaging Conditions”
Rev.0.5.0	2014/02/03	47	Update “Minimum Horizontal Operation Period in Each Readout Drive Mode”
Rev.0.5.0	2014/02/03	63	Update “Spot Pixel Specifications”
Rev.0.5.0	2014/02/03	64	Update “The Annual Number of White Pixels Occurrence”
Rev.0.5.0	2014/02/03	65	Update “Measurement Method for Spot Pixels”
Rev.0.5.0	2014/02/03	66	Update “Spot Pixel Pattern Specifications”
Rev.0.5.0	2014/02/03	67	Update “Stain Specifications”
Rev.0.5.0	2014/02/03	68	Update “Marking”
Rev.0.6.0	2014/03/18	66	Update “Spot Pixel Pattern Specifications”
E14615	2014/06/23	3	The formal version release. Update “Storage guarantee temperature(min)” -30℃→-40℃