微纳光电子材料与器件工艺原理

Film Deposition
Part II: Si Oxidation

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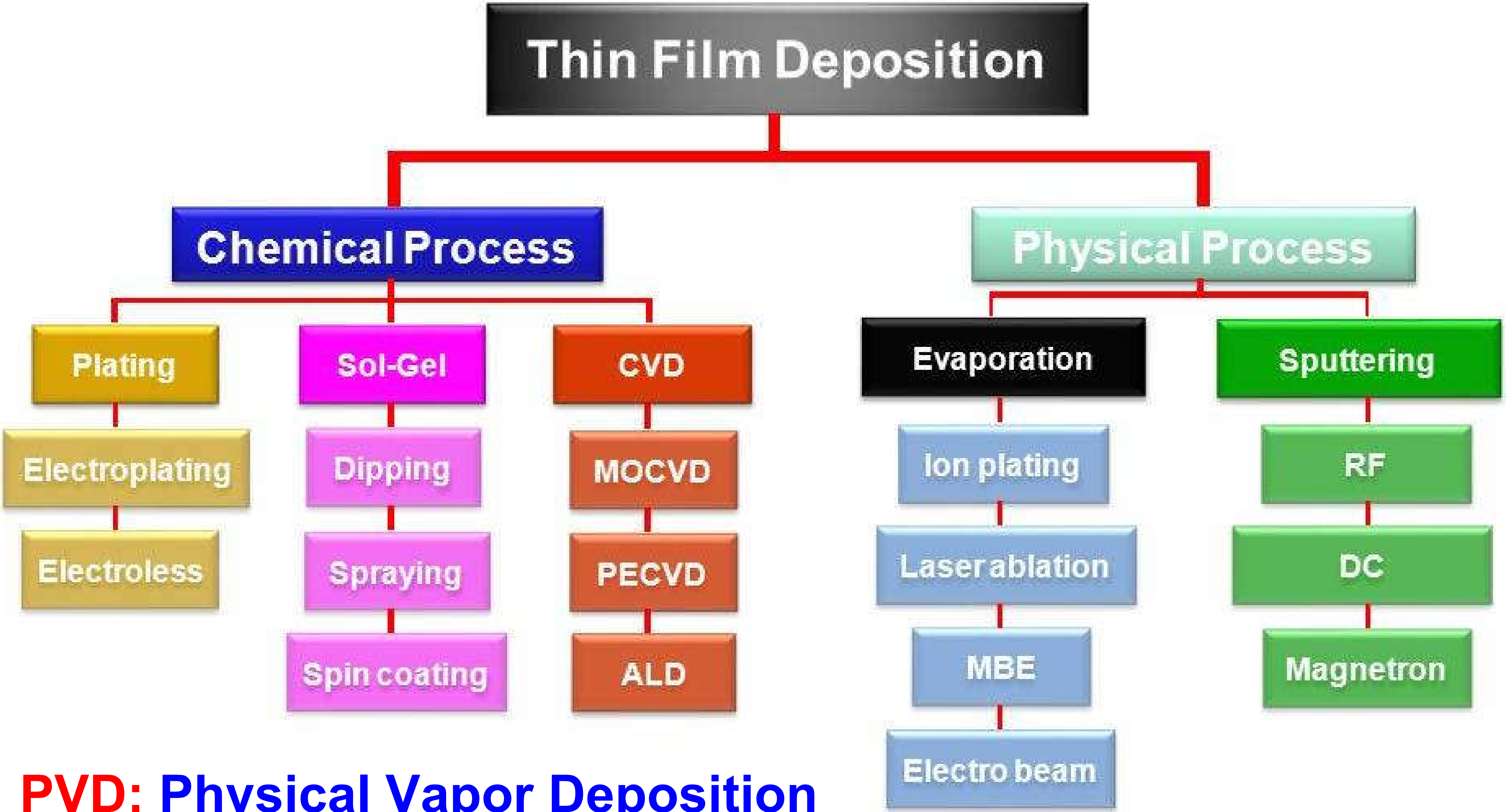
Film Deposition

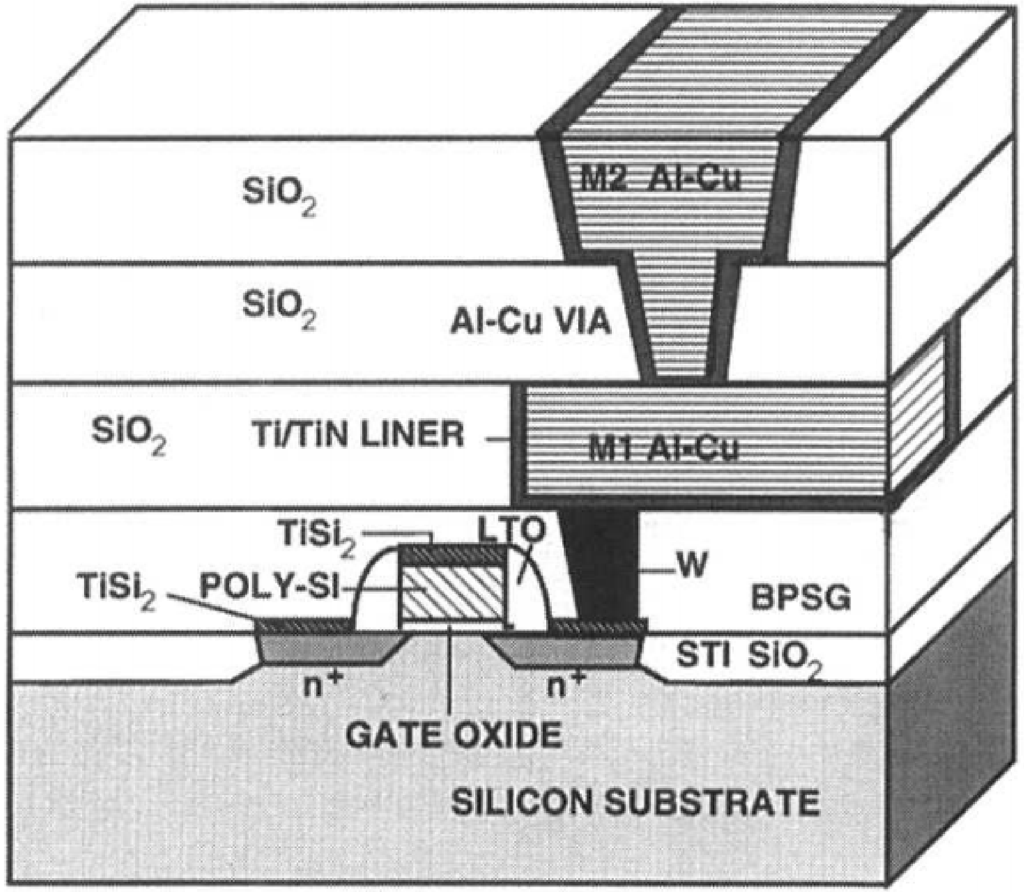


PVD: Physical Vapor Deposition

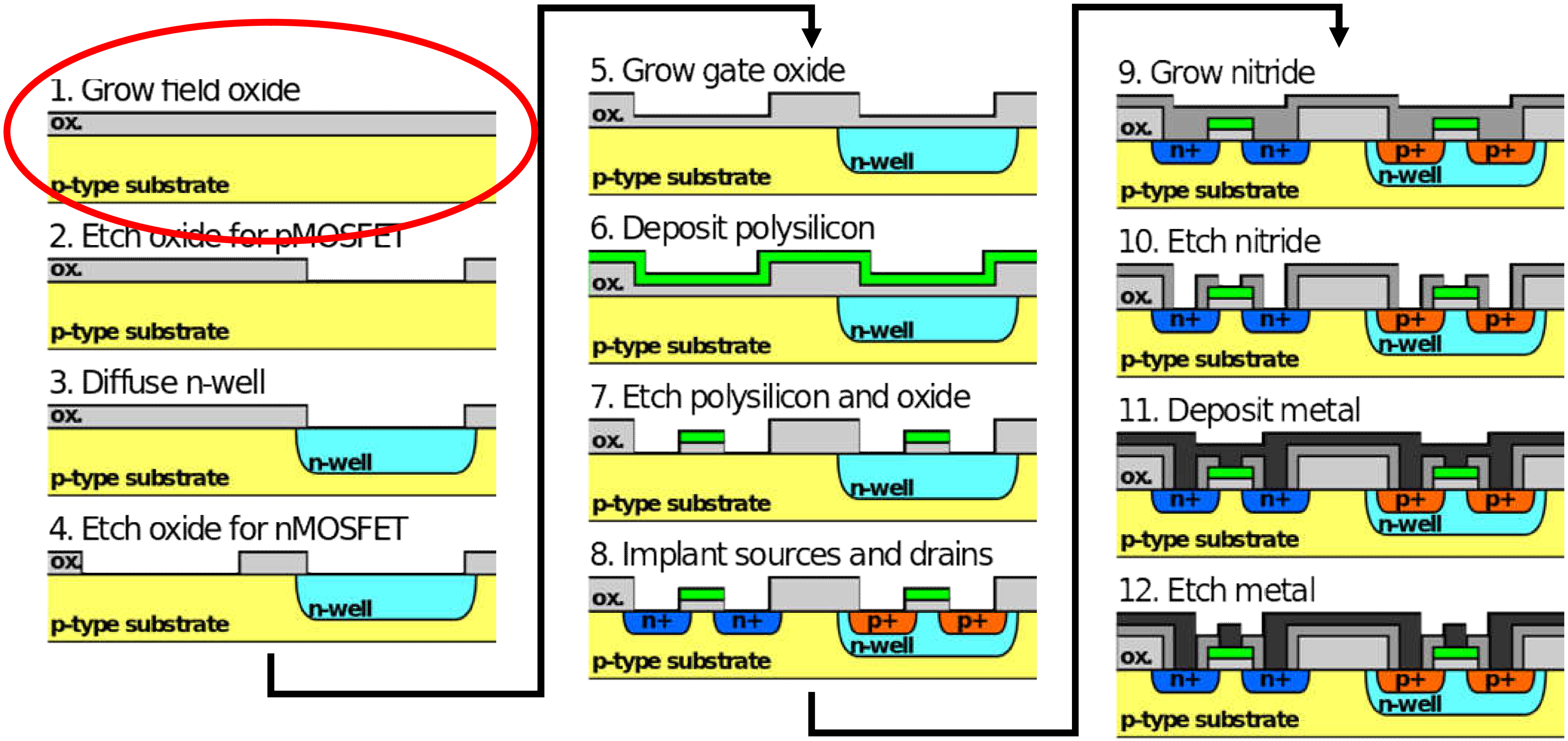
CVD: Chemical Vapor Deposition

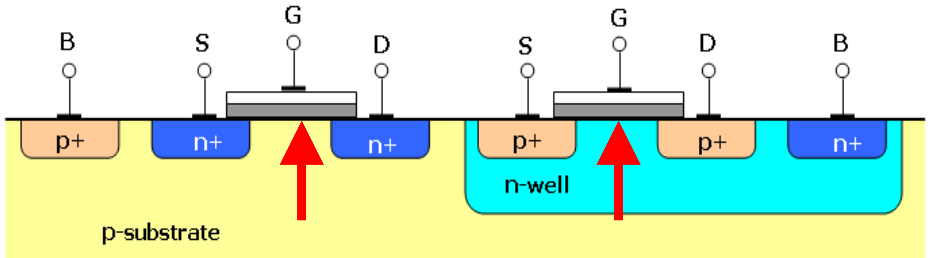
Thin Film in CMOS

- **CVD**
  - Si
  - poly-Si
  - W, SiO_2, ...
- **PVD**
  - Al, Ti
  - ...
- **Electrodeposition**
  - Cu



CMOS Transistors





Properties of SiO_2

- Very stable
  - for Ge, GeO_2 is soluble in water, and decompose at 450 ^oC
  - for GaAs, GaO_x and AsO_x have many defects
- Easily etched
  - wet etch (HF solution) or dry etch (F based plasma)
- Good diffusion barrier (low dopant diffusivity $D_{ox} << D_{Si}$)
- High quality insulator
  - band gap ~ 8 eV, resistivity > 10^{16} Ω*cm
- High dielectric strength (> 500 V/μm)
- Low interface state / defect density (< 10^{10} cm^{-2})

Properties of SiO_2

TABLE 9.3 Properties of Thermal Silicon Dioxide

DC resistivity ($\Omega \cdot$ cm), 25°C	10^{14}–10^{16}	Melting point (°C)	~1700
Density (g/cm^3)	2.27	Molecular weight	60.08
Dielectric constant	3.8–3.9	Molecules/cm^3	2.3×10^{22}
Dielectric strength (V/cm)	$5\text{–}10 \times 10^6$	Refractive index	1.46
Energy gap (eV)	~8	Specific heat (J/g · °C)	1.0
Etch rate in buffered HF (nm/min)[a]	100	Stress in film on Si (N/m^2)	$2\text{–}4 \times 10^8$ Compression
Infrared absorption peak (μm)	9.3		
Linear expansion coefficient (°C^{-1})	5.0×10^{-7}	Thermal conductivity (W/cm · °C)	0.014

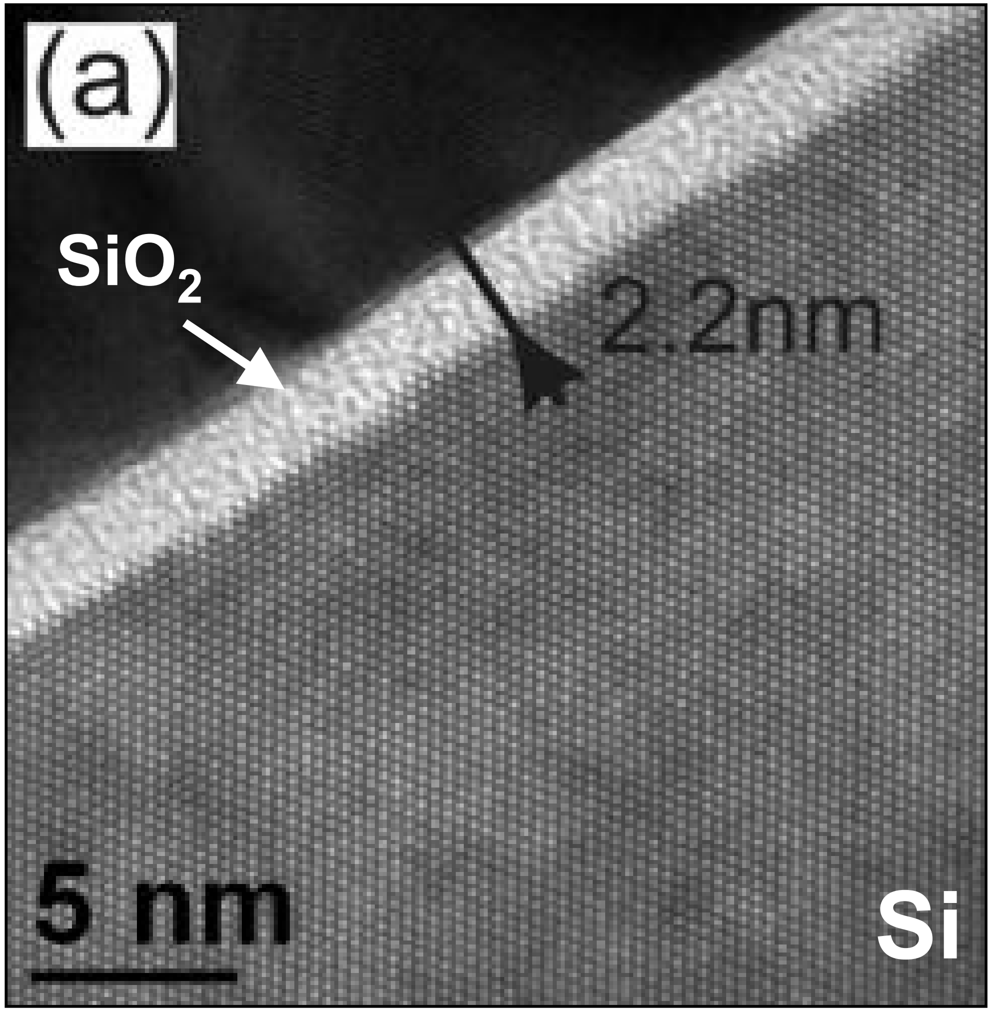
Source: After Wolf and Tauber (1986).

[a]Buffered HF:28 ml HF, 170 ml H_2O, 113 g NH_4F.

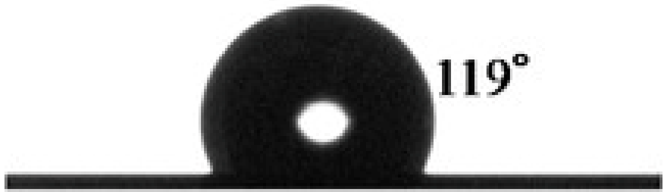
Table 7.2 Diffusivities of Elements in SiO_2[a]

Element	D at 1100°C (cm^2/s)	D at 1200°C (cm^2s)
B	3×10^{-17} to 2×10^{-14}	2×10^{-16} to 5×10^{-14}
Ga	5.3×10^{-11}	5×10^{-8}
P	2.9×10^{-16} to 2×10^{-13}	2×10^{-15} to 7.6×10^{-13}
Sb	9.9×10^{-17}	1.5×10^{-14}
Ar	1.2×10^{-16} to 3.5×10^{-15}	2×10^{-15} to 2.4×10^{-14}

Native Oxide



clean Si (oxide removed by HF)
hydrophobic



Si with native oxide
hydrophilic

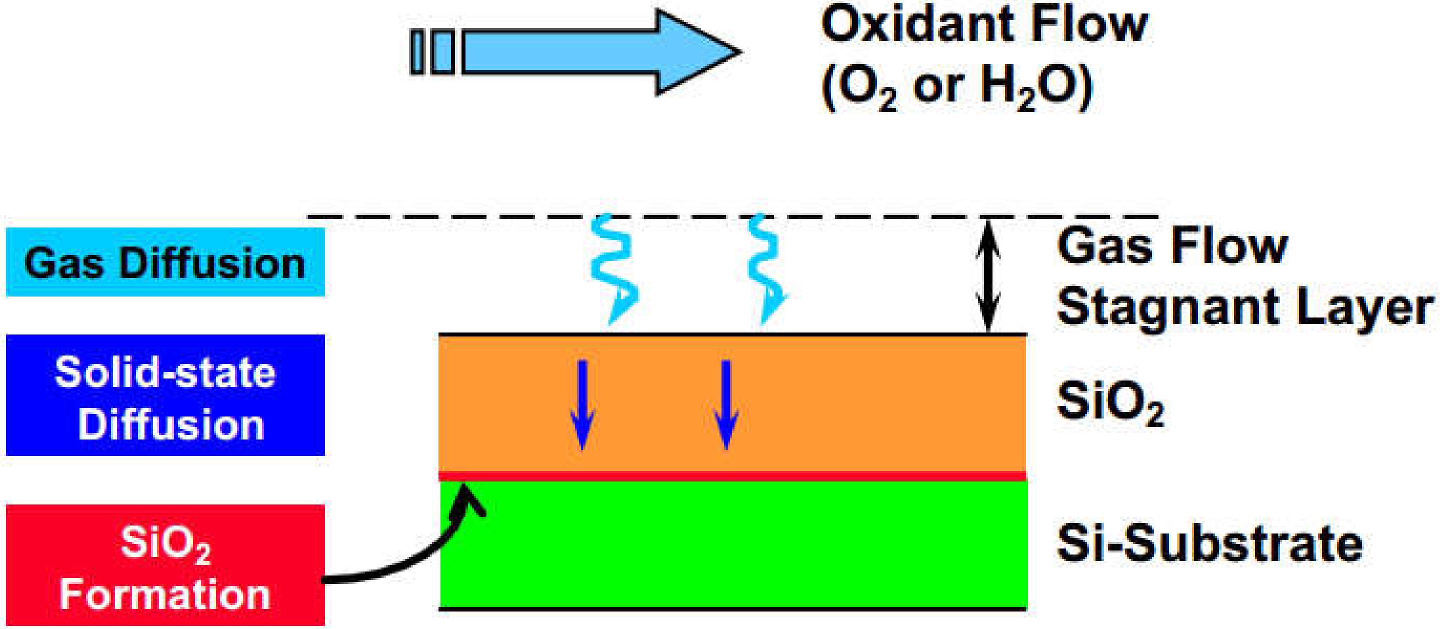
Si forms native oxide in the air (1~2 nm, a few hours)

Q: amorphous or crystalline SiO_2 ?

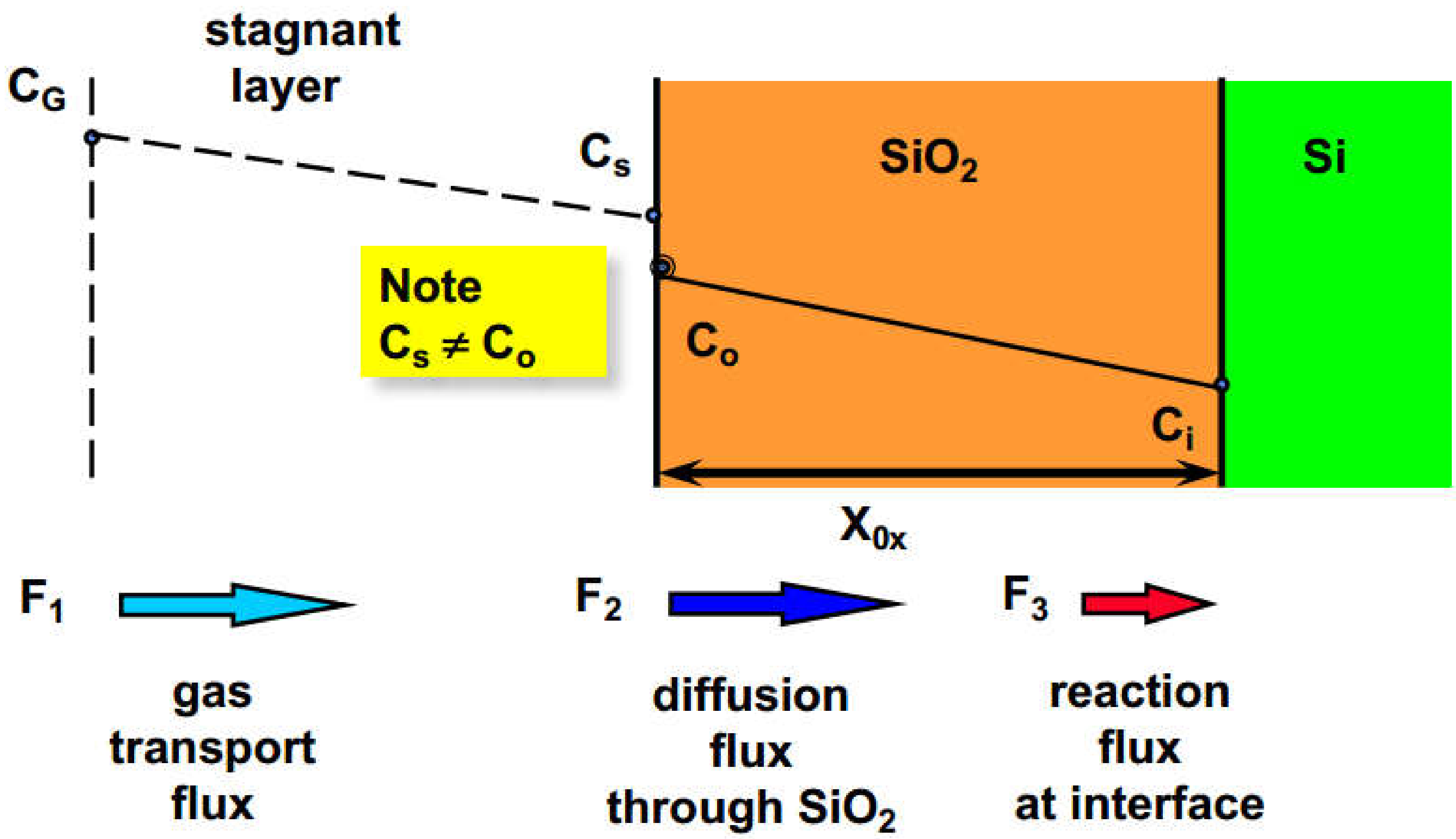
Thermal Oxide Growth

dry oxidation	Si (s) + O_2 (g) = SiO_2 (s)
wet oxidation	Si (s) + H_2O (g) = SiO_2 (s) + H_2 (g)

Video



The Deal-Grove (D-G) Model

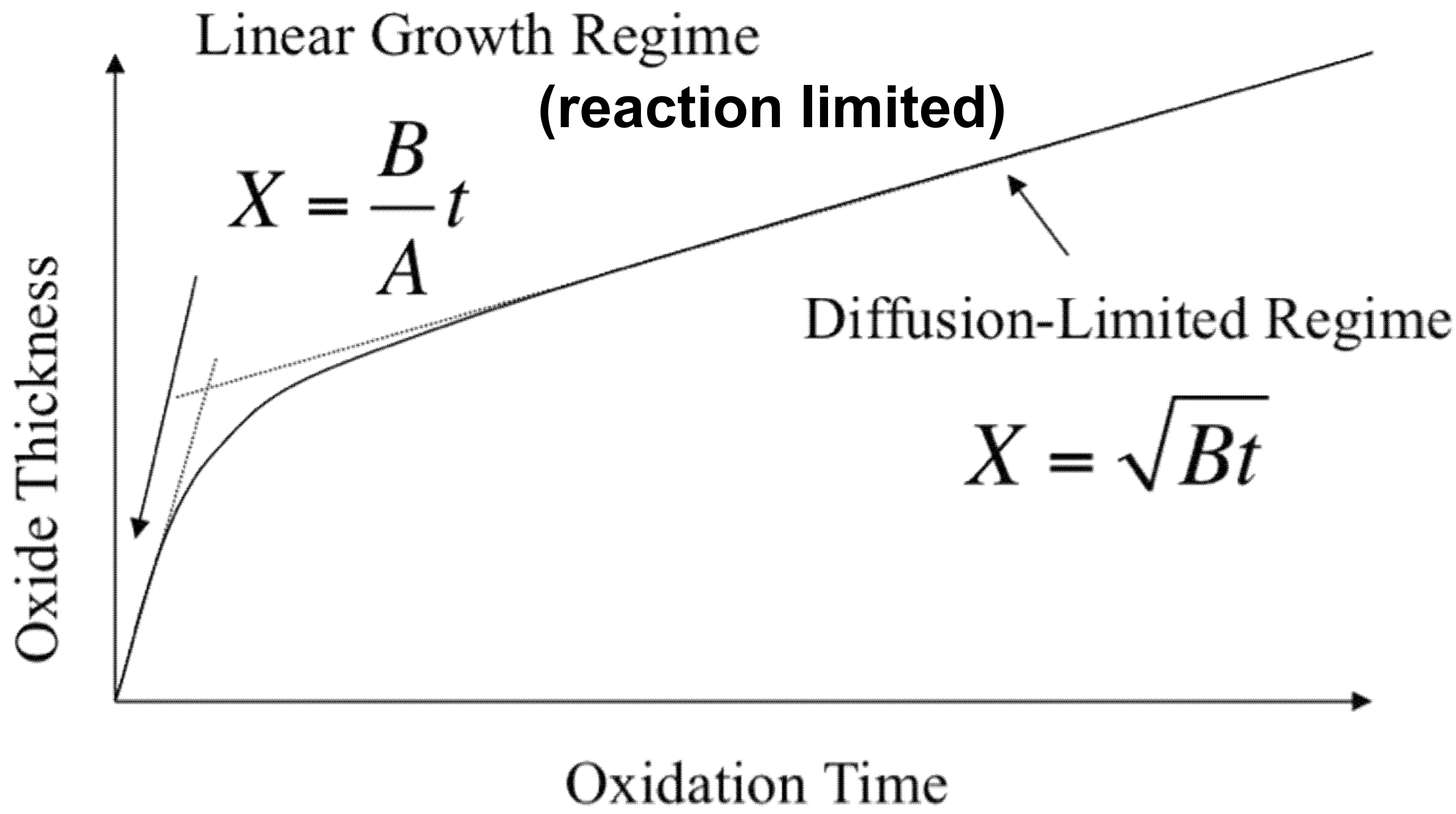


- F: oxygen flux –
  the number of oxygen molecules that crosses a plane per unit area per second

The Deal-Grove (D-G) Model

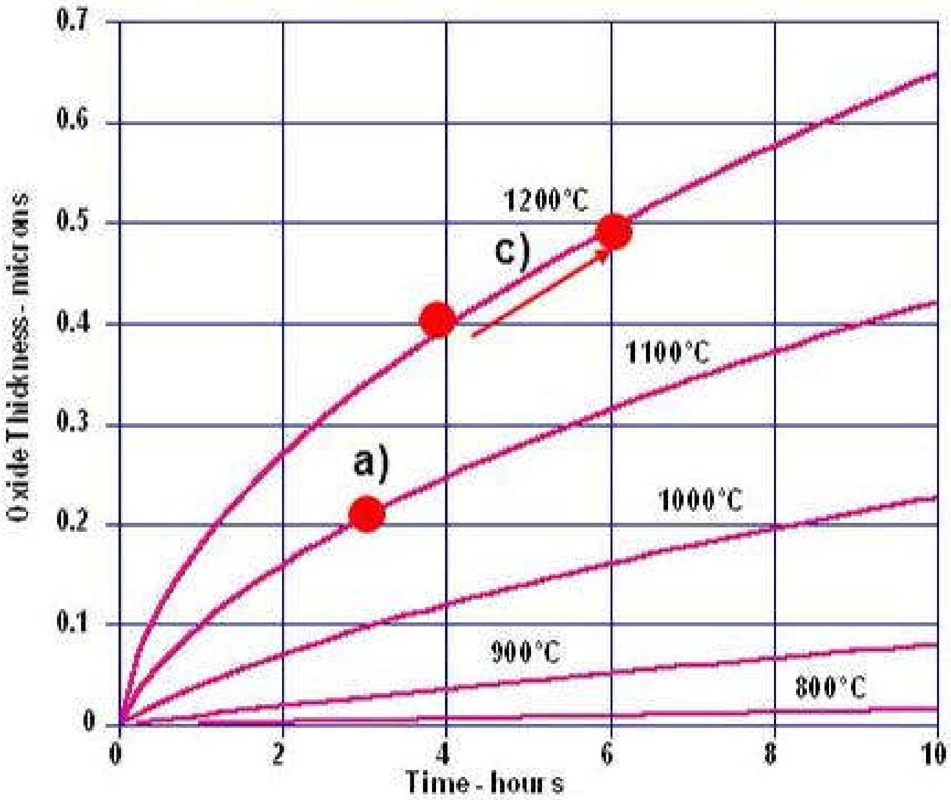
$$X_{ox} = \frac{A}{2}\left\{\sqrt{1+\left(\frac{t+\tau}{A^2/4B}\right)}-1\right\}$$

A	**related to reaction**
B	**related to diffusion**
τ	**initial native oxide thickness**



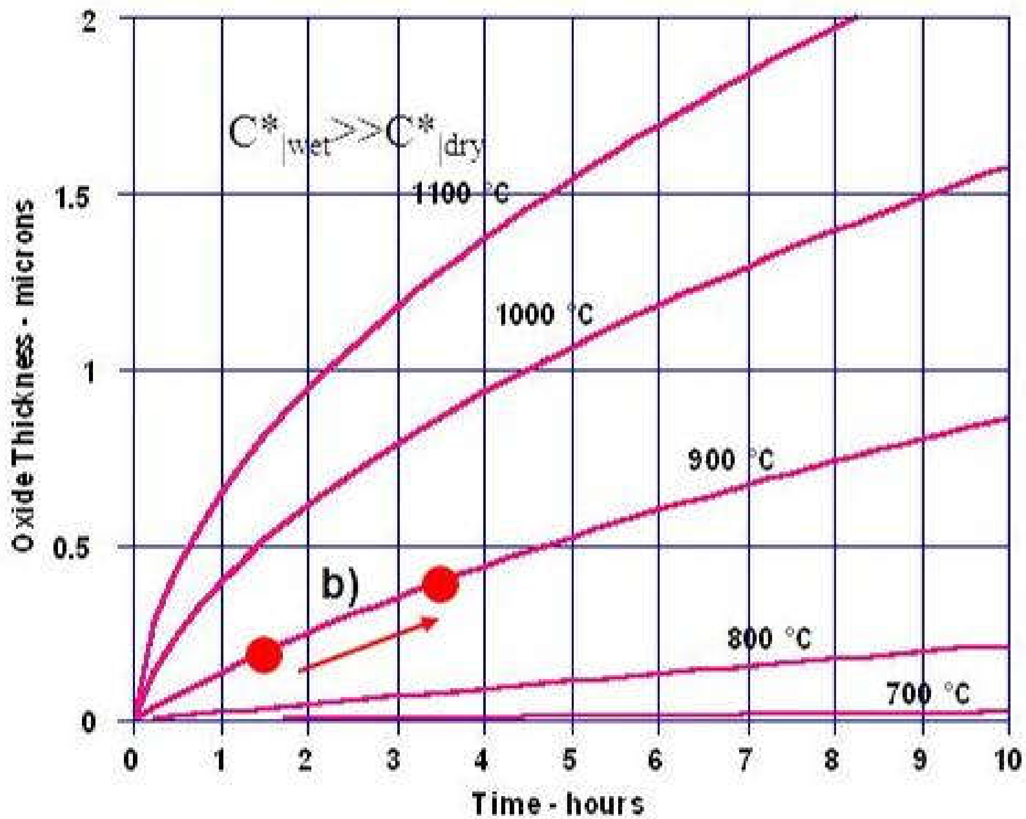
Dry vs. Wet Oxidation

Dry oxidation - used up to 100-200 nm



Calculated (100) silicon dry O_2 oxidation rates using Deal Grove.

Wet oxidation - used for thicker oxides

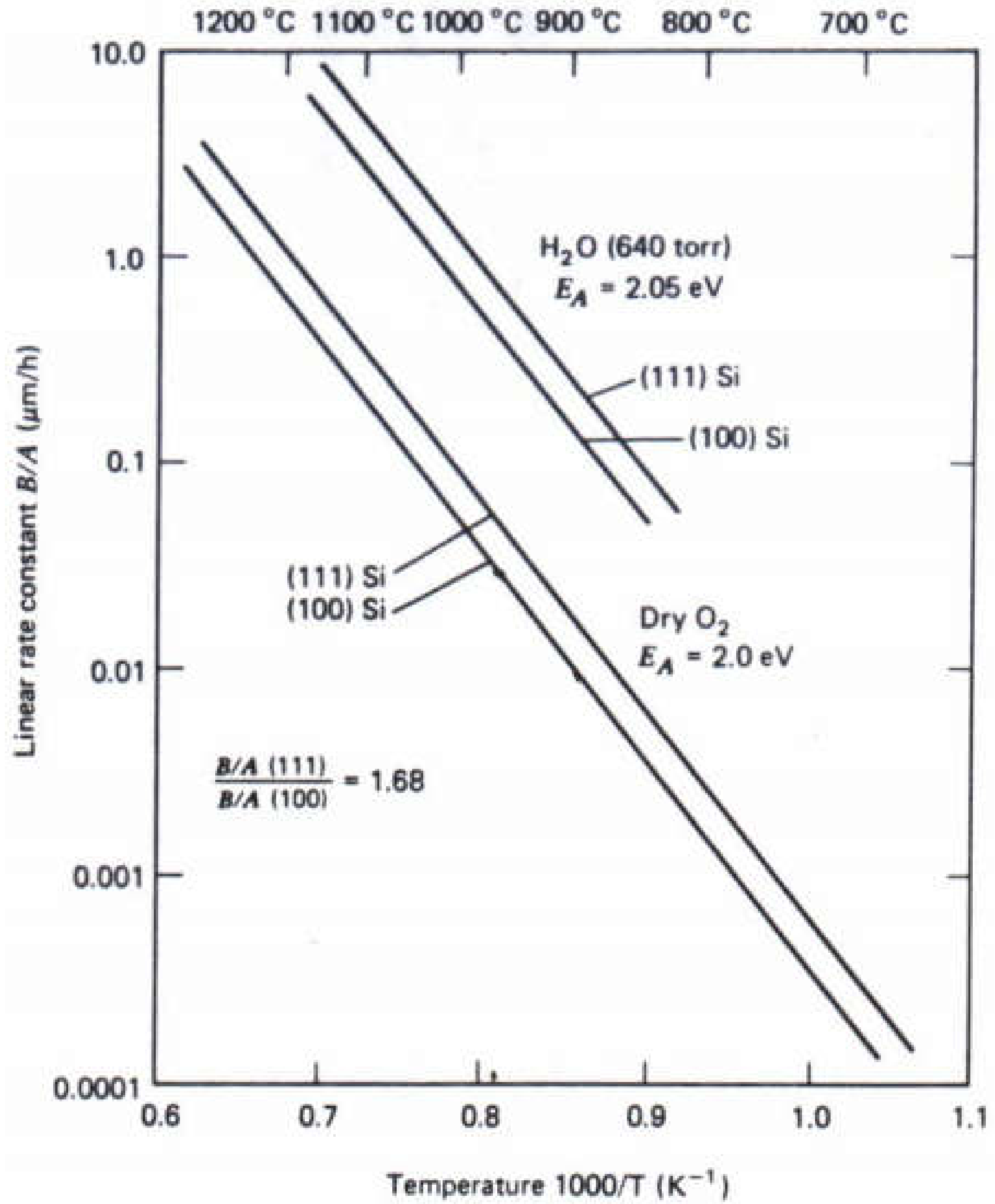


Calculated (100) silicon H_2O oxidation rates using Deal Grove.

Video

wet oxidation is 10~100 times faster than dry oxidation because H_2O has higher solubility/diffusivity in SiO_2

Crystal Orientation

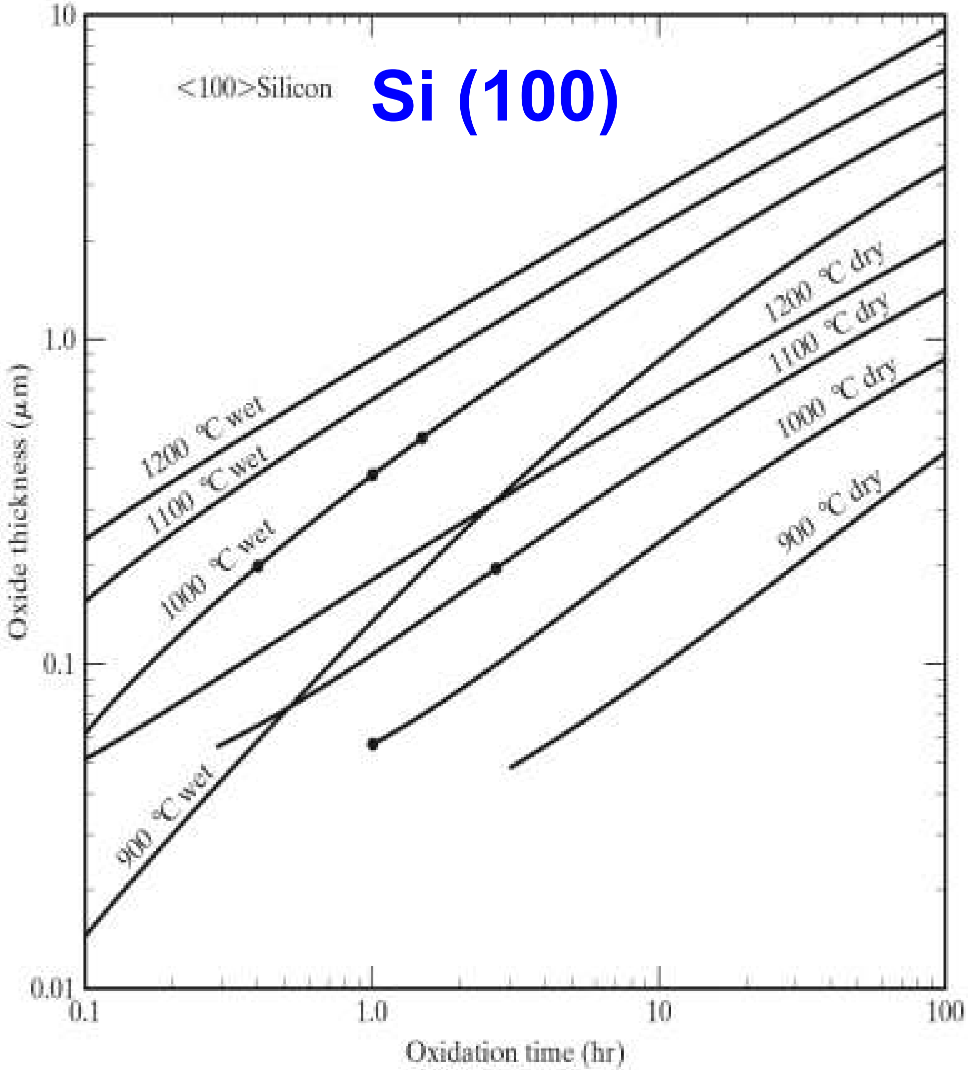


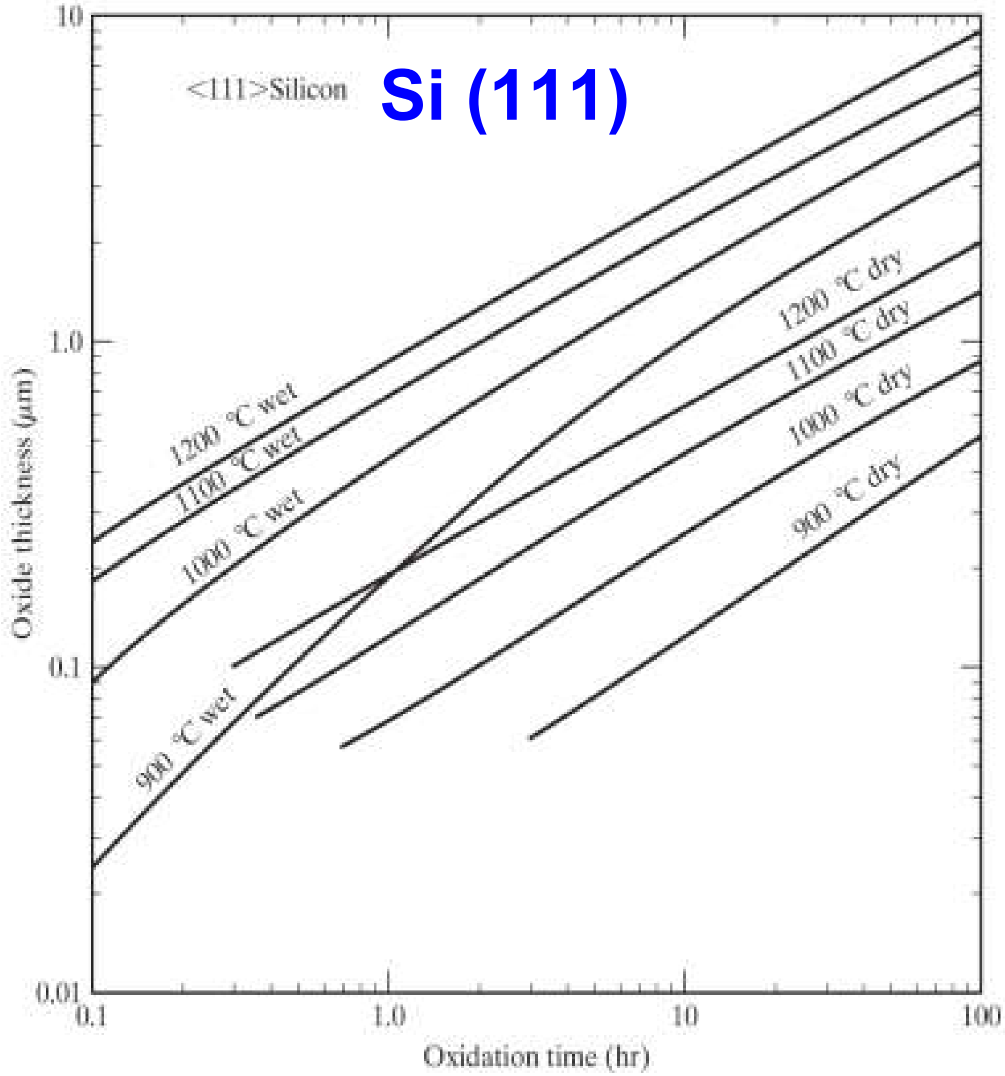
Si (111) has smaller *A*, but same *B* with Si (100)

higher growth rate at initial stage

why ??

Crystal Orientation



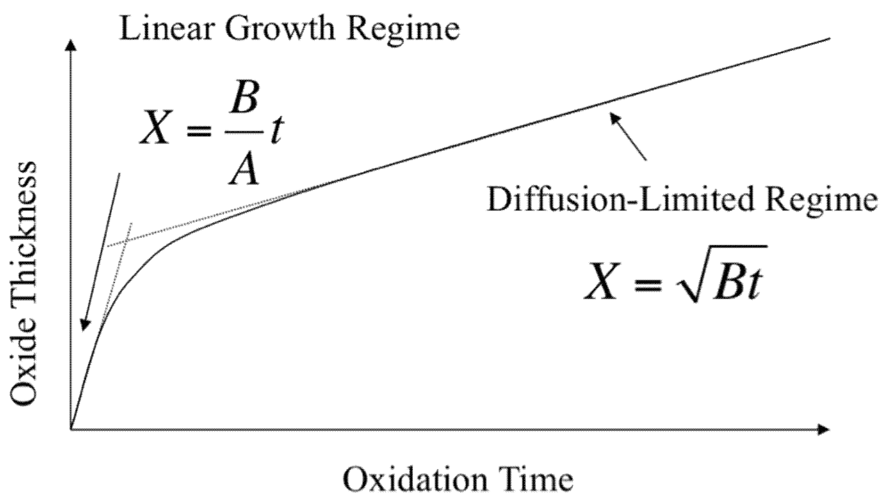


similar rates at long time oxidation (diffusion limited)

Thermal Oxidation

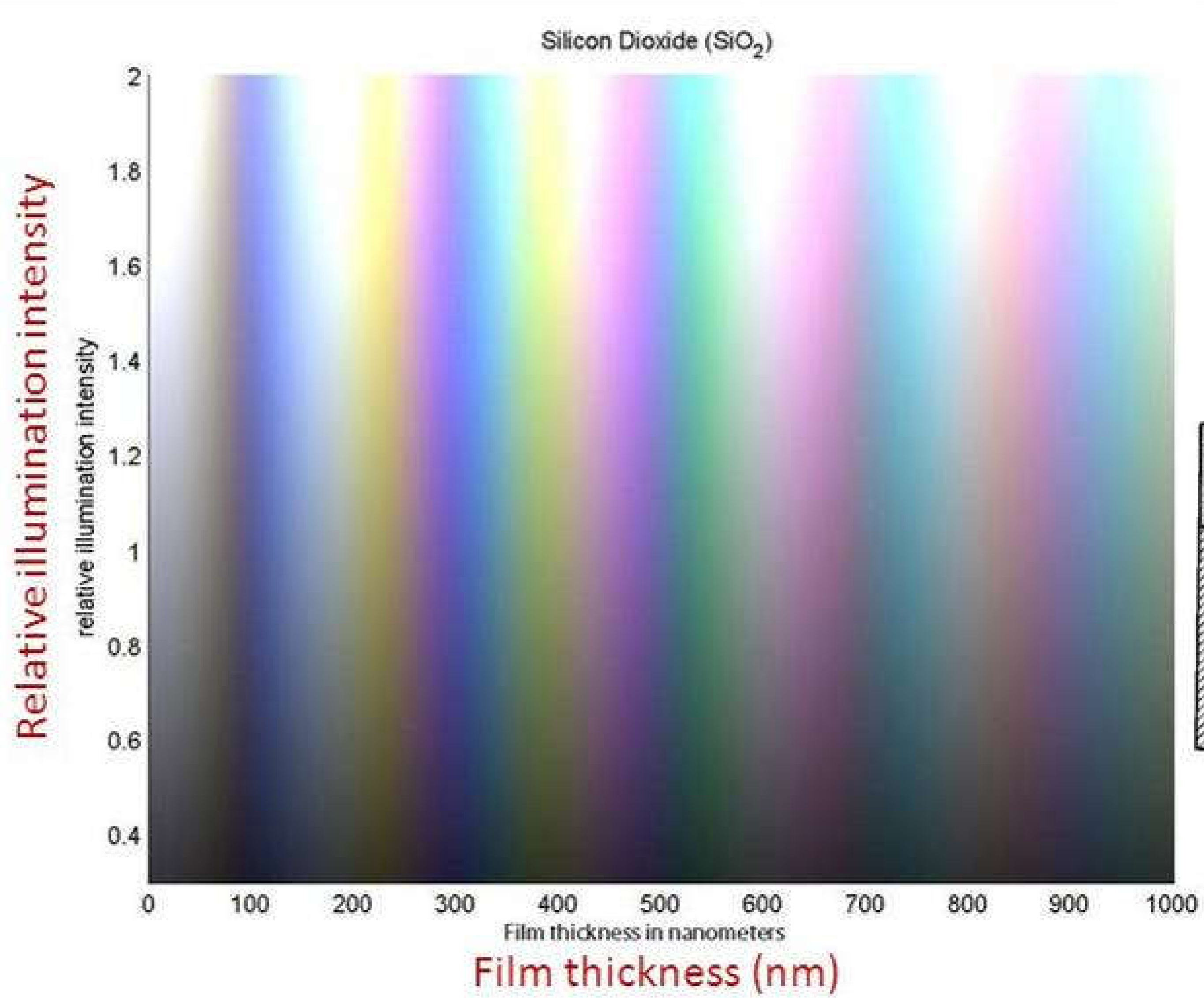
$$X_{ox} = \frac{A}{2}\left\{\sqrt{1+\left(\frac{t+\tau}{A^2/4B}\right)}-1\right\}$$

- **Process Parameters**
  - Time
  - Temperature
  - Gas type (O_2, H_2O, ...)
  - Gas pressure
  - Crystal orientation
  - Dopant (B, P, As, ...)

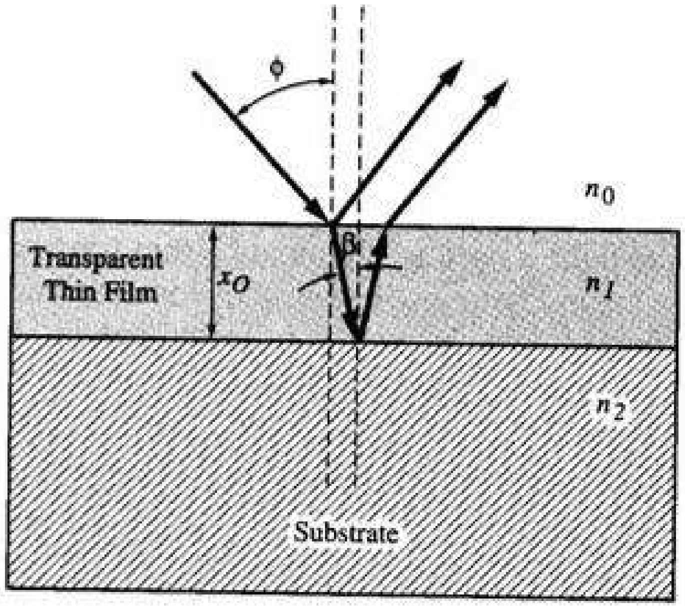


- **Control Parameters**
  - Oxide thickness
  - Film quality (defects, dielectric strength, ...)

SiO_2 Film Thickness Measurement

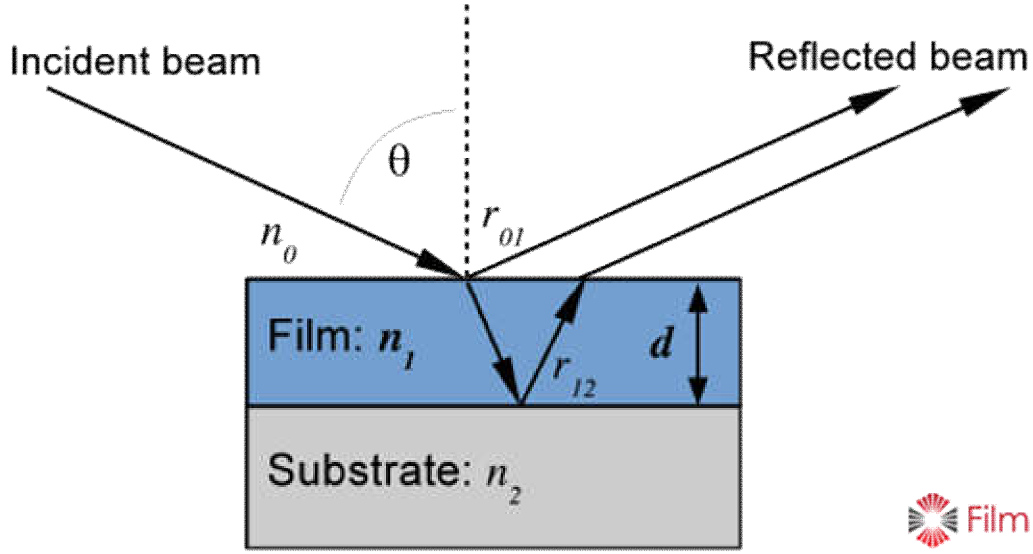


color difference



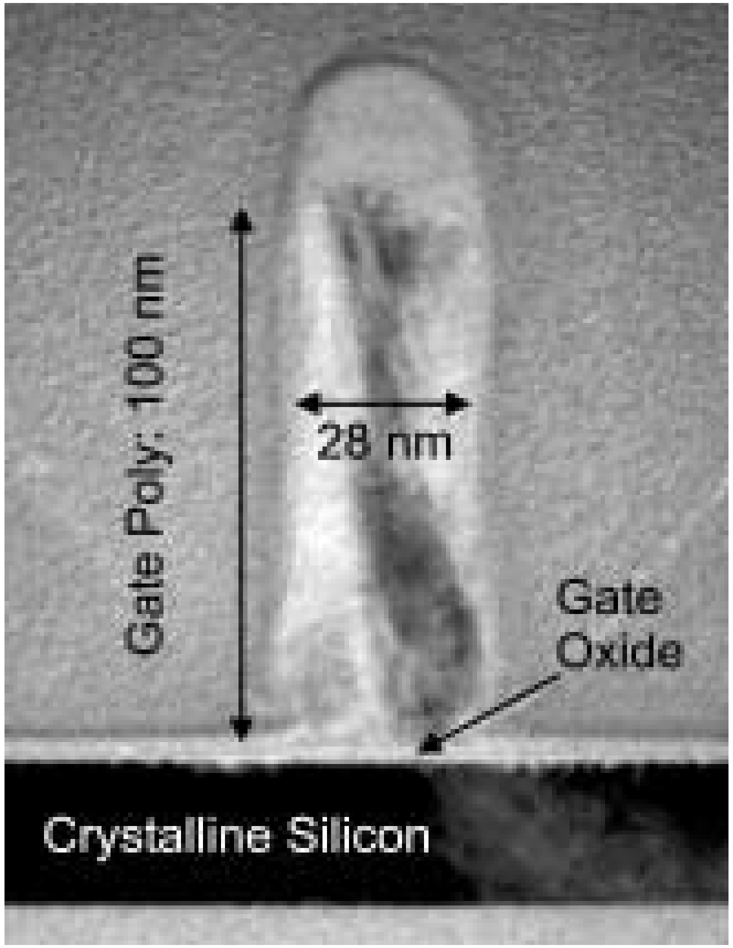
SiO_2 Film Thickness Measurement

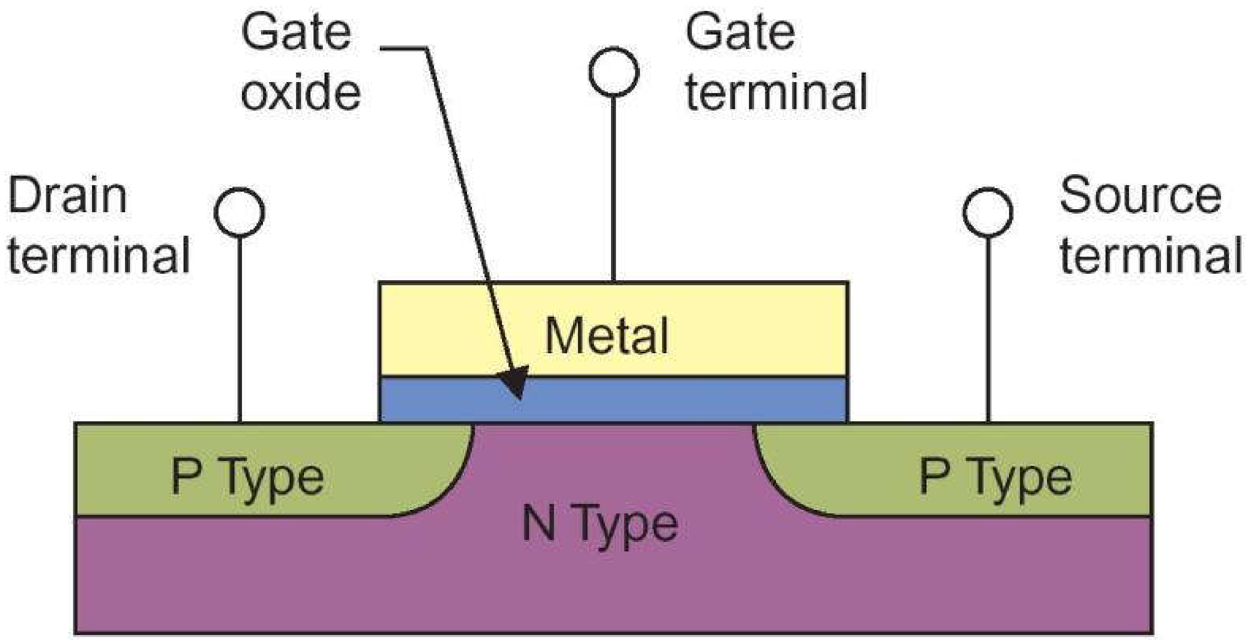
Spectroscopic Ellipsometer



SiO_2 in CMOS

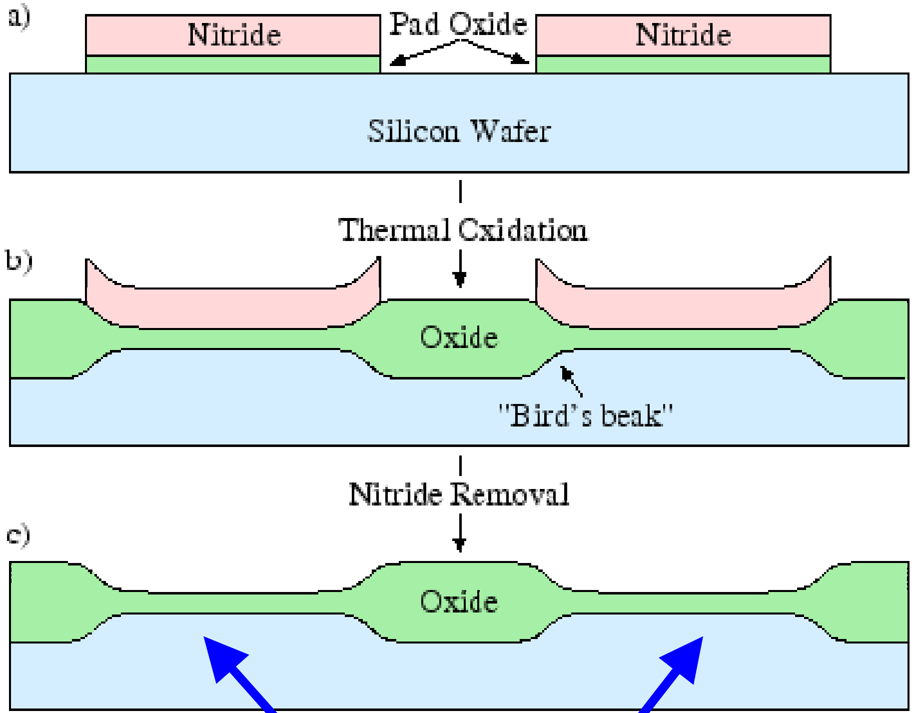
gate oxide for transistors

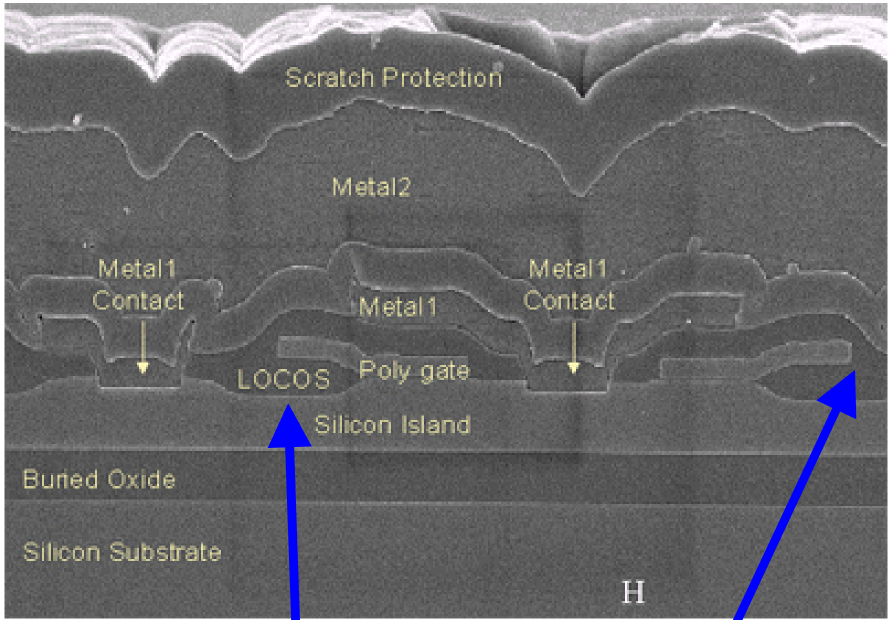




SiO_2 in CMOS

Local Oxidation of Si (LOCOS)





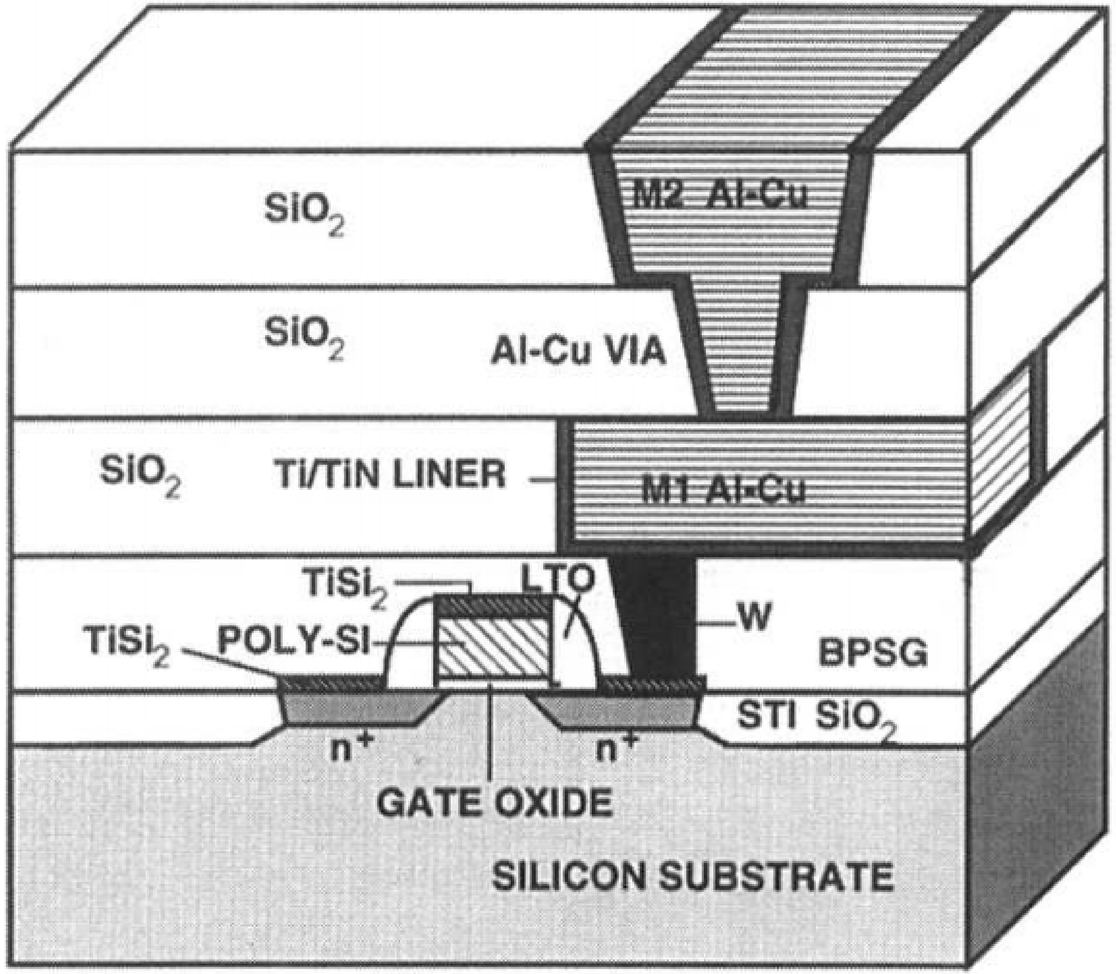
For isolation

transistor region

SiO_2 in CMOS

other methods to deposit SiO_2

temperature



Q: why?

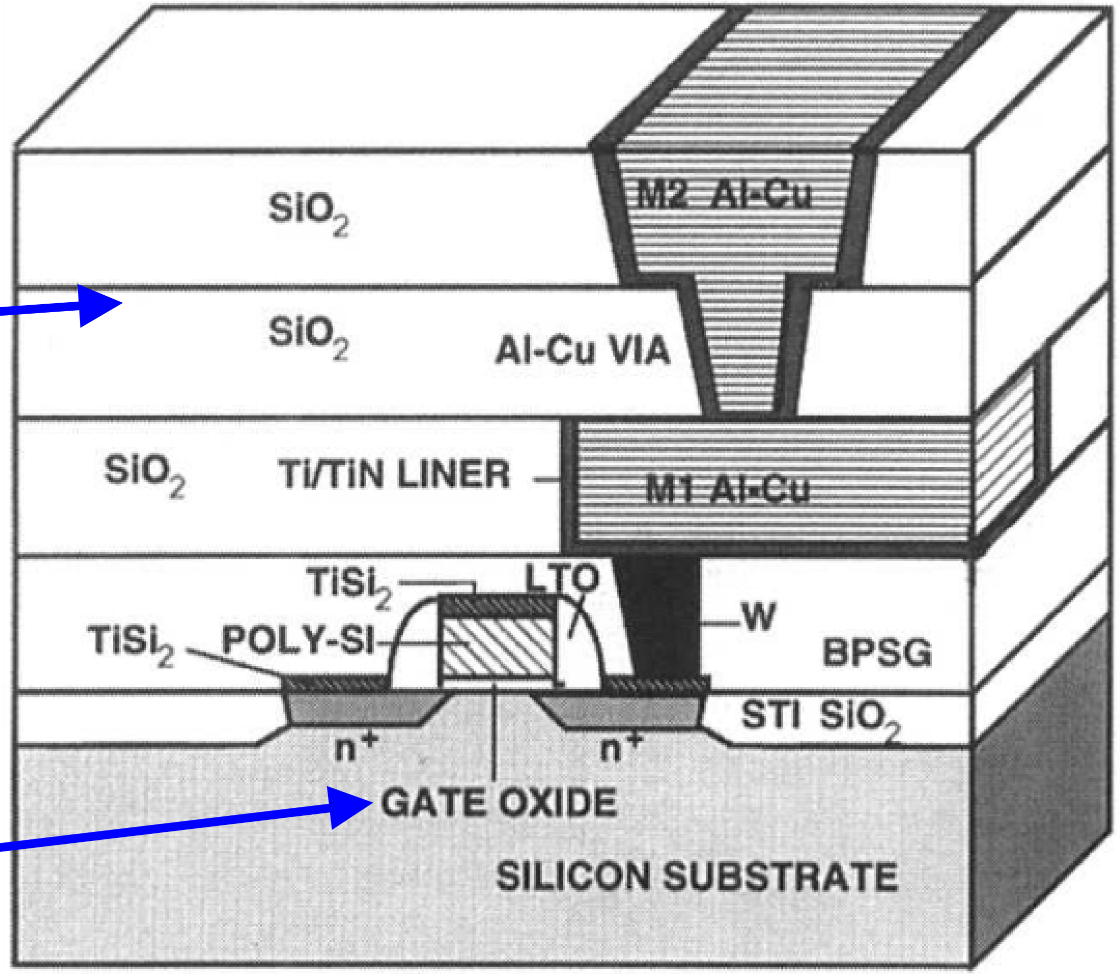
SiO_2 in CMOS

$$C = \frac{\kappa \varepsilon_0 A}{t}$$

low κ dielectric for insulating reduce *RC* delay

high κ dielectric for gate oxide

$$I_{D,Sat} = \frac{W}{L} \mu C \frac{(V_G - V_{th})^2}{2}$$



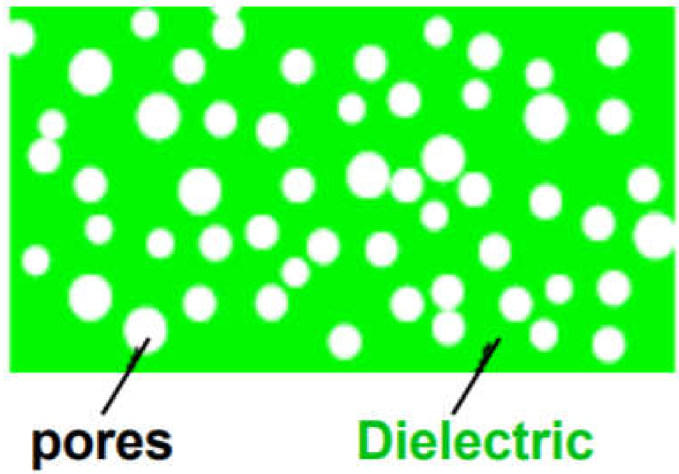
Porous SiO_2 for Low κ Dielectric

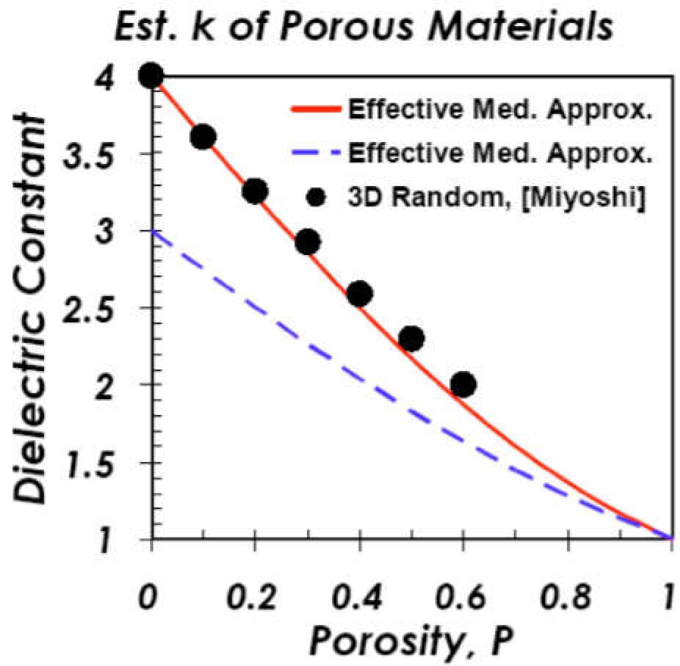
SiO_2

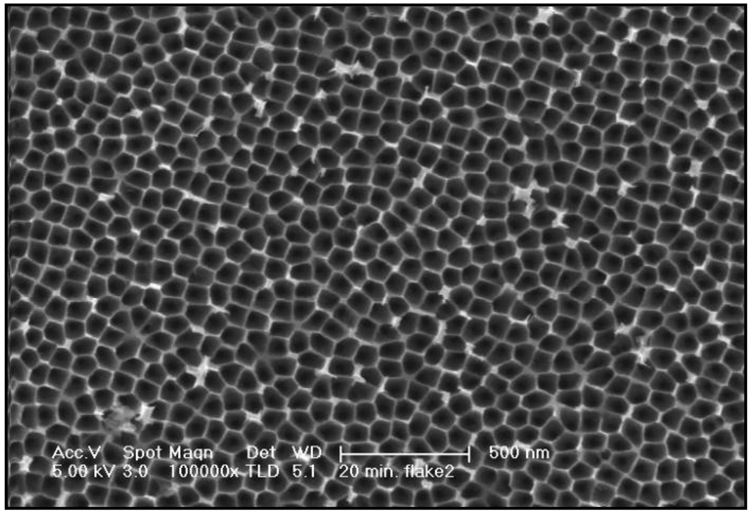
$\kappa = 3.9$

air

$\kappa = 1.0$

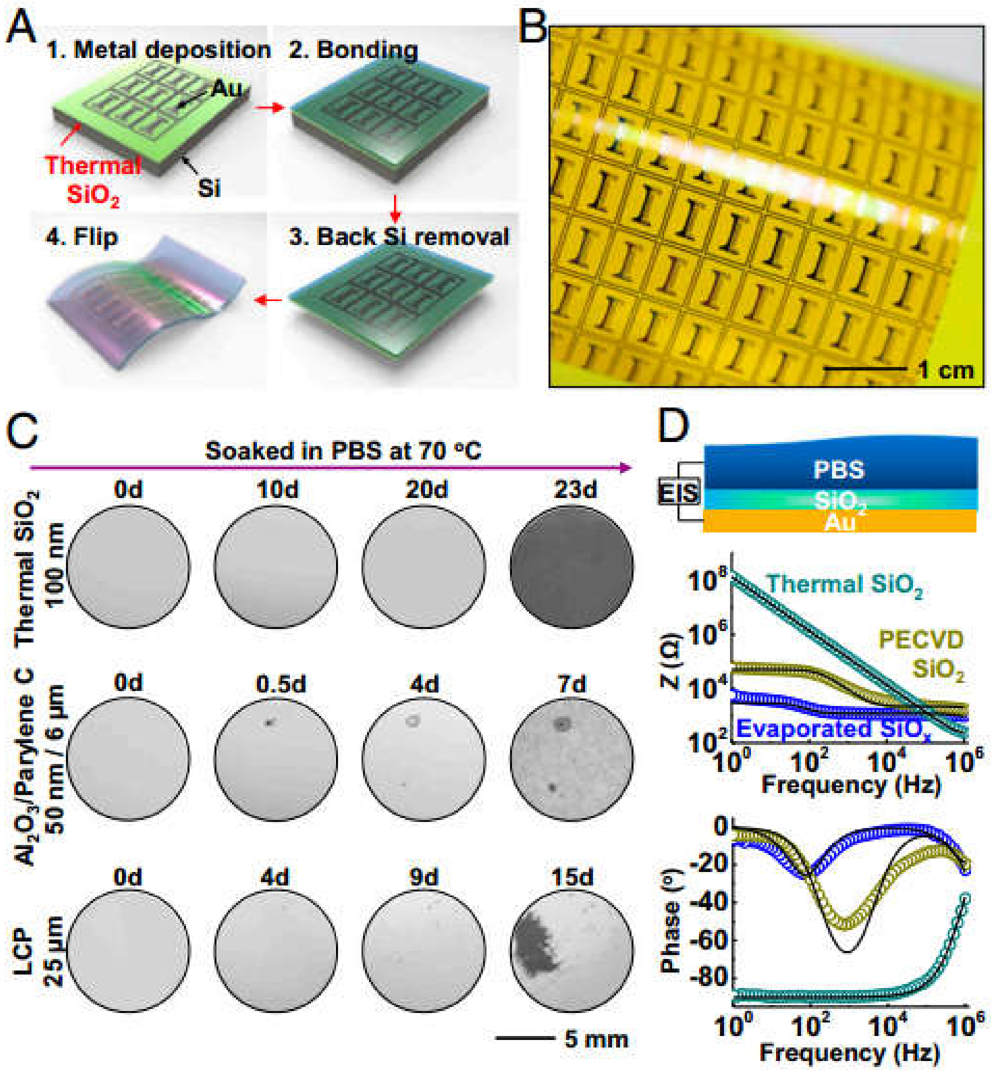






SiO_2 in Biointegrated Devices

Thermal oxide is the best moisture barrier



useful for implantable devices

At room temperature, it will take > 100 years to dissolve 1 μm thermal SiO_2 in water

H. Fang, *et al.*, *Proc. Natl. Acad. Sci.* **113,** 11682 (2016)

Thank you for your attention