微纳光电子材料与器件工艺原理

Packaging and Integration

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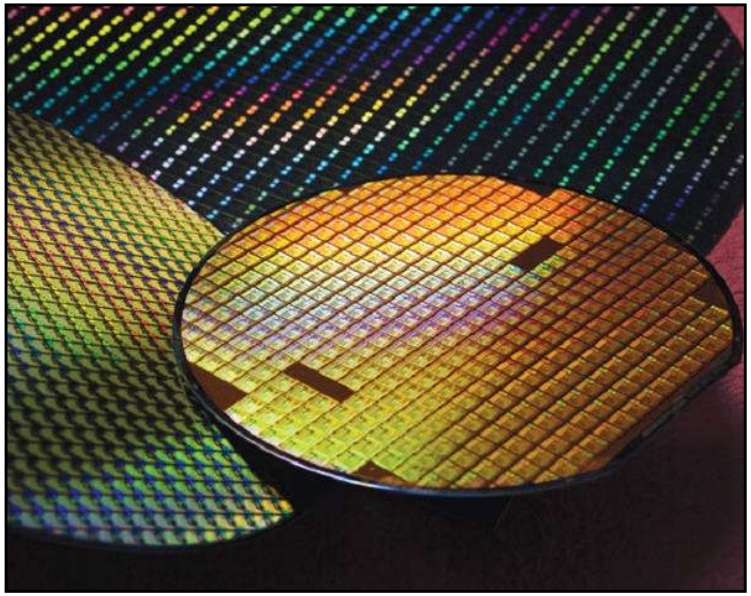
Packaging

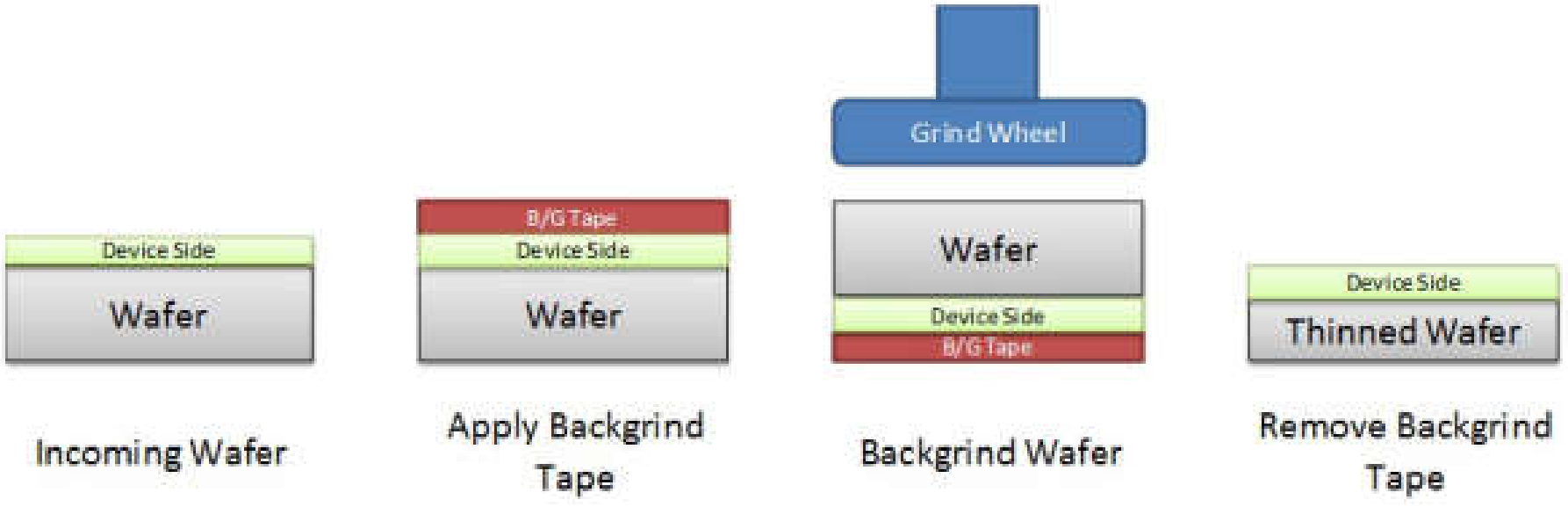


Si wafers

IC chips

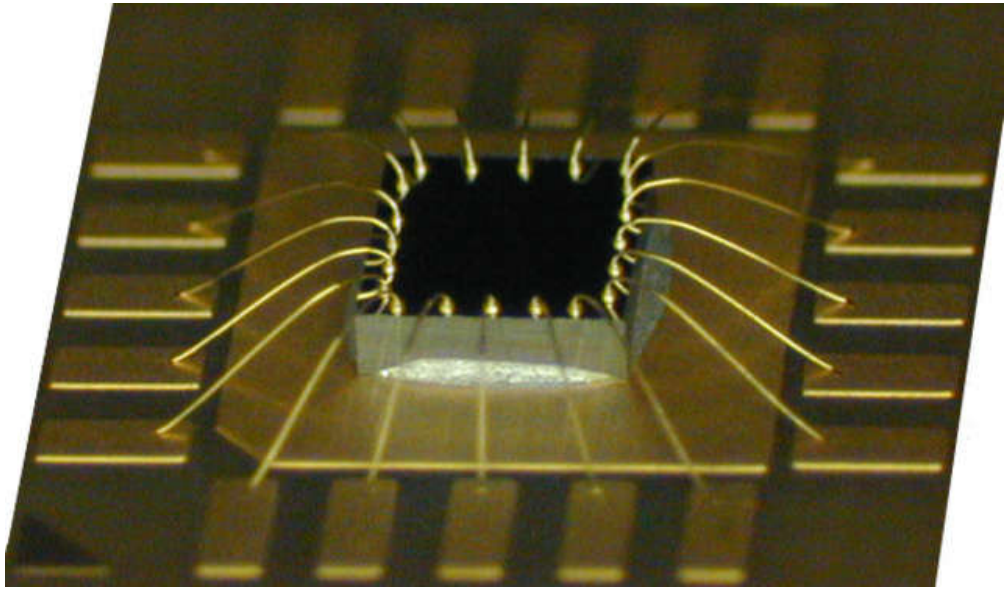
Video

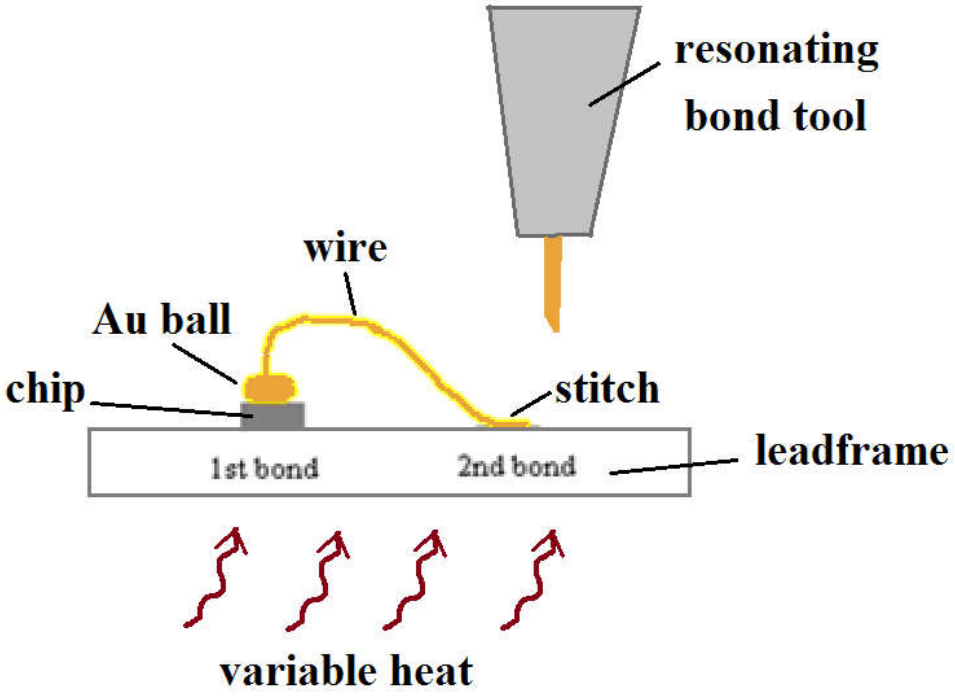
Wafer Thinning



can be as thin as 20 μm

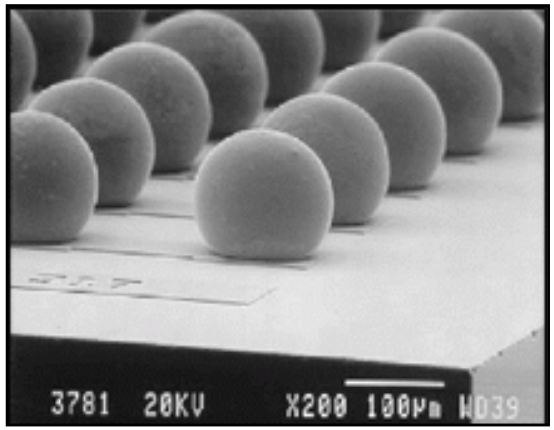
Wire Bonding

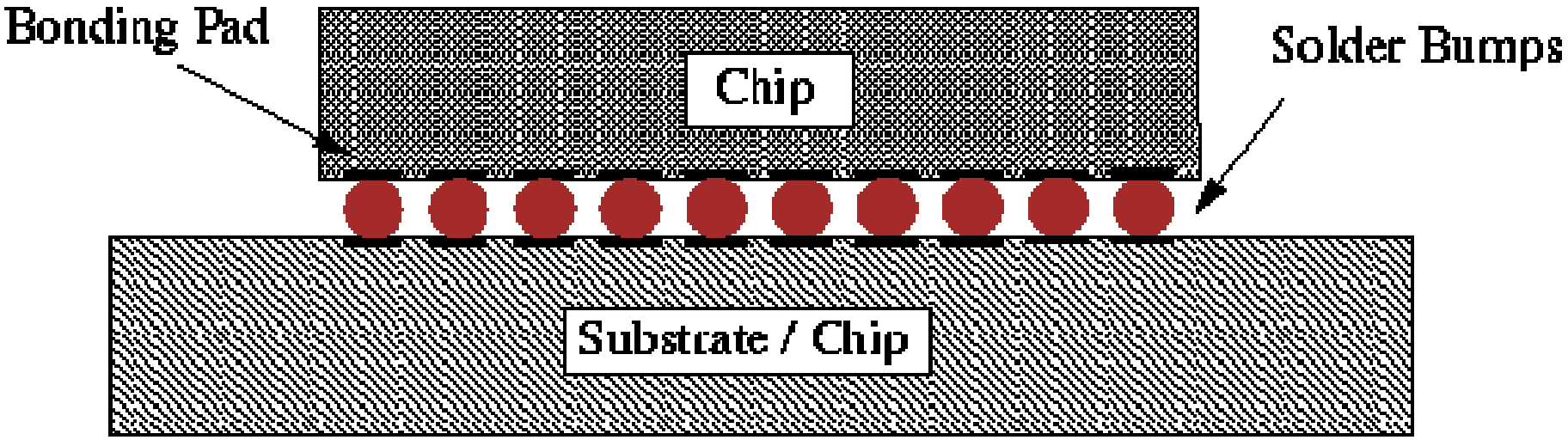




'Flip-Chip' Die Bonding

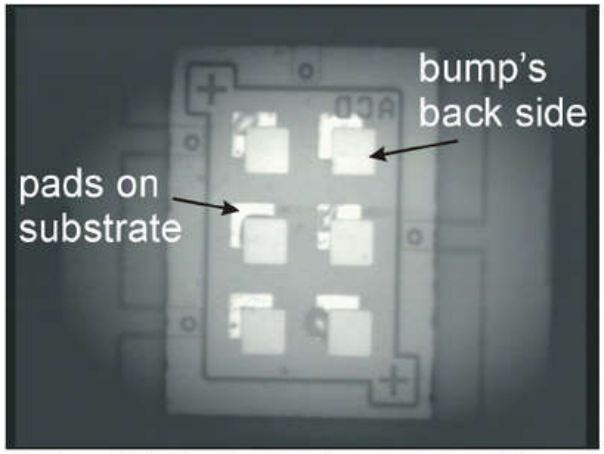
Metals alloys: Pb, Cu, Ag, Sn, ...
low melting point

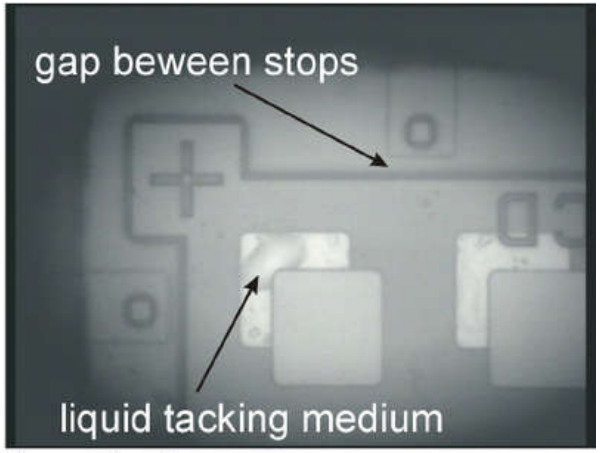




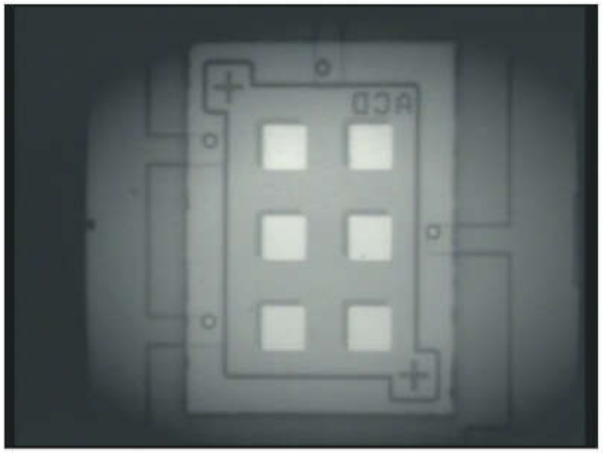
Infrared Imaging

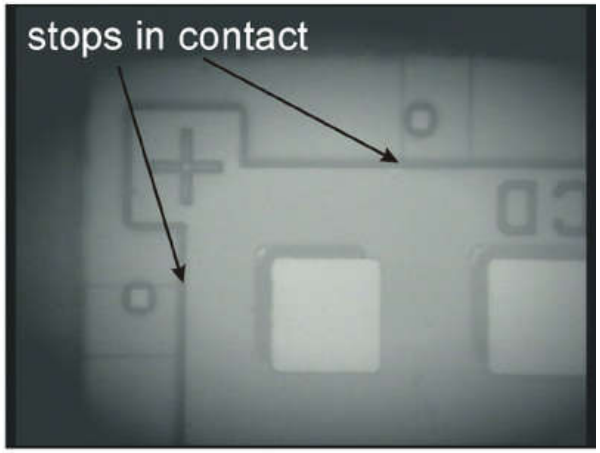
Si is transparent at near-infrared (> 1100 nm)





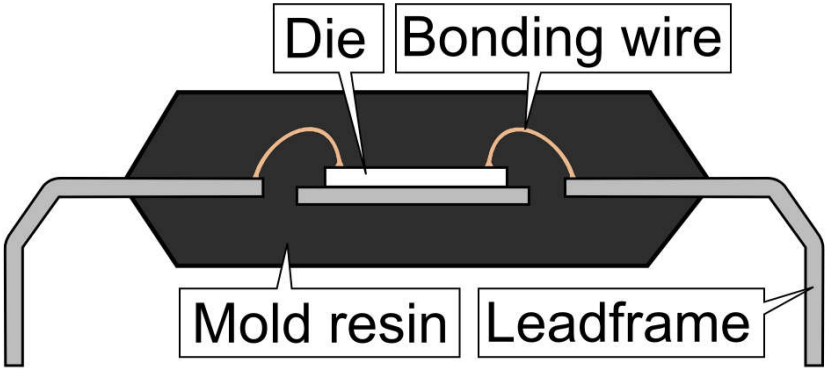
After pick & place: stops are not in contact to each other

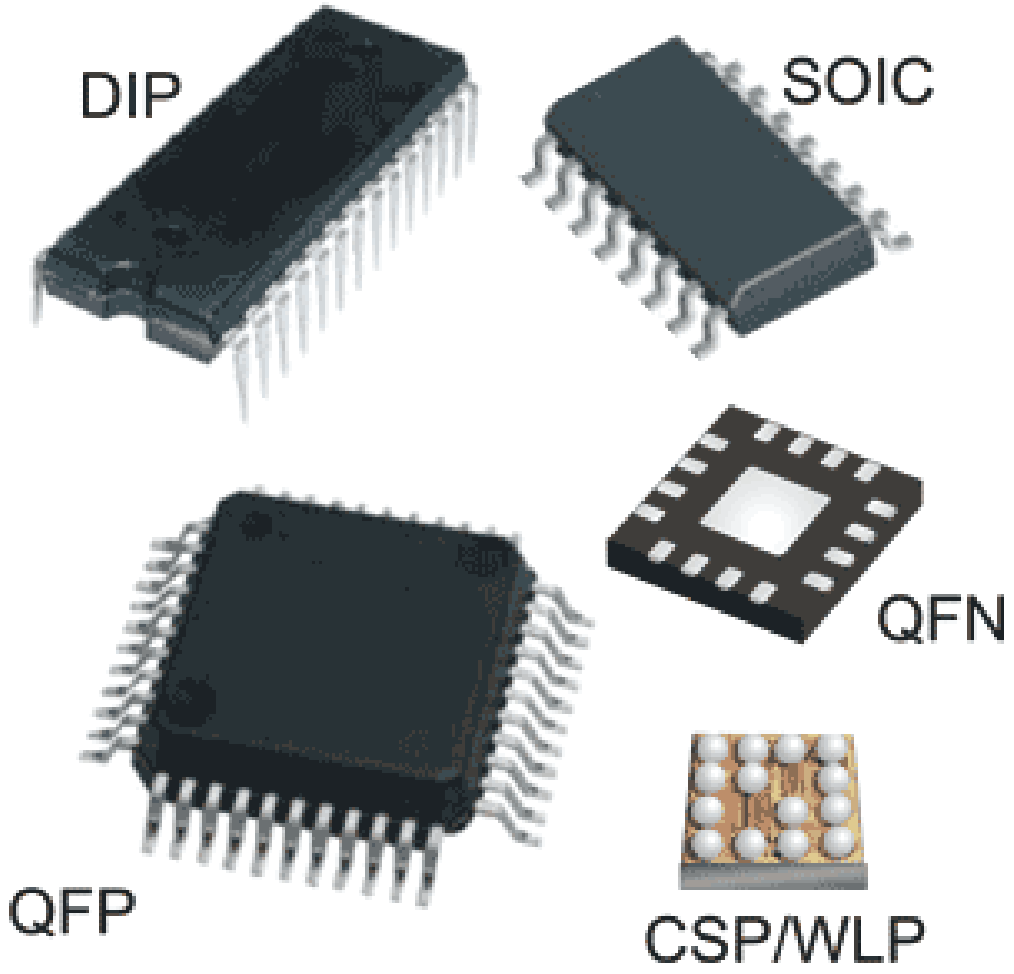




After reflow: stops have reached each other

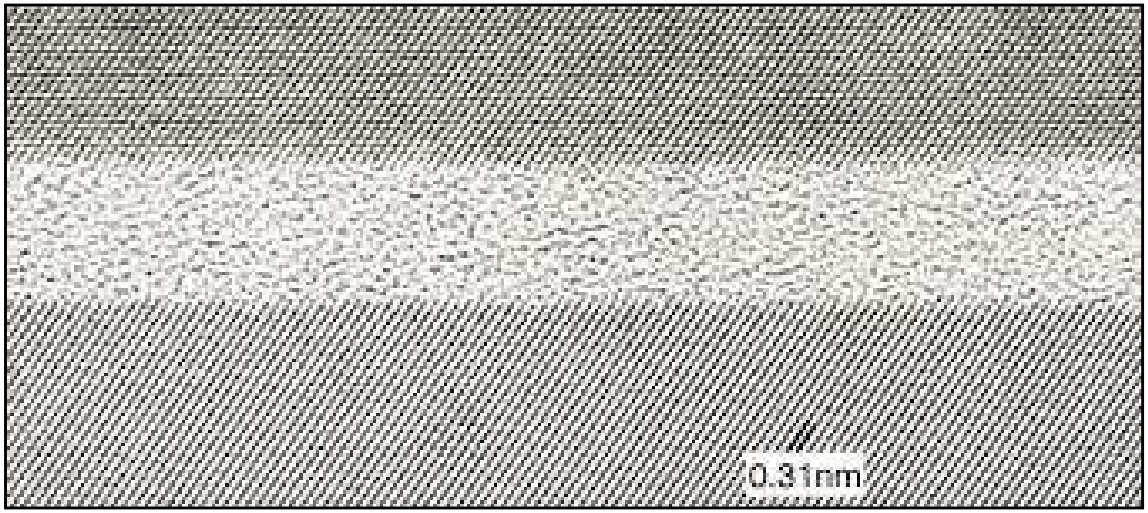
Chip Packaging





Wafer Bonding

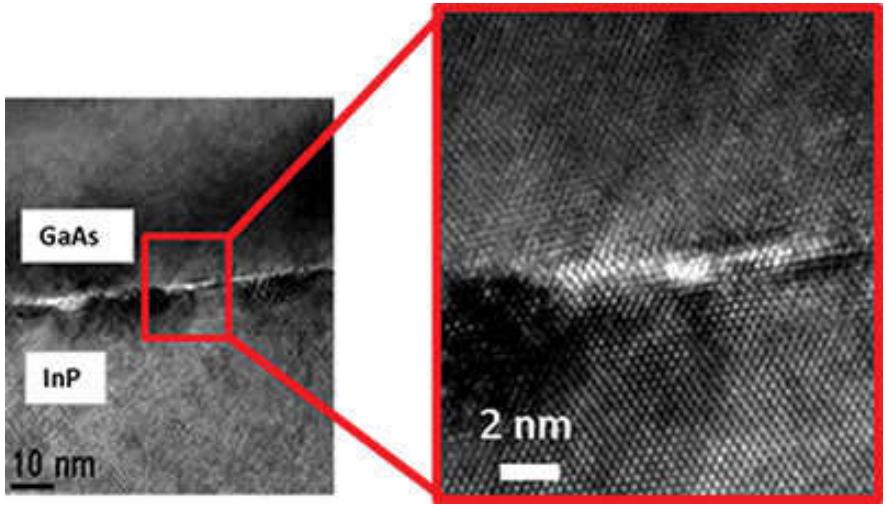
when direct growth is difficult ...

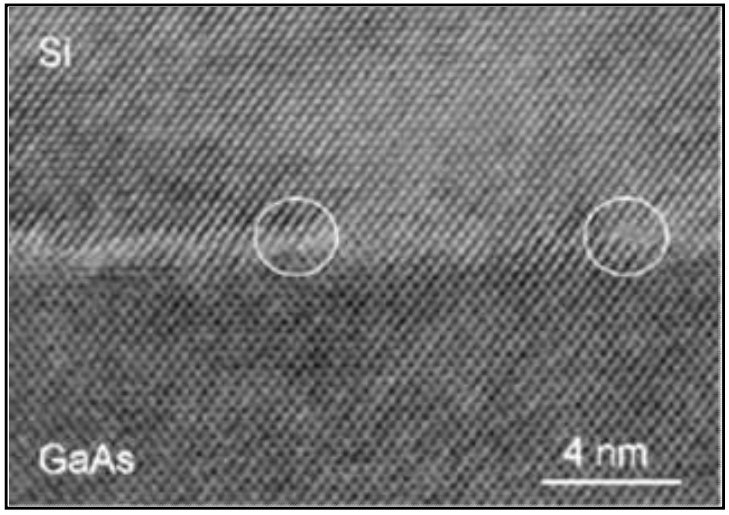


Si

SiO_2

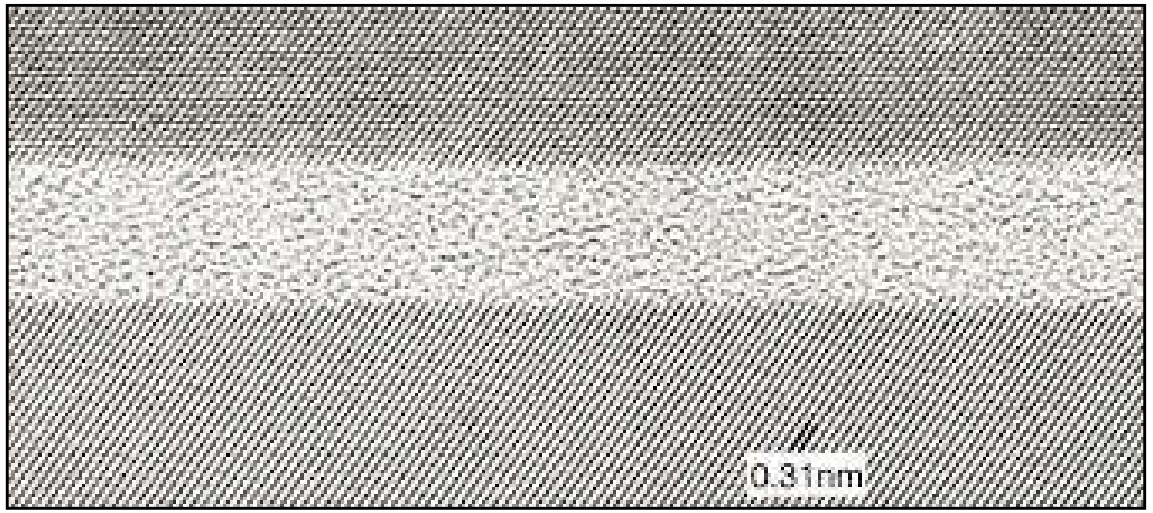
Si





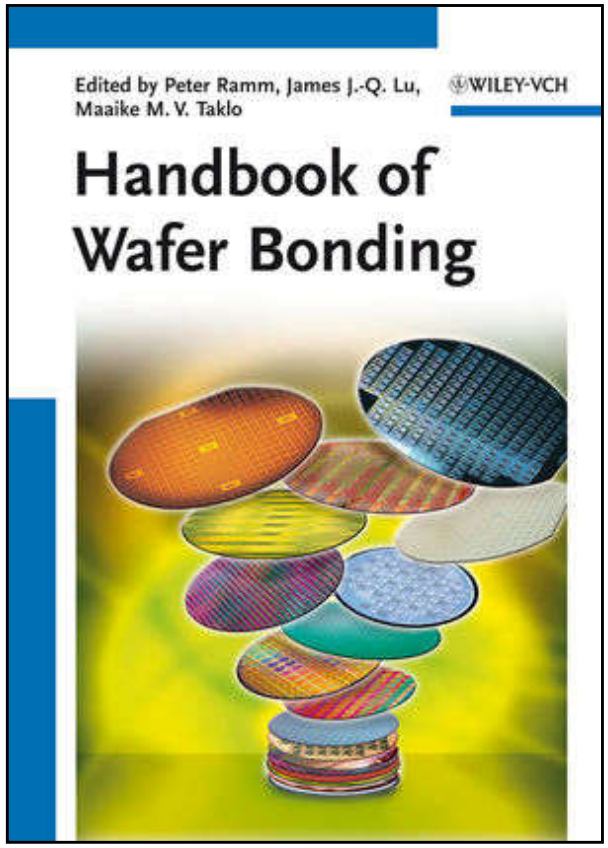
Wafer Bonding

- **Direct wafer-wafer bonding**
  - very clean and smooth surface
  - high temperature (> 1000 °C) for atom diffusion



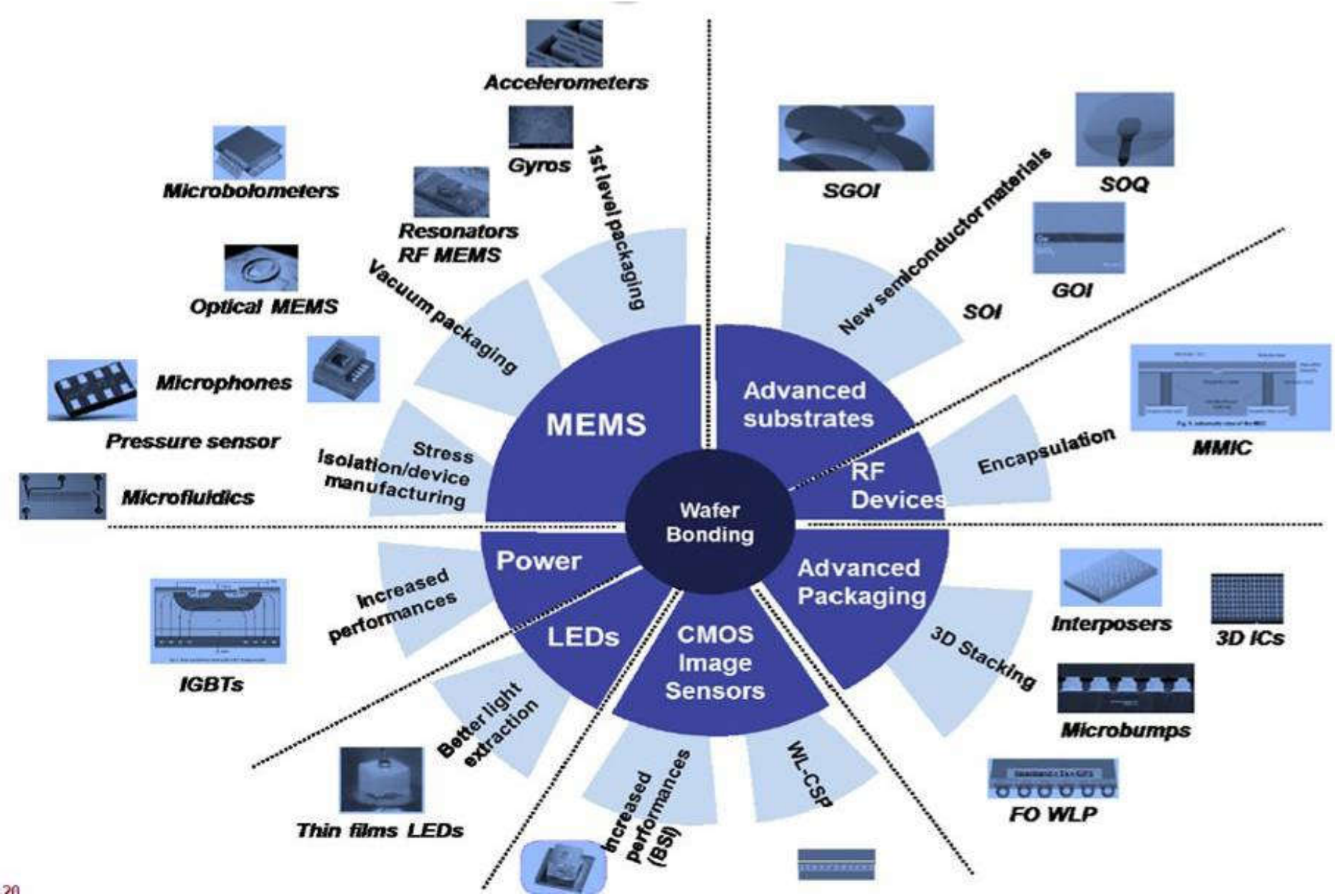
Wafer Bonding

- Direct bonding
- Surface activated bonding
- Plasma activated bonding
- Anodic bonding
- Eutectic bonding
- Glass frit bonding
- Adhesive bonding
- Thermocompression bonding
- Reactive bonding
- Transient liquid phase diffusion bonding
- ...



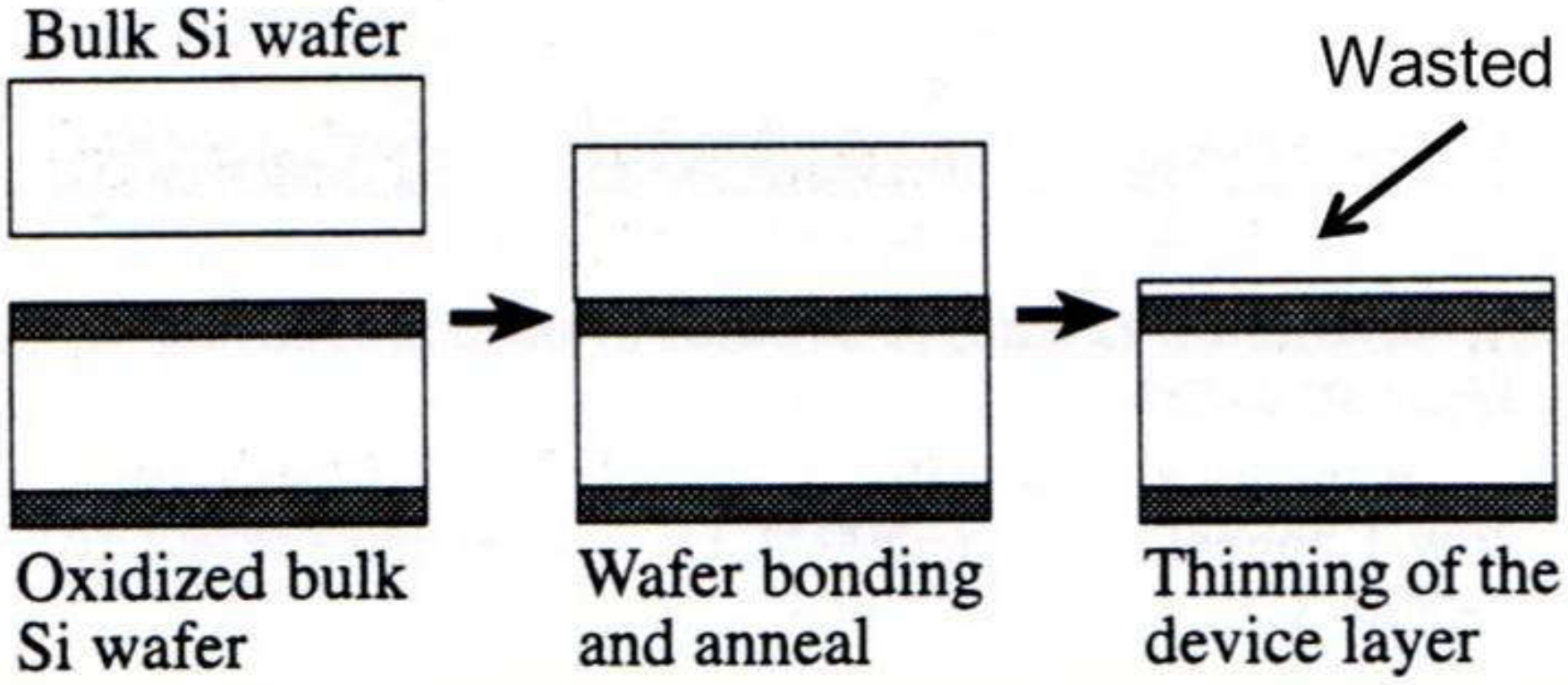
https://en.wikipedia.org/wiki/Wafer_bonding

Wafer Bonding: Applications



Make Silicon-on-Insulator (SOI)

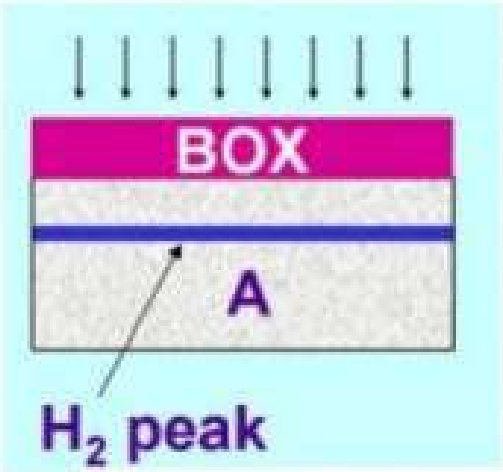
Bonding + Etch back

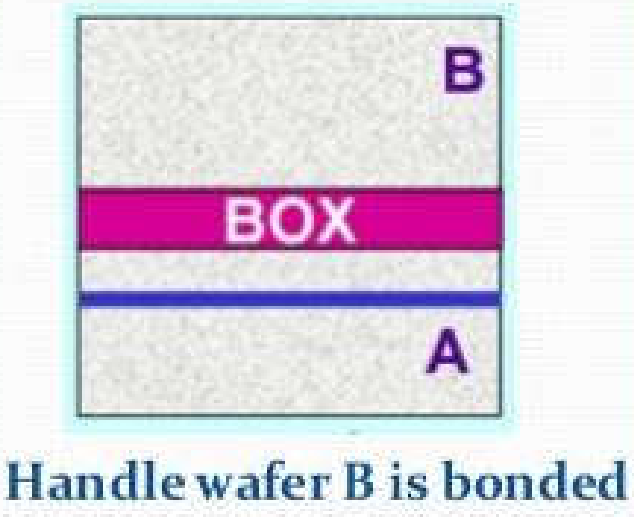


Make Silicon-on-Insulator (SOI)

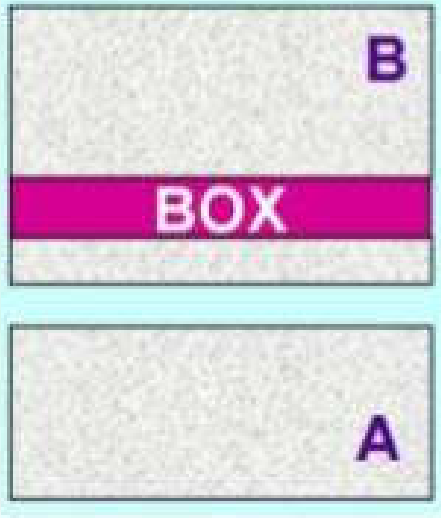
'Smart-Cut'

Hydrogen implantation through thermal oxide dose ~1-5e16 cm-2





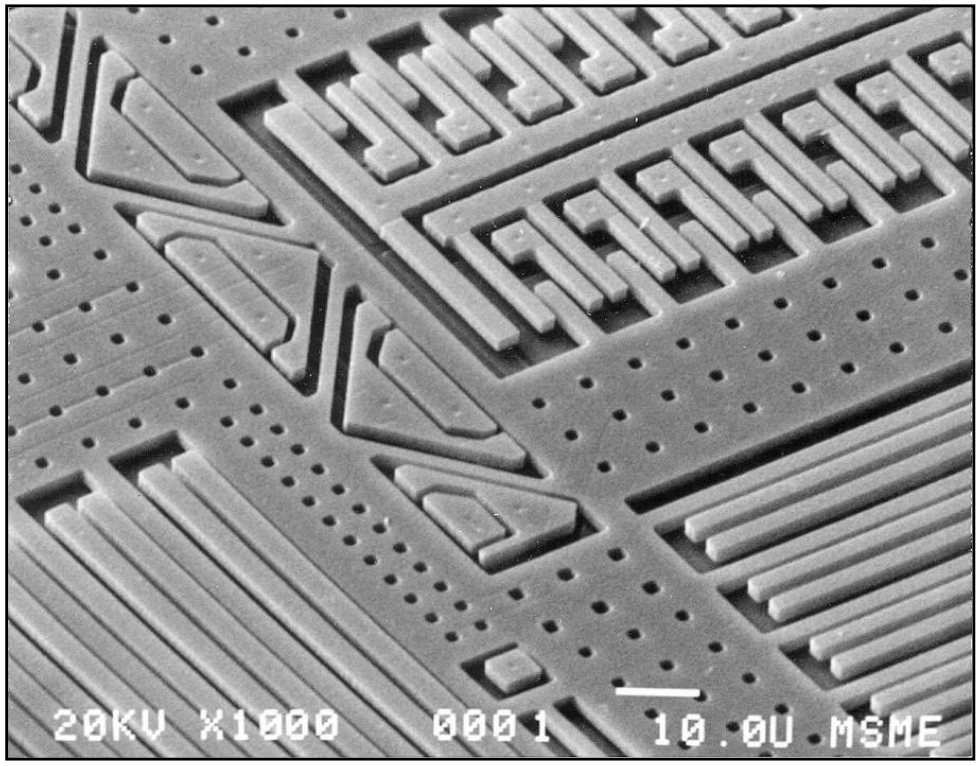
At ~400-600°C wafer A separates from B at H2 peak



After low temperature splitting, SOI wafer (B) is annealed ~1100°C to strengthen the bond, whereas wafer A is reused. SOI film thickness set by H2 implant energy and BOX thickness

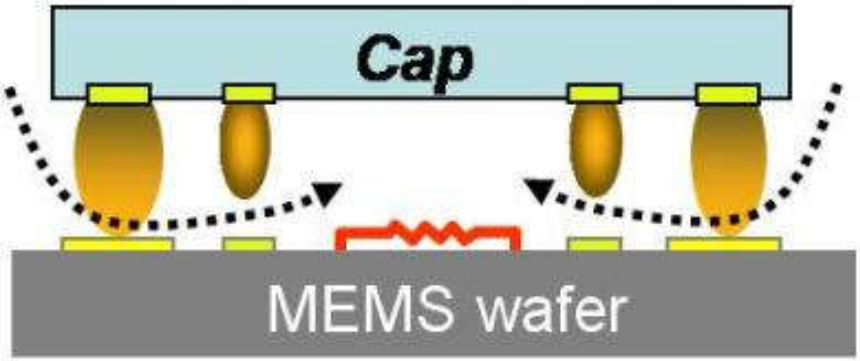
MEMS

- **Micro-Electro-Mechanical Systems (MEMS)**

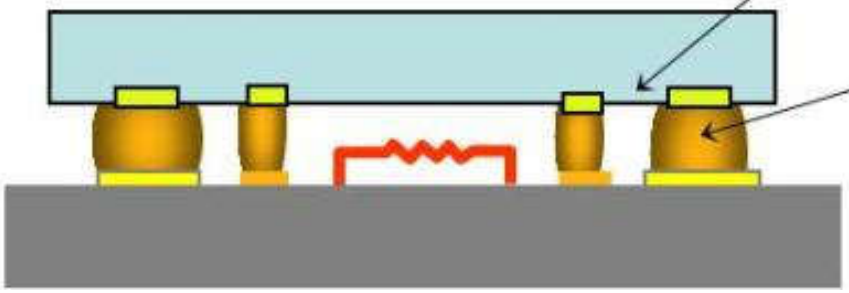


MEMS

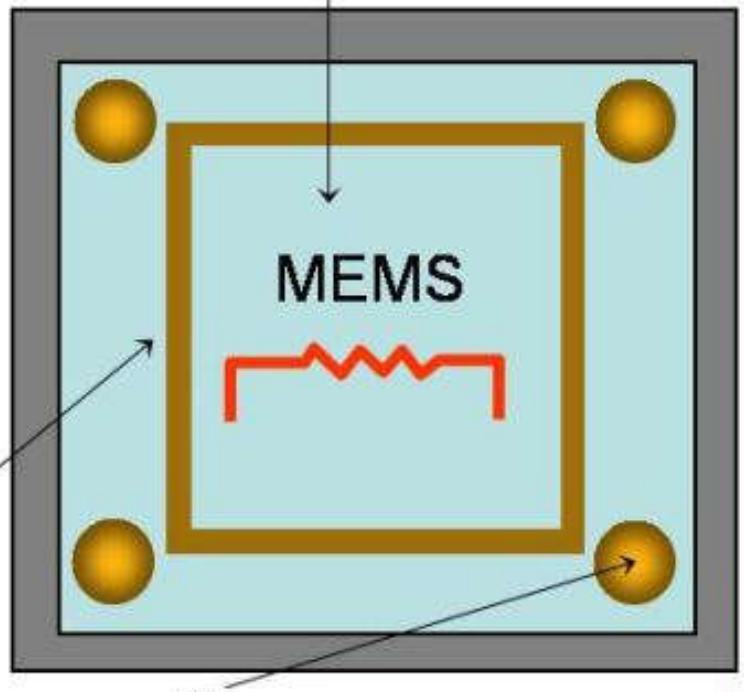
1. Oxide reduction
2. Vacuum
3. Gettering



4. Controlled Collapse Hermetic Sealing



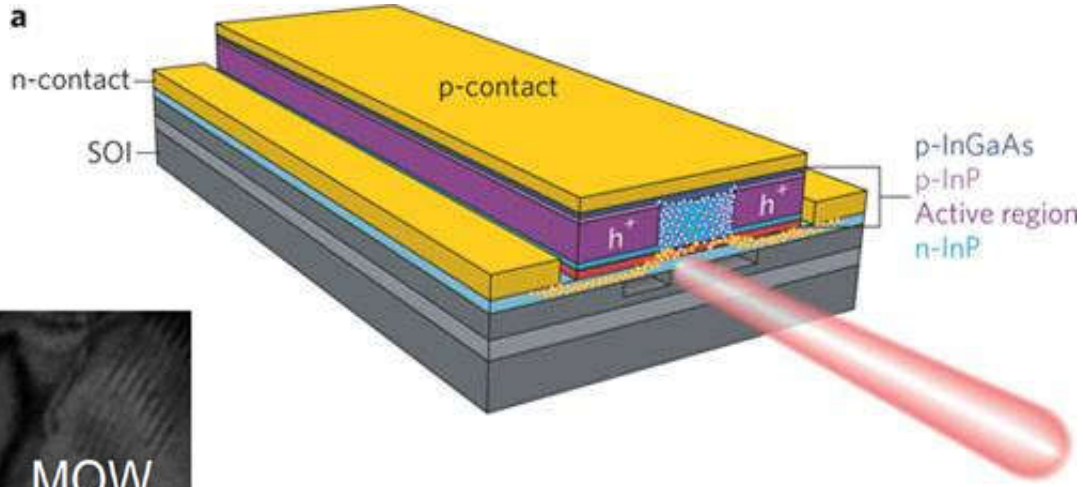
Controlled atmosphere or vacuum

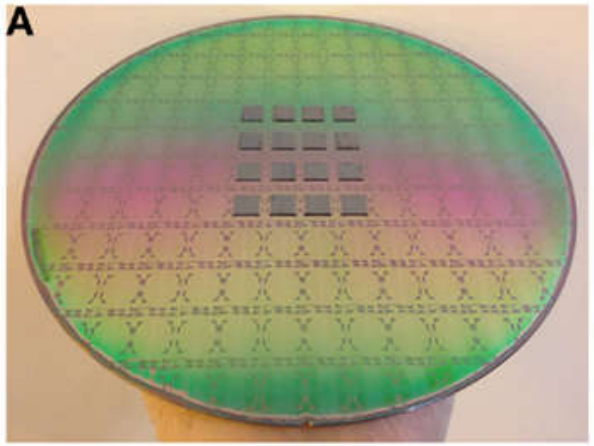


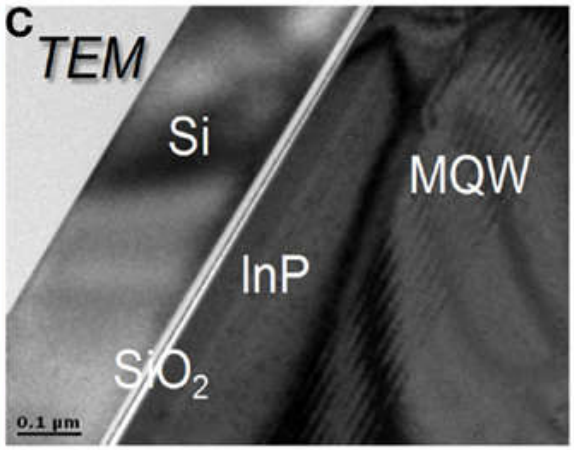
Solder ring

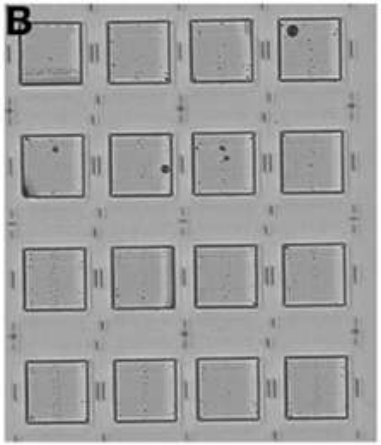
interconnection

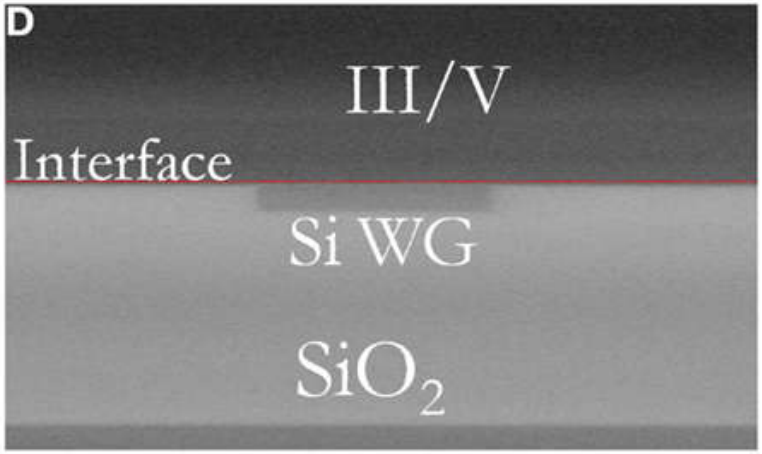
III-V Lasers on Si



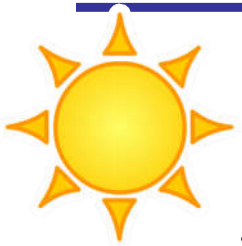


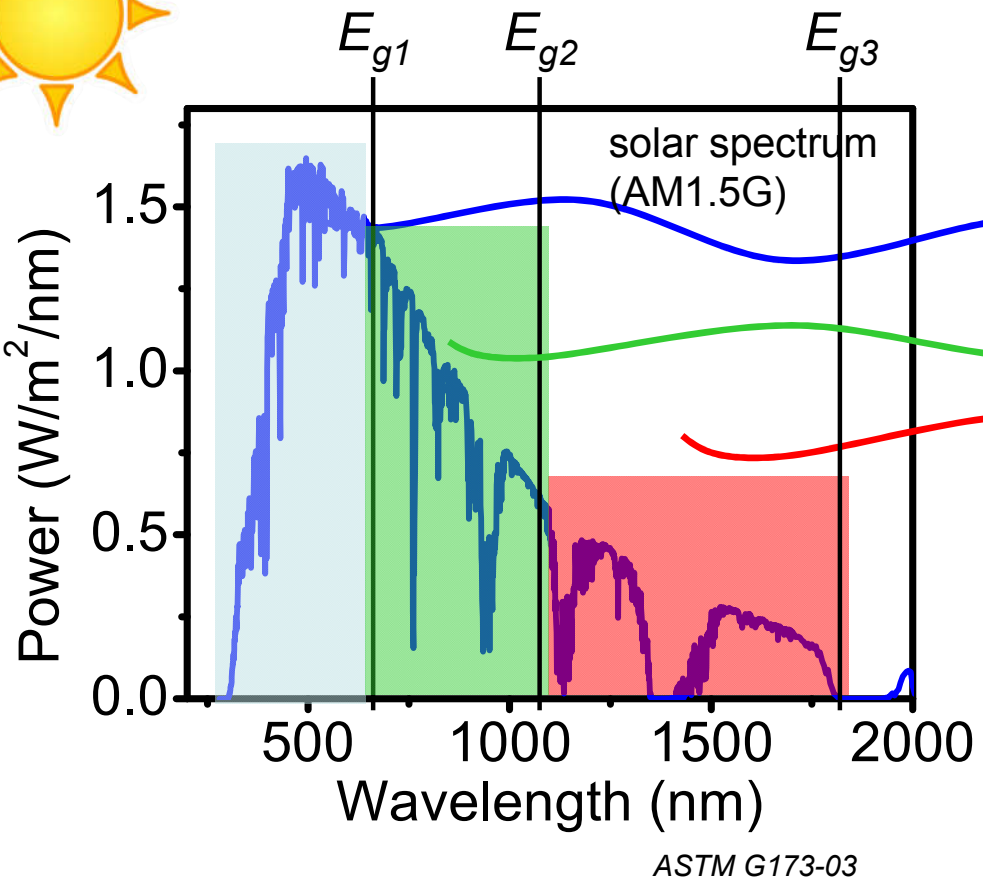


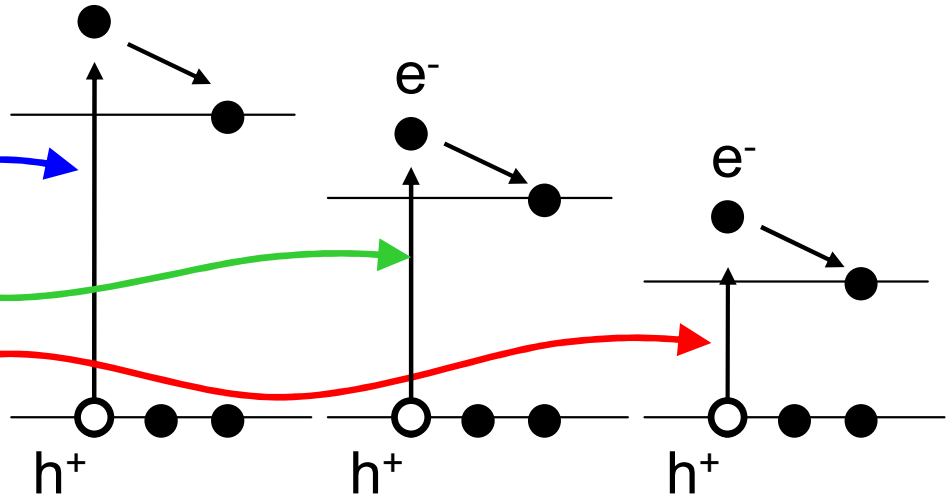




Multijunction (MJ) Solar Cells







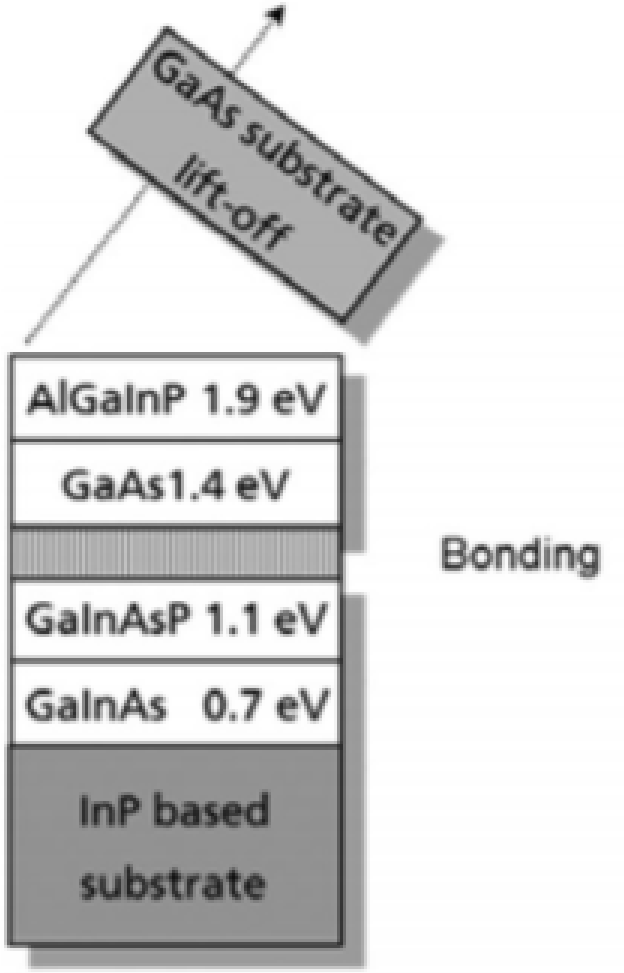
1J: η = 37%
2J: η = 50%
3J: η = 56%
infinite J: η = 72%

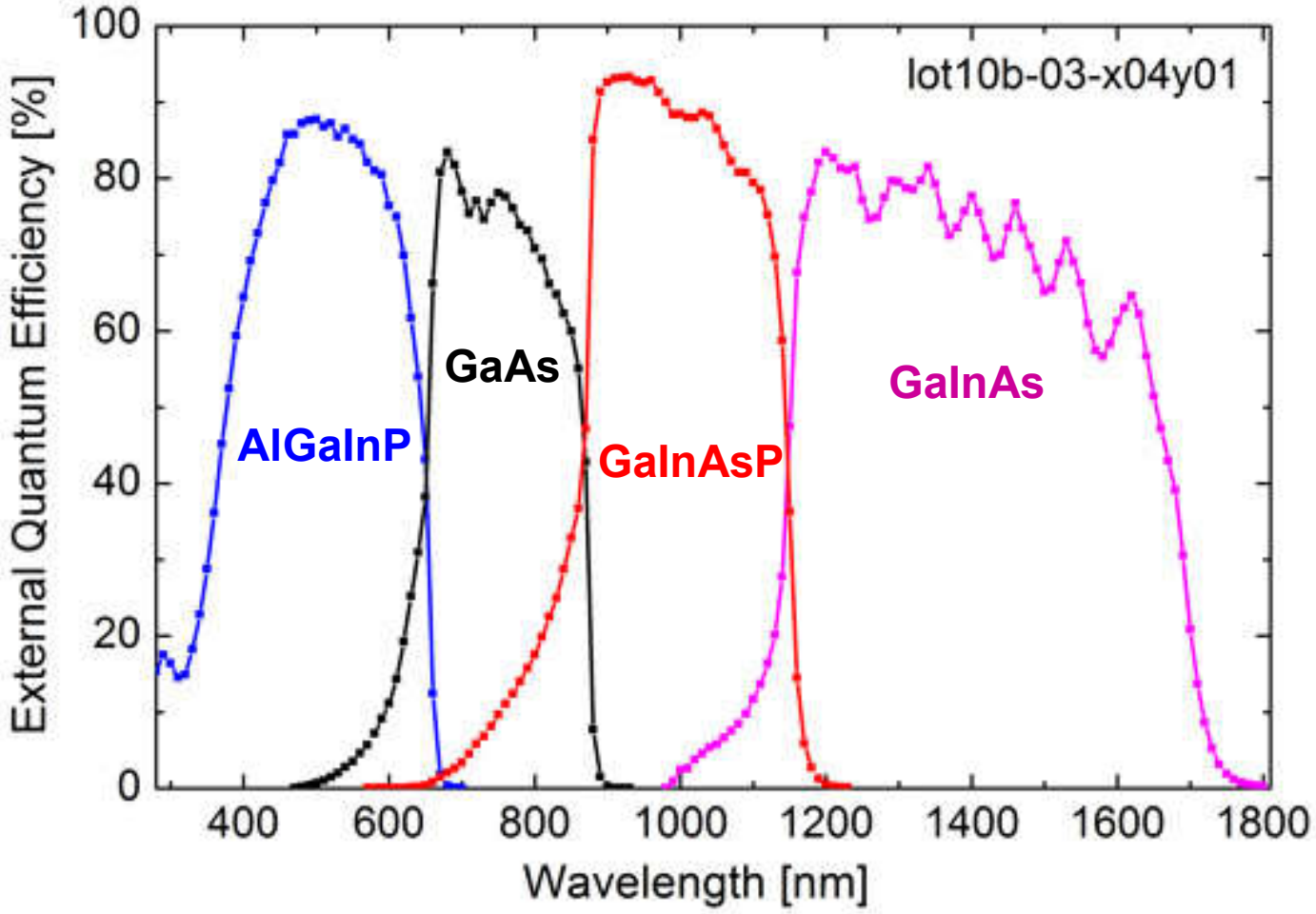
Use the entire solar spectrum

W. Shockley and H. A. Queisser, *J. Appl. Phys.* **32**, 510 (1961)
C. H. Henry, *J. Appl. Phys.* **51**, 4494 (1980)

Stacked MJ Solar Cells

bonded AlGaInP/GaAs // GaInAsP/GaInAs solar cells



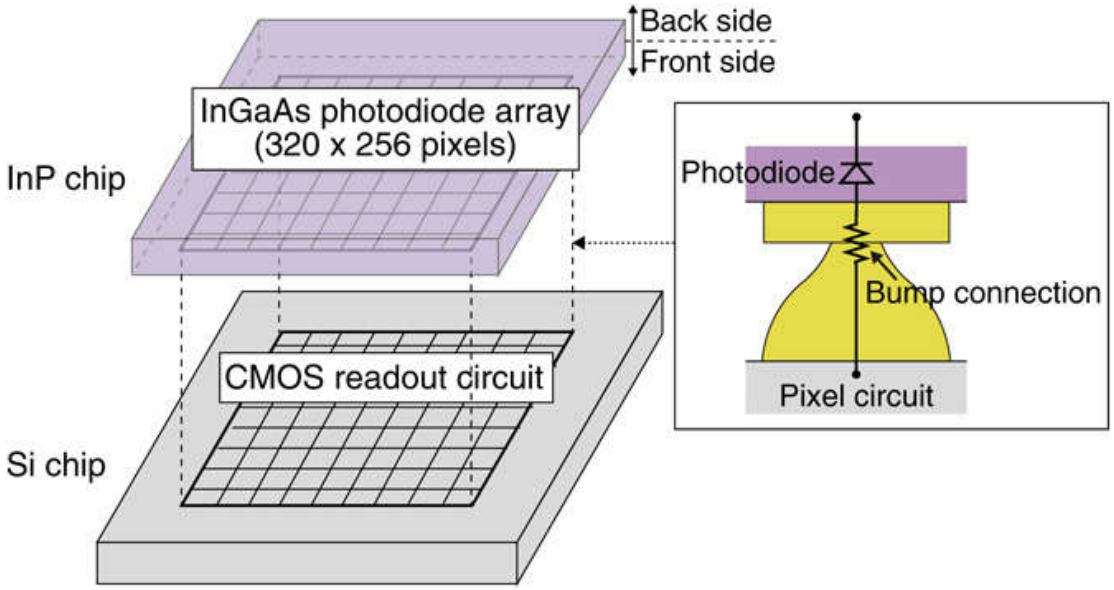


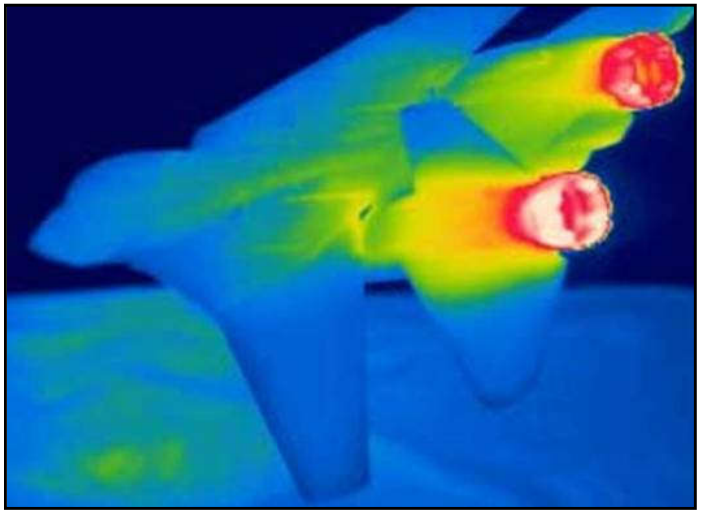
World record efficiency: 46%

F. Dimroth, *et al.*, *IEEE J. Photovolt.* **6**, 343 (2016)

UV and IR Imaging Sensors

- Silicon only absorbs well from 400 nm to 1100 nm
- IR sensors: InGaAs, HgCdTe, ...
- UV sensors: GaN, ...
- sensor arrays bonded with Si circuits



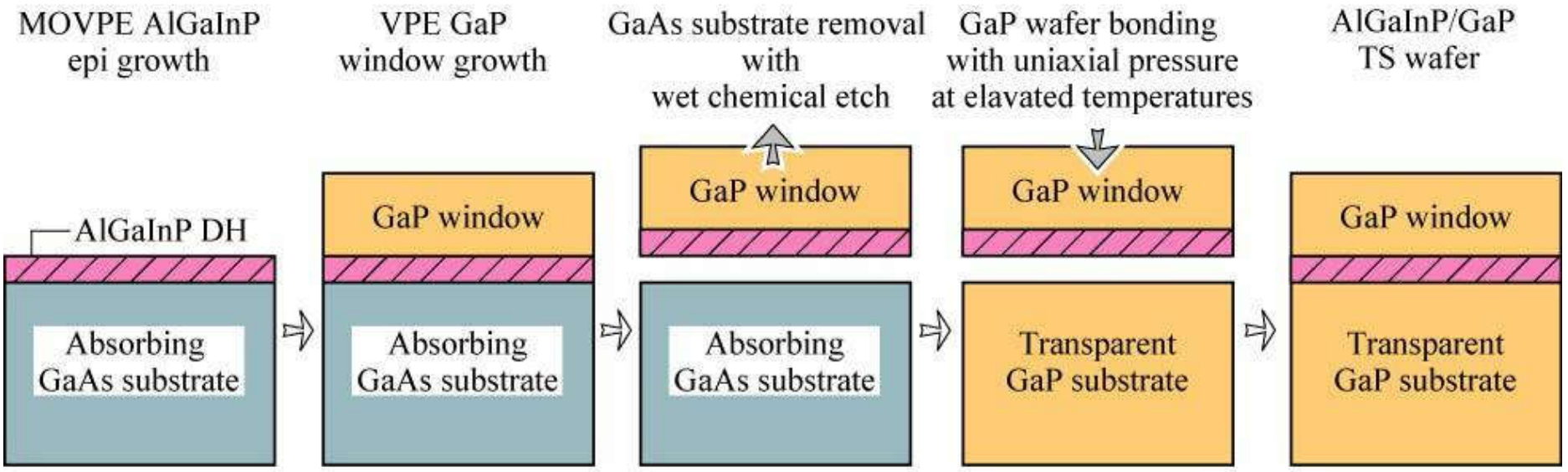


infrared imaging

T. Shuto, *et al.*, *Jpn. J. App. Phys.* **53**, 04EB01 (2014)

Red LEDs

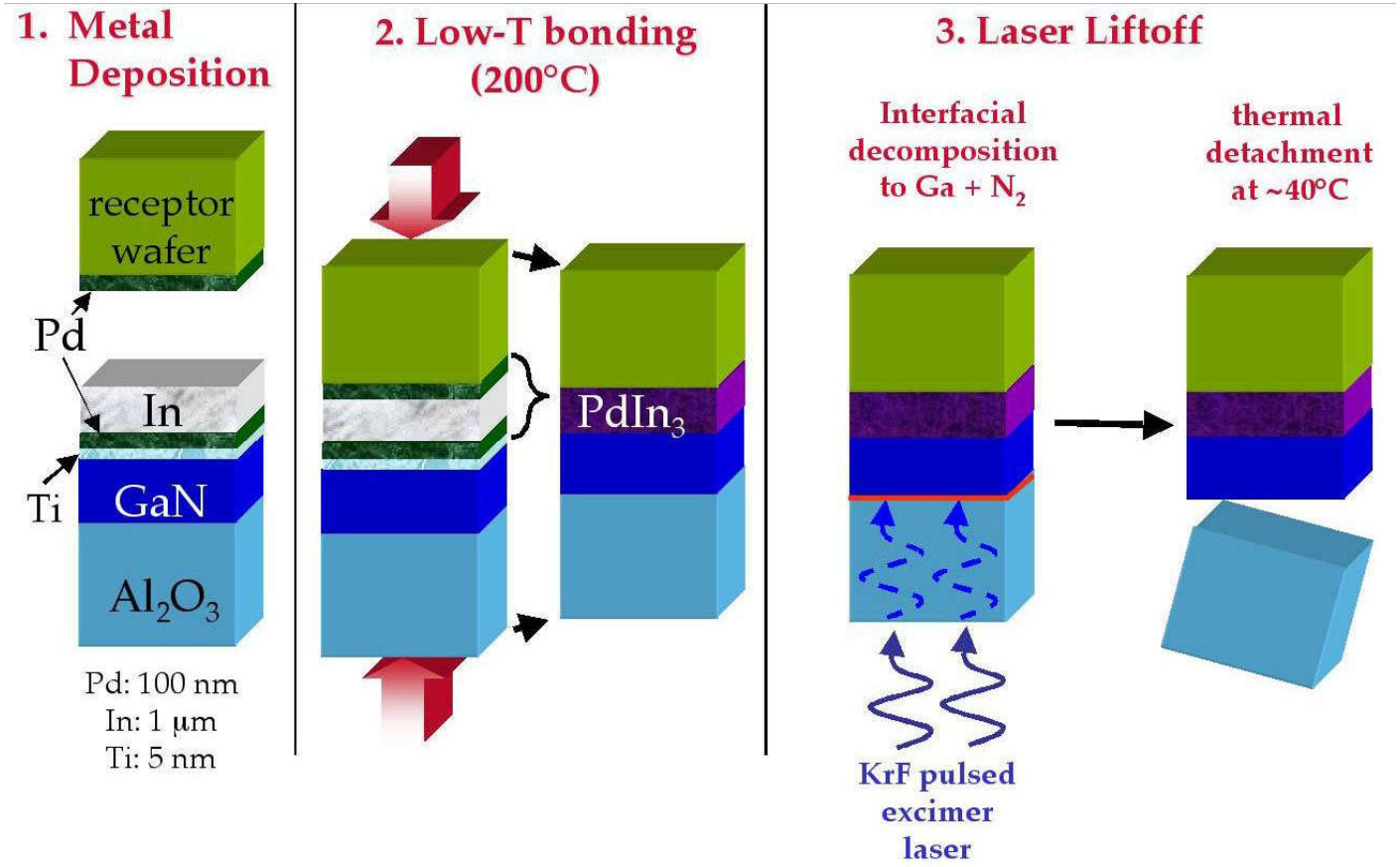
- AlGaInP red LEDs grown on GaAs substrates
- GaAs strongly absorbs red light
- GaP is transparent in red, but not lattice matched
- bond LEDs on GaP, and remove GaAs



F. A. Kish, *et al.*, *App. Phys. Lett.* **64**, 2839 (1994)

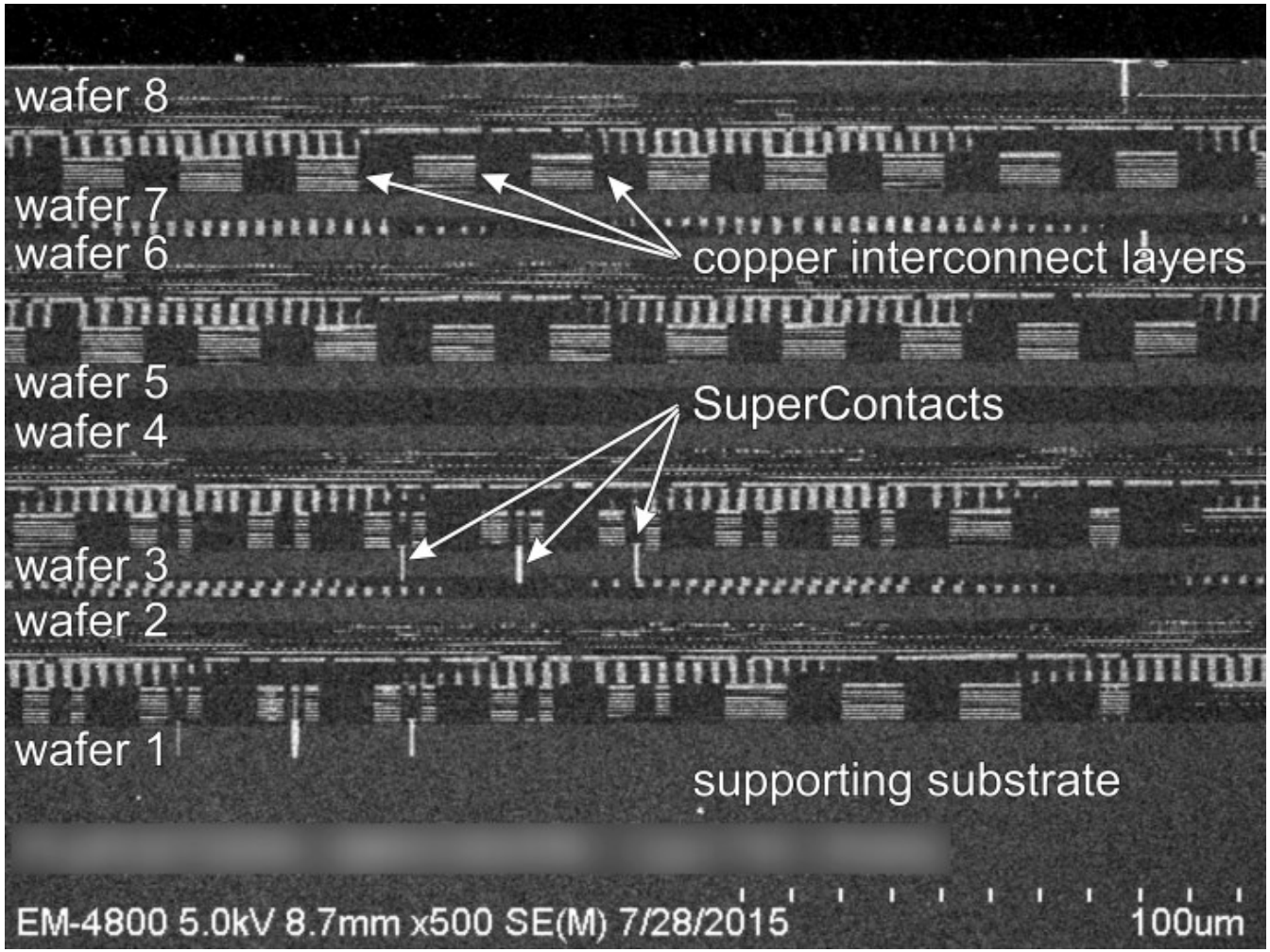
Blue LEDs

- GaN blue LEDs grown on sapphire substrates
- Sapphire is electrically and thermally insulating
- bonded onto a thermally conductive substrate



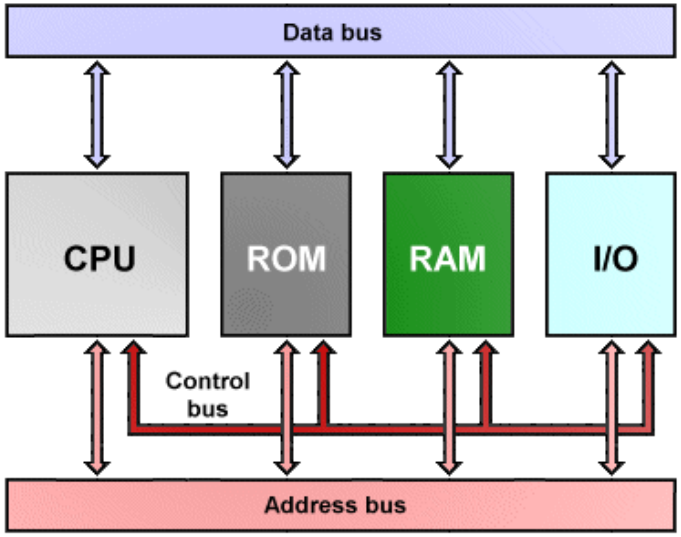
Memory Chips

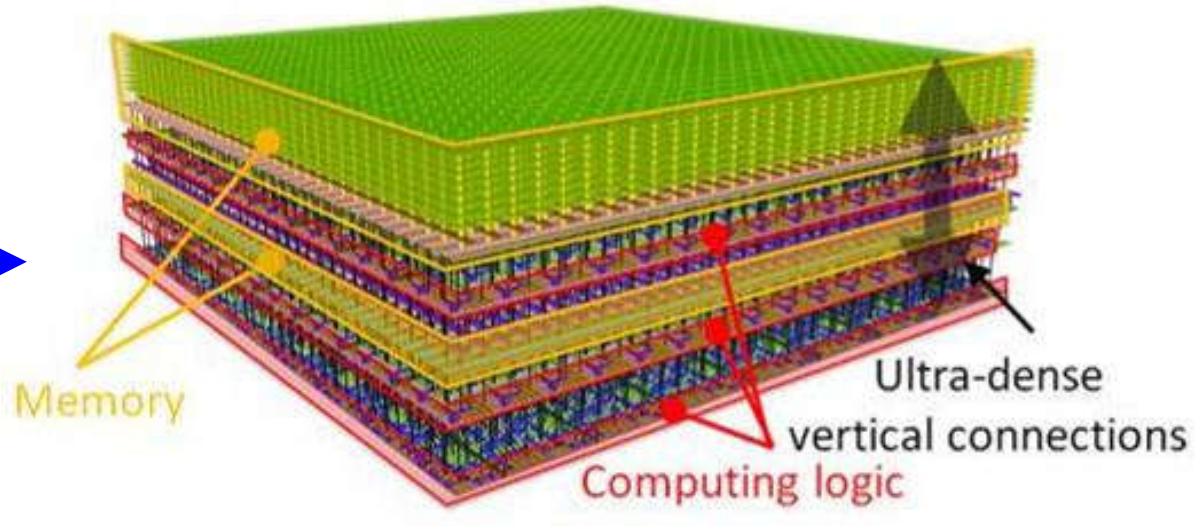
- **Increase the memory volume by 3D chip stacks**



3D IC

- **Logic + Memory + Sensing + ...**





conventional **3D IC**

M. M. Shulaker, *et al.*, *Nature* **547**, 74 (2017)

Thank you for your attention