FIR Synthesis report

1. Detailed RTL Component Information:

   根據作業要求，此次 FIR 運算過程，只使用 1 個 32bis 乘法器和 1 個 32bits 加法器。

```
---------------------------------------------
Detailed RTL Component Info :
+---Adders :
           2 Input   32 Bit       Adders := 2
           2 Input   12 Bit       Adders := 2
           2 Input    4 Bit       Adders := 2
+---Registers :
                     12 Bit    Registers := 1
                      4 Bit    Registers := 1
+---Multipliers :
                     32x32  Multipliers := 1
+---Muxes :
           2 Input   32 Bit        Muxes := 3
          12 Input   32 Bit        Muxes := 4
           2 Input   12 Bit        Muxes := 3
           2 Input    4 Bit        Muxes := 2
          12 Input    4 Bit        Muxes := 2
           2 Input    3 Bit        Muxes := 3
          12 Input    3 Bit        Muxes := 2
           2 Input    2 Bit        Muxes := 2
           2 Input    1 Bit        Muxes := 4
          12 Input    1 Bit        Muxes := 24
           3 Input    1 Bit        Muxes := 1
```

FIR 運算加法器只使用 1 個

2. Cell Usage:

```
Report Cell Usage:
+------+--------+------+
|      |Cell    |Count |
+------+--------+------+
|1     |BUFG    |     9|
|2     |CARRY4  |    29|
|3     |DSP48E1 |     3|
|4     |LUT1    |     5|
|5     |LUT2    |    44|
|6     |LUT3    |    74|
|7     |LUT4    |    47|
|8     |LUT5    |    63|
|9     |LUT6    |    76|
|10    |FDCE    |    15|
|11    |LD      |   240|
|12    |LDC     |    64|
|13    |LDP     |     1|
|14    |IBUF    |   161|
|15    |OBUF    |   169|
+------+--------+------+
```