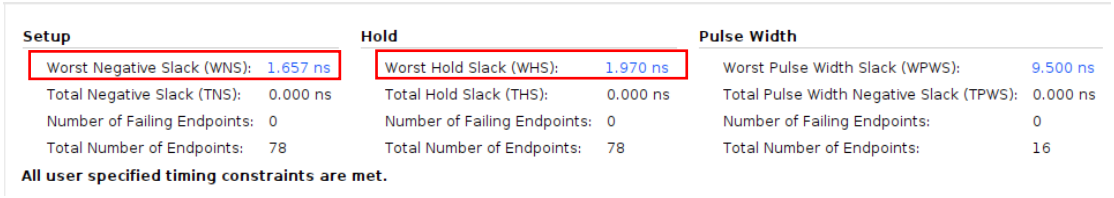
FIR Timing report

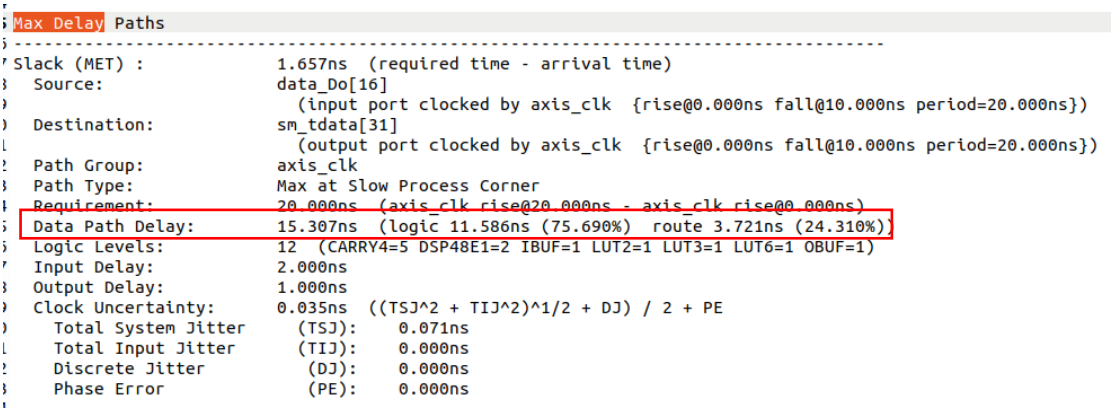
1. Slack & Max delay path

根據 timing report 報告中顯示，可以發現 Data Path Delay 時間為 15.307ns，為我的 Data arrival time，而根據我所設置的 Input delay, Output Delay, Clock Uncertainty 時間分別為 2ns, 1ns, 0.035ns，我給定 clock cycle time 是 20ns，因此我的 Data required time 為 16.965ns(20-2-1-0.035)，因此我整個電路最長路徑的 slack 約為 1.657ns。



Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.657 ns	Worst Hold Slack (WHS):	1.970 ns	Worst Pulse Width Slack (WPWS):	9.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	78	Total Number of Endpoints:	78	Total Number of Endpoints:	16

All user specified timing constraints are met.



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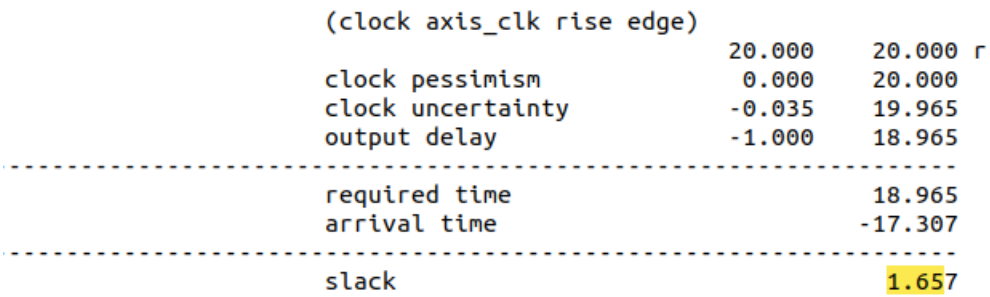
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             1.657ns  (required time - arrival time)
  Source:                 data_Do[16]
                            (input port clocked by axis_clk  {rise@0.000ns fall@10.000ns period=20.000ns})
  Destination:            sm_tdata[31]
                            (output port clocked by axis_clk  {rise@0.000ns fall@10.000ns period=20.000ns})
  Path Group:             axis_clk
  Path Type:              Max at Slow Process Corner
  Requirement:            20.000ns  (axis_clk rise@20.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        15.307ns  (logic 11.586ns (75.690%)  route 3.721ns (24.310%))
  Logic Levels:           12  (CARRY4=5 DSP48E1=2 IBUF=1 LUT2=1 LUT3=1 LUT6=1 OBUF=1)
  Input Delay:            2.000ns
  Output Delay:           1.000ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```



```
                          (clock axis_clk rise edge)
                                                      20.000     20.000 r
                          clock pessimism              0.000     20.000
                          clock uncertainty           -0.035     19.965
                          output delay                -1.000     18.965
-----------------------------------------------------------------------
                          required time                          18.965
                          arrival time                          -17.307
-----------------------------------------------------------------------
                          slack                                   1.657
```

2. 最大頻率

尋找最大操作頻率時，需要先找到最長延遲路徑，從 Timing report 可以發現，FIR 運算會造成相當大的 Delay 且與其他比對後，發現他是最長路徑，因此我們需要把 clock cycle time 提高，從報告可以發現，我的 Data path delay 為 15.307ns，因此最高操作頻率，大概可以落在 62.5MHz。