CS 6110 Project Proposal

Steve Barrus

28th February 2005

Goal

The goal of this project is to verify the correctness of a 32-bit Brent-Kung adder circuit and a 32-bit Ladner-Fischer adder circuit. Both of these adder ciruits are tree adders designed to be fast for adding two numbers together at the expense of size and complexity. Verifying correctness of any 32-bit adder circuit is challenging because there are 2^{64} possible inputs and doing an exhaustive simulation would take an enormous amount of time. Using HOL will make a correctness proof more managable than an exhaustive simulation.

Work Plan

Here is the tenative schedule for work on this project (broken down into sub-goals).

3/3	Model and prove correctness for a simple ripple-carry adder.
3/10	Model and prove correctness for gray, black cells.
3/17	Model a 16-bit Brent-Kung adder.
3/24	Prepare mid-term presentation.
3/31	Prove correctness for 16-bit version of Brent-Kung.
4/7	Extend 16-bit model to 32-bits and prove correctness.
4/14	Model and prove correctness for 32-bit Ladner-Fischer adder.
4/21	Prepare final presentation and final report.
4/26	Project due.

Extensions

If verifying the correctness of these two prefix adders turns out to be too simple, one possible way to extend this project would be to verify more adders like Kogge-Stone, Sklansky, or Han-Carlson. Another way to extend this project would be to include timing. Other characteristics could be included like number of logic levels, maximum fanout, wiring tracks, or total number of cells.

Fall-back

If verifying these two adder proves to be to difficult, the scope of this project can be reduces to only include the 32-bit Brent-Kung adder and not the Ladner-Fischer adder. Also, it could be reduces by verifying 16-bit versions of these two adders.