Ethan Norfleet, WORK LOG

Thursday, February 16, 2023

Finished execute and memory cycle. Wrote load store processor. Revised design document. [8 hours]

Wednesday, February 15, 2023

Finished fetch and decode cycles. Made wires out of each cycle to immediate registers. Put scan of updated datapath diagram into comp arch working document. [4 hours]

Sunday, February 12, 2023

Finished 2-way and 4-way mux testing. [2 hours]

Saturday, February 11, 2023

Fixed bugs and compile test problems. Completed imgen tests. [3 hours]

Friday, February 10, 2023

Worked on issues with compiler and modelsim. [2 hours]

Wednesday, February 8, 2023

I wrote testing plan tables for the wri and rea instructions in our design document. I also created a Verilog program to test the 4-way MUX. [50 minutes]

Monday, February 6, 2023

I wrote testing plan tables for the add, grt, sub, eq, jalr, lui, jal, addi, lw, sw, and bne instructions in our design document. [50 minutes]

Milestone 4 Work:

Monday, January 31, 2023

We looked over each other's work on the tasks that we were assigned and made any changes to problems that were noticed. [50 minutes]

Saturday, January 28, 2023

We worked on improving some of the unit tests and implementing some of the components. We assigned tasks for each team member to complete by next meeting. My tasks were to review and edit the data path, to create new unit tests for the ALU component, and to implement the Im Gen component. [1 hour]

Milestone 3 Work:

Wednesday, January 25, 2023

We looked over each other's work on the tasks that we were assigned and made any changes to problems that were noticed. [40 minutes]

Sunday, January 22, 2023

We created handwritten sketches of a block diagram of our datapath. We assigned tasks for each team at the meeting to complete by the next meeting My task was to create unit tests for the logic components. [2 hours]

Milestone 2 Work:

Wednesday, January 18, 2023

We determined naming conventions as a group. We made up conventions that were consistent across similar components and made the use of a particular instance of a component clear. We also made a table of component specifications as a group. [1 hour]

Monday, January 16, 2023

We looked over the RTLs each team member had created and revised them if any improvements were necessary. [30 minutes]

Sunday, January 15, 2023

We created RTL for the R-type instructions, jalr, and jal as a group. We assigned tasks for each team member at the meeting to complete by the next meeting. My task was to create RTL for the bne, wri, and rea. [1 hour and 10 minutes]

Milestone 1 Work:

Friday, January 11, 2023

We translated our Assembly RelPrime and GCD code into machine code. We also added read and write to the machine language instruction table and wrote the assembly code for reading from input port and writing to output port in the assembly code for common operations section of our design document. [60 minutes]

Sunday, January 8, 2023

We decided to build a load-based processor. We worked on and mostly completed the body of our design document. We decided on tasks that each team member before our next meeting, which we agreed would be after lab on Wednesday, January 11. My task was translating the high-level code of the GCD method from Moodle into the assembly language we are making. [2 hours and 30 minutes]

Friday, January 6, 2023

We set up our Git repository and cloned local copies to our computers. We also created a title page and an outline for the body of our design document. [35 minutes]