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Junctionless Ge p-Channel Metal–Oxide–Semiconductor Field-Effect Transistors Fabricated on Ultrathin Ge-on-Insulator Substrate

Dan Dan Zhao[1,2,3*], Tomonori Nishimura[1,2], Choong Hyun Lee[1,2], Kosuke Nagashio[1,2], Koji Kita[1,2], and Akira Toriumi[1,2]

[1]*Department of Materials Engineering, The University of Tokyo, Bunkyo, Tokyo 113-8656, Japan*
[2]*CREST, Japan Science and Technology Agency (JST), Bunkyo, Tokyo 113-8656, Japan*
[3]*College of Nuclear Science and Technology, Beijing Normal University, Beijing 100875, P. R. China*

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A junctionless field-effect transistor (FET) has been proposed using a Si nanowire FET. It avoids the junction formation process and shows less sensitivity to the channel interface. We discuss the junctionless FET on a Ge-on-insulator substrate, which combines the higher mobility in Ge than in Si with all the advantages of a junctionless FET. The device shows similar current–voltage (I–V) characteristics to conventional FETs, and the on/off current (I_{on}/I_{off}) ratio is larger than 10^4. The field-effect mobility seems to be rather flat with regard to the carrier density.

In the field of microelectronics, new materials and new device architectures are required in order to continue Moore's law. Germanium (Ge), with its intrinsically better transport properties, lower dopant activation temperature, and narrower band gap (hence lower supply voltage and power dissipation),[1,2] is gaining much attention for further device scaling. Ge-on-insulator (GeOI), which combines the higher carrier mobility in Ge than in Si with better electrostatic channel control of fully depleted metal–oxide–semiconductor field-effect transistor (MOSFET) technology, has been recently investigated in terms of the performance and scalability of Ge p-MOSFETs.[3–10]

Junctionless FETs using Si nanowire FETs on Si-on-insulator (SOI) substrates have been very recently reported.[11] Compared with conventional FETs, the junctionless FETs have advantages that no source/drain (S/D) formation is needed and carrier transport is less sensitive to the channel interface. However, the junctionless FETs fabricated on heavily doped SOI have shown a comparatively low mobility. Considering the advantage of Ge over Si in terms of carrier mobility, we expect that the junctionless FETs fabricated on GeOI will show better performance. Thus, this paper discusses junctionless FETs fabricated on a GeOI substrate. The current–voltage (I–V) characteristics and the field-effect mobility are investigated. The opportunities and prospects for this device are also discussed.

A heavily doped p-type GeOI wafer with ~100-nm-thick buried SiO_2 was used. From secondary ion mass spectroscopy (SIMS) analysis, the substrate-doping concentration was around $10^{19}\,cm^{-3}$. First, Ge was thinned by a careful wet etching process. The final thicknesses of Ge were about 11.2, 14.2, 19.7, 29.8, and 94.5 nm, which were determined by the spectroscopic ellipsometry. Next, mesa-type Ge islands were defined by wet etching. After a methanol and HCl cleaning process, Ni was deposited by e-beam evaporation and then was patterned by the lift-off process, followed by annealing at 400 °C for 5 min in N_2 ambient. Finally, Al was deposited as the back-gate electrode.

Figure 1 shows a schematic perspective of the junctionless Ge MOSFET structure studied in this work. NiGe was used for the S/D electrodes. X-ray diffraction patterns for as-deposited and annealed Ni/GeOI samples are shown in Fig. 2. The initial Ni thickness was 48 nm, which was determined by

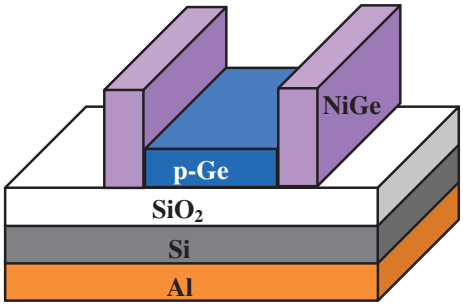

Fig. 1. A schematic perspective of the junctionless Ge MOSFET structure.

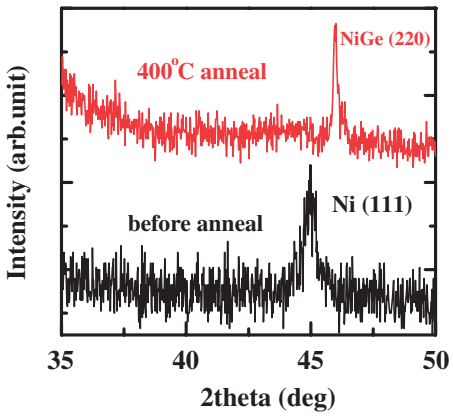

Fig. 2. X-ray diffraction spectra for both as-deposited and annealed Ni/GeOI samples. The 48 nm Ni completely reacted with Ge, and NiGe was formed after annealing.

grazing incidence X-ray reflectometry (GIXR). The initial Ni (111) peak at $2\theta = 45°$ completely disappeared after annealing the sample in N_2 ambient at 400 °C for 5 min, indicating a complete reaction of the Ni film with Ge. A sharp peak at $2\theta = 46°$ was observed after annealing, and the peak was identified as NiGe (220),[12] which indicates that NiGe S/D electrodes were formed after annealing.

The I–V characteristics of junctionless Ge p-MOSFETs with various Ge thicknesses at drain voltage (V_{ds}) of −10 mV are shown in Fig. 3. The channel length (L) is fixed at 100 μm. The drain current (I_{ds}) is normalized by the channel width (W). When the Ge thickness is 94.5 nm, the back-gate voltage (V_{gs}) seems to have no effect on the drain current. As the Ge thickness is decreased to thinner than 30 nm, the drain

*E-mail address: ddzhao@adam.t.u-tokyo.ac.jp

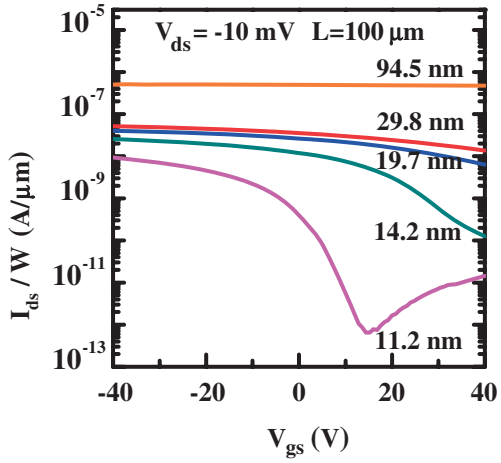

Fig. 3. The current–voltage characteristics of the junctionless Ge p-MOSFETs with various Ge thicknesses. Drain current vs gate voltage for drain voltage of −10 mV. All devices were fabricated on heavily doped substrates and had the same channel length of 100 μm. The on current is normalized by the channel width. The on/off current ratio for the thinnest GeOI device between $V_{gs} = -40$ and 40 V is larger than 10^4.

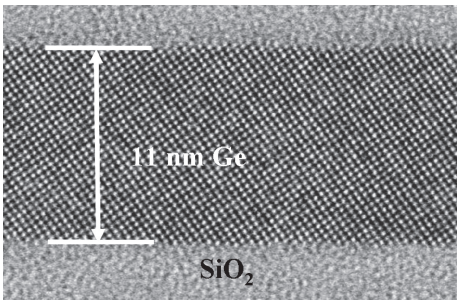

Fig. 4. A transmission electron microscopy image of the thinnest GeOI, which indicates that the Ge thickness is only 11 nm and that good crystalline quality is maintained after the thinning process.

current is modulated by the back-gate voltage. Figure 4 is a cross-sectional transmission electron microscopy (TEM) image of the thinnest GeOI, which indicates that the Ge thickness is only 11 nm and still has good crystalline quality after the thinning process. The on/off current (I_{on}/I_{off}) ratio of the device on the 11 nm GeOI is larger than 10^4 between $V_{gs} = -40$ and 40 V. In the junctionless MOSFET, carriers are located inside the Ge film, and the channel is a resistor without the gate voltage. By applying a negative gate voltage, a hole accumulation layer is formed at the interface and majority carriers (holes) flow both at the interface and in the bulk. When a positive gate voltage is applied, holes are electrostatically depleted, and drain current decreases. Therefore, the depletion layer width is a critical parameter for the junctionless FET to achieve the off-state. By assuming a simple depletion layer, the relationship between the maximum depletion layer width W_m and the impurity concentration N_B can be approximated as

$$W_m = \sqrt{\frac{4\varepsilon_s kT \ln(N_B/n_i)}{q^2 N_B}}, \tag{1}$$

where k, q, ε_s, n_i are the Boltzmann constant, the elementary charge, the permittivity of the semiconductor, and the intrinsic carrier concentration of the semiconductor, respectively.[1)] The maximum depletion layer width of Ge with an impurity concentration of 10^{19} cm^{-3} is estimated to be about 11 nm considering the dielectric constant and intrinsic carrier concentration of Ge to be 16.0 and 2.4×10^{13} cm^{-3} at room temperature, respectively. Thus, by reducing the Ge thickness to thinner than its maximum depletion layer width so as to fully deplete the channel of carriers, we could successfully turn off the device.

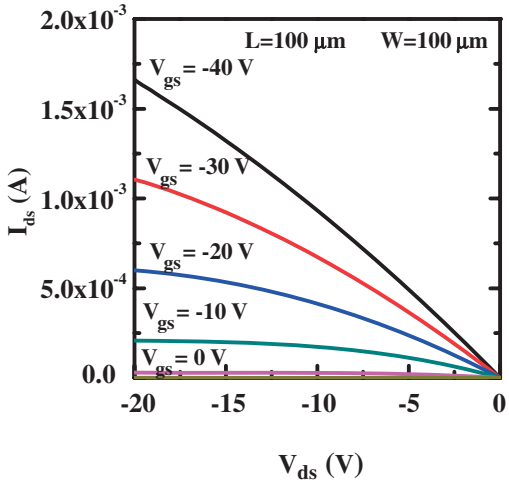

Fig. 5. Output characteristics of the Ge junctionless p-MOSFET fabricated on 11-nm-thick heavily doped GeOI substrate. These characteristics are quite similar to those of conventional MOSFETs. The channel length and width are both 100 μm.

The output characteristics of the 11-nm-thick Ge junctionless FET are shown in Fig. 5. The channel length and width are both 100 μm. The drain current first increases linearly with the drain voltage, and then gradually approaches a saturated value. These characteristics are quite similar to those of conventional MOSFETs.

The field effect mobility μ_{eff} of a MOSFET with channel length L and width W can be expressed as

$$\mu_{eff} = \frac{L}{W}\frac{I_{ds}}{V_{ds}}\frac{1}{Q}, \tag{2}$$

where Q is the channel charge density (C/cm^2), and can be determined from the gate-to-channel capacitance/unit area, C_{gc}, according to

$$Q = qN_s = \int_{-\infty}^{V_{gs}} C_{gc}\, dV_{gs}. \tag{3}$$

Then C_{gc} is measured using the following equation

$$\frac{1}{C_{gc}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}, \tag{4}$$

where C_{ox} and C_{dep} are the oxide capacitance and depletion layer capacitance.

In the present 11-nm-thick Ge junctionless FET, the capacitance of SiO_2 is much smaller than the depletion layer capacitance, so carrier density N_s can be approximated by

$$N_s = \frac{Q}{q} = C_{ox}\frac{V_{gs} - V_{th}}{q}. \tag{5}$$

Here, V_{th} is the threshold voltage and was estimated from the transconductance–gate voltage (g_m–V_{gs}) characteristics. C_{ox}

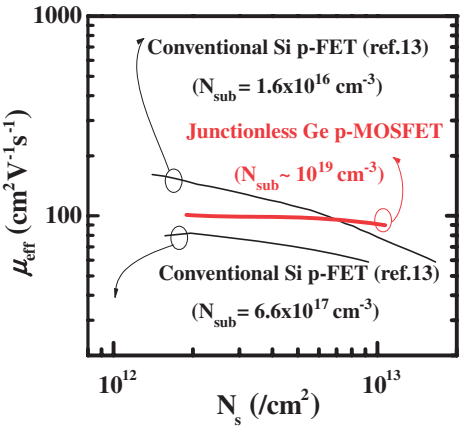

Fig. 6. Mobility of the junctionless Ge p-MOSFET fabricated on 11-nm-thick heavily doped GeOI substrate. The mobility of junctionless Ge p-MOSFET at $N_{sub} \sim 10^{19}\,cm^{-3}$ is around $100\,cm^2 \cdot V^{-1} \cdot s^{-1}$ and is higher than conventional Si MOSFET mobility at $N_{sub} = 6.6 \times 10^{17}\,cm^{-3}$. In addition, the mobility seems to be rather flat with regard to the carrier density N_s.

was estimated from the saturated capacitance–voltage (C–V) curve between the back-gate and S/D electrodes in the negative bias condition. The parasitic capacitance was well subtracted by using two devices with different gate lengths, and C_{ox} was estimated to be $3.6 \times 10^{-8}\,F/cm^2$. Using eqs. (2) and (5), we estimated the hole mobility as shown in Fig. 6. The hole mobility of conventional Si p-MOSFETs with different substrate doping concentration[13] are also shown for comparison. The mobility of the 11-nm-thick Ge junctionless p-FET at $N_{sub} \sim 10^{19}\,cm^{-3}$ is around $100\,cm^2 \cdot V^{-1} \cdot s^{-1}$ and is higher than conventional Si p-FET mobility at $N_{sub} = 6.6 \times 10^{17}\,cm^{-3}$. In addition, the mobility seems to be rather flat with regard to the carrier density, N_s. In conventional inversion-mode MOSFETs, the minority carriers are accumulated at the semiconductor/insulator interface, and they are necessarily scattered by the interface roughness and/or by charges trapped in the insulator or at the interface. As N_s increases, the scattering events also increase, thus the carrier mobility decreases. In the junctionless Ge MOSFETs, however, majority carriers are located inside the Ge film, and are comparatively less sensitive to the interface. When the device is turned on, the whole Ge film acts as the channel like a resistor, thus, the mobility is comparatively independent of the carrier density and close to the mobility in bulk Ge. The mobility of holes in heavily doped ($\sim 10^{19}\,cm^{-3}$) p-type bulk Ge is about $100\,cm^2 \cdot V^{-1} \cdot s^{-1}$, which is much higher than that in Si ($40\,cm^2 \cdot V^{-1} \cdot s^{-1}$). It is worth while mentioning that the electron mobility in bulk n-Ge ($1000\,cm^2 \cdot V^{-1} \cdot s^{-1}$) is one order higher than that in n-Si ($100\,cm^2 \cdot V^{-1} \cdot s^{-1}$) with $N_{sub} \sim 10^{19}\,cm^{-3}$.[1)] Thus, junctionless MOSFETs in Ge will be much more promising than those in Si.

The key challenge of the junctionless FETs is to make the ultrathin Ge film, because the most important point is to deplete majority carriers in the heavily doped channel for the off-state. In the case of Si junctionless MOSFETs, a high-impurity-concentration channel is needed to make the ohmic contact, while in the case of Ge, all metals on p-Ge show the ohmic contact property, since the Fermi level at the metal/Ge interface is strongly pinned near the valence band edge of Ge.[14)] Thus, it is worth mentioning that the contact resistance in junctionless Ge p-MOSFETs has particularly high flexibility against unexpected doping density decrease in Ge. Furthermore, this fact means that a lightly doped thin Ge film on insulator will be usable for p-type junctionless FETs instead of a heavily doped Ge wire on insulator. In fact, junctionless Ge p-MOSFETs using lightly n-doped ($\sim 10^{14}\,cm^{-3}$) GeOI substrates have been preliminarily reported.[15,16)] The details will be reported elsewhere.

In summary, we have proposed and demonstrated junctionless Ge p-MOSFETs on an ultrathin GeOI. The higher carrier mobility in Ge than in Si suggests that Ge will be more appropriate for junctionless MOSFETs. In particular, lightly doped GeOI substrates can also be used for junctionless p-MOSFETs thanks to the strong Fermi level pinning at the metal/Ge contact. This is another advantage of Ge junctionless p-MOSFETs over Si ones. We think that such devices will surmount the performance limit of Si MOSFETs.

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