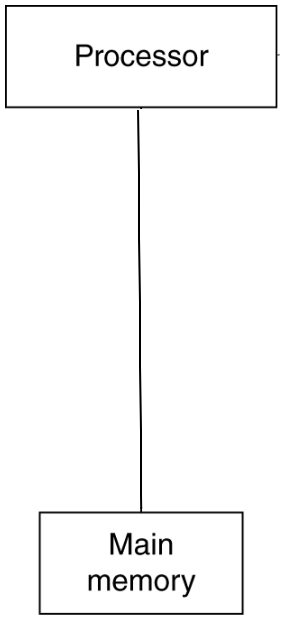
Topic V22

Input/Output Devices

Reading: (Section 6.9)

Storage and I/O

I/O connections



Storage and I/O

I/O connections

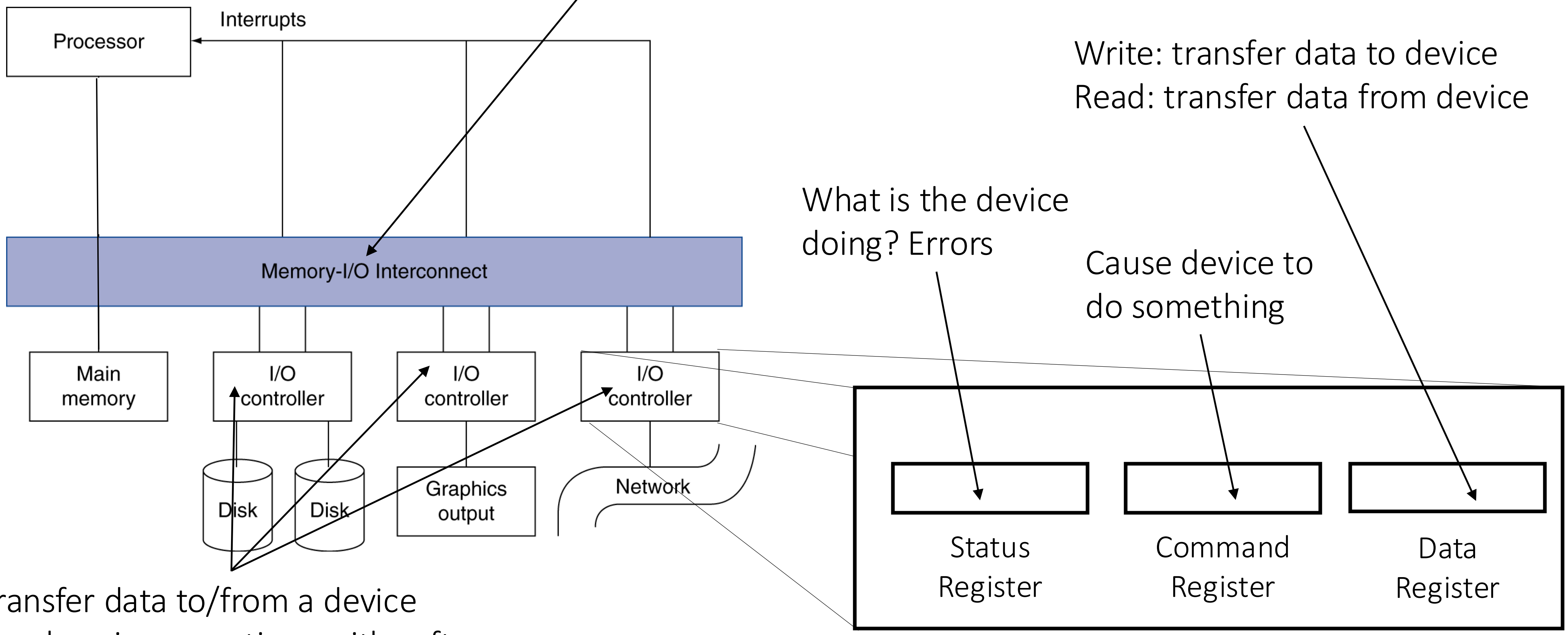
Interconnect an be a “bus”

- a “bus” set of parallel wires
- a pair of “serial” wires
- an interconnect switch

Write: transfer data to device
Read: transfer data from device

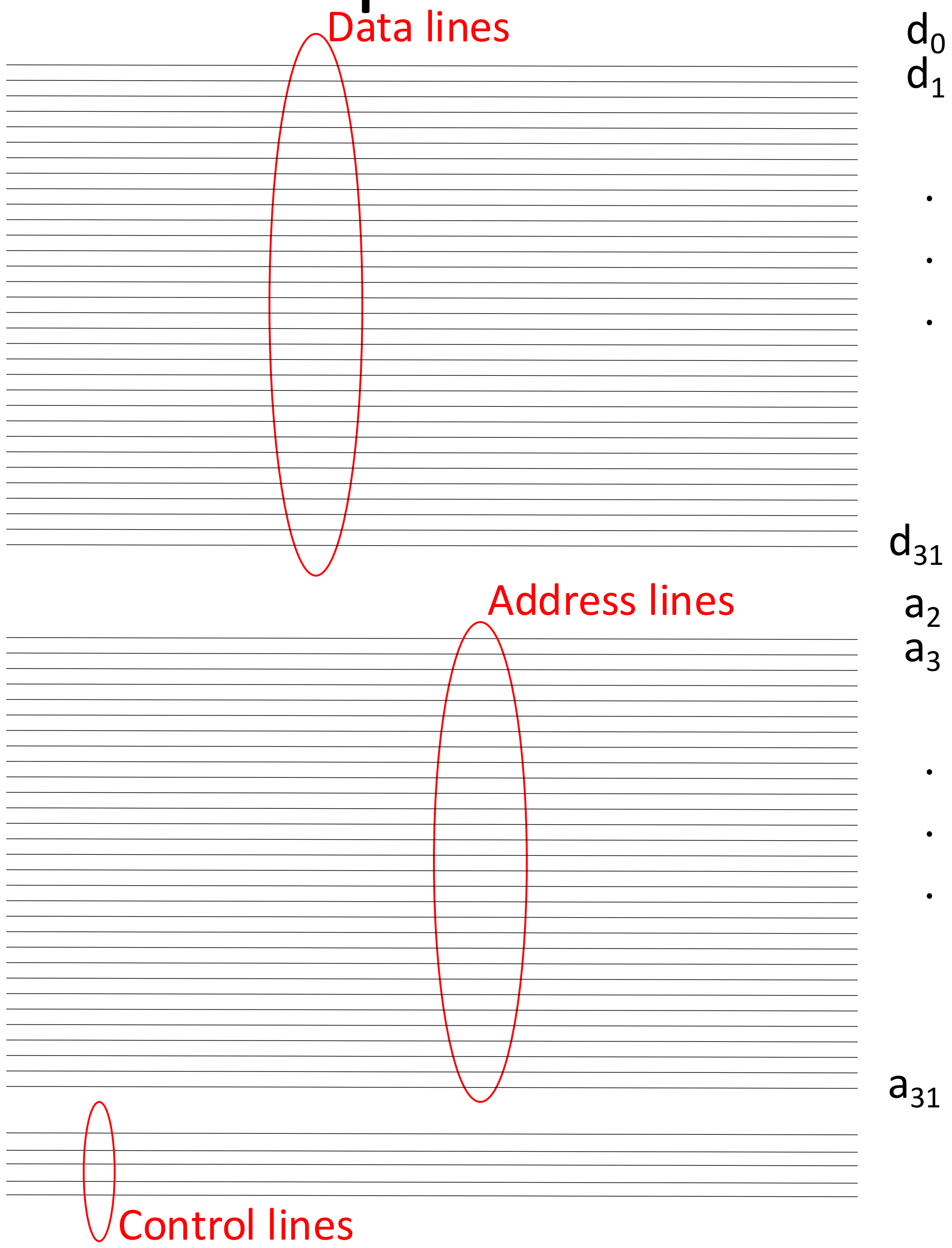
What is the device doing? Errors

Cause device to do something



- Transfer data to/from a device
- Synchronize operations with software

What is a parallel bus?



Memory Mapped I/O × I/O Instructions

Memory mapped I/O

Use a memory address to access an I/O register

Address decoder captures I/O accesses

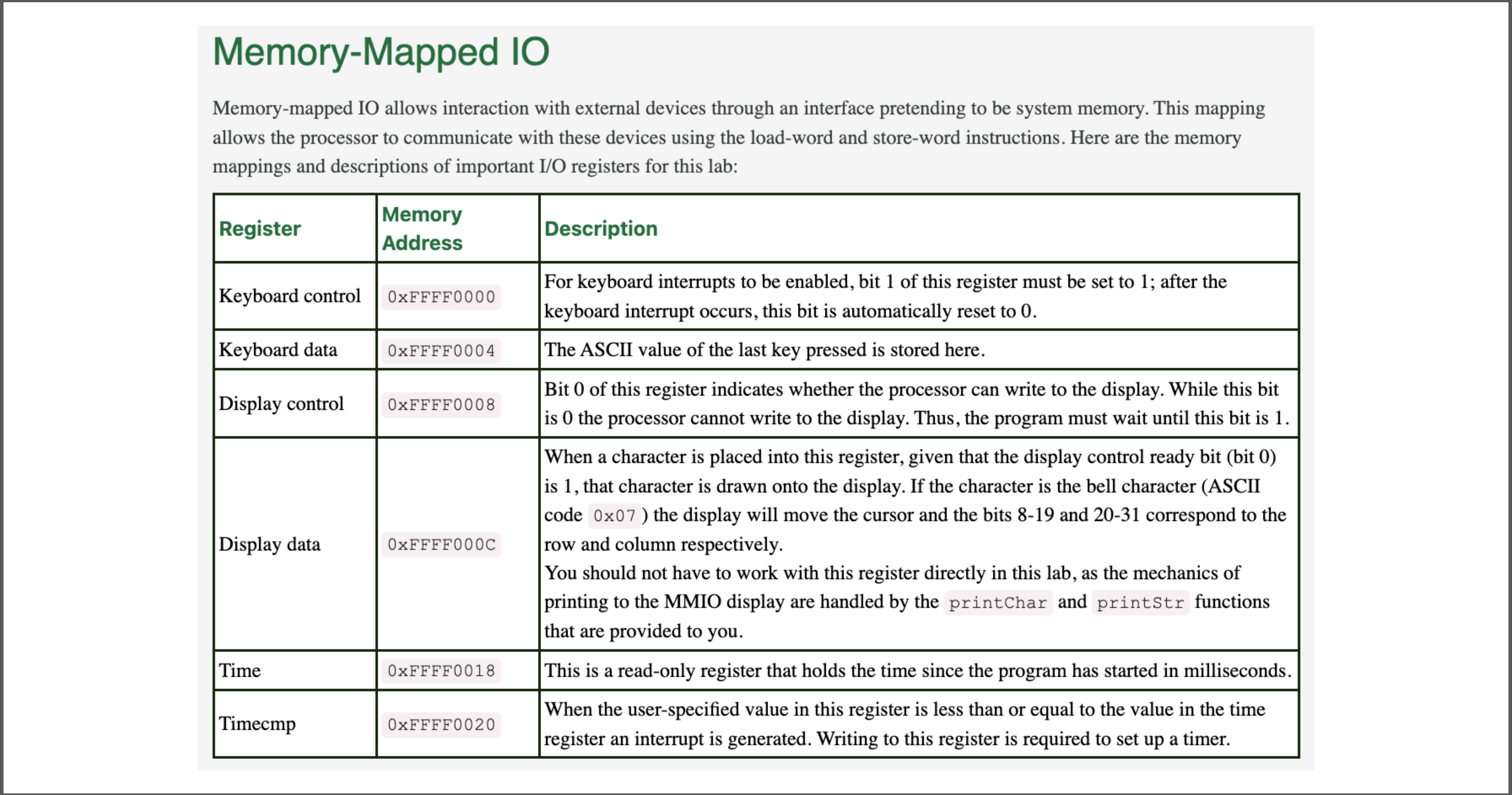
OS ensures that I/O-mapped addresses are only accessible to kernel

I/O instructions

Separate instructions to access I/O registers

Can only be executed in kernel mode

Example: x86



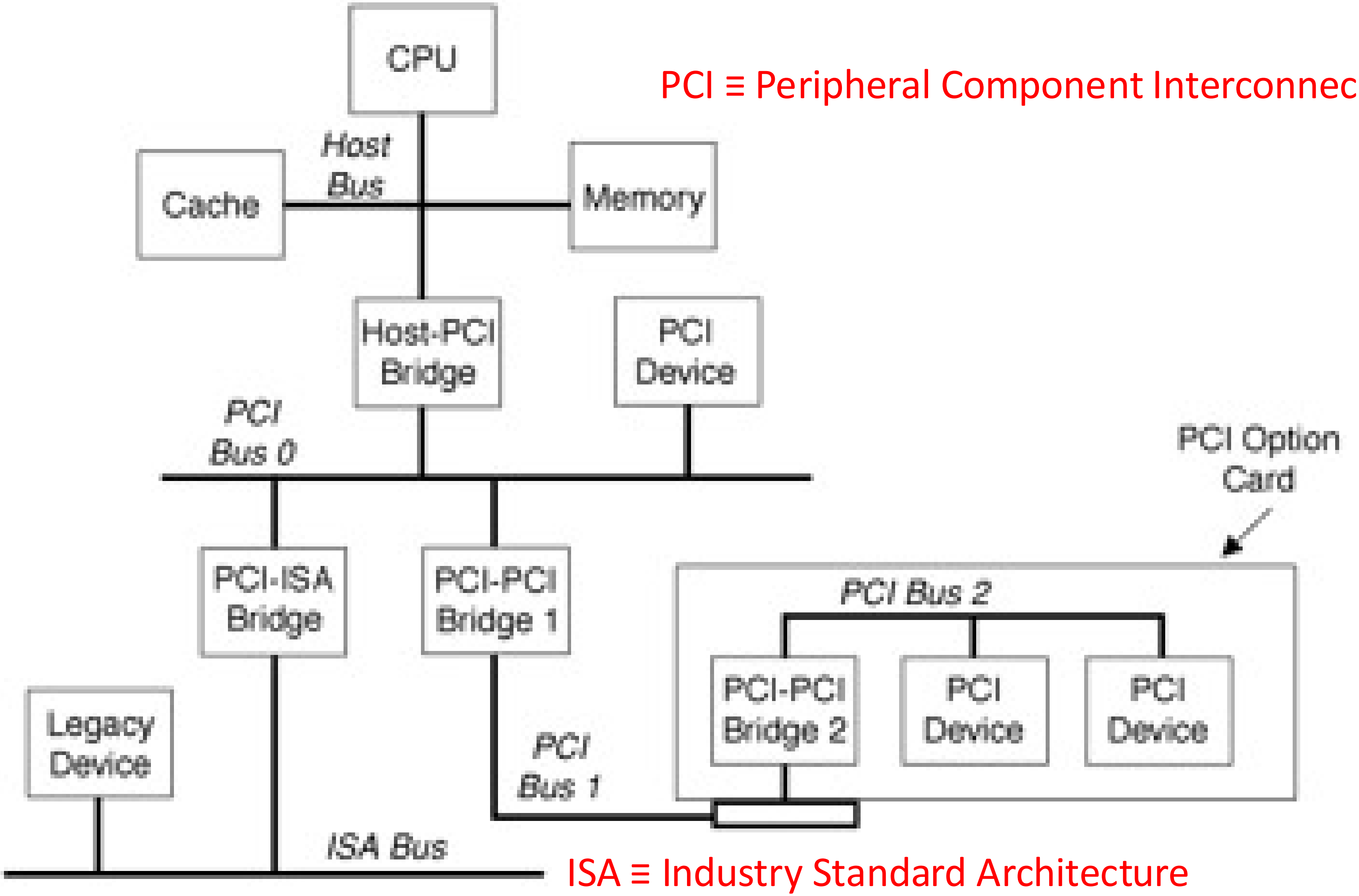
Memory-Mapped IO

Memory-mapped IO allows interaction with external devices through an interface pretending to be system memory. This mapping allows the processor to communicate with these devices using the load-word and store-word instructions. Here are the memory mappings and descriptions of important I/O registers for this lab:

Register	Memory Address	Description
Keyboard control	`0xFFFF0000`	For keyboard interrupts to be enabled, bit 1 of this register must be set to 1; after the keyboard interrupt occurs, this bit is automatically reset to 0.
Keyboard data	`0xFFFF0004`	The ASCII value of the last key pressed is stored here.
Display control	`0xFFFF0008`	Bit 0 of this register indicates whether the processor can write to the display. While this bit is 0 the processor cannot write to the display. Thus, the program must wait until this bit is 1.
Display data	`0xFFFF000C`	When a character is placed into this register, given that the display control ready bit (bit 0) is 1, that character is drawn onto the display. If the character is the bell character (ASCII code `0x07`) the display will move the cursor and the bits 8-19 and 20-31 correspond to the row and column respectively. You should not have to work with this register directly in this lab, as the mechanics of printing to the MMIO display are handled by the `printChar` and `printStr` functions that are provided to you.
Time	`0xFFFF0018`	This is a read-only register that holds the time since the program has started in milliseconds.
Timecmp	`0xFFFF0020`	When the user-specified value in this register is less than or equal to the value in the time register an interrupt is generated. Writing to this register is required to set up a timer.

Processor-Memory Bus × I/O buses

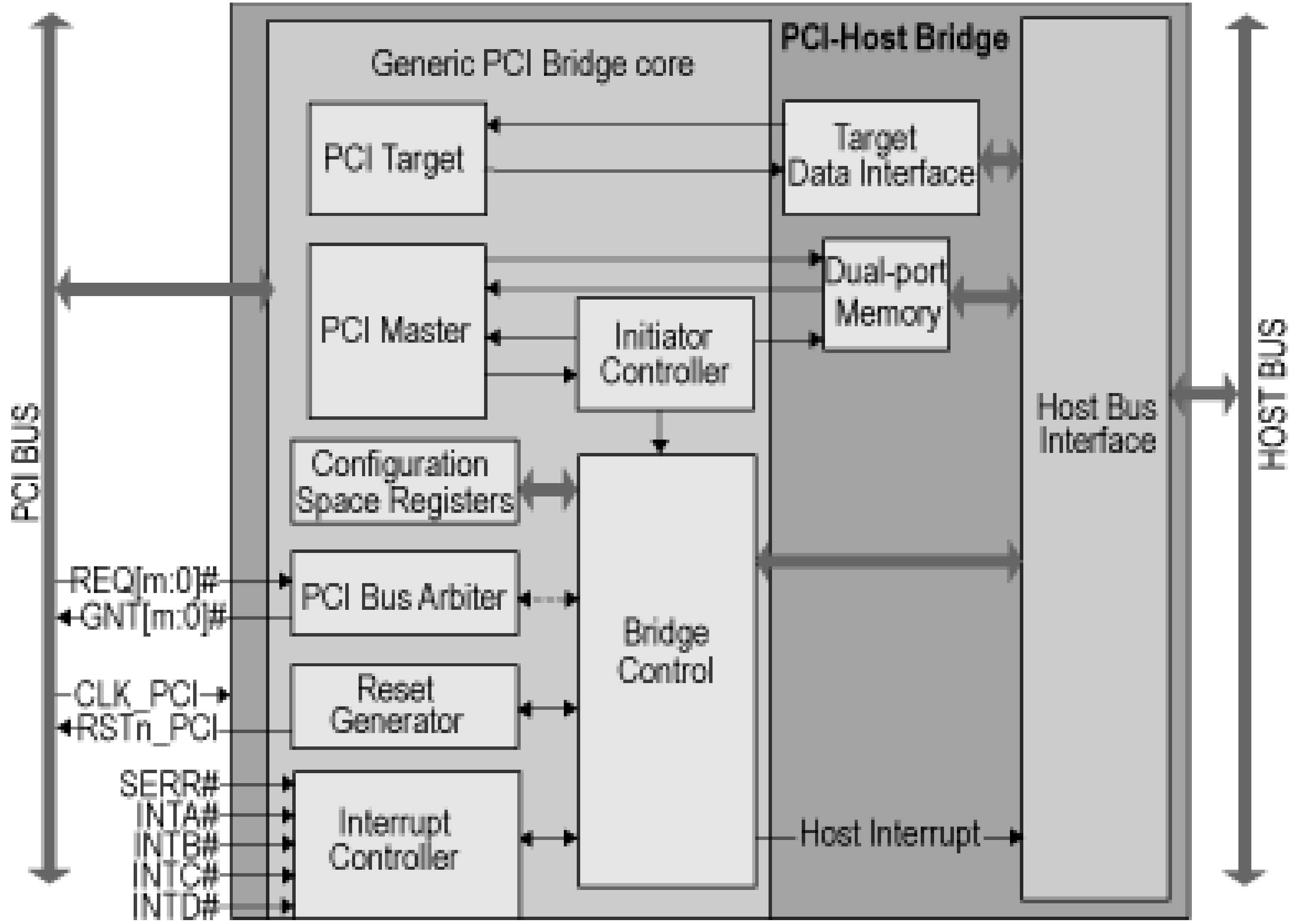
PCI ≡ Peripheral Component Interconnect



ISA ≡ Industry Standard Architecture

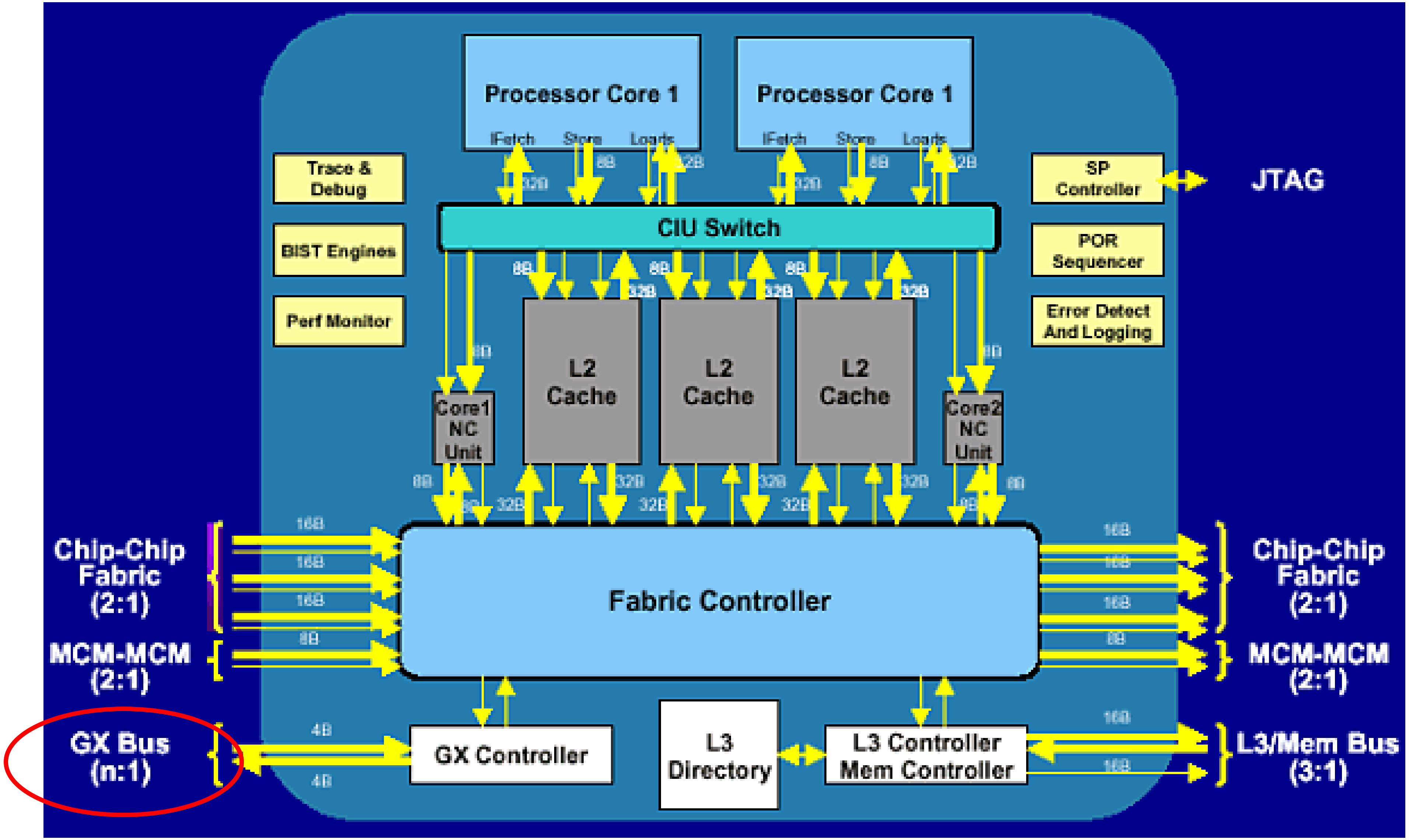
Doug Abbott, PCI Bus Demystified, Second Edition

A PCI-Host Bridge



http://www.cast-inc.com/ip-cores/interfaces/pci-hb/

The IBM POWER4 Interconnections



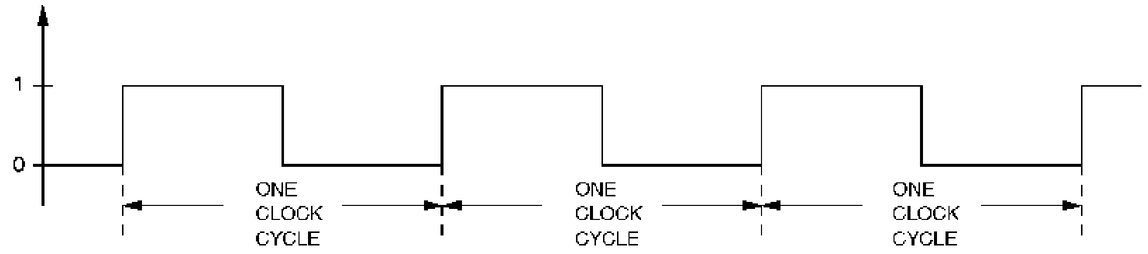
I/O Bus

http://ixbtlabs.com/articles/ibmpower4/

Bus Synchronization

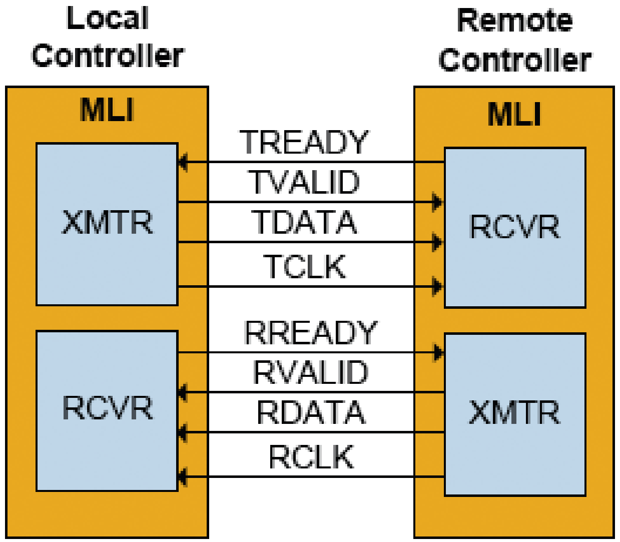
Synchronous

Uses a bus clock



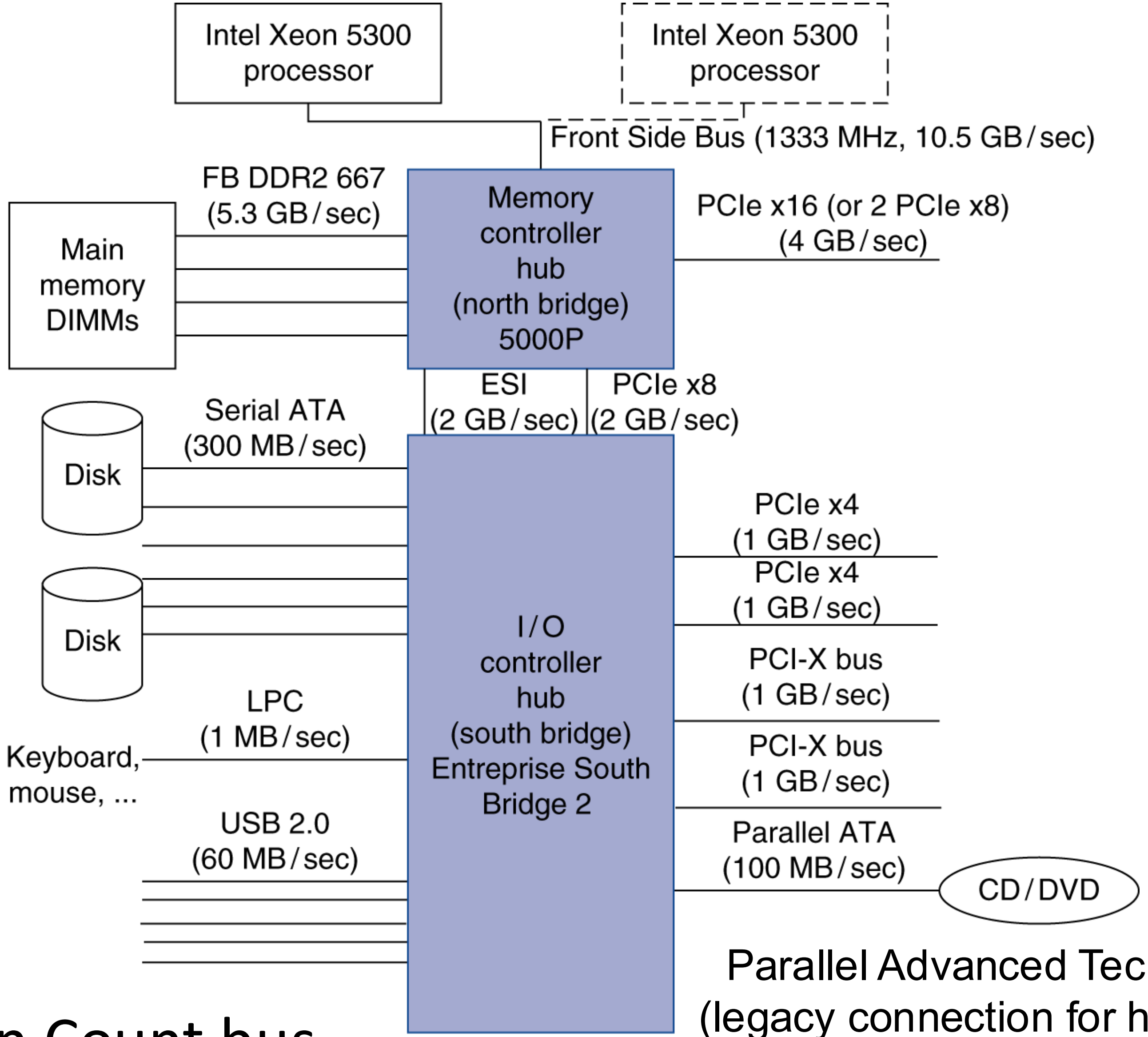
Asynchronous

Uses request/acknowledge control lines for handshaking



Typical x86 PC I/O System

DIMMs = Dual Inline memory modules


Intel Xeon 5300 processor
Intel Xeon 5300 processor
Front Side Bus (1333 MHz, 10.5 GB/sec)
FB DDR2 667 (5.3 GB/sec)
Main memory DIMMs
Memory controller hub (north bridge) 5000P
PCIe x16 (or 2 PCIe x8) (4 GB/sec)
ESI (2 GB/sec)
PCIe x8 (2 GB/sec)
Serial ATA (300 MB/sec)
Disk
Disk
LPC (1 MB/sec)
Keyboard, mouse, ...
USB 2.0 (60 MB/sec)
I/O controller hub (south bridge) Entreprise South Bridge 2
PCIe x4 (1 GB/sec)
PCIe x4 (1 GB/sec)
PCI-X bus (1 GB/sec)
PCI-X bus (1 GB/sec)
Parallel ATA (100 MB/sec)
CD/DVD

Parallel Advanced Technology Attachment (PATA)
(legacy connection for hard drivers, optical disks, …)

LPC = Low-Pin Count bus

I/O Management

- I/O is mediated by the OS
  - Multiple programs share I/O resources
    - Need protection and scheduling
  - I/O causes asynchronous interrupts
    - Same mechanism as exceptions
  - I/O programming is fiddly
    - OS provides abstractions to programs