Topic V27

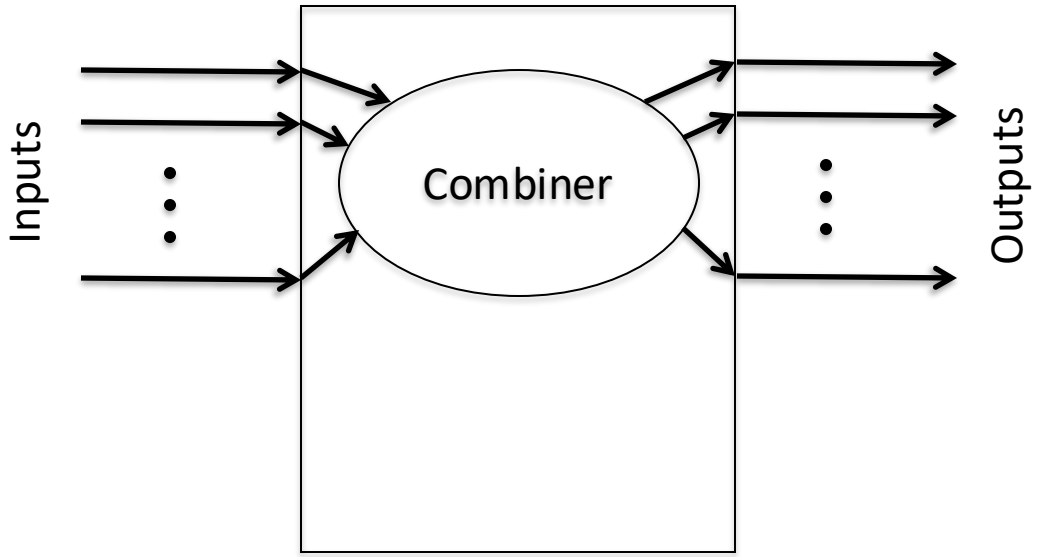
Datapath Building Blocks

Reading: (Section 4.3)

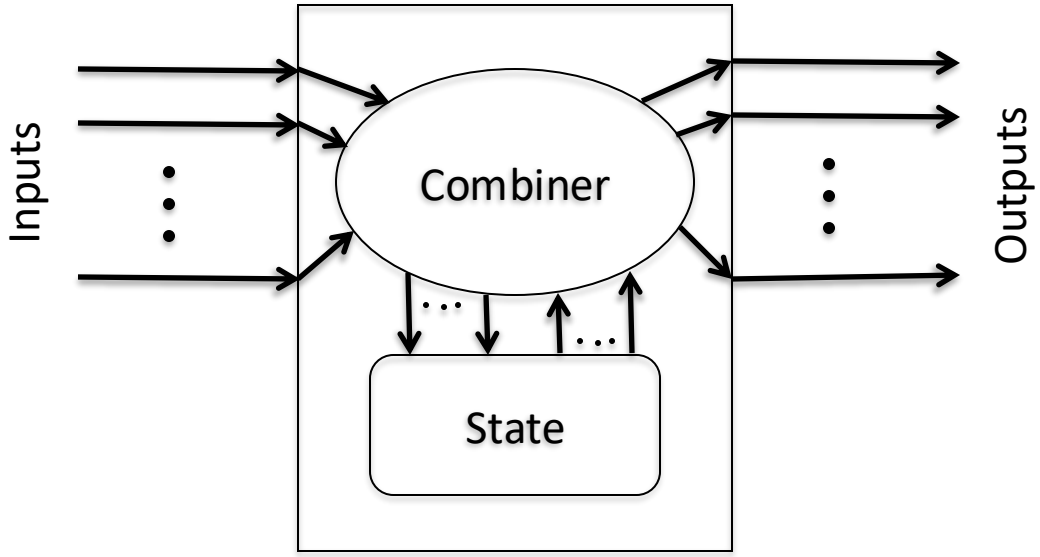
Logic Design Basics

Information encoded in binary

- Low voltage = 0, High voltage = 1
- One wire per bit
- Multi-bit data encoded on multi-wire buses



Combinatorial

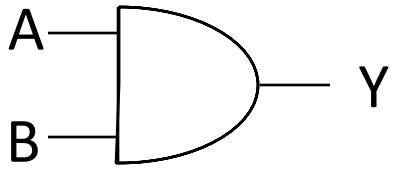


Sequential

Combinatorial Elements

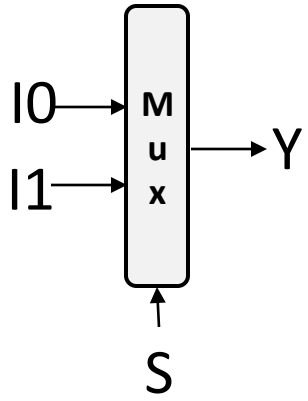
AND-gate

Y = A & B



Multiplexer

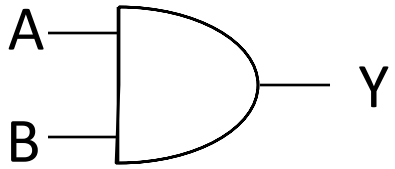
Y = S ? I1 : I0



Combinatorial Elements

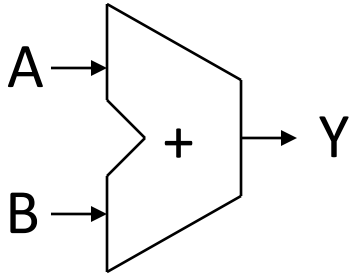
AND-gate

Y = A & B



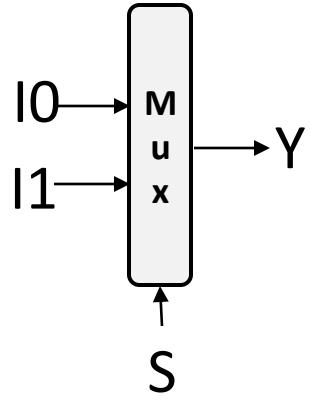
Adder

Y = A + B



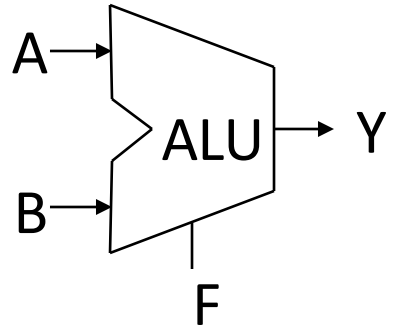
Multiplexer

Y = S ? I1 : I0



Arithmetic/Logic Unit

Y = F(A, B)

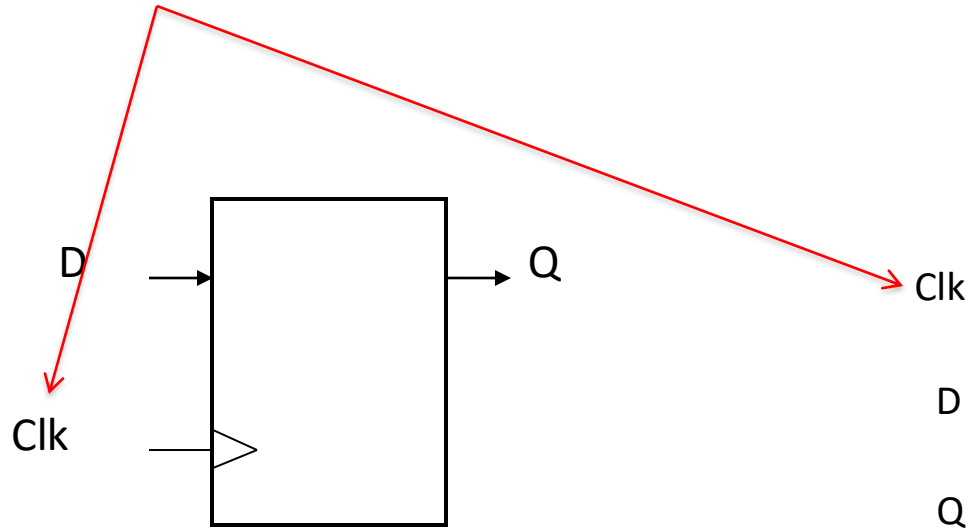


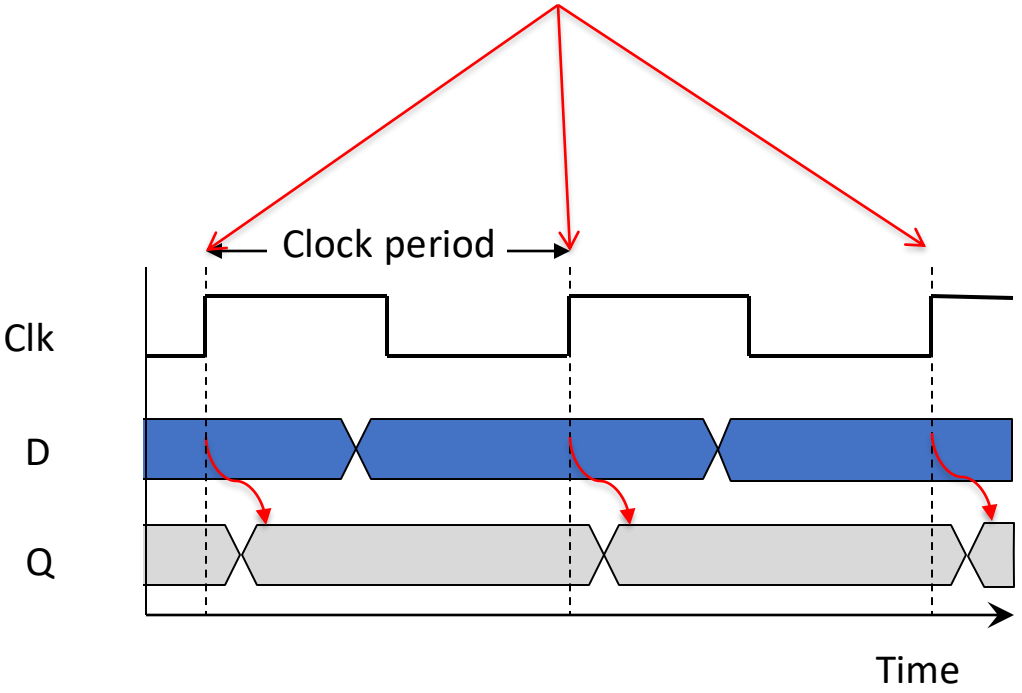
Sequential Elements: Register

Stores data in a circuit

Uses a Clock signal to determine when to update the stored value

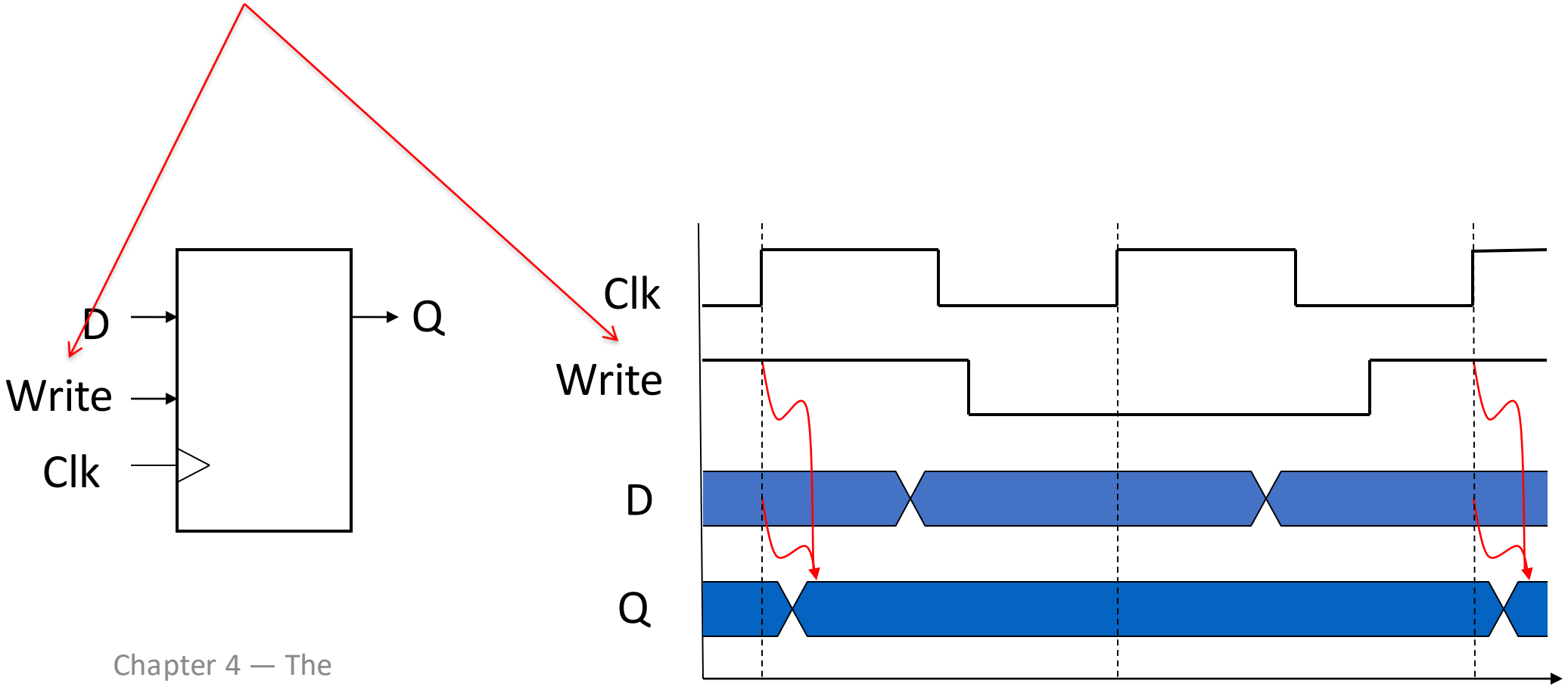
Edge-triggered: update when Clock changes from 0 to 1





Register with Write Control

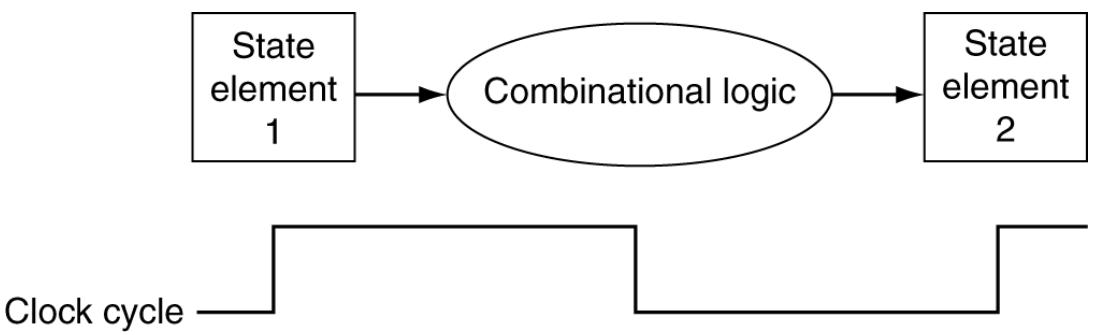
Only updates on clock edge
when write control input is 1

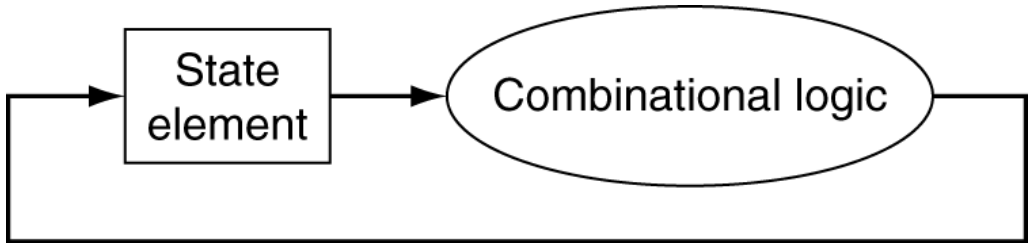


Clocking Methodology

Combinational logic transforms data during clock cycles

- Between clock edges
- Input from state elements, output to state element
- Longest delay determines clock period

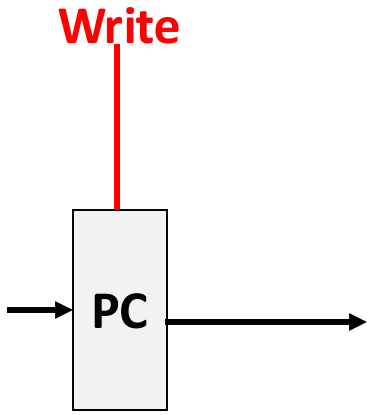




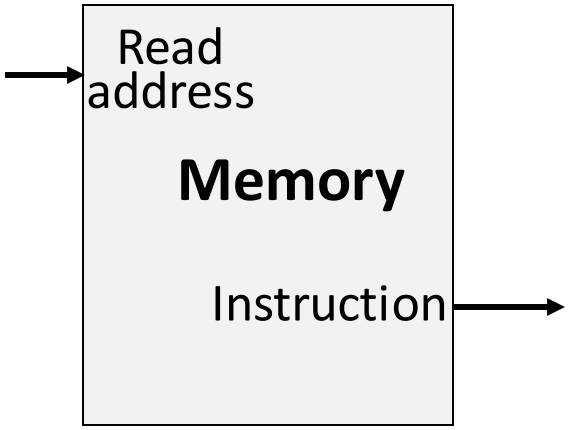
Building a Datapath

- Datapath
  - Processes data and addresses in the CPU
    - Registers, ALUs, muxes, memories, …
- We will build a RISC-V Datapath incrementally
  - Refining the overview design

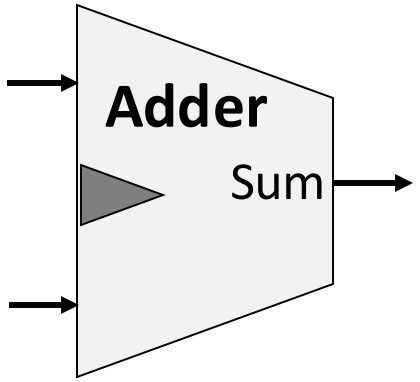
Datapath: Instruction Memory



Program Counter

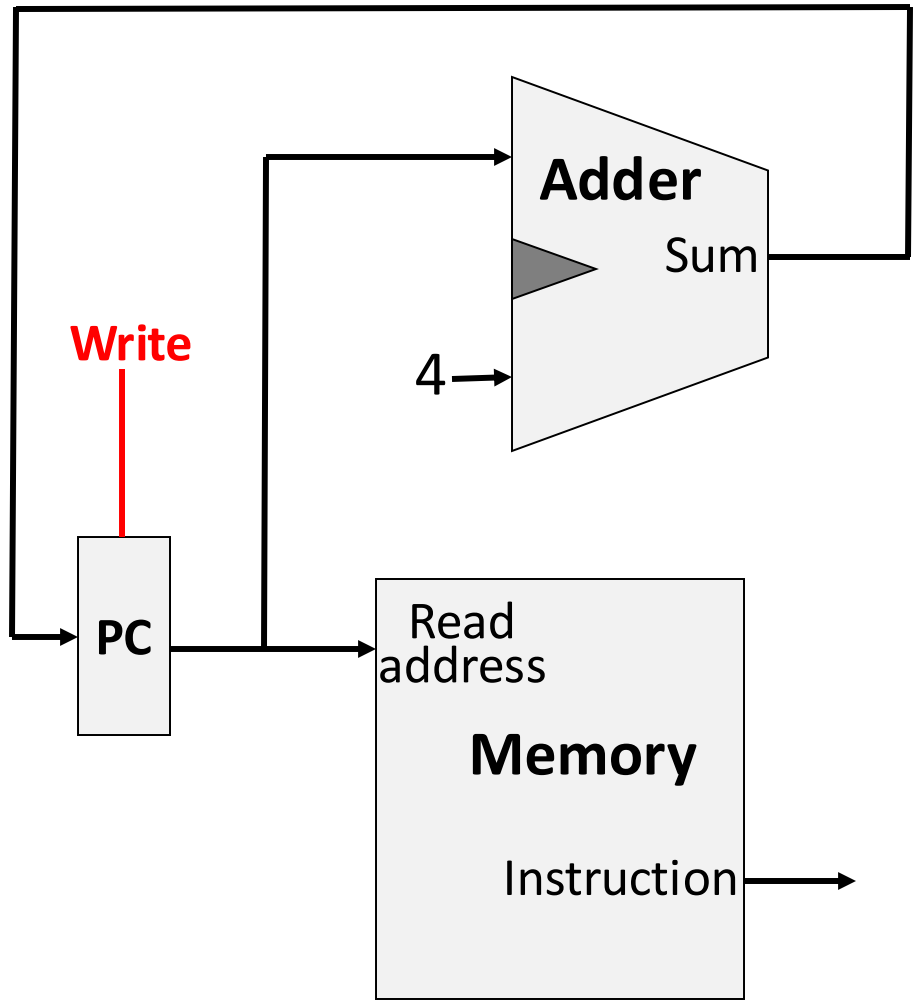


Instruction Memory

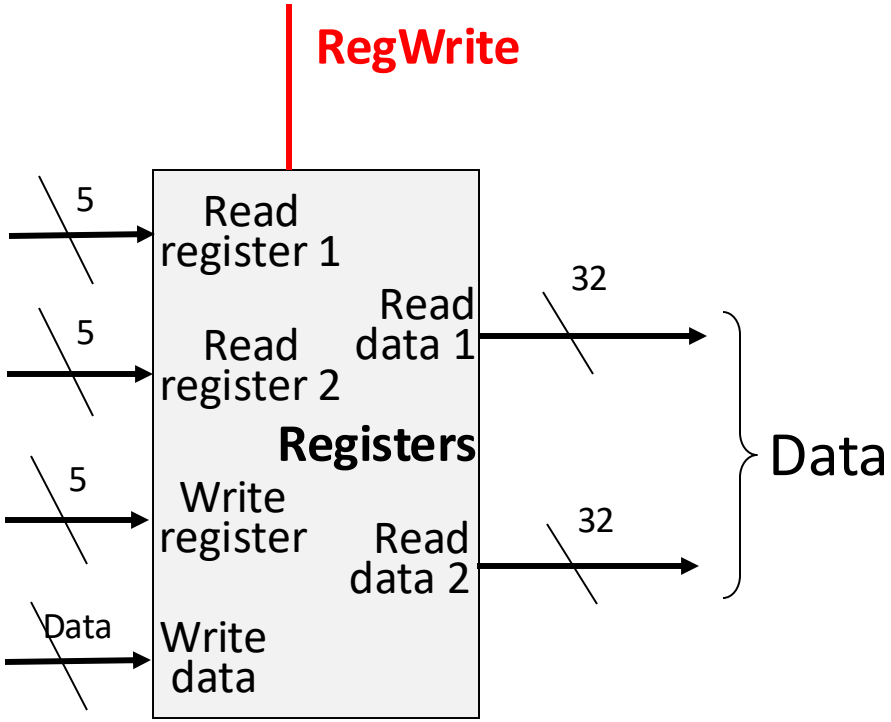


Adder

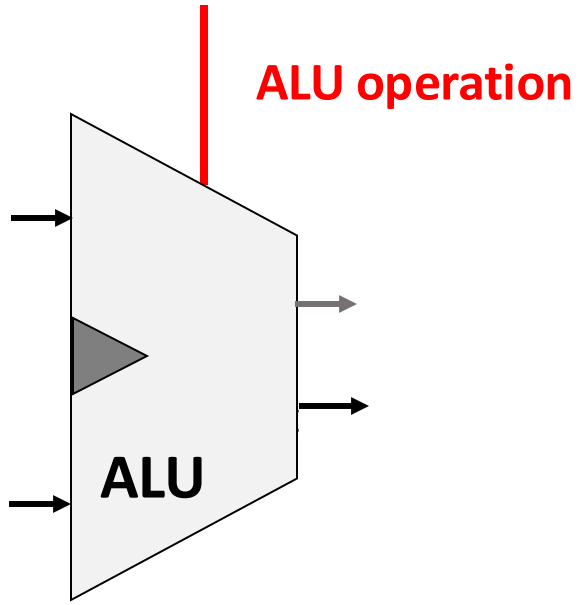
Datapath: PC Incrementor



Datapath: Register File and ALU

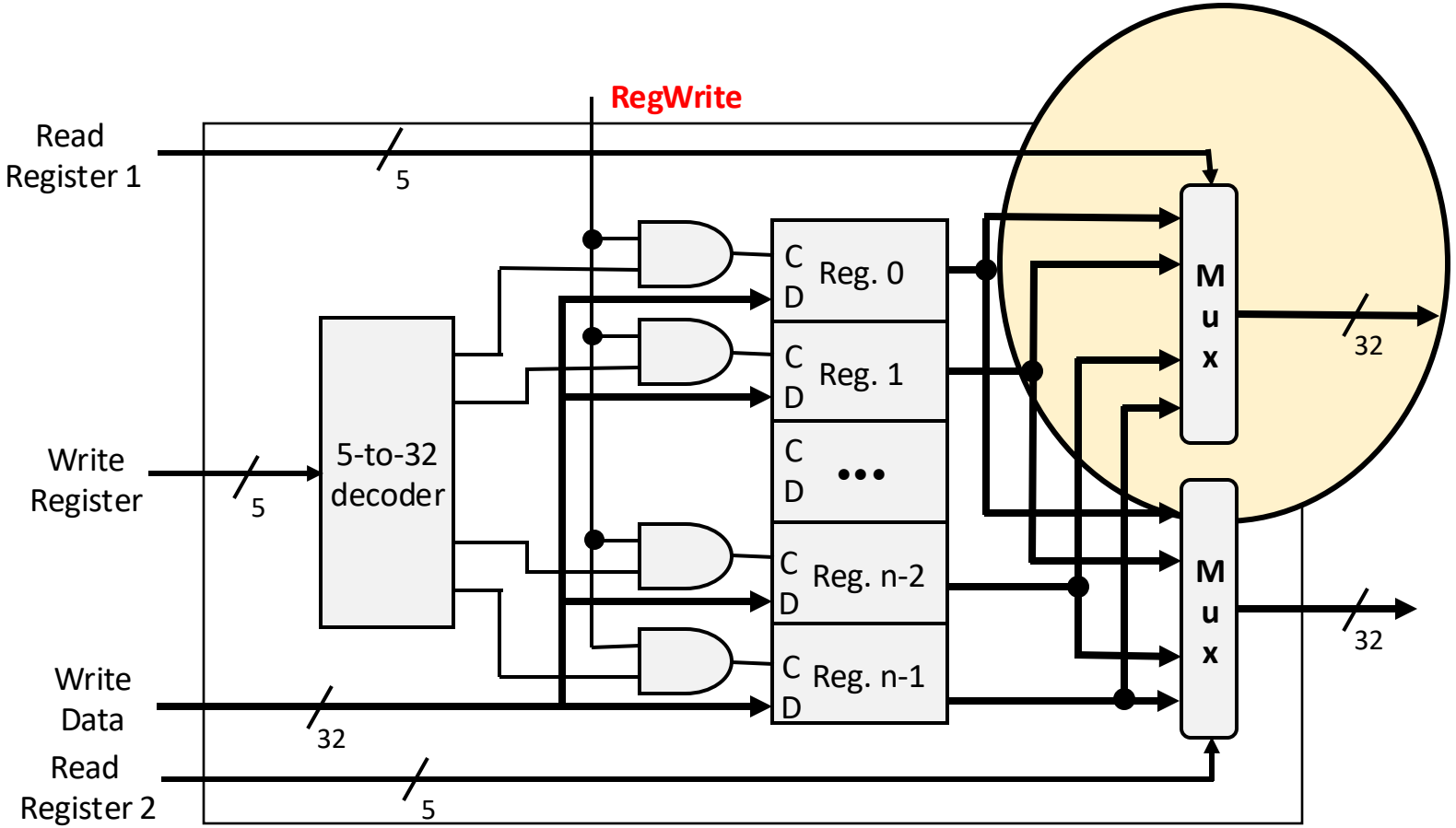


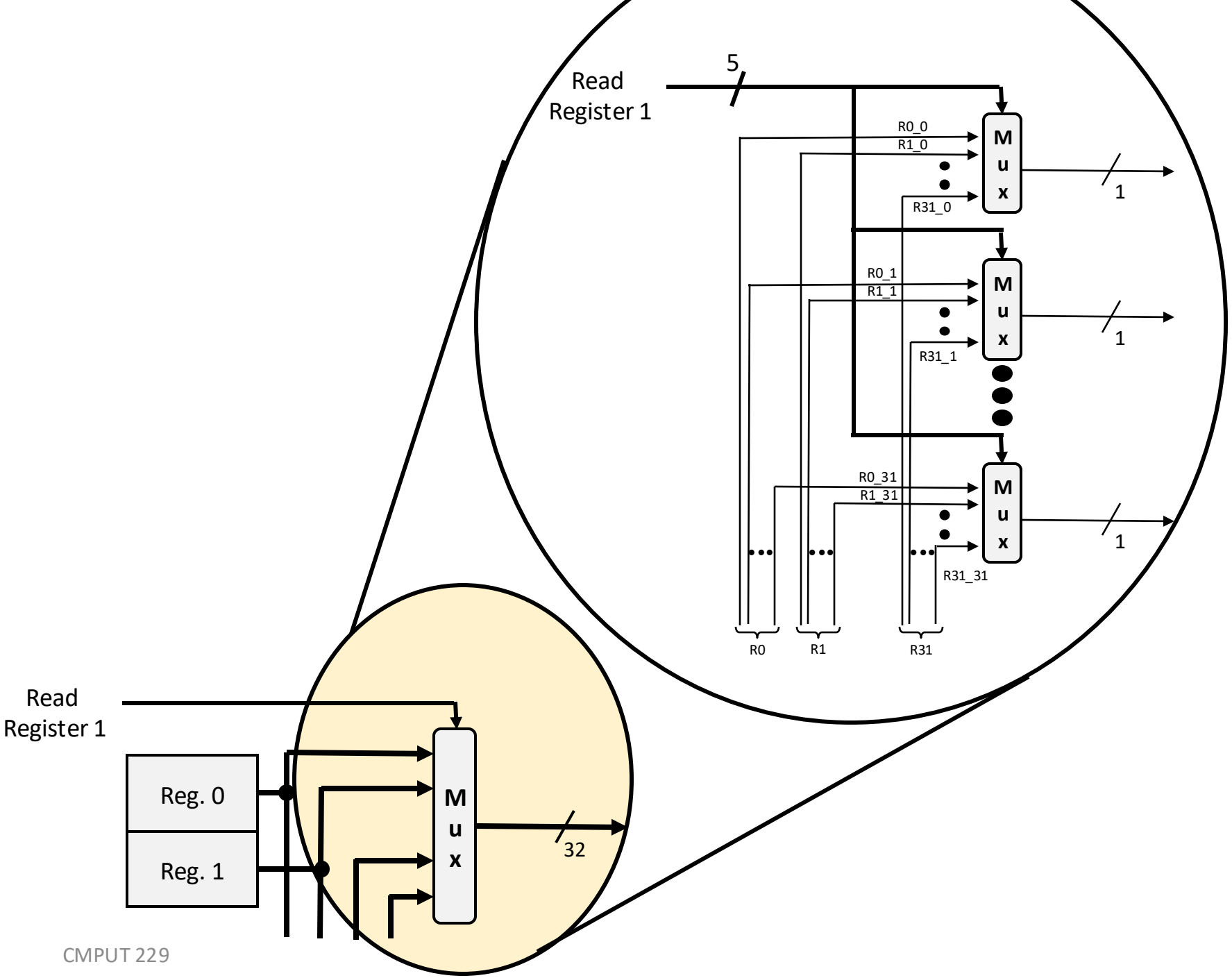
Registers



ALU

A Two Read Port File with n Registers




Read
Register 1
5
R0_0
R1_0
R31_0
M
u
x
1
R0_1
R1_1
R31_1
R0_31
R1_31
R31_31
R0
R1
R31
Read
Register 1
Reg. 0
Reg. 1
32