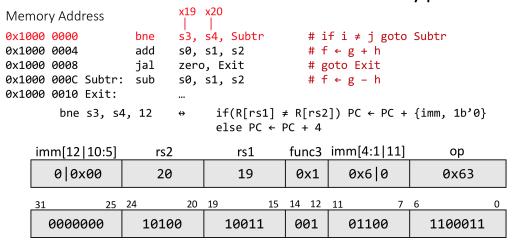
CMPUT 229 - Quiz # 2 - Fall 2010

Name: Solution

Question 1 (100 points): The figure below displays the slide used in class to explain the format of a branch-not-equal instruction. The table below lists two branch instructions that were fetched by a processor. It shows the memory address from which the instruction was fetched and the hexadecimal representation of the fetched instruction. For each instruction, indicate the address of the next instruction executed in case of a branch-taken and in case of a branch-not-taken outcome.

Fetching Address	Fetched Instruction		Address of Next Instruction Executed				
1 cooming riddress			Branch Not Taken		Branch Taken		
0x1000 1000	0x2A62 8E63		0x1000 1004		0x1000 12BC		
0x1000 4FCC	0xF662 84E3		0x1000 4FD0		0x1000 4F34		
imm[12:1]	=	0 0 010101 11:	10	imm[12:1]	=	1 1 11101	1 0100
imm[12:0]	= (0 0010 1011 110	00	imm[12:0]	=	1 1111 011	0 1000
after sign extension	. =	0x0000 021	3C	after sign exten	sion =	OxFFF	F FF68
PC	=	0x1000 100	00	Original PC	=	0x100	0 4FCC
	+	0x0000 02I	3C		+	OxFFF	F FF68
Target Address	=	0x1000 12I	3C	Target Address		0x100	0 4F34

Branch Instructions: SB-Type



In memory we would see: 0x01499663