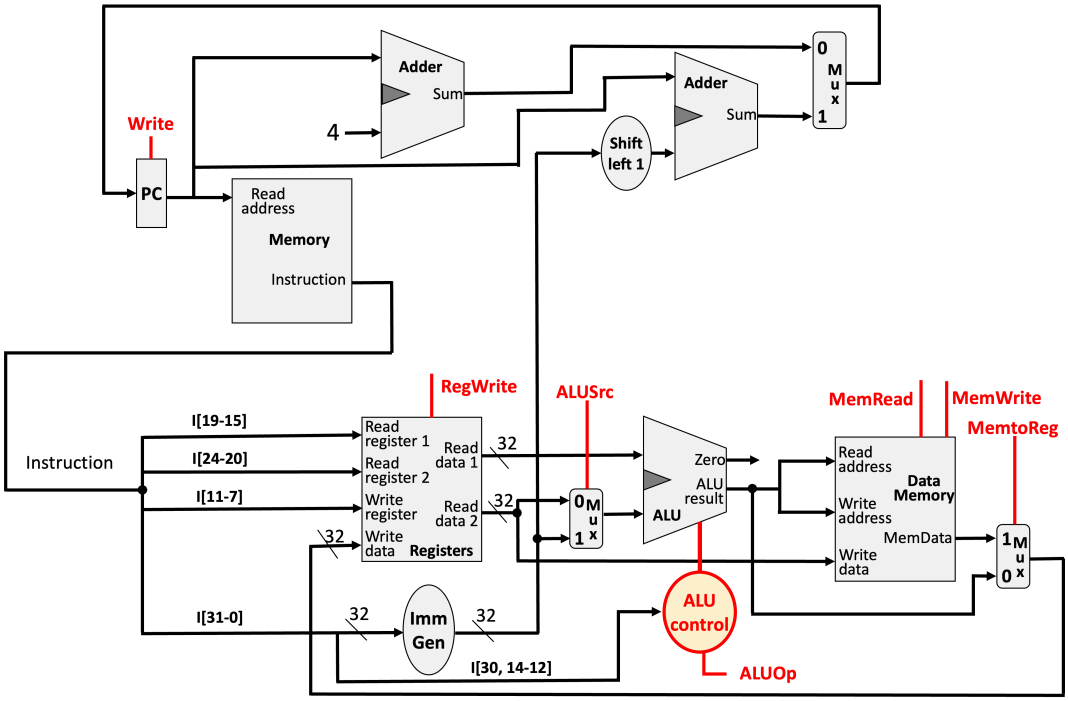

Figure 1: A diagram for a single-cycle datapath.

Question 4 (20 points): In this question we will examine the design of a datapath for a RISC-V processor.

1. (**5 points**) Figure **??** contains a block diagram for a single-cycle datapath design for a RISC-V processor. This diagram shows two separate memories: an instruction memory and a data memory. However, we know that a computer has only one memory. If we change the datapath design so that if features a single memory, there would be a structural hazard in the pipeline: the memory has to be accessed for both instruction fetching and data access in the same cycle. What is the solution adopted in modern computers to enable the use of a single memory while avoiding this structural hazard?

2. (**5 points**) For the single-cycle datapath show in Figure **??**, state what operation is performed in the ALU, and what happens with the result produced by the ALU, for the execution of the following instructions:

`sub s0, s1,s2` :

`sb t1, 8(t0)` :

`beq t2, t3, label` :

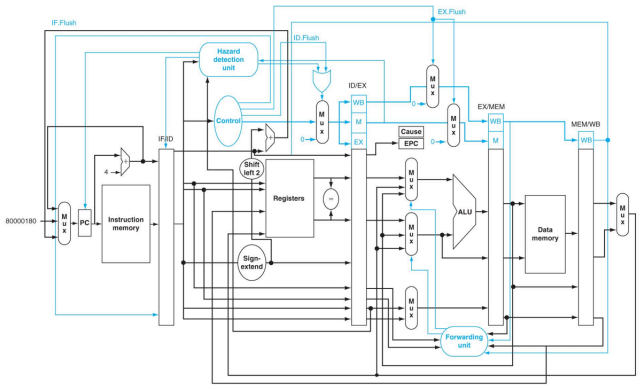

Figure 2: A diagram for pipelined datapath.

3. (**5 points**) Figure **??** shows the diagram from a possible design for a five-cycle pipeline for a RISC-V processor. However, with the design as presented, there is an issue with the specification of destination register for instructions that change the value of a register. Explain what the issue is and how it can be corrected.

4. (**5 points**) The diagram in Figure **??** does not show the paths needed for forwarding. Assume that the following sequence of instructions are executed in this pipeline:

```
...
lw t0, 16(t2)
add t1, t3, t5
sub t0, t1, t0
...
```

Explain the forwardings that are needed to prevent delays in the execution of these instructions. What are all the changes to the design in Figure **??** that are needed to execute these instructions without delay. You can explain with a combination of text and drawing in the figure.