Topic V32

Write Strategy

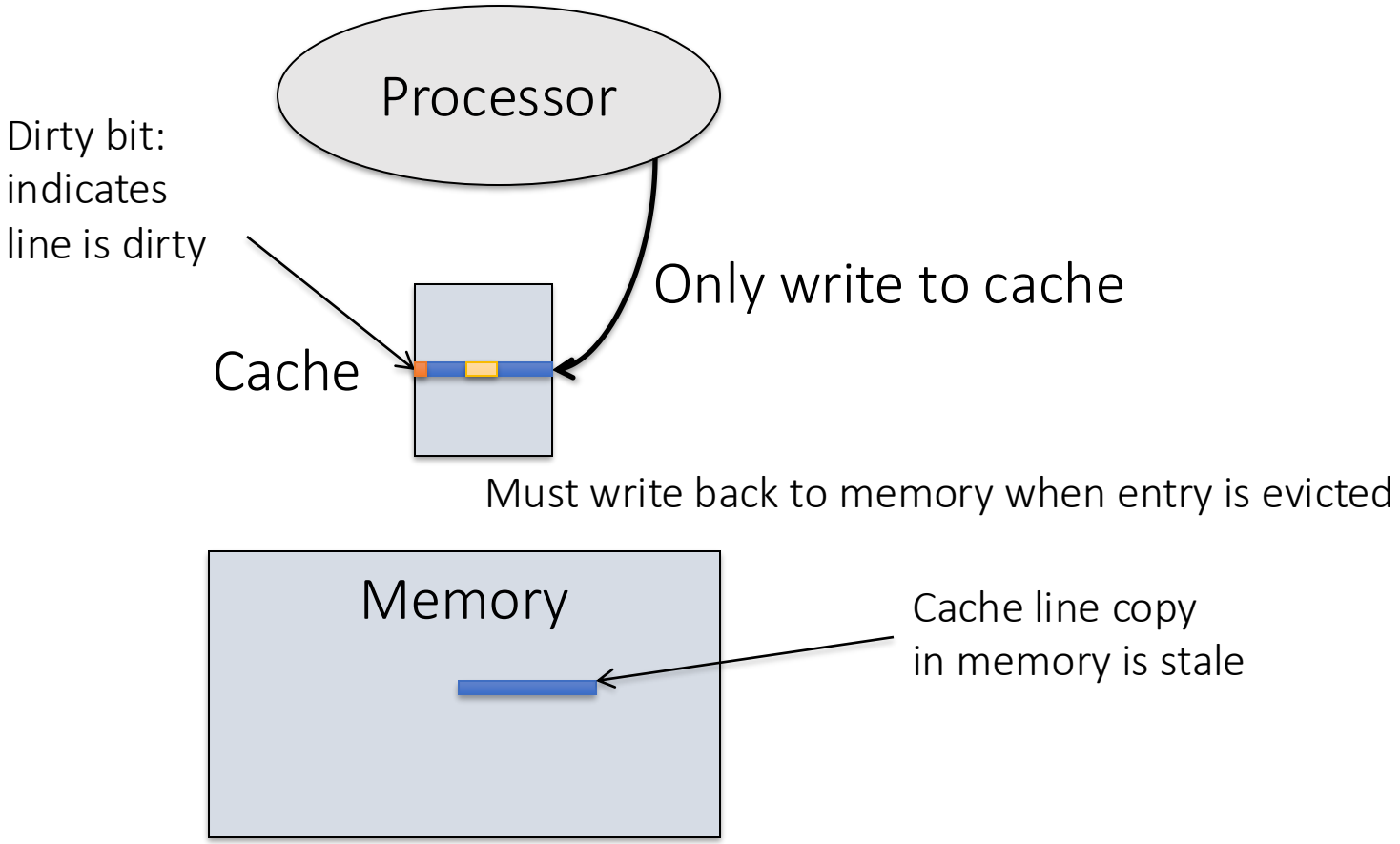
Reading: (Section 5.4)

Write Strategy

What should happen on a write?

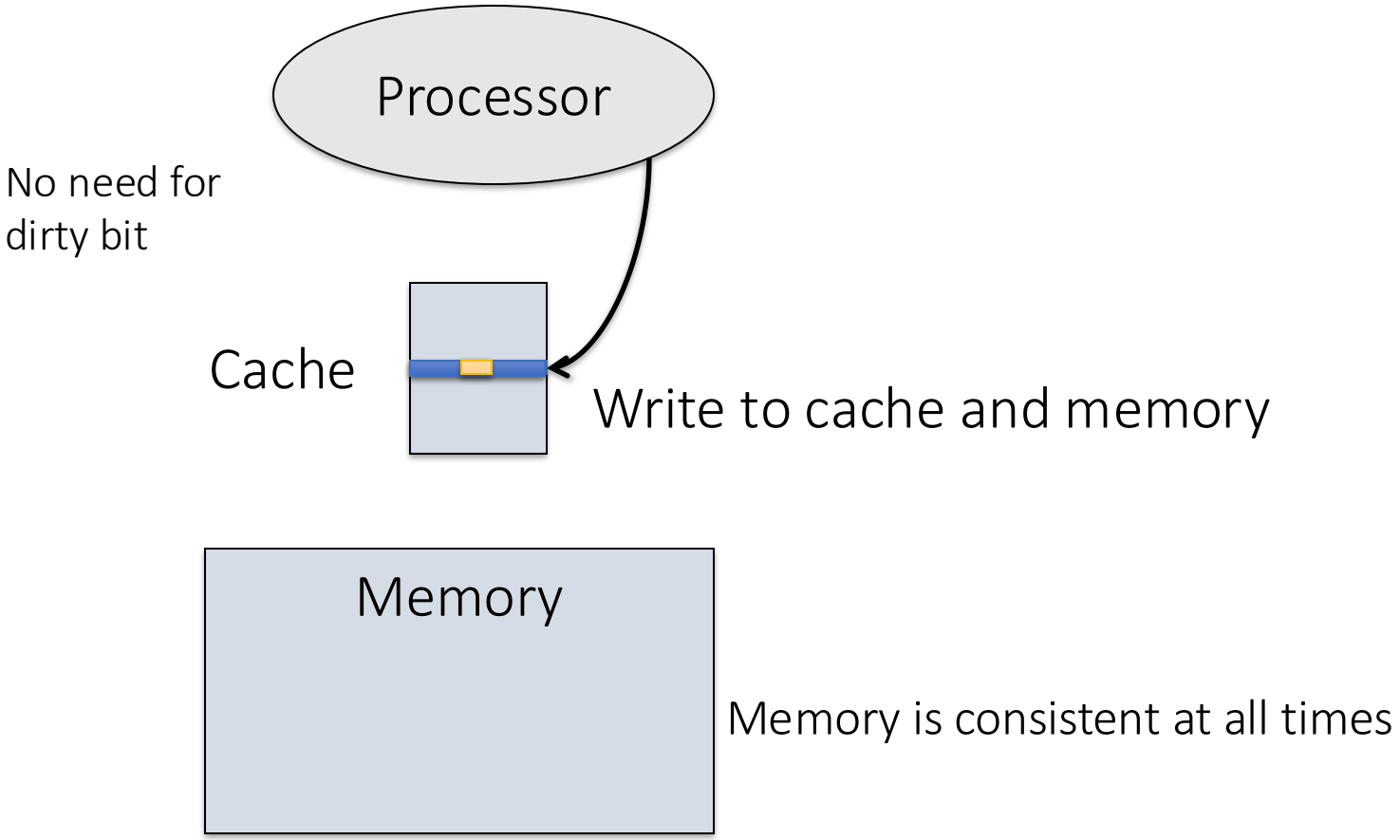
Write Strategy (on a hit)

Write Back



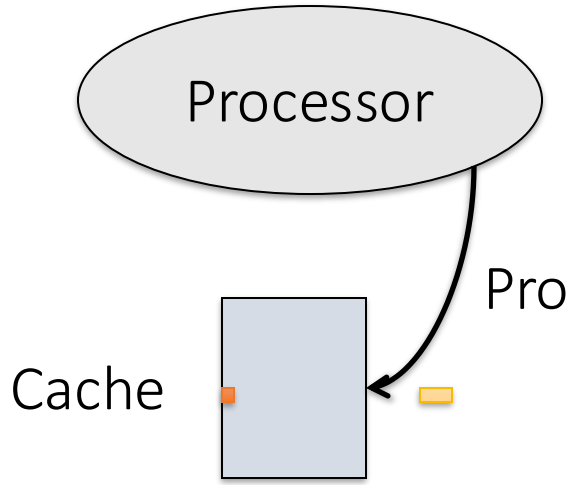
Write Strategy (on a hit)

Write Through



Write Strategy (on a miss)

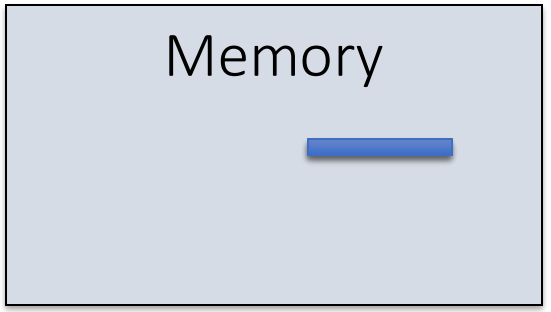
Write Allocate
with Write Back



Now line
is dirty

Processor issues write

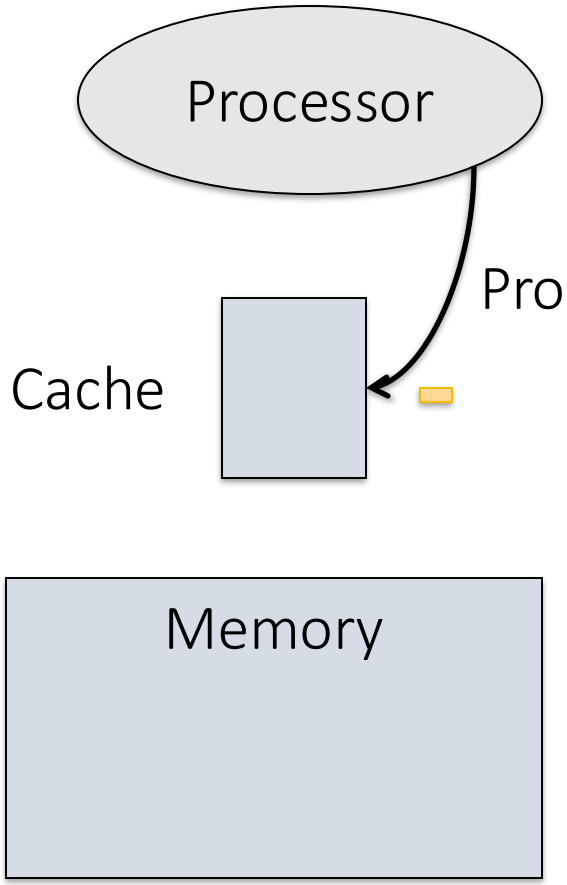
But line is not in the cache



Must fetch line from memory

And then write on it

Write Strategy (on a miss)



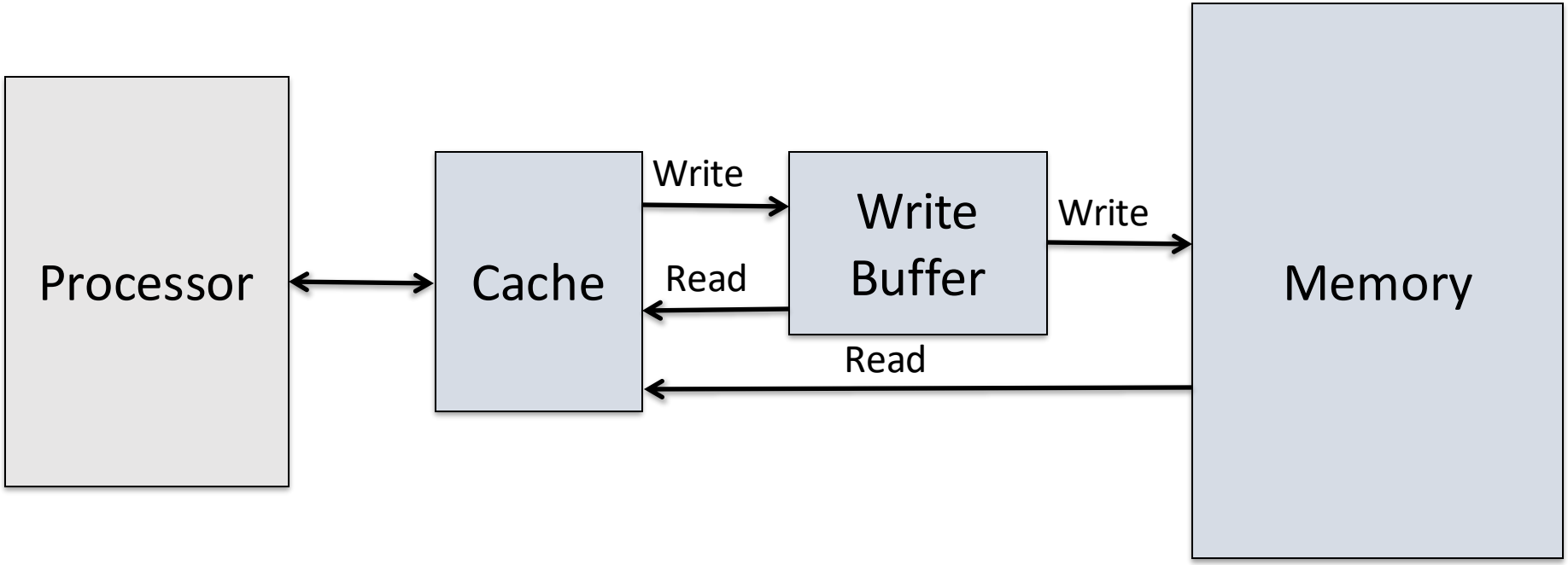
Write Around
with Write Through

Processor issues write

But line is not in the cache

Write only to memory

Write Buffer



Intrinsity FastMATH (example)

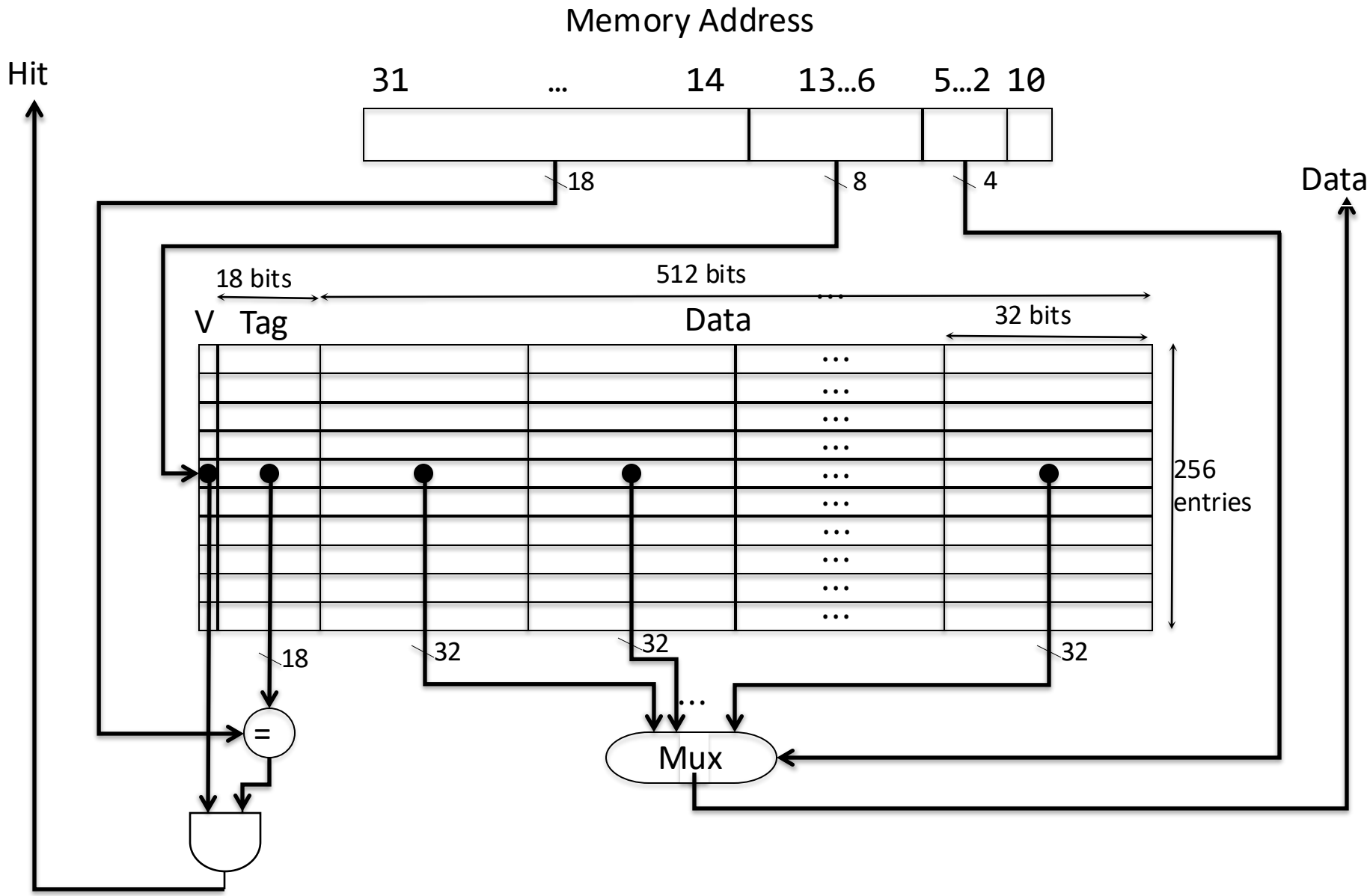
Embedded MIPS processor

- Instruction and data access on each cycle

- Split cache: separate I-cache and D-cache
  - Each 16KB: 256 blocks × 16 words/block
  - D-cache: write-through or write-back

- SPEC2000 miss rates
  - I-cache: 0.4%
  - D-cache: 11.4%

Intrinsity FastMATH (example)



In Ryzen 9 CPUs, the L1 instruction cache is 4-way associative, while the L1 data cache is 8-way set associative.

Here's a more detailed breakdown:

- **L1 Instruction Cache:** 4-way associative
- **L1 Data Cache:** 8-way set associative
- **Cache Line Size:** 64 bytes
- **L2 Cache:** 8-way set associative
- **L3 Cache:** 12-way set associative

Cache	
Cache L1:	64 KB (per core)
Cache L2:	512 KB (per core)
Cache L3:	64 MB