

Question 5 (30 points):

Bkpt	Address	Code	Basic	Source
	0x00400000	0x02500513	addi x10,x0,0x00000025	0: main: addi a0, zero, 37
	0x00400004	0x01c000ef	jal x1,0x0000000e	9: jal makeEven
	0x00400008	0x01c00513	addi x10,x0,0x0000001c	10: addi a0, zero, 28
	0x0040000c	0x024000ef	jal x1,0x00000012	11: jal makeOdd
	0x00400010	0x01100513	addi x10,x0,0x00000011	12: addi a0, zero, 17
	0x00400014	0x01900593	addi x11,0,0x00000019	13: addi a1, zero, 25
	0x00400018	0x024000ef	jal x1,0x00000012	14: jal addUp
	0x0040001c	0x00000067	jalr x0,x1,0x00000000	15: ret
	0x00400020	0xffff00293	addi x5,x0,0xffffffff	16: makeEven: addi t0, zero, -1
	0x00400024	0x0012c293	xori x5,x5,0x00000001	17: xori t0, t0, 1
	0x00400028	0x00557533	andi x10,x10,x5	18: andi a0, a0, t0
	0x0040002c	0x000002e7	jalr x5,x1,0x00000000	19: jalr t0, ra, 0
	0x00400030	0x00156513	ori x10,x10,0x00000001	20: makeOdd: ori a0, a0, 1
	0x00400034	0xffc00093	addi x1,x1,0xffffffff	21: addi ra, ra, -4
	0x00400038	0x00400067	jalr x0,x1,0x00000004	22: jalr zero, ra, 4
	0x0040003c	0x00b00533	addi x10,x10,x11	23: addUp: addi a0, a0, a1
	0x00400040	0x01a00093	addi x1,x1,0x0000001a	24: addi ra, ra, 26
	0x00400044	0xf600e67	jalr x28,x1,0xffffffff	25: jalr t3, ra, -26

(a) RARS Screenshot

Address	Binary Code	callVec	returnVec
0x1000103C	0xFFFFFFFF		
0x1000103C	0x01a08093	0	1
0x10001038	0x01a08093	0	0
0x1000103C	0x00b50533	0	0
0x10001038	0x00408067	0	1
0x10001034	0xffc08093	0	0
0x10001030	0x00156513	0	0
0x1000102C	0x000082e7	0	1
0x10001028	0x00557533	0	0
0x10001024	0x0012c293	0	0
0x10001020	0xffff00293	0	0
0x1000101C	0x00008067	0	1
0x10001018	0x024000ef	1	0
0x10001014	0x01900593	0	0
0x10001010	0x01100513	0	0
0x1000100C	0x024000ef	1	0
0x10001008	0x01c00513	0	0
0x10001004	0x01c000ef	1	0
0x10001000	0x02500513	0	0

(b) Binary Code stored in memory, vectors

Figure 1: RARS screenshot of the RAS-Example.s program. Unusual forms of return instructions are used to illustrate that any `jalr` instruction with source register `ra` is regarded as a return instruction. (a) In RARS the lower memory addresses are at the top. (b) In the memory representation our convention is that the lower addresses are at the bottom of the page.

The binary codes of the instructions of a RISC-V program can be stored in an array in memory. For example, Figure 1(a) has a RARS screenshot of a sample program. Assume that the binary representation of this program is stored in memory starting at the address `0x10001000` as shown in Figure 1(b). Figure 1(b) also shows two binary vectors `callVec` and `returnVec` that mark which instructions are a function call and which instructions are return statements. Binary vectors like these are useful when building a simulator. Later passes through the code can simply inspect the values in these binary vectors to decide if an action corresponding to a call or a return statement should be taken.

Write RISC-V assembly code for the function `RAS`. It receives as an argument the address of the first instruction of a RISC-V program. This program has been assembled and starting at that address in memory you find the binary code for the instructions. The end of the program is signalled by the sentinel word `0xFFFFFFFF`. Your `RAS` function does the following:

- sets to 1 the bits in the `callVec` that correspond to a function call instruction
- sets to 1 the bits in the `returnVec` that correspond to a return statement
- returns the number of function calls and the number of return statements found in the program.

Assume that all the bits in the `callVec` and `returnVec` binary vectors are 0 prior to the calling

of the function `RAS`. The bit vectors `callVec` and `returnVec` are long enough to contain one bit for each instruction in the program.

The existing bit vector library makes available a `setBit` function with the following specification:

- Arguments:
 - `a0`: address of a bit vector
 - `a1`: an index into the bit vector specifying a bit
- Effect:
 - the bit specified is set

`RAS` must call the function `CallReturn` to determine if a given instruction is either a function call or a return statement. It must call the function `SetBit` (not shown) to set a bit in the bit vector.

- Arguments:
 - `a0`: address of first instruction in the program
 - `a1`: address of bit vector `callVec`
 - `a2`: address of bit vector `returnVec`
- Return Value:
 - `a0`: number of function call instructions found
 - `a1`: number of return statements found

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256 RAS:
257     addi sp, sp, -32
258     sw    s0, 0(sp)
259     sw    s1, 4(sp)
260     sw    s2, 8(sp)
261     sw    s3, 12(sp)
262     sw    s4, 16(sp)
263     sw    s5, 20(sp)
264     sw    s6, 24(sp)
265     sw    ra, 28(sp)
266     mv    s0, zero           # numCalls <- 0
267     mv    s1, zero           # numReturns <- 0
268     mv    s3, zero           # InstrCounter <-- 0
269     mv    s2, a0             # InstrPointer <- address of first instruction
270     mv    s5, a1             # callVec
271     mv    s6, a2             # returnVec
272     addi s4, zero, -1         # s4 <- Sentinel value
273 NextInstr: lw    t0, 0(s2)     # t0 <- currentInstruction
274     beq    t0, s4, ProgEnd     # if found sentinel
275     mv    a0, s2
276     jal    ra, CallReturn
277     addi s2, s2, 4             # InstrPointer++
278     addi s3, s3, 1             # InstrCounter++
279     beqz   a0, NextInstr
280     addi a1, s3, -1           # a1 <- CurrentInstruction position
281     beq    a0, s4, IsReturn    # if CallReturn set a0 == -1
282     mv    a0, s5             # a0 <- callVec
283     jal    setBit
284     addi s0, s0, 1             # numCalls++
285     j      NextInstr
286 IsReturn: mv    a0, s6         # a0 <- returnVec
287     jal    setBit
288     addi s1, s1, 1             # numReturns++
289     j      NextInstr
290 ProgEnd:  mv    a0, s0         # a0 <- numCalls
291     mv    a1, s1             # a1 <- numReturns
292     lw    s0, 0(sp)
293     lw    s1, 4(sp)
294     lw    s2, 8(sp)
295     lw    s3, 12(sp)
296     lw    s4, 16(sp)
297     lw    s5, 20(sp)
298     lw    s6, 24(sp)
299     lw    ra, 28(sp)
300     addi sp, sp, 32
301     jalr x0, ra, 0

```

Figure 2: A solution for RAS.