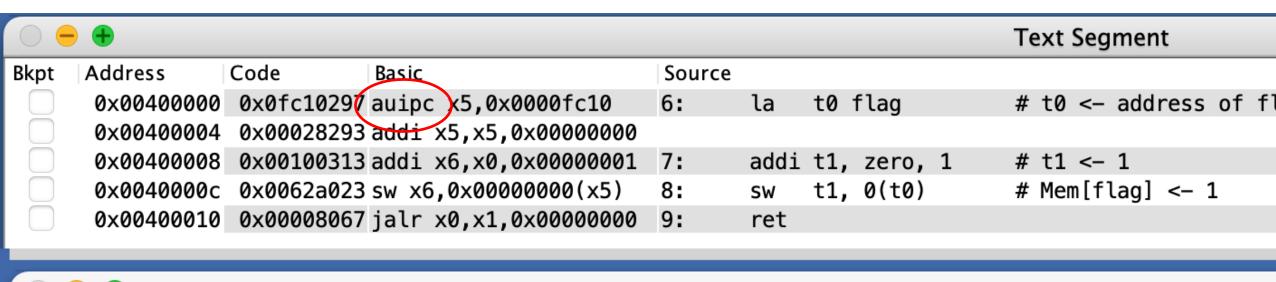
Topic VOA

Using la and the IsBra Programming Example Readings: (Section 2.6-2.7)

Load Address

The la pseudo instruction



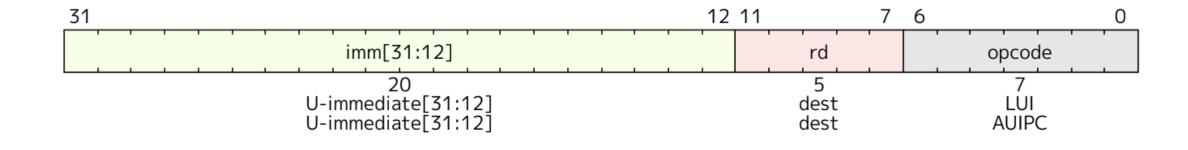
○ ○ ○					Data Segment
Address		Value (+0)	Value (+4)	Value (+8)	Value (+c)
	0×10010000	0x00000001	0x00000000	0x00000000	0×00000000
	0x10010020	0×00000000	0×00000000	0x00000000	0×00000000
	0×10010040	0×00000000	0×00000000	0×00000000	0×00000000



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Unprivileged Architecture

Version 20240411



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2.4. Integer Computational Instructions | Page 27

LUI (load upper immediate) is used to build 32-bit constants and uses the U-type format. LUI places the 32-bit U-immediate value into the destination register *rd*, filling in the lowest 12 bits with zeros.

AUIPC (add upper immediate to pc) is used to build pc-relative addresses and uses the U-type format. AUIPC forms a 32-bit offset from the U-immediate, filling in the lowest 12 bits with zeros, adds this offset to the address of the AUIPC instruction, then places the result in register rd.

PC: 0x00400000 + 0x0fc10000 0x10010000

0 6	•									Text Segr	nent	
Bkpt	Address	Code	Basic		Source							
	(0x00400000)	0x0fc10297	auipc x5,0x	0000fc10	6:	la	t0 1	flag		# t0 <- a	address o	f fl
	0x00400004	0x00028293	addi x5,x5,	0×00000 000								
	0x00400008	0x00100313	addi x6,x0,	0×00000001	7:	addi	t1,	zero,	1	# t1 <- :	1	
	0x0040000c	0x0062a023	sw x6,0x0000	00000(x5)	8:	SW	t1,	0(t0)		# Mem[fla	ag] <- 1	
	0x00400010	0x00008067	jalr x0,x1,	0×00000000	9:	ret						
	+									Dat	a Segmen	nt
Addr	ess	Value (+0	1)	Value (+4)		Val	lue (+	-8)		Value (+c	:)	
	0×100100	000	0×00000001		0×0000000	90		0×06	000000		0x00000	000

0x00000000

0x00000000

0x00000000

0x00000000

0x00000000

0x00000000

0x00000000

0x00000000

0x10010020

0×10010040

Sample Question

One way to implement a "branch always" (bra) instruction, is to use the beq instruction and to make both registers the same. For example:

beq t0, t0, LABEL

Binary format of a branch instruction:

31 25	24 20	19 15	14 12	11 7	6 0
imm[12 10:5]	rs2	rs1	func3	imm[4:1 11]	ор

Write the RISC-V code for a function IsBra that receives the binary code of a beq instruction in a0 and returns 1 in a0 if it is a bra and returns 0 in a0 otherwise.

Sample Question

Write the RISC-V code for a function IsBra:

- Input parameter:
 - a0: binary code of a beg instruction;
- Return value:
 - a0 = 1: the beg instruction is a bra
 - a0 = 0: the beq instruction is not a bra

	31 25	24 20	19 15	14 12	11 7	6 0
a0 =	imm[12 10:5]	rs2	rs1	func3	imm[4:1 11]	ор

First we shift the content of a0 to the right by 15 bits:

Now we AND the result with 0x01F:

	31 25	24 20	19 15	14 12	11 7	6 0
a0 =	imm[12 10:5]	rs2	rs1	func3	imm[4:1 11]	ор

Then we shift the content of a0 to the right by 20 bits: srli t0, a0, 20

Now we AND the result with 0x01F:

andi t3, t2, 0x01F

Finally, we use a beq instruction to find if rs1 and rs2 are the same register:

beq t1, t3, braTrue

a0, zero, 1

zero, ra, 0

	31							5	4		0
t1 =		0000	0000	0000	000	0 0000 00	00	000		rs1	
	31							5	4		0
t3 =		0000	0000	0000	000	0 0000	0000	000		rs2	

jalr zero, 0(ra)

IsBra:

addi

jalr

```
# t0 ← a0 >> 15
      srli t0, a0, 15
            t1, t0, 0x01F
      andi
                            # t1 ← rs1
      srli t2, a0, 20
                            # t2 ← a0 >> 20
            t3, t2, 0x01F # t2 \leftarrow rs2
      andi
            t1, t3, braTrue
                              # if rs1 = rs2 goto braTrue
      beq
      addi
            a0, zero, 0
                              # a0 ← 0
      jalr
            zero, ra, 0
                              # return
                                            Textbook uses the syntax:
braTrue:
```

a0 ← 1

#return

Alternatively, we can AND a0 with 0x000F8000 but you cannot use a constant larger than 12 bits in an andi instruction:

```
li t0, 0x0F8 # t0 \leftarrow 0x0000 00F8 slli t1, t0, 12 # t1 \leftarrow 0x000F 8000 OR lui t1, 0x000F8 # t0 \leftarrow 0x000F 8000
```

Now we can AND a0 with a1 to obtain: and t2, t1, a0

Now we can do something similar to extract the rs2 field:

li t3,
$$0x01F$$
 # t0 \leftarrow $0x0000 001F$ slli t4, t0, 20 # t1 \leftarrow $0x01F0 0000$

OR

lui t4,
$$0x01F00$$
 # t0 \leftarrow $0x01F0$ 0000

Now we can AND a0 with a1 to obtain: and t5, t4, a0

Finally we can shift t5 to the right by 5 before comparing with t2:

srli t6, t5, 5 # t6 ← t5 >> 5
beq t6, t2, braTrue

•••

000	111	000
000		000

000	000	111
000	000	

