CMPUT 229 - Quiz # 2 - Fall 2010

Name: Solution

Question 1 (100 points): The figure below displays the slide used in class to explain the format of a branch-not-equal instruction. The table below lists two branch instructions that were fetched by a processor. It shows the memory address from which the instruction was fetched and the hexadecimal representation of the fetched instruction. For each instruction, indicate the address of the next instruction executed in case of a branch-taken and in case of a branch-not-taken outcome.

Fetching Address	Fetched Instruction	Address of Next Instruction Executed	
		Branch Not Taken	Branch Taken
0x1000 1000	0x2A62 8E63	0x1000 1004	0x1000 12BC
0x1000 4FCC	0xF662 84E3	0x1000 4FD0	0x1000 4F34

imm[12:1]	=	0 0 010101 1110
imm[12:0]	=	0 0010 1011 1100
after sign extension	=	0x0000 02BC
PC	=	0x1000 1000
	+	0x0000 02BC
Target Address	=	0x1000 12BC

imm[12:1]	=	1 1 111011 0100
imm[12:0]	=	1 1111 0110 1000
after sign extension	=	0xFFFF FF68
Original PC	=	0x1000 4FCC
	+	0xFFFF FF68
Target Address	=	0x1000 4F34

Branch Instructions: SB-Type

```
Memory Address                x19  x20
                               |    |
0x1000 0000          bne      s3, s4, Subtr      # if i ≠ j goto Subtr
0x1000 0004          add      s0, s1, s2         # f ← g + h
0x1000 0008          jal      zero, Exit         # goto Exit
0x1000 000C Subtr:   sub      s0, s1, s2         # f ← g – h
0x1000 0010 Exit:            …

        bne s3, s4, 12    ⇔    if(R[rs1] ≠ R[rs2]) PC ← PC + {imm, 1b'0}
                               else PC ← PC + 4
```

imm[12|10:5]	rs2	rs1	func3	imm[4:1|11]	op
0|0x00	20	19	0x1	0x6|0	0x63

31 25	24 20	19 15	14 12	11 7	6 0
0000000	10100	10011	001	01100	1100011

In memory we would see: 0x01499663