Topic V04

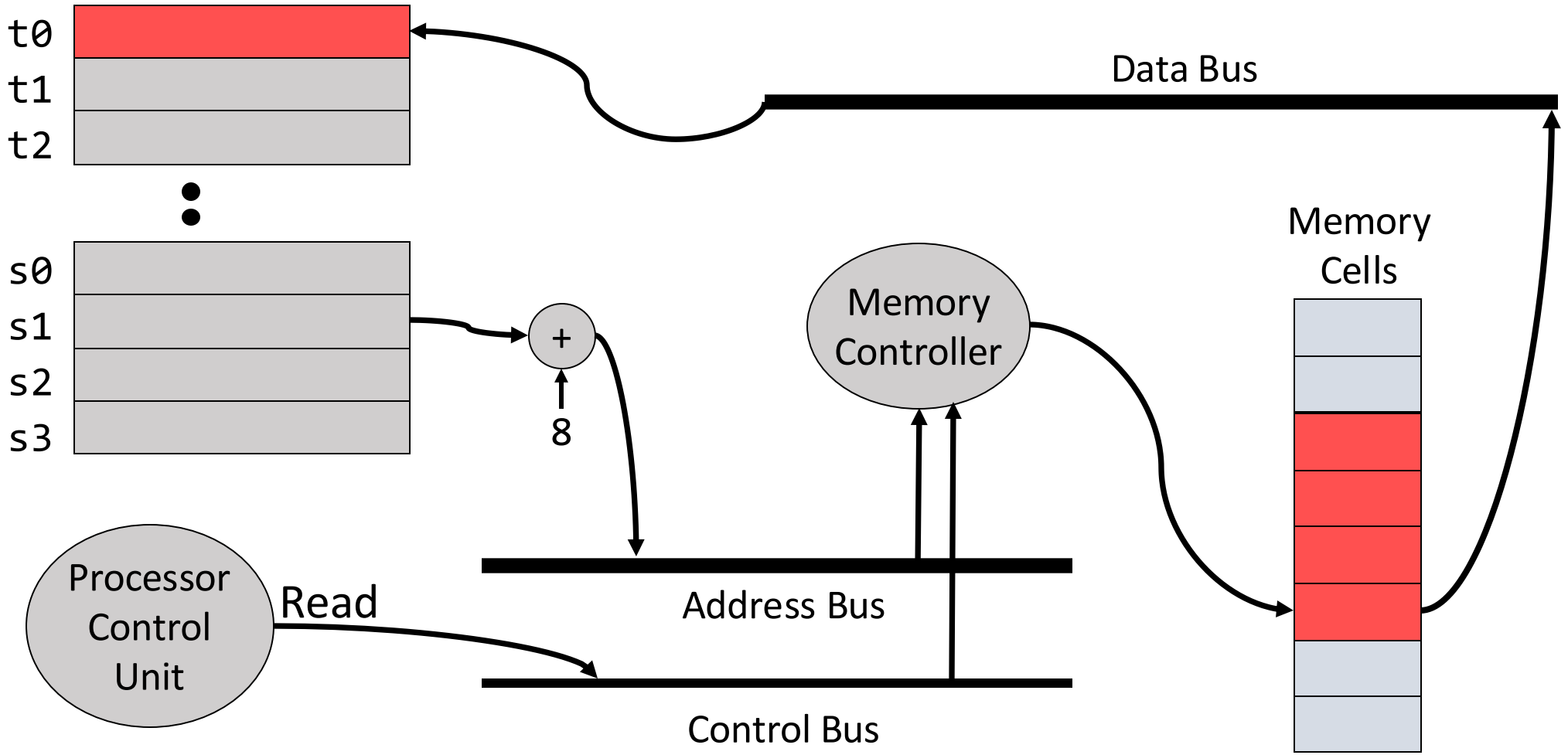
Data Transfer Between
Memory and Registers

Reading: (Section 2.3)

Example of a lw execution

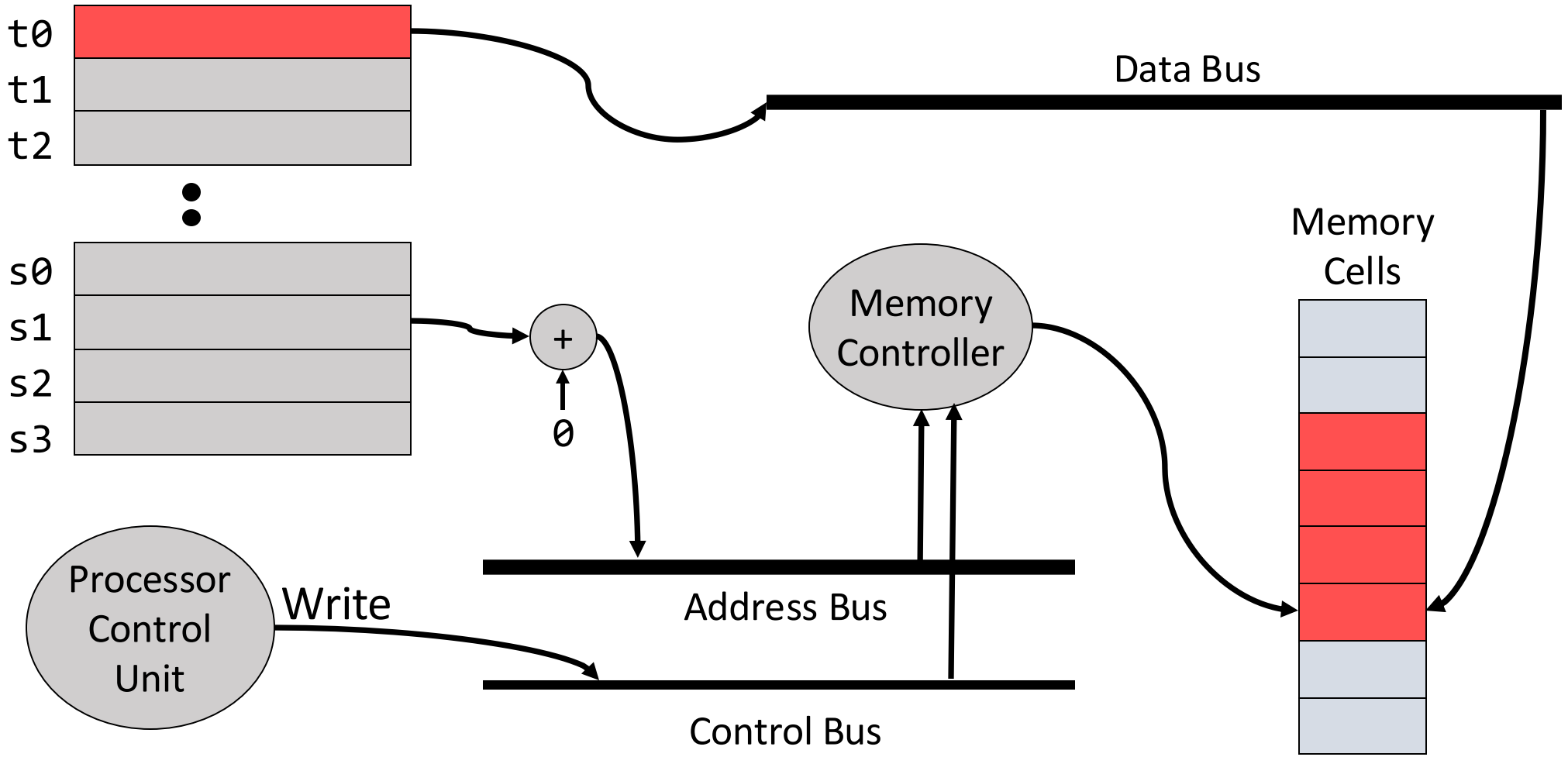
RISC-V assembly

```
lw    t0, 8(s1)    #  t0 ← A[2]
```



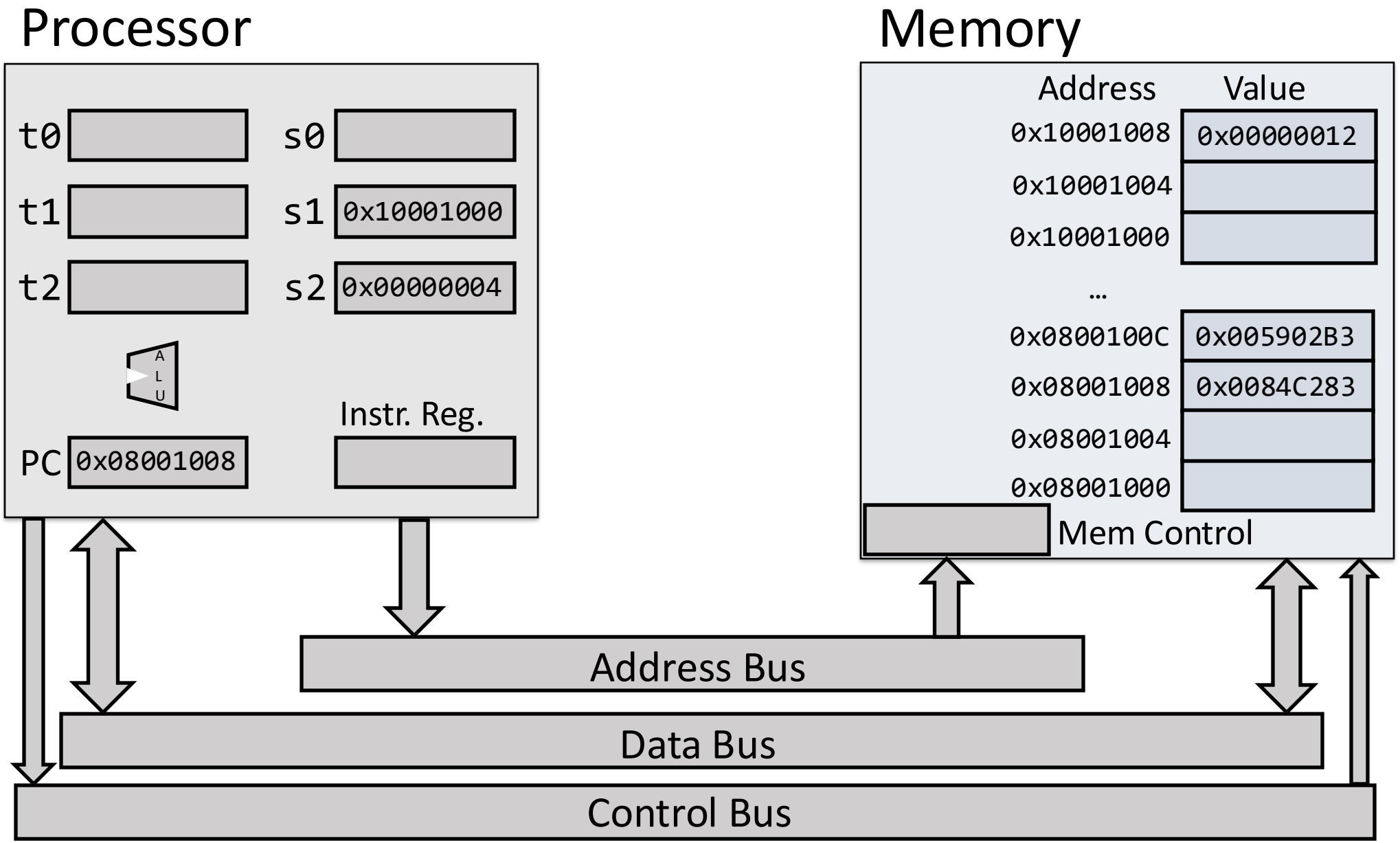
Example of a sw execution

RISC-V assembly `sw t0, 0(s1)` `# A[0] ← t0`

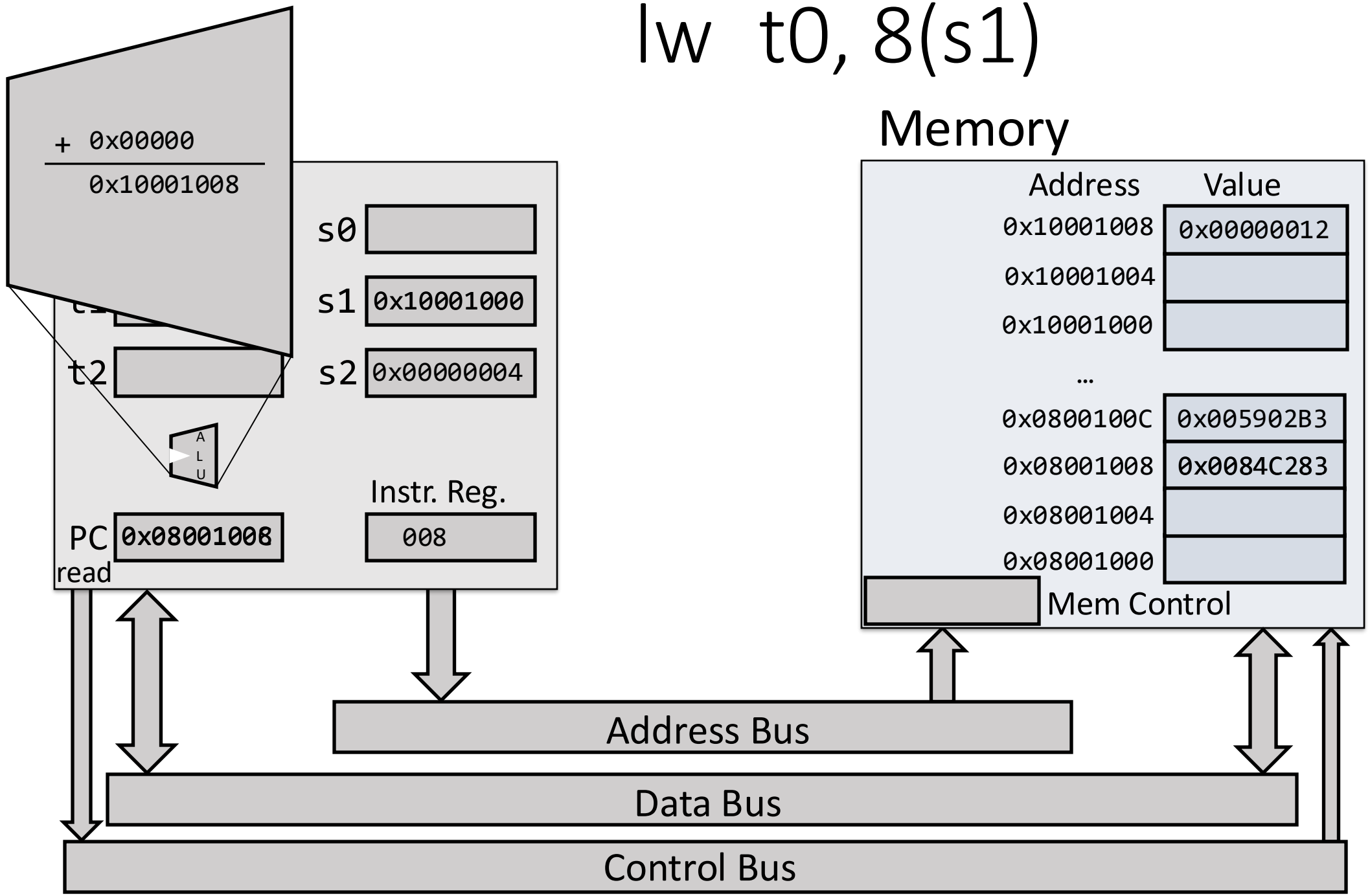


What really happens when a load instruction is executed?

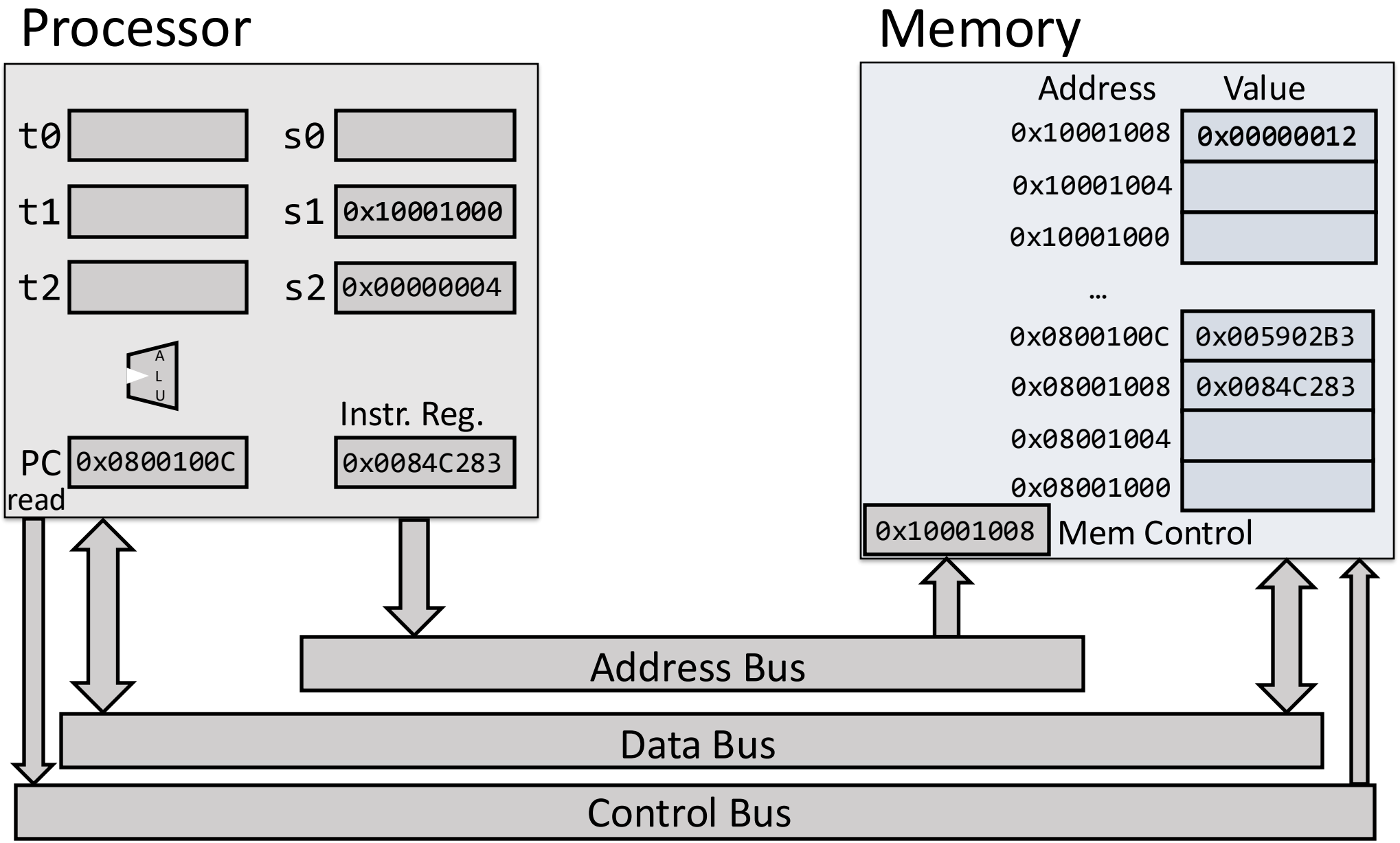
lw t0, 8(s1)


Processor
t0
t1
t2
s0
s1
0x10001000
s2
0x00000004
A
L
U
Instr. Reg.
PC
0x08001008
Memory
Address
Value
0x10001008
0x00000012
0x10001004
0x10001000
…
0x0800100C
0x005902B3
0x08001008
0x0084C283
0x08001004
0x08001000
Mem Control
Address Bus
Data Bus
Control Bus

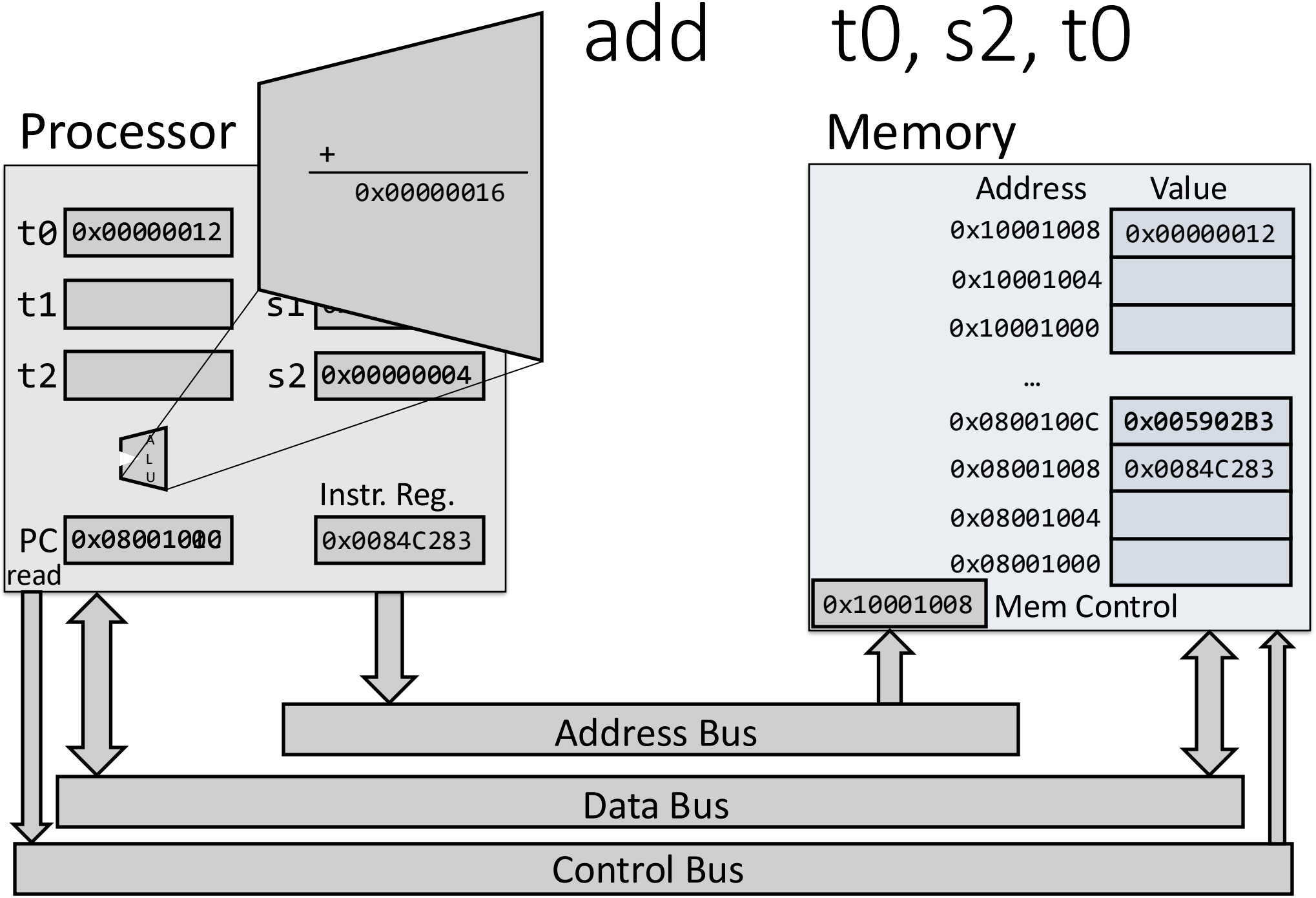
lw t0, 8(s1)


+ 0x00000
0x10001008
s0
s1
0x10001000
t2
s2
0x00000004
A
L
U
Instr. Reg.
PC
0x08001008
008
read
Memory
Address
Value
0x10001008
0x00000012
0x10001004
0x10001000
...
0x0800100C
0x005902B3
0x08001008
0x0084C283
0x08001004
0x08001000
Mem Control
Address Bus
Data Bus
Control Bus

lw t0, 8(s1)


Processor
t0
s0
t1
s1
0x10001000
t2
s2
0x00000004
A
L
U
Instr. Reg.
PC
0x0800100C
0x0084C283
read
Memory
Address
Value
0x10001008
0x00000012
0x10001004
0x10001000
…
0x0800100C
0x005902B3
0x08001008
0x0084C283
0x08001004
0x08001000
0x10001008
Mem Control
Address Bus
Data Bus
Control Bus

add t0, s2, t0


Processor
+
0x00000016
t0
0x00000012
t1
t2
s2
0x00000004
A
L
U
Instr. Reg.
PC
0x08001000
0x0084C283
read
Memory
Address
Value
0x10001008
0x00000012
0x10001004
0x10001000
…
0x0800100C
0x005902B3
0x08001008
0x0084C283
0x08001004
0x08001000
0x10001008
Mem Control
Address Bus
Data Bus
Control Bus

What we learned