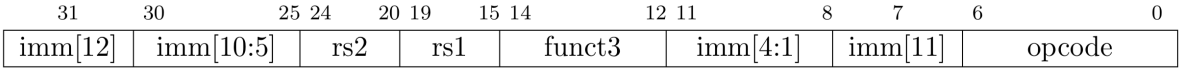
Question 1: (0 points)
Bank of Questions

A RISC-V with a Large Register File (V05, V0A)

RISCV-LRF is a RISC-V instruction-set architecture with a large register file. RISCV-LRF has 128 registers and the instruction formats have to accommodate this change. Consider a branch instruction. Assume that the instruction still has to be 32-bits long and that any changes made to the instruction format only increase/decrease the size of the immediate field. Recall that in the original RISC-V architecture, the branch instruction uses the following format:



Question 2: (10 points)
How many bits are available for the immediate bit field for a branch instruction in RISCV-LRF?

Question 3: (10 points)
How does the range of a branch in RISCV-LRF compares with the range of a branch in the original RISC-V architecture?

Question 4: (20 points)
Assume that in a program that uses RISCV-LRF the current PC address is `0x 0000 0010`. How many branches (no jump instructions) are necessary to get to address `0x FFFF FF00`? Provide the binary representation for the immediate field for the branch(es) instruction(s) required.