Fixed Point FPGA-based Hardware Implementation of a 32-tap Low Pass FIR Filter for Audio Applications

CE-325: Digital System Design | Huzaifah Tariq Ahmed & Samiya Ali Zaidi | Dr. Syed Arsalan Jawed

Description

This project focuses on implementing a 32-tap low-pass Finite Impulse Response (FIR) filter on an FPGA for audio applications. Using a fixed-point representation, the filter is designed to allow frequencies below 500Hz while attenuating those above 1kHz. Verilog code is developed to create the filter's hardware architecture, and audio files are stored in ROM to test the filter's functionality.

Filter Specifications

FIR - Least Squares

1. Transition Band: 500 - 1KHz
2. Sampling Frequency, Fs: 40KHz
3. Order: 31
4. Taps: 32
5. Wpass: 1
6. Wstop: 1
7. Minimum Attenuation: -20dB

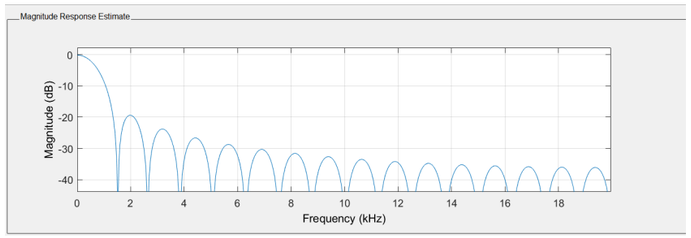


Figure 1: Magnitude Response Estimate of the Designed Filter

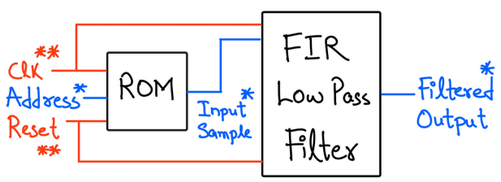


Figure 2: Overall Top Level Architecture

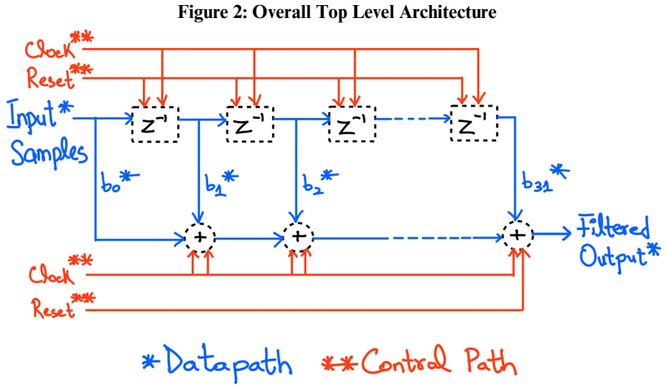
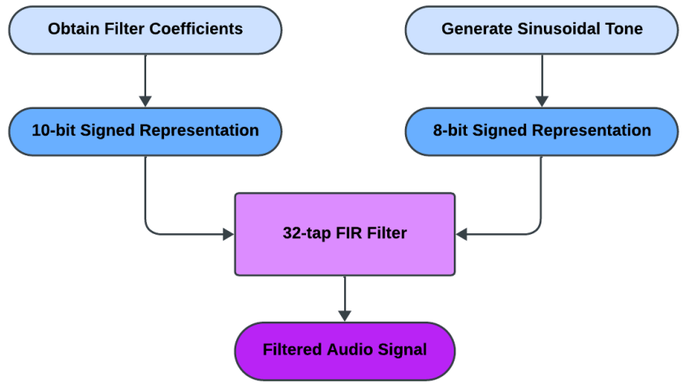
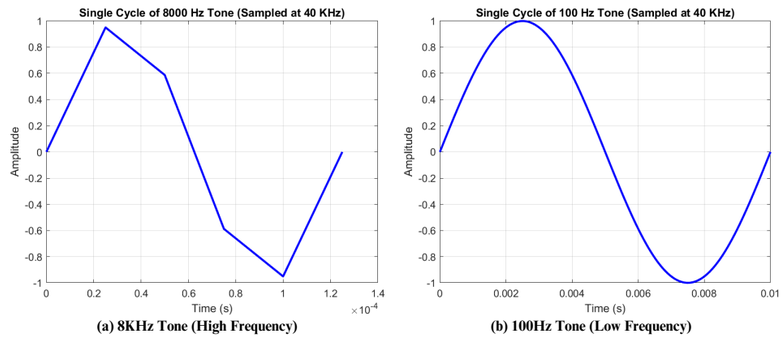


Figure 3: FIR Low Pass Filter Architecture

Methodology



Tones Used



(a) 8KHz Tone (High Frequency) (b) 100Hz Tone (Low Frequency)

Figure 4: Tones Used to Test the Designed Filter

Waveform for the 100Hz Tone

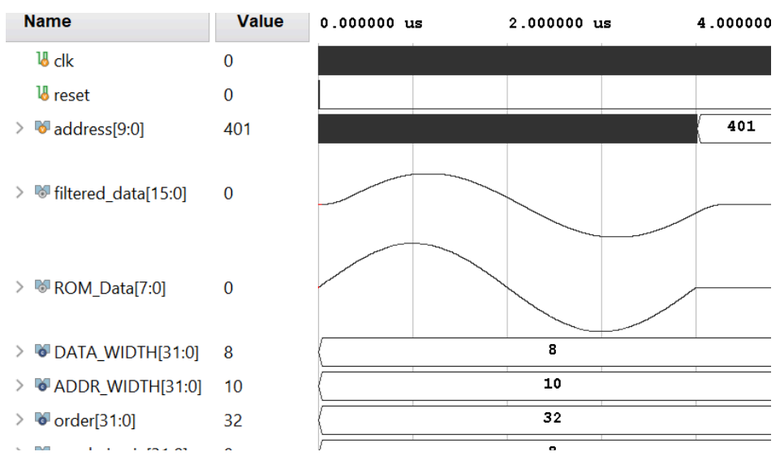


Figure 5: Xilinx Vivado Waveform for 100Hz Tone

Waveform for the 8KHz Tone

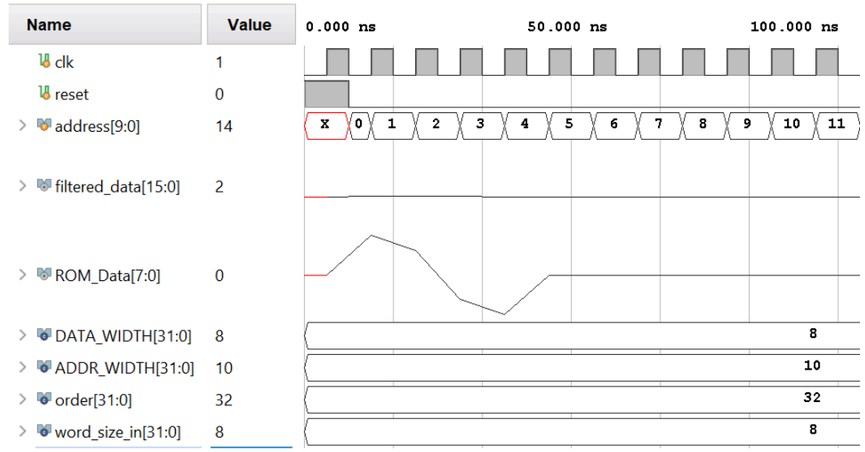
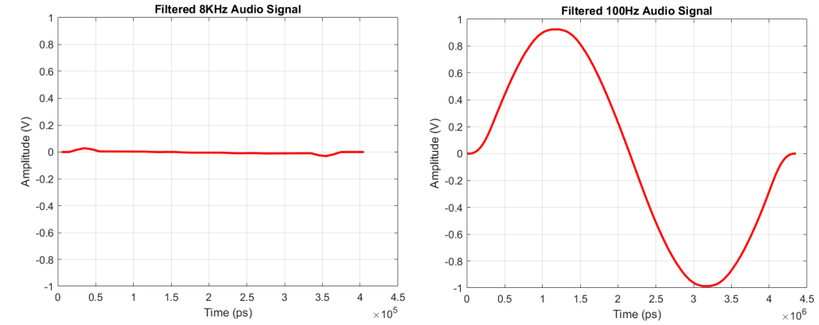


Figure 6: Xilinx Vivado Waveform for 8KHz Tone

Filtered Tones Plotted in MATLAB



(a) 8KHz Tone (High Frequency) (b) 100Hz Tone (Low Frequency)

Figure 7: Filtered Tones Plotted in MATLAB

Conclusion

In conclusion, our project successfully implemented a 32-tap low-pass FIR filter on an FPGA for audio applications. Filter coefficients were scaled from MATLAB for a 10-bit representation, and audio tones were scaled for an 8-bit representation. The Verilog-designed filter effectively attenuated frequencies above 1kHz while allowing those below 500Hz to pass through, as demonstrated by blocking the 8kHz frequency and permitting the 100Hz frequency.

Acknowledgments

We express our sincere gratitude to Dr. Arsalan Jawed for his invaluable guidance and the knowledge imparted through the course Digital System Design.

Tools Used: