No of Pages : 2 **Course Code : 18XW35**

Roll No:
(To be filled in by the candidate)

PSG COLLEGE OF TECHNOLOGY, COIMBATORE - 641 004

SEMESTER EXAMINATIONS, NOVEMBER 2019

MSc - SOFTWARE SYSTEMS Semester : 3

18XW35 MICROPROCESSOR AND EMBEDDED SYSTEMS

Time : 3 Hours **Maximum Marks : 100**

INSTRUCTIONS:

1. Answer **ALL** questions. Each question carries 20 Marks.
2. Subdivision (a) carries 3 marks each, subdivision (b) carries 7 marks each and subdivision (c) carries 10 marks each.
3. Course Outcome :

Qn.1	CO 1	Qn.2	CO2	Qn.3	CO3	Qn.4	CO4	Qn.5	CO5

Table

1. a) "Instruction set architecture is an abstraction to the processor architecture". Comment on this statement.

   b) i) What do you mean by byte and word addressable memory layout? (3)

   ii) The performance of a pipeline processor is much harder to predict and may vary more widely between different programs. Is this statement true? Justify your answer. (4)

   c) State and explain the instruction formats of 8086 with proper instructions that vary in the length as an example.

2. a) To avoid bubbles in pipeline, instruction shuffling is one of the most well-known technique to be followed. But how does instruction shuffling preserve the semantic of the program?

   b) i) Complex instructions simplify programming side but makes compiler complicated". Is it true? Justify (3)

   ii) What is the purpose of splitting the memory as odd and even banks? How will it behave while reading/writing byte or word from memory in the context of 8086 architecture? (4)

   c) Explain the various pipeline architectures in processor and discuss about its issues, merits and demerits. Also explain the techniques to effectively explore the advantages of pipeline architecture.

3. a) How stack will be used in case of register spilling in your program?

   b) i) What is the functional difference between *ret* and *iret* instructions? (3)

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ii) Differentiate between vectored and non-vectored interrupt. (4)

c) Describe the primitive steps to write interrupt service routine and handling of IVT. Also discuss about how interrupt is handled using 8259A PIC with neat diagram.

4. a) "Pentium processor is a CISC processor with a RISC feature". What does it mean?

b) i) In which case, the fetching stage of a pipeline will use the content of the TLB in Pentium architecture? (3)

ii) How IVT is manipulated while processor is working in protected mode? (4)

c) Discuss about the architecture and the purpose of 8255 PPI (Programmable Peripheral Interface) and explain how it is used to drive a multiple 7 segment display unit.

5. a) How does real time embedded system differ from non-real time system?

b) i) How task scheduling is done in real time operating system? . (3)

ii) Describe the working principle of watchdog timer in embedded system. (4)

c) Explain the architecture of Pentium processor of Intel by highlighting it features. Also explain about how protected mode is implemented in x86 based processor.

/END/

FD/JU