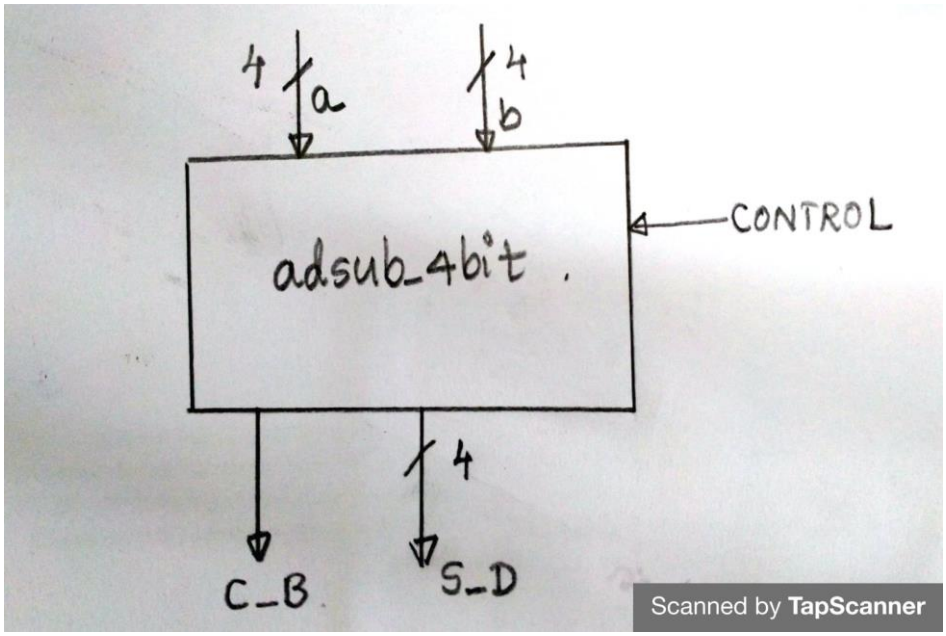
1. Write a structural style VHDL code for a 4bit adder/subtractor. The 4bit adder/subtractor comprises of 1 bit full adders. Use suitable switches for inputs and LEDs for outputs in the CPLD board.



---------- VHDL CODE FOR 4_BIT ADDER_SUBTRATCOR WITH CONTROL SIGNAL----------

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
--define the entity with ports
entity adsub_4bit is
Port ( a : in STD_LOGIC_VECTOR (3 downto 0);



    );
end adsub_4bit;

-----DEFINE THE ARCHITECTURE FOR ADDER_SUBTRACTOR
architecture rtl of adsub_4bit is
--DEFINE THE COMPONENT FULL ADDER USED-----
```

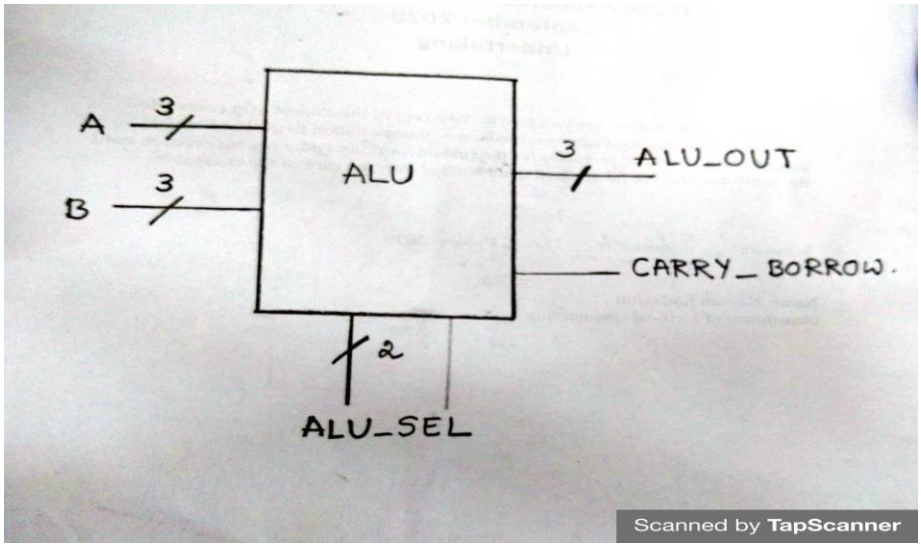
```
--DEFINE THE INTERMEDIATE  SIGNALS IF REQUIRED-----
--DEFINE THE  FUNCTIONALITY WITH STRUCTURAL MODELING--
begin
end rtl;

----------VHDL CODE FOR 1 bit full adder----------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
--Define input and output ports
entity fulladder is
Port ( x : in STD_LOGIC;
y : in STD_LOGIC;
z : in STD_LOGIC;
sum : out STD_LOGIC;
cout : out STD_LOGIC);
end fulladder;

--Defining the architecture of full adder in dataflow modelling style
architecture b_fa of fulladder is
begin
sum =x xor y xor z;
cout = (x and y) or (x and z) or (y and z);
end b_fa;
```

2. Write a behavioural style VHDL code for an ALU described below.

Select inputs	ALU operation
00	A+B
01	A-B
10	A and B
11	A xor B



----------VHDL CODE FOR 3-BIT ALU----------

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use ieee.NUMERIC_STD.all; ---------- USED FOR ARITHMETIC COMPUTATIONS.
----------DECLARE THE ENTITY----------
entity ALU is
    Port (
    A, B  : in  STD_LOGIC_VECTOR(2 downto 0);  -- 2 inputs 3-bit
    --- ENTER THE REMAING PORTS-------
          );
end ALU;
--------- WRITE THE ARCHITECTURE IN BEHAVIOURAL MODELLING STYLE WITH CONDITIONAL STATEMENTS----------
```

```
architecture Behavioral_ALU of ALU is
---------DECLARE THE SIGNALS IF REQUIRED---------
begin



end Behavioral_ALU;
```