EE214 : Digital Systems Lab
Lab 1

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1 Aim

To design an optimal circuit for the given problem and implement them using the both 2 input logic gates and 4:1 multiplexer.

2 Summary of the experiment

Problem Statement:
Four switches (SW1, SW2, SW3, SW4) are a part of the control circuitry in a copying machine. Switches are at various points along the path of the copy paper. Each switch is normally open and as the paper passes over a switch, the switch closes. (Switch gives a '1' when closed and a '0' when open) It is impossible for switches SW1 and SW4 to be closed simultaneously. Design a logic circuit to produce a 'HIGH' output whenever two or more switches are closed at the same time. Assume SW1 to be MSB. Design the above using:

1. Suitable 2- input Logic gates
2. 4:1 mux and suitable 2-input logic gates

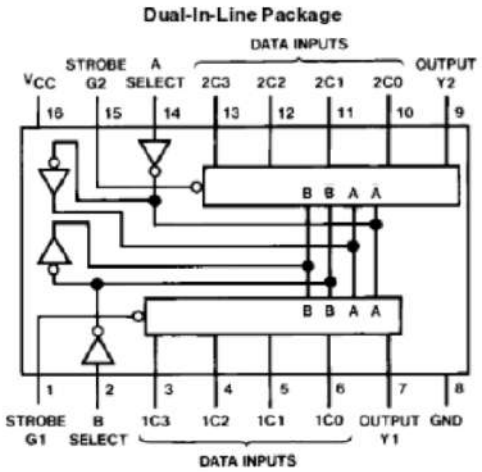
3 Components used:

IC 74153(4:1 MUX) 7408(AND), 7432(OR), resistor array, DIP switches, LED displays, breadboard, power supply.

3.1 IC chips circuitry:

Connection Diagram

Dual-In-Line Package



Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

Figure 2. Function Table and Connection Diagram of 74153

Figure 1: IC HCF 4007

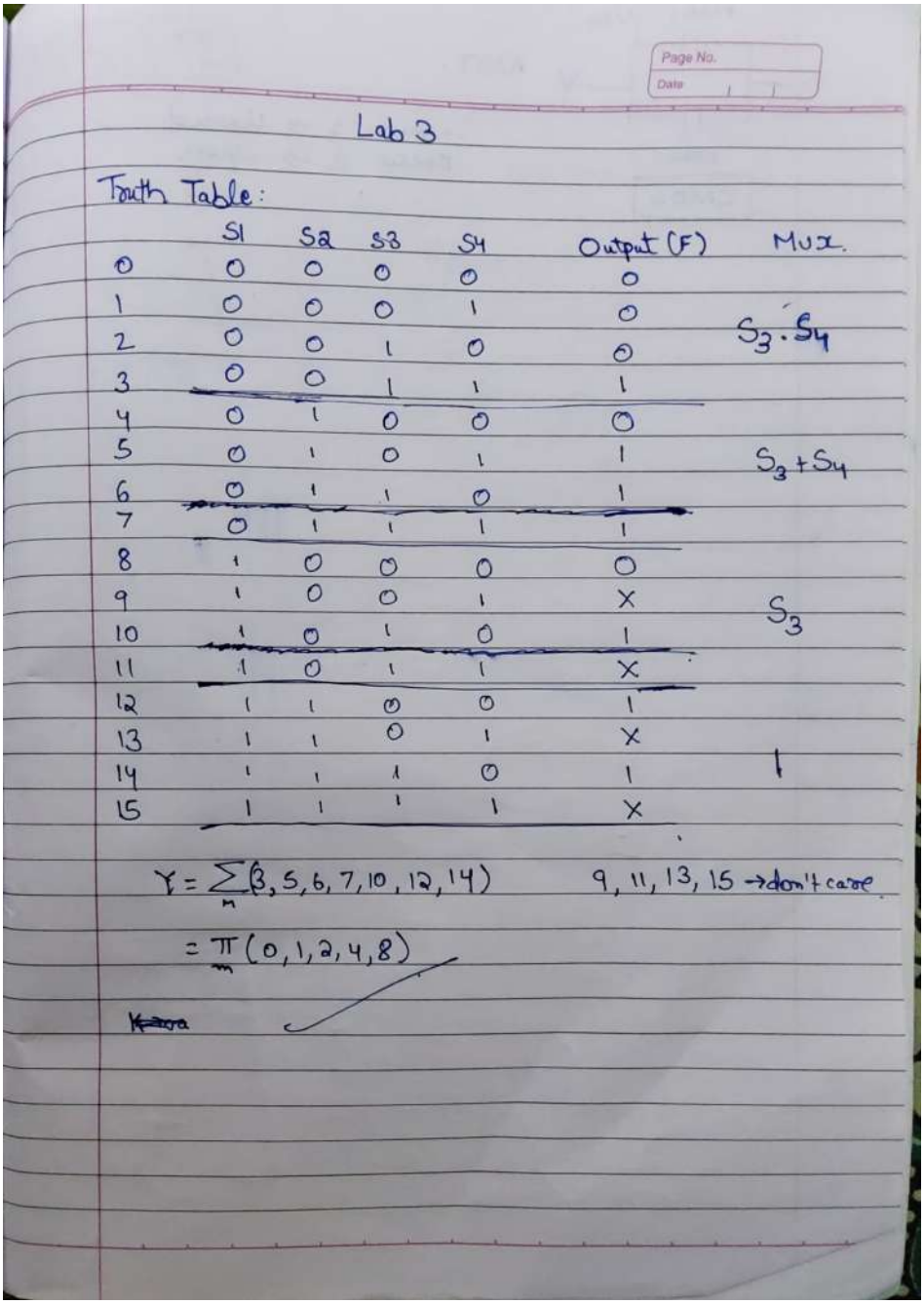
4 Design Procedure:

We can design a truth table following the logic given in the question, which can be seen in the figure. Then we have to use a K-MAP to simplify the circuit and then use boolean algebra logic to further simplify the POS form. These Truth table and simplifications can be seen in the next section.

This simplified expression can be modelled using 3 (2 input) OR gates and 2 (2 input) AND gates.

The signals S1, S2, act as select lines for MUX and S3 and S4 can be given as the input to the MUX in the way mentioned in the figure to achieve the required logic.

5 Simplification and Truth Tables:



Lab 3

Truth Table:

	S1	S2	S3	S4	Output (F)	Mux.
0	0	0	0	0	0	
1	0	0	0	1	0	
2	0	0	1	0	0	$S_3 \cdot S_4$
3	0	0	1	1	1	
4	0	1	0	0	0	
5	0	1	0	1	1	$S_3 + S_4$
6	0	1	1	0	1	
7	0	1	1	1	1	
8	1	0	0	0	0	
9	1	0	0	1	X	
10	1	0	1	0	1	S_3
11	1	0	1	1	X	
12	1	1	0	0	1	
13	1	1	0	1	X	
14	1	1	1	0	1	1
15	1	1	1	1	X	

$Y = \sum_m (3, 5, 6, 7, 10, 12, 14)$ 9, 11, 13, 15 → don't care

$= \prod_m (0, 1, 2, 4, 8)$

Figure 2: Truth Table and Simplification

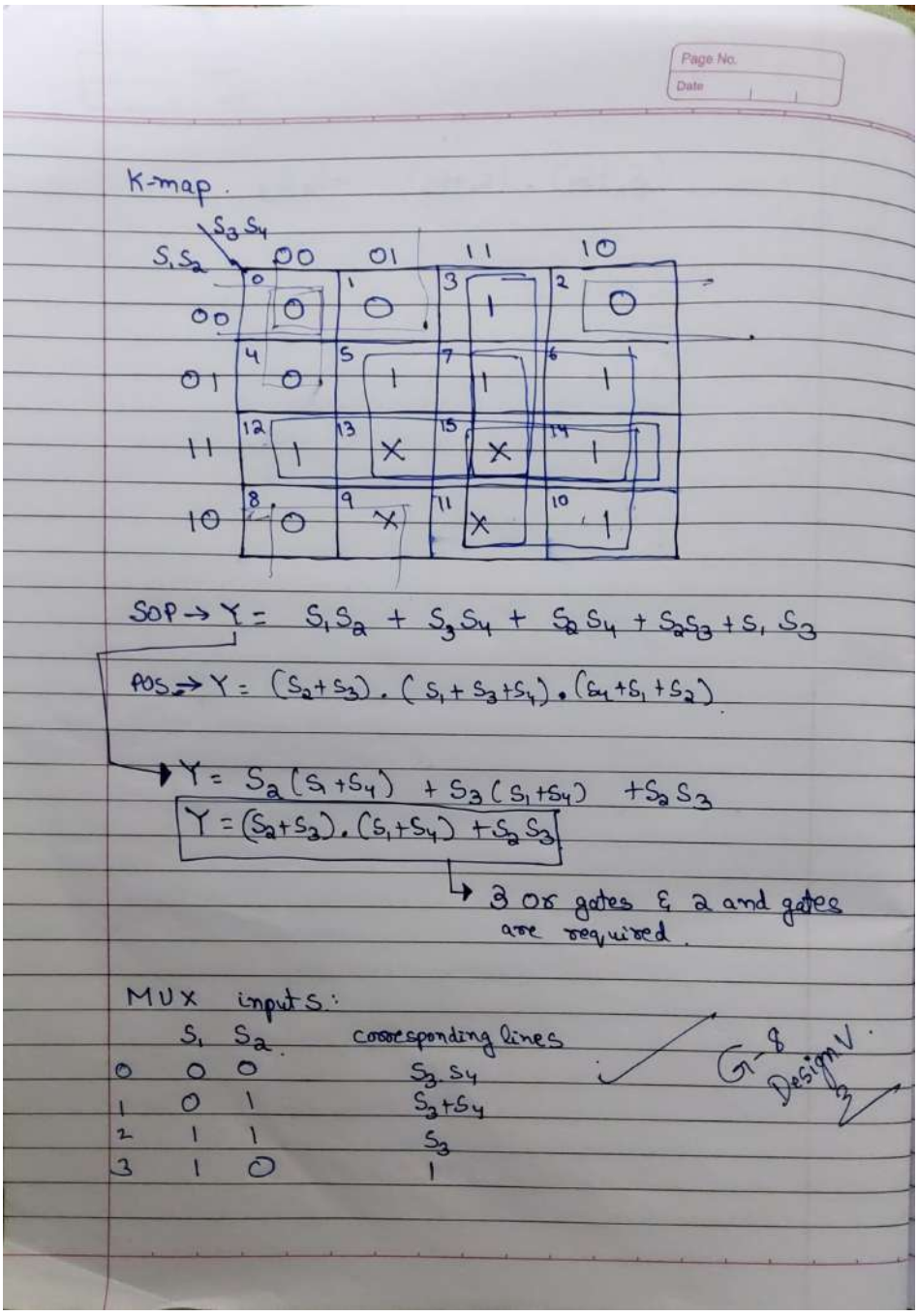


Figure 3: Truth Table and Simplification

6 Circuit Snapshots:

I have attached 4 states of each of the required circuits here, however all the 16 states can be seen in the drive folder, which is given below.

Link to drive containing all the images: `https://drive.google.com/drive/folders/1c7uESPDe_aDJag6hfm4VUHU6UCmdx9usp=sharing`

6.1 Design using logic gates:

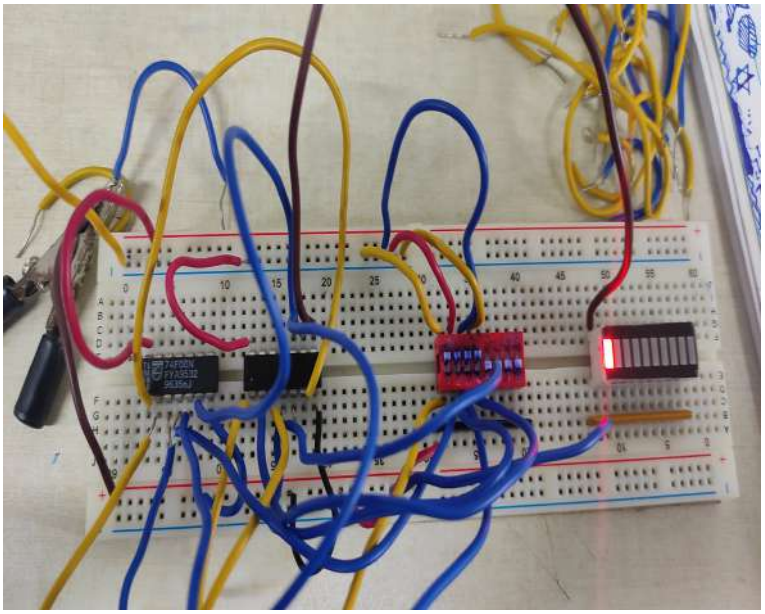


Figure 4: Logic Gate state 1

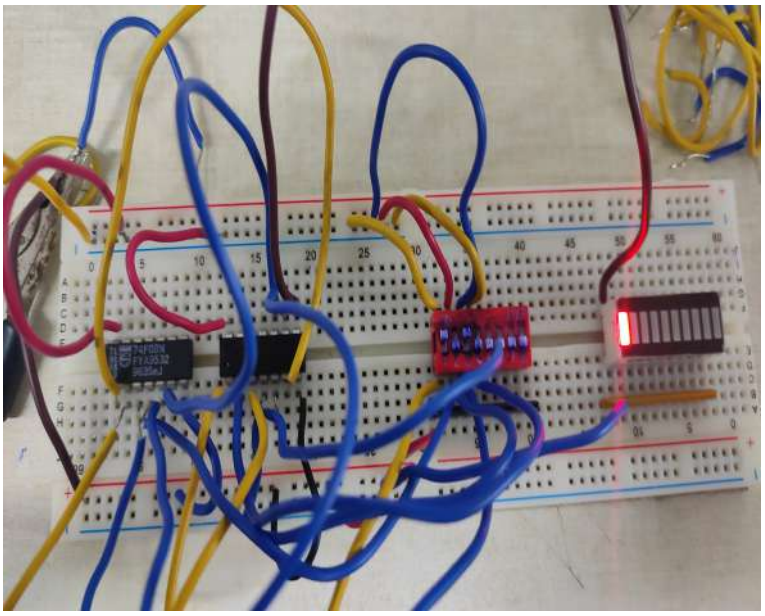


Figure 5: Logic Gate state 2

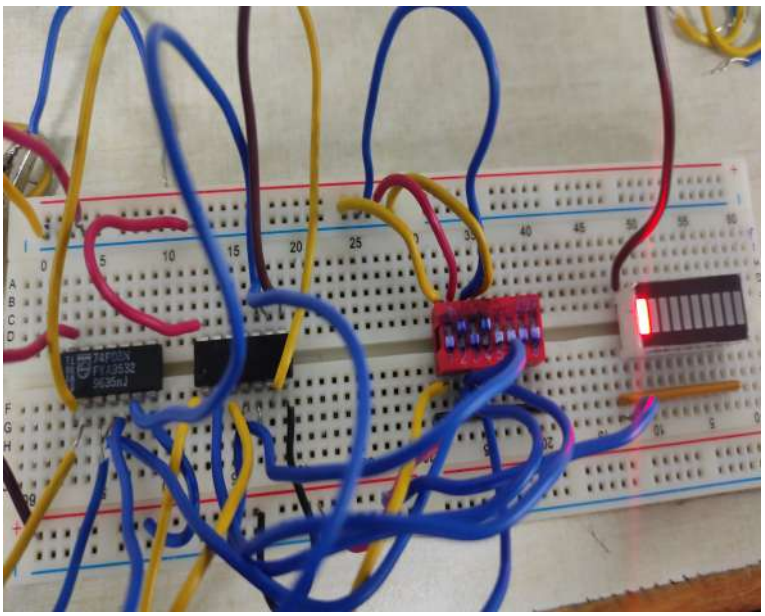


Figure 6: Logic Gate state 3

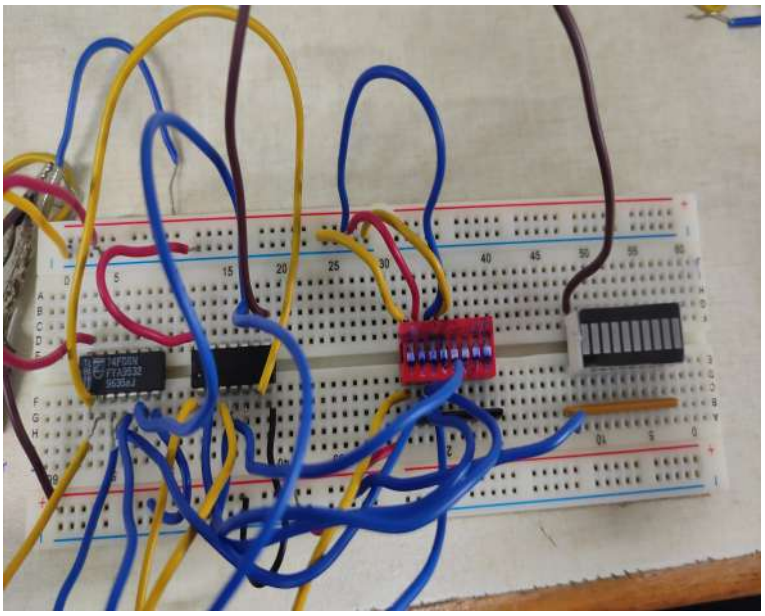


Figure 7: Logic Gate state 4

6.2 Design using multiplexer:

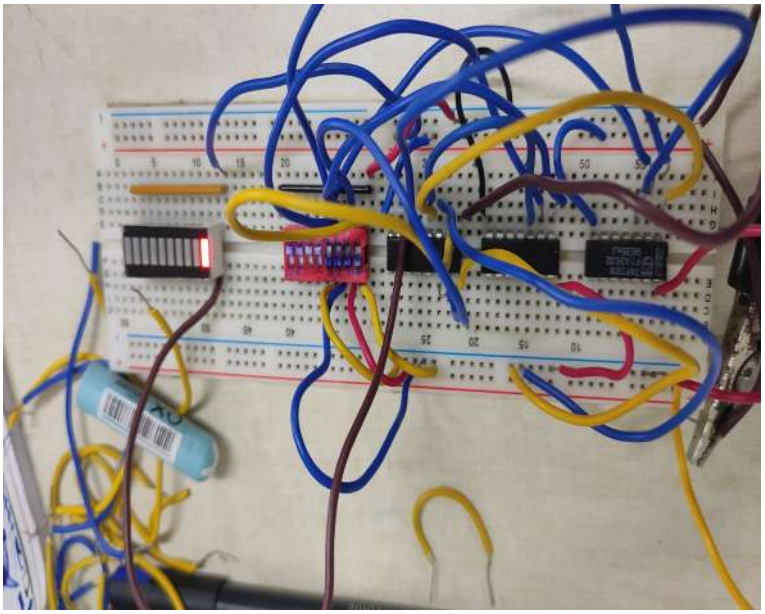


Figure 8: MUX state 1

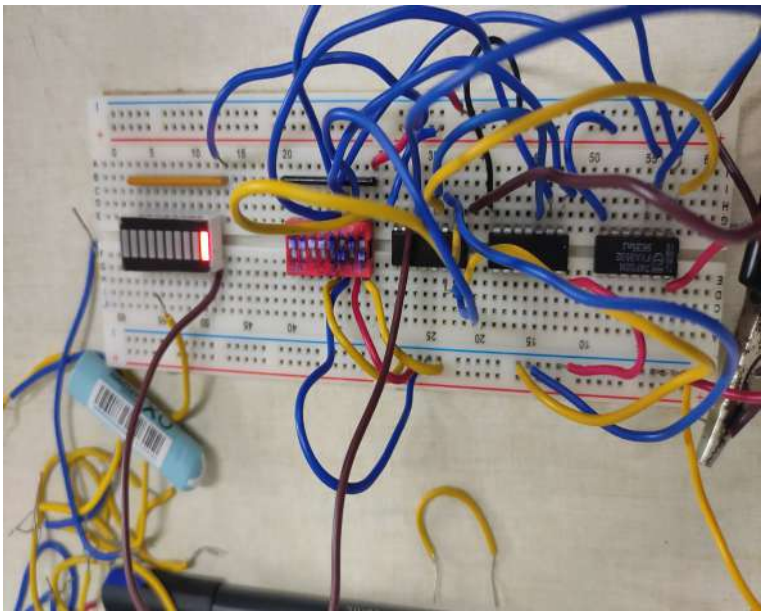


Figure 9: MUX state 2

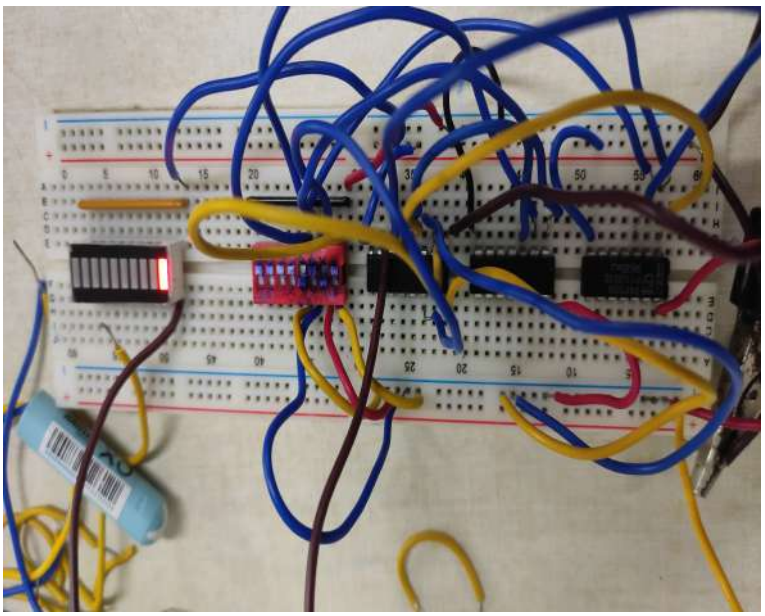


Figure 10: MUX state 3

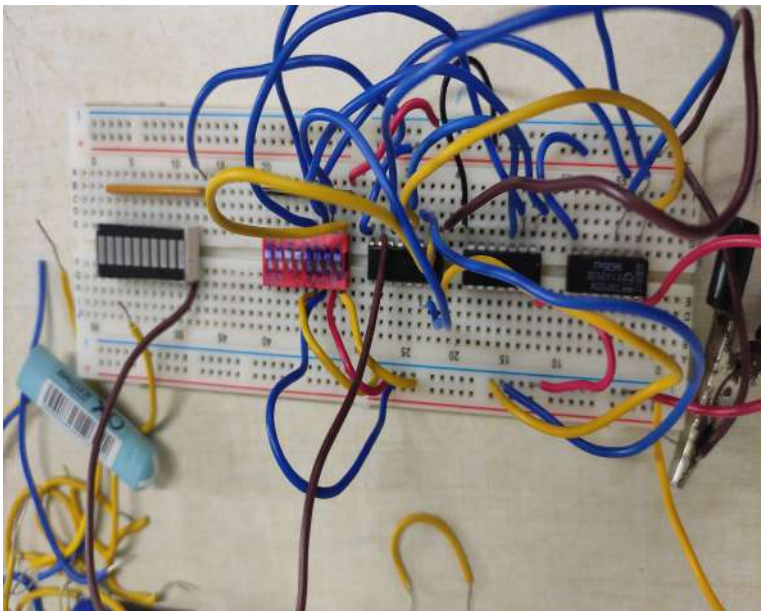


Figure 11: MUX state 4

7 Results and Discussions:

The snapshots corresponding to each of the gates exactly represents the required logic logic hence we have implemented the solution using both 2 input basic logic gates and the 4:1 MUX.

8 Conclusion:

We have designed the optimal circuit for the given problem and implemented it using the both 2 input logic gates and 4:1 multiplexer.