Experiment-5

NMOS Common Source Amplifier Characteristics

Simulation Exercise

1. Use the following model of CD 4007 to write the netlist of a common source amplifier:

   *CD4007 MOS Array

   * N4007 (NMOS on CD4007 CMOS integrated circuit)

   .model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6

   + Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)

   * P4007 (PMOS on CD4007 CMOS integrated circuit)

   .model MP4007 PMOS (Kp=500u Vto=-1.5 Lambda=0.04 Gamma=0.6

   + Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=4.0p Cbs=4.0p Pb=.8 Cgso=0.2p Cgdo=0.2p Is=16.64p N=1)

2. Use the NMOS model of the IC and write a netlist to plot I_D vs V_{DS} characteristics for the same with the voltage VGS varied from 0 V to 5 V in steps of 0.2 V.
3. Show all the curves on a single plot.
4. First voltage sweep (V_{DS}) is for X-axis and second voltage sweep (V_{GS}) is for different sets.
   (a) From these characteristics, obtain r_{DS} (linear region) for each value of V_{GS}.
   (b) Also, obtain r_0 in saturation region.
5. Estimate the value of threshold voltage by writing a ngspice netlist to plot I_D vs V_{GS} by varying V_{GS} from 0 to 5 V.
6. Now design a NMOS common source amplifier as shown in Figure 1 (obtain the values of R_2, and R_D) for I_D = 1.5 mA, V_{DS} = 4 V, V_{GS} =3 V, V_{DD}= 10 V (let R_1 = 7.5 k). (You need not connect the capacitors and load resistor at this stage).

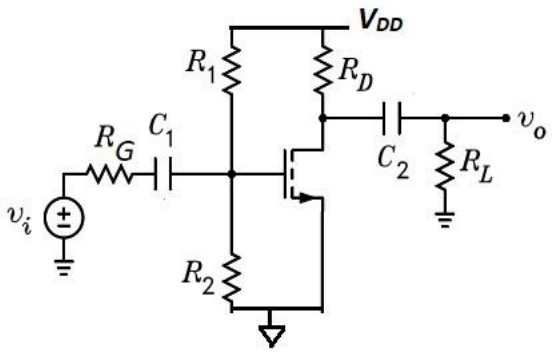

Figure 1

7. Write the netlist for your designed circuit.

8. Run the simulation and verify the results with your calculated values

9. Let the values of all the capacitors be 2.2 μF and R_L=100 k, observe the output voltage waveform and input voltage waveform for V_{in} = 200 mVp−p at 1kHz.

10. Measure the frequency response of the amplifier by varying the frequency from 10 Hz to 1 MHz.

Hardware Exercise Objectives:

1. To study the effect of proper biasing on the performance of NMOS Common Source amplifier
2. To study the frequency response of the CS amplifier

Equipment/Components Required:

1. MOSFET IC – CD 4007
2. Resistors of suitable values
3. Capacitors – 2.2 μF
4. Regulated power supply – 10V
5. Arbitrary Function Generator
6. Digital Storage Oscilloscope

Steps:

1. Wire up the circuit as shown in Figure 1 with suitable values of the resistors. Make sure that the NMOS is operating in saturation region. The body terminals of all the NMOS transistors are connected together and brought out on pin 7. Therefore, always connect pin 7 to the lowest potential. The body terminal of all the PMOS transistors

are connected together and brought out on pin 14. Therefore, always connect pin 14 to the highest DC voltage in your circuit.

2. Bias the circuit using regulated power supply and take the input from AFG. Check your calculations against measurements made with a sinusoidal signal having frequency of 2 kHz (use oscilloscope, not multi-meter). Keep the input voltage sufficiently small so as to give an undistorted output.
3. Fix the amplitude of the sinusoidal input to 200 mV_{p-p} and vary the frequency from 30 Hz to 1.5 MHz.
4. Observe the input and output waveforms on DSO. Observe and calculate the voltage gains.
5. Increase the input amplitude to 200 mV_{p-p} to $2V_{p-p}$ in steps of 500 mV and study the frequency characteristics of the amplifier circuit. Is the output signal distorted?
6. Plot the frequency responses of the amplifier (log-log plot) and comment on the salient features you observe.