Lab-6 Report

SOP Implementation with 4:1 Multiplexer

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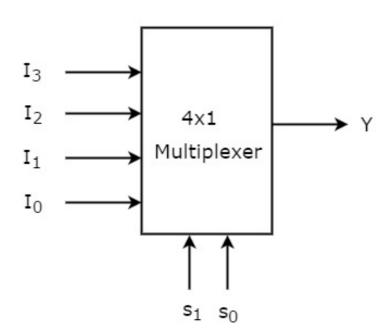
<u>Aim</u>: Implement following SOP with 4:1 MUX. Treat A, B as select lines (S_1, S_0) .

$$Y = f(A, B, C, D) = \Sigma m(3,5,7,10,12,15) + d(9,11,13,14)$$

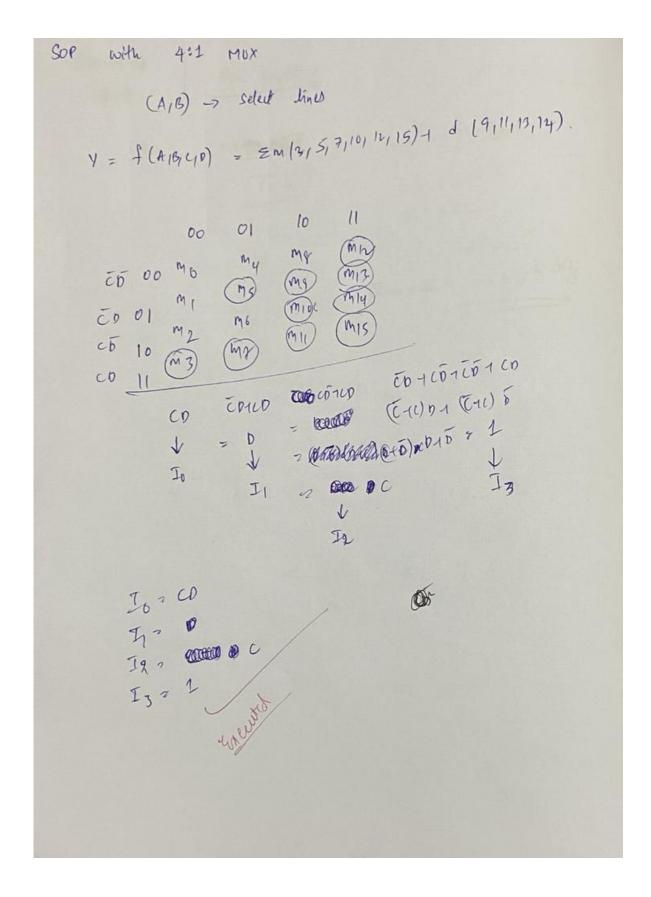
Components used:

- 1. Digital MUX DM74153
- **2.** Digital AND gate 7408
- **3.** Power supply
- **4.** Breadboard
- **5.** 1k resistor arrays (X2)
- **6.** LED display
- **7.** DIP switches

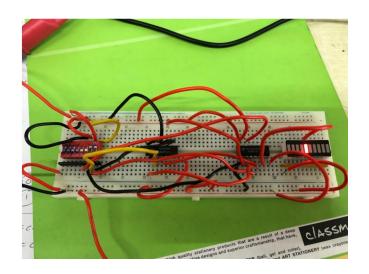
Diagram of 4:1 MUX:

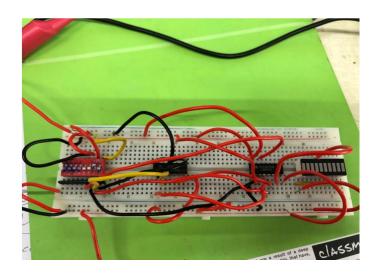


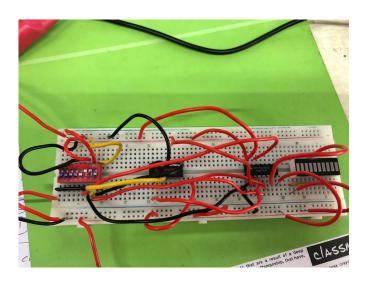
Design Procedure & Circuit diagram:

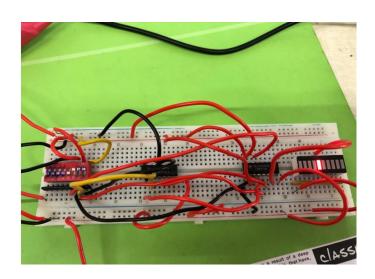


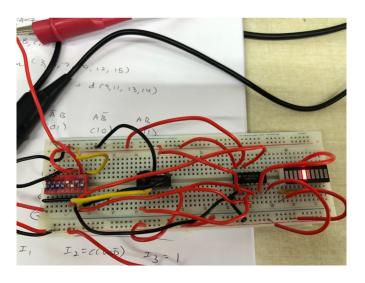
Snapshots of MUX implementation:

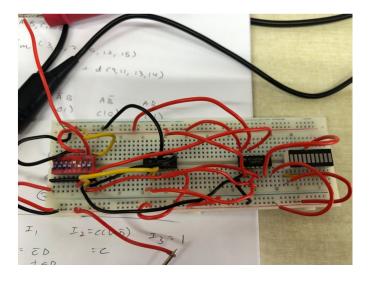


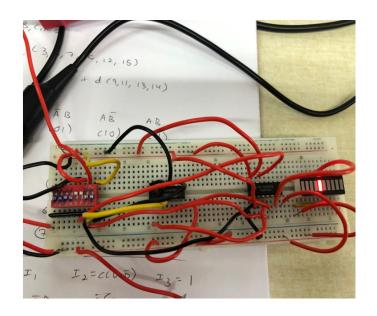


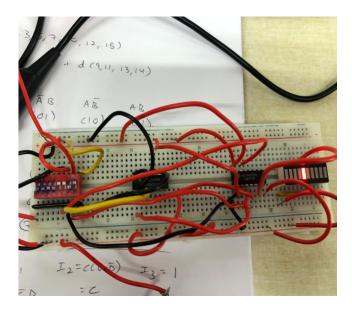


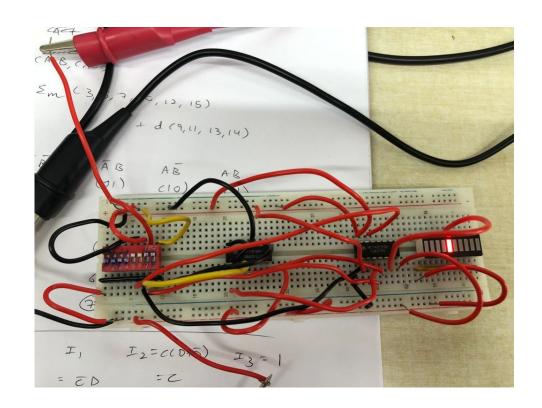




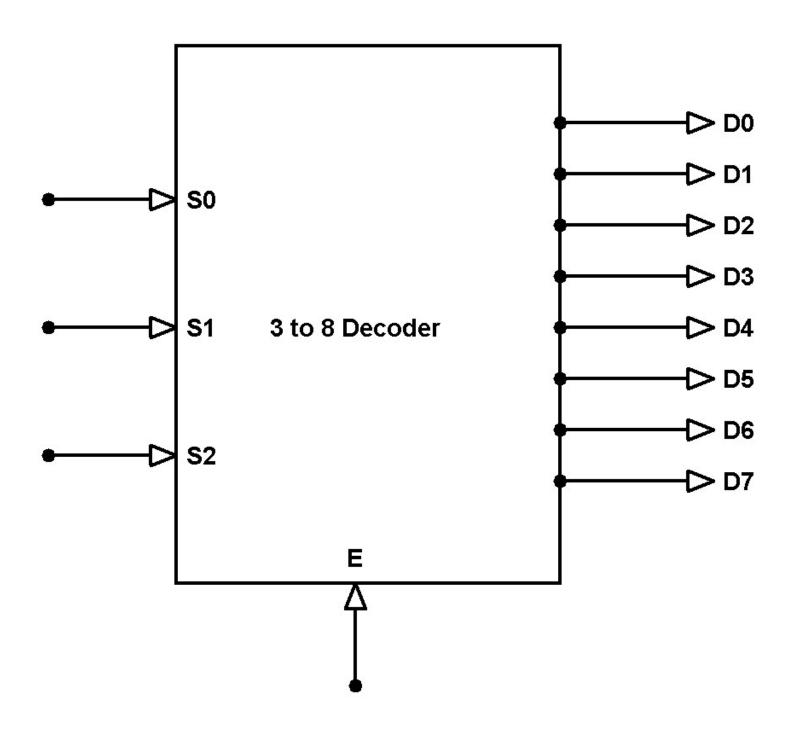




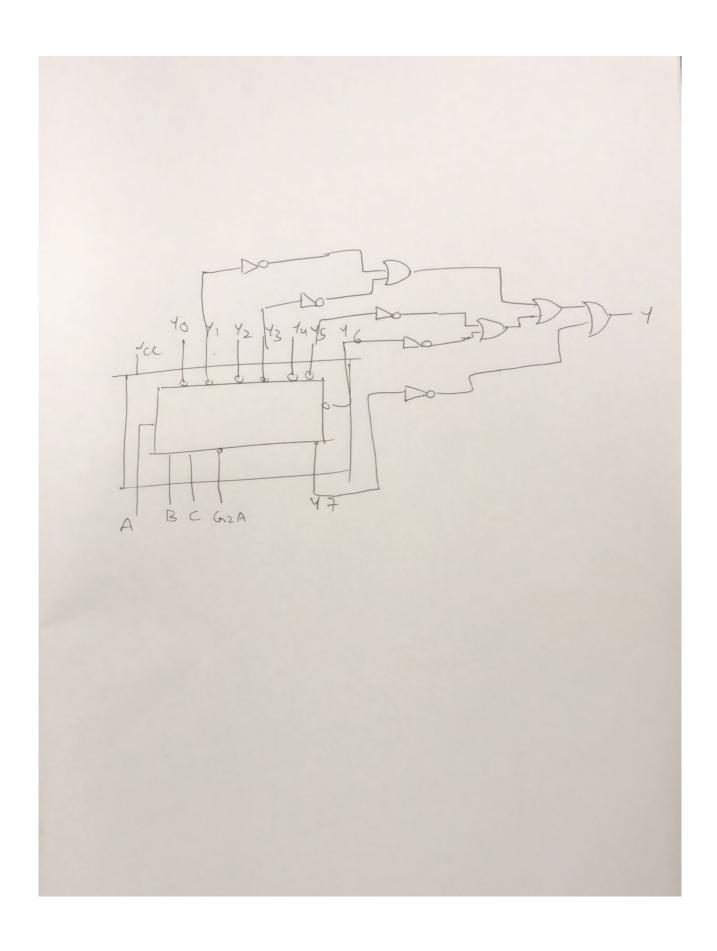




Decoder:



Design Procedure & Circuit diagram:



Results and Discussions:

The snapshots corresponding to each of the MUX states exactly represents the required logic represented by the minimized logic expressions. Hence we have implemented the following SOP with 4:1 MUX. Treat A, B as select lines (S_1 , S_0).

Conclusions:

I've learnt that Digital IC MUX DM74153 and 3:8 Decoder can be used to implement SOP minimized boolean expression, obtained. The inputs for selector lines to Multiplexers are given via switches and the outputs are observed through LEDs. I explored the technicalities involved with multiplexers and decoders, and also learnt how to operate as per the SOP function.