

Lab-10 Report

MOD-8 & MOD-6 Asynchronous Up-Counters

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Aim of the experiment:

1. Design and implement a mod-8 asynchronous up counter. Clearly indicate the minimum number of JK Flip-flops required (if any) and NAND gates required (if any).
2. Design and implement a mod-6 asynchronous up counter. Clearly indicate the minimum number of JK Flip-flops required (if any) and NAND gates required (if any).

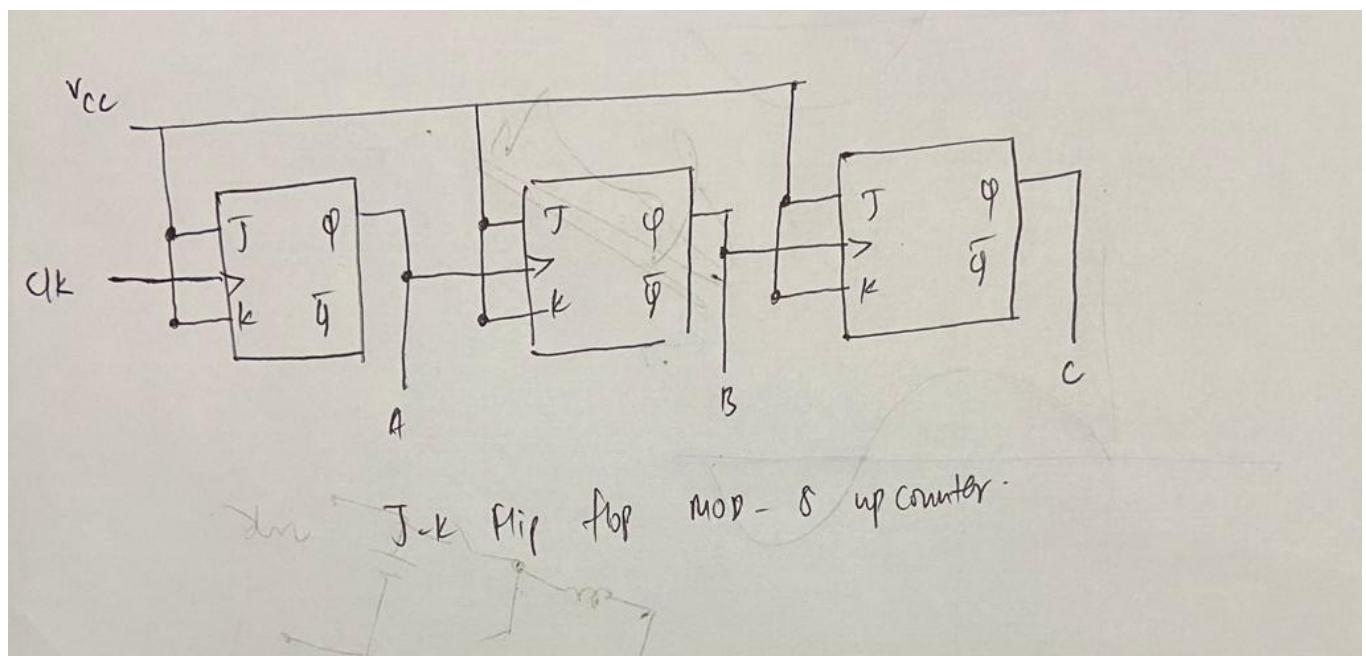
Components used:

1. SN7476 - DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR
2. IC-7400 - NAND gate
3. Power supply
4. Breadboard
5. 1k resistor arrays (X2)
6. LED display

Design Procedure & Circuit diagram:

For mod-8 asynchronous up-counter, the design procedure requires 3 JK flip-flops connected in series with the output Q given as clock signal to the next flip-flop and \bar{Q} as output from each of the flip-flops.

This implementation using JK flip-flops is given as,



Similarly, for mod-6 asynchronous up-counter, the design procedure requires 3 JK flip-flops connected in series with the output Q given as clock signal to the next flip-flop and Q as output from each of the flip-flops and also by seeing the truth table we can find the following inference

We use IC 7400(NAND gate), for converting the initial Mod 8 design to Mod 6 design.

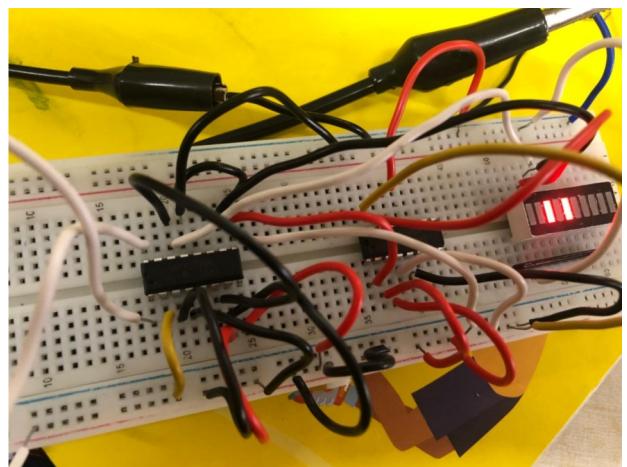
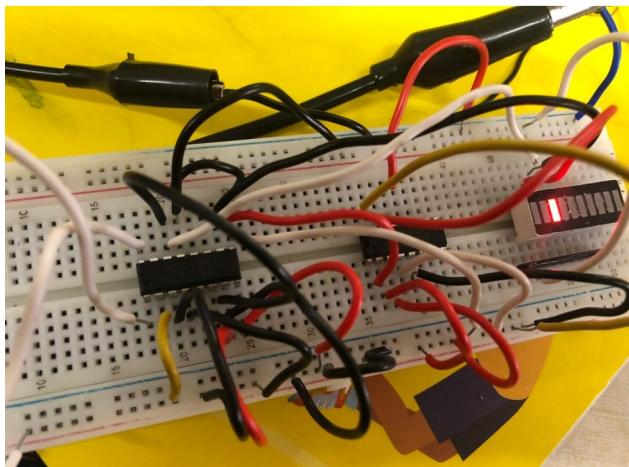
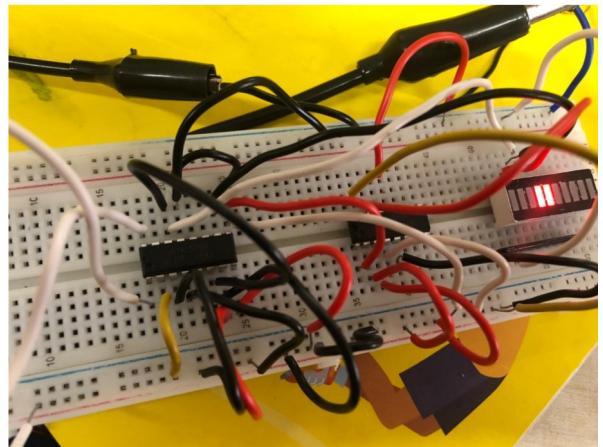
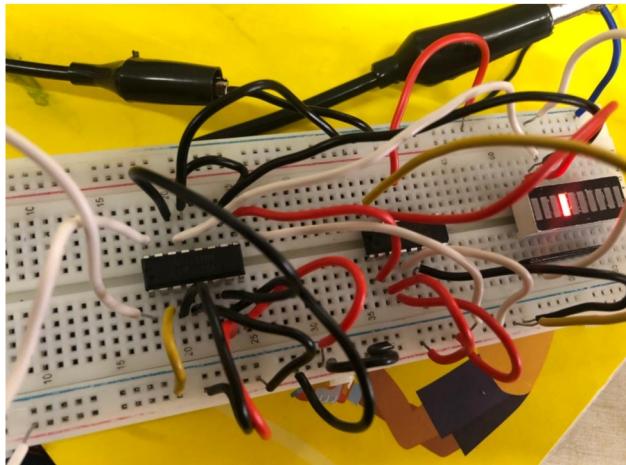
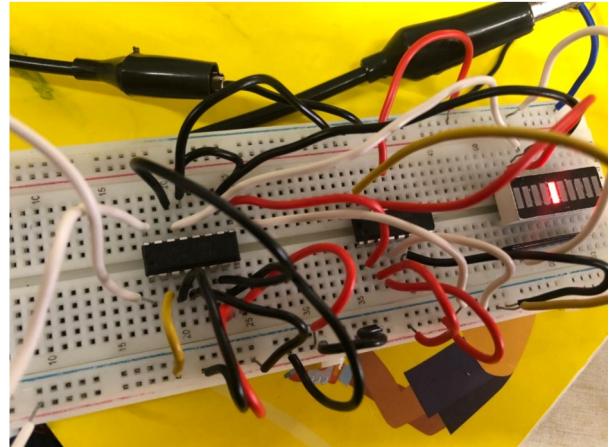
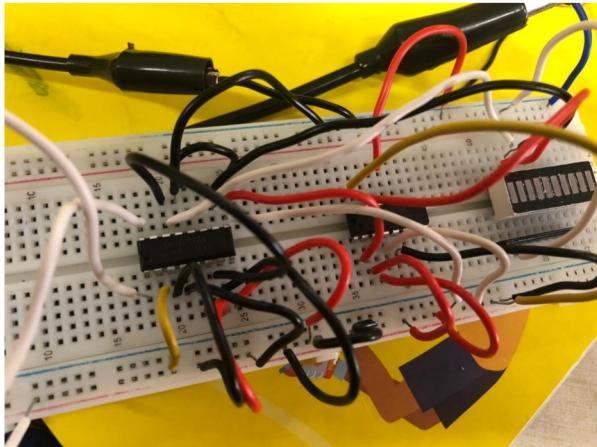
Logic design for Mod – 8 Asynchronous counter is

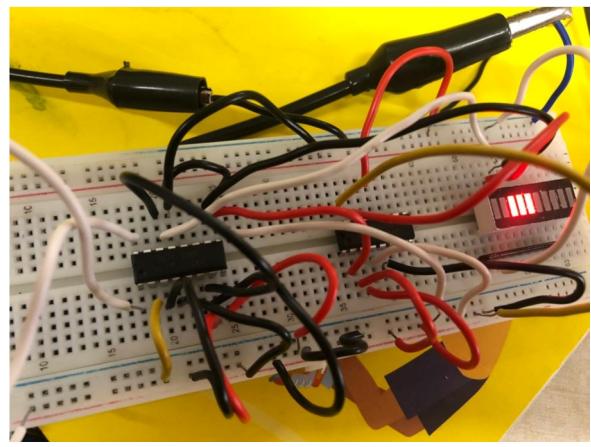
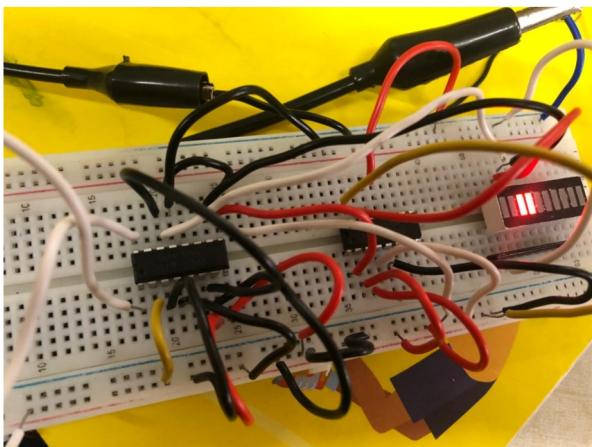
<u>Output₁</u>	<u>Output₂</u>	<u>Output₃</u>	<u>Decimal number</u>
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

For Output₁ = 1 and Output₂ = 1, we get decimal representation as 6,7. To remove this, set clear variables of each JK flip flop to the output of the NAND gate, with inputs as Output₁ & Output₂.

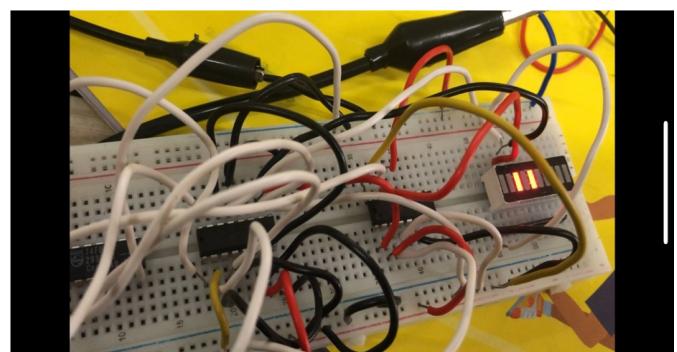
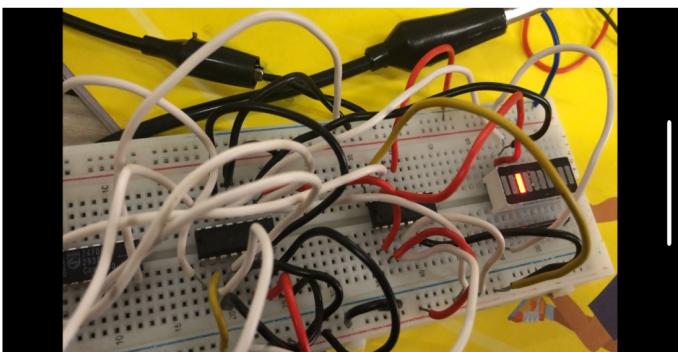
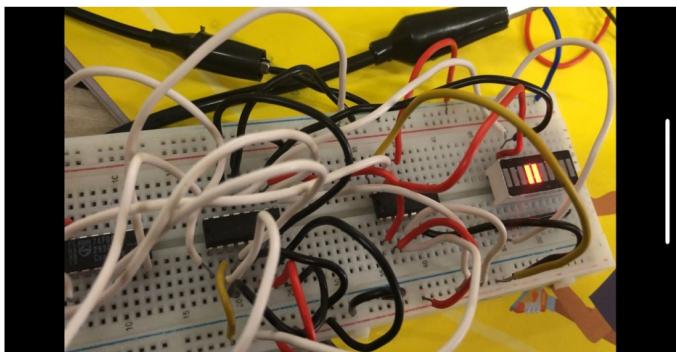
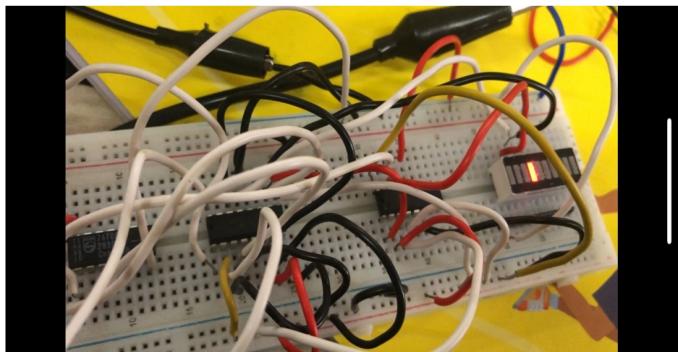
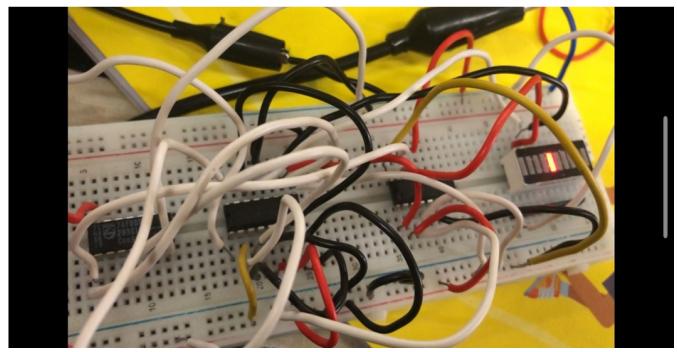
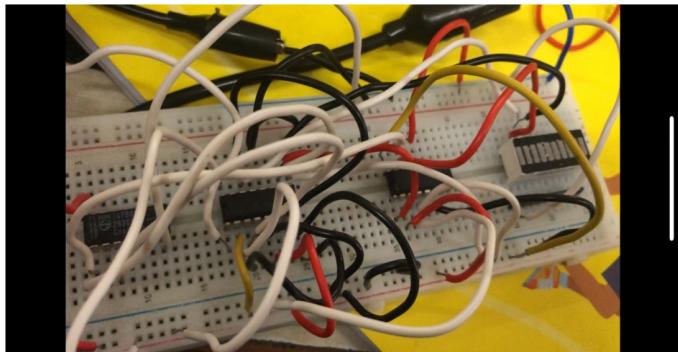
Snapshots of circuit:

MOD-8 ASYNCHRONOUS COUNTER





MOD-6 ASYNCHRONOUS COUNTER



Results and Discussion:

In this experiment, we explored the design procedures of asynchronous counters given the specifications/state-transition diagram and implemented the same on the breadboard using Digital J-K Flip-flop ICs. We observed the outputs via LED arrays and the states of LEDs (on/off) change every 1 second as the clock frequency is 1 Hz Arbitrary function generator (AFG) in asynchronous counters, as all flip-flops don't share a common clock, we can't exactly say the time-gap between successive states change in LEDs because of delays in the circuital elements.

We also used the transition/ logic diagram to convert Mod-8 counter to Mod-6 counter using NAND iC's.