LAB REPORT -4

NMOS Common Source Amplifier

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Q2. Plot ID vs V_{DS} characteristics:

I-V Characteristics of CD4007

*CD4007 MOS Array

* N4007 (NMOS on CD4007 CMOS integrated circuit)

.model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)

* P4007 (PMOS on CD4007 CMOS integrated circuit)

.model MP4007 PMOS (Kp=500u Vto=-1.5 Lambda=0.04 Gamma=0.6+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=4.0p Cbs=4.0p Pb=.8 Cgso=0.2p Cgdo=0.2p Is=16.64p N=1)

*Fixing gate bias at 3.5V

vgg 1 0 dc 2v

rg 1 2 680

M1 3 2 0 0 MN4007

Rd 3 4 100

*DC source of 0v to measure current

vid 5 4 dc 0v

vdd 5 0 dc 0v

*DC analysis to sweep vds from 0 to 5V

.dc vdd 0 5 0.2 vgg 2 5 0.5

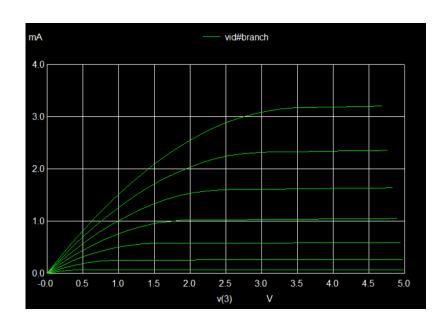
.control

run

plot vid#branch vs v(3)

.endc

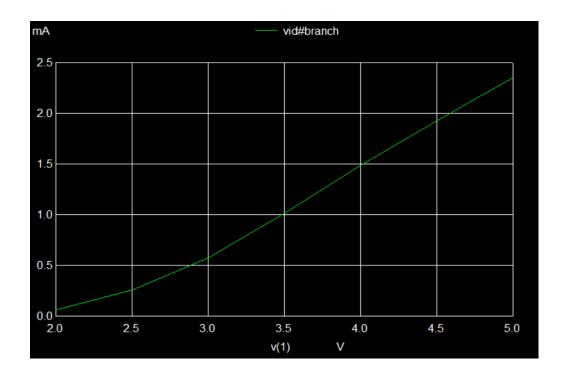
.end

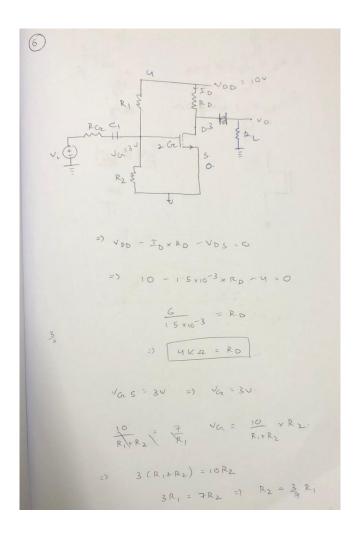


Q5. ngspice netlist to plot ID vs VGS by varying VGS from 0 to 5 V.

I-V Characteristics of CD4007

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* N4007 (NMOS on CD4007 CMOS integrated circuit)
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Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)
* P4007 (PMOS on CD4007 CMOS integrated circuit)
.model MP4007 PMOS (Kp=500u Vto=-1.5 Lambda=0.04 Gamma=0.6+ Xj=0 Tox=1200n Phi=.6 Rs=0
Rd=0 Cbd=4.0p Cbs=4.0p Pb=.8 Cgso=0.2p Cgdo=0.2p Is=16.64p N=1)
*Fixing gate bias at 3.5V
vgg 1 0 dc 2v
rg 1 2 5k
M1 3 2 0 0 MN4007
Rd 3 4 100
*DC source of 0v to measure current
vid 5 4 dc 0v
vdd 50 dc 2v
*DC analysis to sweep vds from 0 to 5V
.dc vgg 2 5 0.5
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Q8. Simulation and verify the results with your calculated values:

output voltage waveform and input voltage waveform for Vin = 200 mVp-p at 1kHz

.model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)

M1 3 4 0 0 MN4007

Vdd 1 0 10v Vd 1 2 0 Vd1 1 5 0 Vin 7 0 3V

Rd 2 3 4k R1 5 4 7.5k R2 4 0 3.214k Rl 8 0 100k Rg 6 7 1k

C1 4 6 2.2u C2 3 8 2.2u

.dc 0 3 3 .control op run print v(3) v(4) i(vd1) .endc .end

Q9. The output voltage waveform and input voltage waveform for V_{in} = 200 m V_{p-p} at 1kHz.

output voltage waveform and input voltage waveform for Vin = 200 mVp-p at 1kHz

.model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)

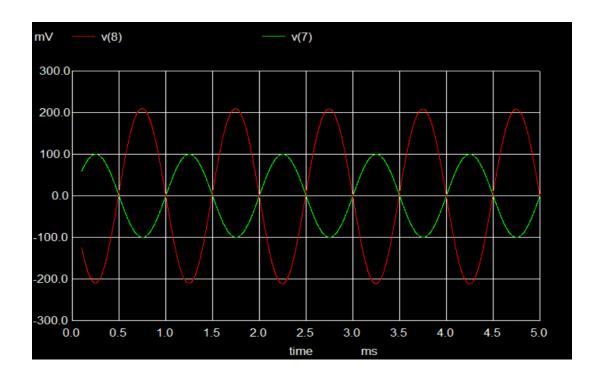
M1 3 4 0 0 MN4007

Vdd 1 0 10v Vd 1 2 0 Vd1 1 5 0 Vin 7 0 sin (0 100m 1k 0 0 0)

Rd 2 3 4k R1 5 4 7.5k R2 4 0 3.214k Rl 8 0 100k Rg 6 7 1k

C1 4 6 2.2u C2 3 8 2.2u

.tran 0.001ms 5ms 0.1ms .control op run plot v(7) v(8) .endc .end

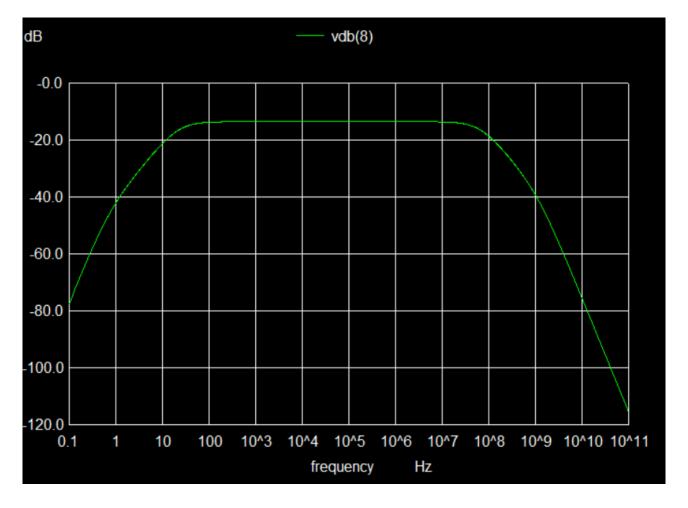


Q10. The frequency response of the amplifier by varying the frequency from 100 Hz to 1 MHz.

output voltage waveform and input voltage waveform for Vin = 200 mVp-p at 1kHz .model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)

M1 3 4 0 0 MN4007 Vdd 1 0 10v Vd 1 2 0 Vd1 1 5 0 Vin 7 0 dc 0 ac=100m Rd 2 3 4k R1 5 4 7.5k R2 4 0 3.214k Rl 8 0 100k Rg 6 7 1k C1 4 6 2.2u C2 3 8 2.2u .ac dec 100 0.1 100G .control

.ac dec 100 0.1 100G .control op run plot vdb(8) xlog .endc .end

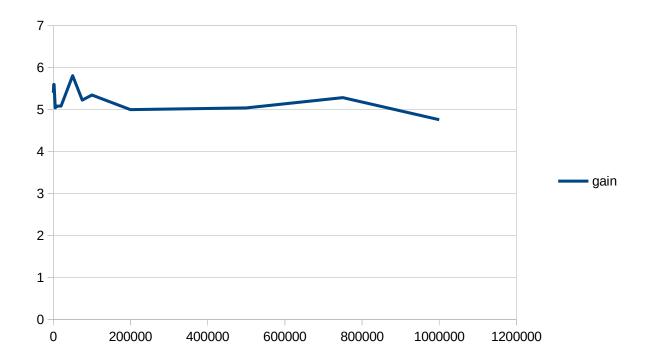


Hardware Implementation:

Q3. Amplitude of the sinusoidal input to 200 mVp-p and vary the frequency from 100 Hz to 1.5 MHz

	200mV P-P			
Vin (in mV)	Vout (in V)	Vin (in V)	Frequency	Gain
200	1.07	0.2	100	5.35
200	1.11	0.2	500	5.55
200	1.12	0.2	1000	5.6
200	1.12	0.2	2000	5.6
230	1.16	0.23	5000	5.04347826086956
240	1.22	0.24	10000	5.08333333333333
210	1.1	0.21	20000	5.23809523809524
240	1.22	0.24	50000	5.08333333333333
220	1.15	0.22	75000	5.22727272727273
260	1.23	0.26	100000	4.73076923076923
230	1.15	0.23	200000	5
240	1.21	0.24	500000	5.04166666666667
230	1.11	0.23	750000	4.82608695652174
250	1.19	0.25	1000000	4.76

Q6.Frequency responses of the amplifier (log-log plot)



The gain is constant over a range of frequencies and increases and decreases before and after the range of frequencies.

Q5. After increasing the input amplitude to 200 mVp-p to 2Vp-p in steps of 500 mV, we get gain value approximately as

Gain	Input signal _{P-P}	
5.4	200 mV	
5.08333	700 mV	
4.91667	1.2 V	
4.45	2 V	

Discussion:

- 1. I understood how to implement a NMOS Common Source Amplifier and found out the required resistances R_2 and R_D that need to be implemented in the circuit for the CMOS to work in amplifier mode.
- 2. Understood the frequency dependent amplification nature of the NMOS Common Source Amplifier.
- 3. Operation of Arbitrary Function Generator (AFG) and Digital Oscilloscope for generation and analysis of Periodic signals at different frequencies and finding out the gain of the signal for various frequencies and various input voltages.