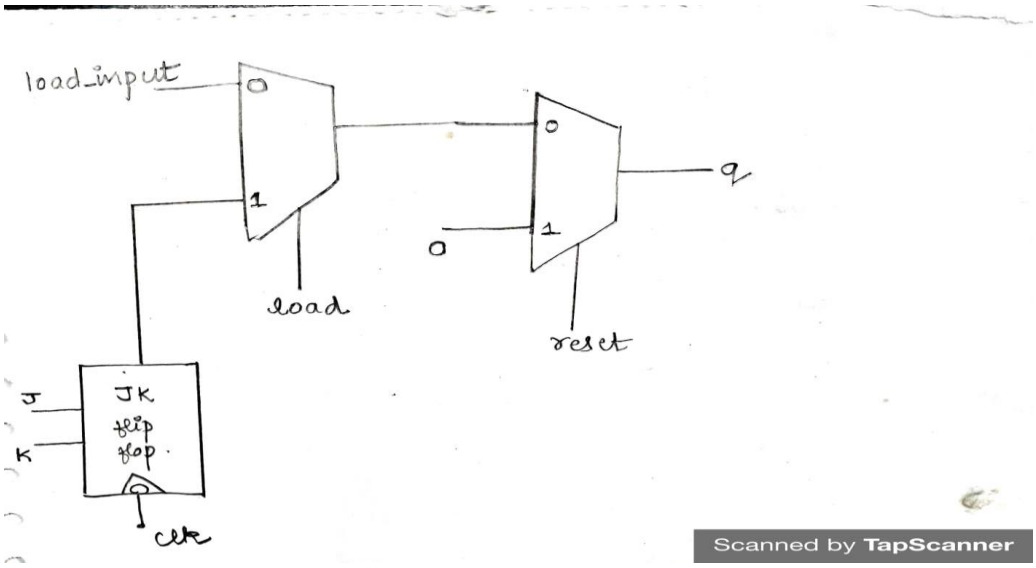
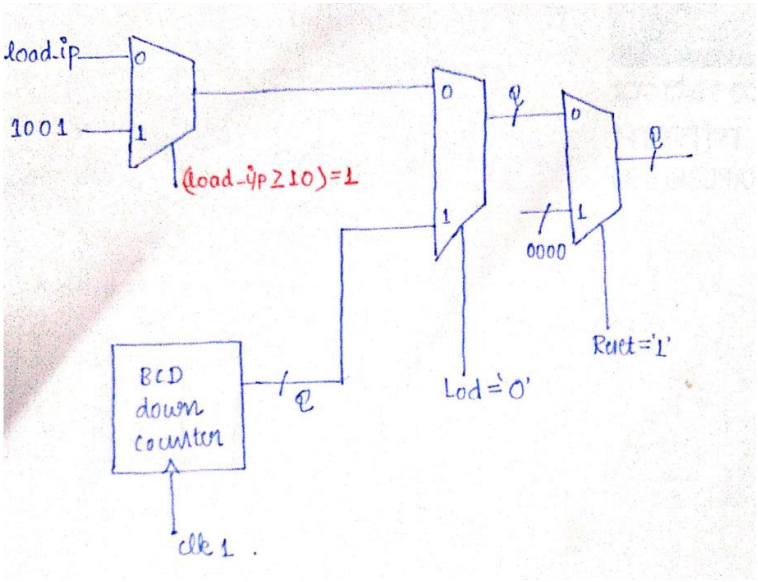
LAB 9 Questions

1. A loadable JK Flip flop (falling edge triggered clock) with asynchronous reset and load is shown below. Write a behavioural style VHDL code, compile it and observe the output in the CPLD board.



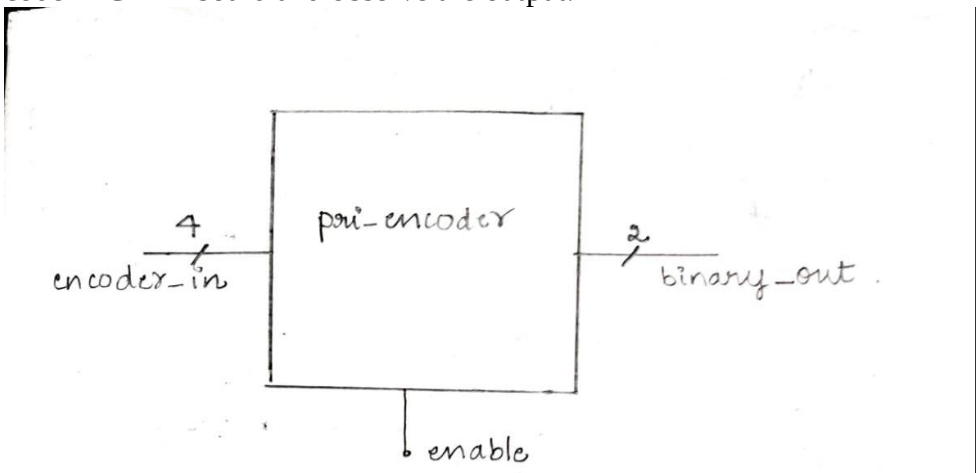

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity JK_FF is
Port (reset,J,K,clk1,Load,Load_input : in STD_LOGIC;
q,qbar : out STD_LOGIC);
end JK_FF ;

architecture Behavioral of JK_FF is
begin

--to be written

end Behavioral;
```

2. Using the above flip flop, write a structural style VHDL code for a BCD down counter, compile it and and observe the output in the CPLD board.




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity bcd_dc is
 Port (reset,clk1,Load : in STD_LOGIC;
Load_input : in std_logic_vector( 3 downto 0);
Q:out std_logic_vector(3 downto 0));
end bcd_dc;

architecture Behavioral of bcd_dc is
signal --to be written

component JK_FF is
--component declaration to be written
end component;

begin

--component instantiation to be written for BCD down counter.

With  load_input   select
Q <= "1001" when "1010" ,
     "1001" when "1011" ,
     "1001" when "1100",
     "1001" when "1101" ,
     "1001" when "1110" ,
      "1001" when "1111" ,
--complete it.
 end Behavioral;
```

3. Write the VHDL code for 4:2 priority encoder. Below is the truth table. Synthesize and dump the code in CPLD board and observe the output.



enable	encoder_in	binary_out
0	X X X X	0 0
1	X X X 1	0 0
	X X 1 0	0 1
	X 1 0 0	1 0
	1 0 0 0	1 1

```
library ieee;
use ieee.std_logic_1164.all;

entity pri_encoder is
port (
      enable     :in  std_logic;
      encoder_in :in  std_logic_vector (3 downto 0);
      bin_out: out std_logic_vector(1 downto 0)
   );
end entity;

architecture rtl of pri_encoder is

begin

--to be written


end rtl;
```