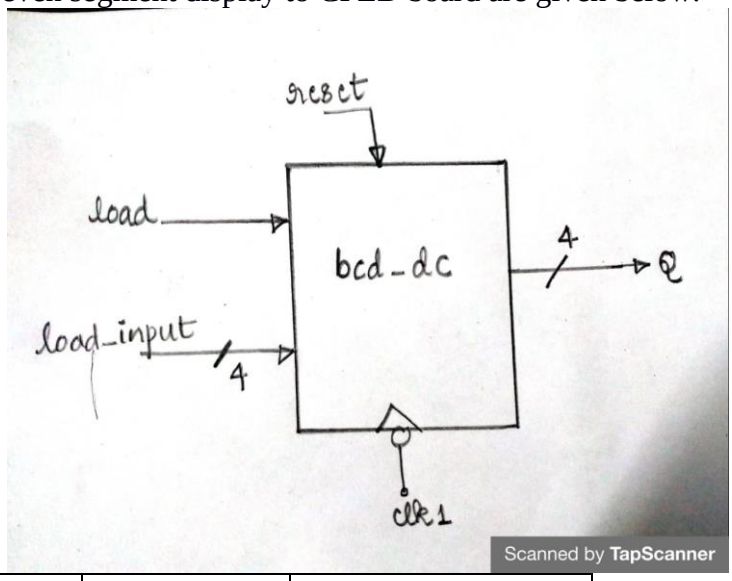
Week-10

1.Write the VHDL code for loadable BCD down counter (which is discussed in week9) and configure the CPLD as BCD down counter by dumping this HDL code. Also observe the outputs of the counter on the seven segment display by connecting to the CPLDs daughter board. The pin connections for seven segment display to CPLD board are given below.



Outputs from CPLD	Pin numbers	Daughter board pins
Q[0]	24	11
Q[1]	25	12
Q[2]	26	13
Q[3]	27	14
Inputs to CPLD		
Clk1	43	
Reset	--	
Load	--	
Load_Input[0]	--	
Load_Input[1]	--	
Load_Input[2]	--	
Load_Input[3]	--	

2. If you have completed the above experiment, emulate the CPLD device as loadable BCD up counter.