EE 677 Foundation of VLSI CAD
Midterm Project Report

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Work done -

Given a complex logic expression, converting it to multiple input AND and OR gates.

The expression reduced to simplest form using ESPRESSO function from PyEDA.

Then the resultant expression is parsed and the input signals and expression is expressed in the form of AND and OR gates.

Object oriented programming used to implement the gating logic.
A class BinBoolOp (modified from the version done in class) has been defined for generic multi-input logic gates.
Classes AndGate, OrGate and NotGate inherit from BinBoolOp and are specific for the particular logic operation.
A connector class which connects the output of one logic gate with the input of another.

These classes have been used to convert the string expression returned by the ESPRESSO function into object oriented approach for further manipulation.

Future work -

Implement the logic expression into NAND2 gates, from multi input AND and OR gates.