Modified Wallace Tree Multiplier using Efficient Square Root Carry Select Adder

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Abstract— **A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, micro processors and digital signal processors etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the whole system and also it is occupying more area consuming. The Carry Select Adder (CSLA) provides a good compromise between cost and performance in carry propagation adder design. A Square Root Carry Select Adder using RCA is introduced but it offers some speed penalty. However, conventional CSLA is still area-consuming due to the dual ripple carry adder structure. In the proposed work, generally in Wallace multiplier the partial products are reduced as soon as possible and the final carry propagation path carry select adder is used. In this paper, modification is done at gate level to reduce area and power consumption. The Modified Square Root Carry Select-Adder (MCSLA) is designed using Common Boolean Logic and then compared with regular CSLA respective architectures, and this MCSLA is implemented in Wallace Tree Multiplier. This work gives the reduced area compared to normal Wallace tree multiplier. Finally an area efficient Wallace tree multiplier is designed using common Boolean logic based square root carry select adder.**

***Keywords*—Wallace Tree Multiplier, Square Root Carry Select Adder (SQRT CSLA), Common Boolean Logic (CBL)**

I. INTRODUCTION

Multiplier is the logic device of great concern in terms of performance of a processor. In any system, the task of processor is very crucial. The task that took most of the processor's time is multiplication thus enhancing the performance of multiplier leads to better performance of processor especially in field of digital signal processing and data processing ASIC. Many application systems based on DSP require extremely fast processing of a huge amount of digital data. The multiplier is an essential element of the digital signal processing such as filtering and convolution. The multiplier is also an important element in microprocessor. The demand of fast processors is increasing for high-speed data processing. Since the multiplier requires the longest delay among the basic operational blocks in digital system [3]. Any multiplier can be divided into three stages: Partial products generation stage these are generated by AND operation, partial products addition stage can be carried by different adders, and the final addition stage. Many high-performance algorithms and architectures have been proposed to accelerate multiplication. The speed of multiplication can be increased by reducing the number of partial products. Various multiplication algorithms such as Booth, Modified Booth, Braun, and Baugh-Wooley have been proposed. This paper work presents two different form of Wallace tree multiplier using two different adder circuits namely Ripple carry adder and carry select adder. After developing these two different forms of Wallace tree multiplier a comparative study is being carried out on the basis of area and power consumption by the two designs. Ripple Carry Adder (RCAs) have the most compact design among all types of adders. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independent generation multiple carries and then select a carry to generate the sum. whereas, the CSLA is not an area efficient because it uses multiple pairs of Ripple Carry Adders(RCA) to generate partial sum and carry by considering carry input as $C_{in}=0$ and $C_{in}=1$. And the final summation and carry are selected by the multiplexers [1].

The basic idea of the proposed architecture is that which replaces the RCA by Common Boolean Logic. The modified SQRT CSLA uses Common Boolean logic term instead of RCA with $C_{in}=1$ in the regular CSLA to achieve lower area with slightly increase in delay The proposed architecture generates a duplicate sum and carry-out signal by using NOT and OR gate and select value with the help of multiplexer. BY using the multiplexer select the correct output according to its previously carry out signal [1]. Thus it can be interpreted from this fact that addition is a sub-process in multiplication criterion that has to be fulfilled. In the process the Wallace tree formation aligned the partial products in form of a tree and then with the help of fast adders final product is obtained.

This paper is organized as follows; Section II describes the conventional and modified Wallace tree architectures and section III explains the Modified Wallace tree Structure with RCA and normal square root CSLA respectively. A section IV deals with proposed Wallace tree architecture using Common Boolean Logic (CBL) based Square Root CSLA. Results are analyzed in the section V. and finally Section VI with the conclusion.

II. WALLACE TREE ARCHITECTURES

The Wallace tree multiplier is considerably faster than a simple array multiplier because its height is logarithmic in word size. However, in addition to the large number of adders required, the Wallace tree's arrangement is much less regular and more complicated. The Wallace tree multiplier is a high speed multiplier [3]. As a result, these are often avoided by designers, because the design complexity is a concern to them.

The summing of the partial product bits in parallel using a tree of carry-save adders became generally known as the "Wallace Tree Multiplier". The three main steps are used to multiply two numbers.

- Formation of partial products.
- Reduction of the partial products matrix into a two row matrix by means of a carry save adder.
- Addition of remaining two rows using a faster Carry Look Ahead Adder(CLA).

A. *Conventional Wallace Tree Multiplier:*

In the conventional Wallace Tree multiplier the partial products are formed by N^2 AND gates in the same manner as that of Dadda multiplier. The formed partial products are collected to group of three or two. Full adders are applied to columns containing three bits and half adders to column containing two bits. Carry save adders are used for the addition of partial products. Since the Wallace multiplier performs the reduction as soon as possible the number of half adders and full adders required is high [4]. The Basic conventional Wallace multiplier for N=8 is shown in Figure 1.

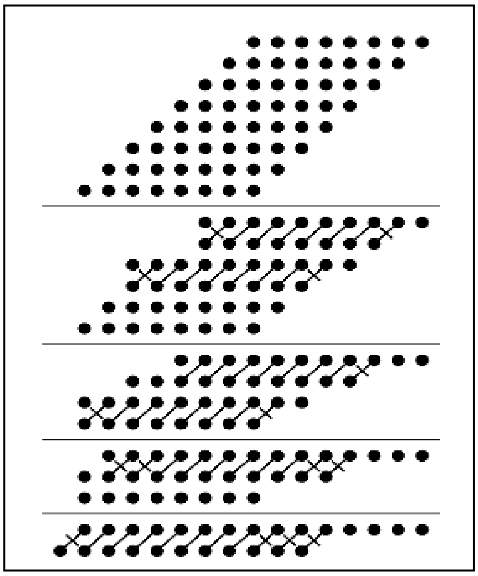

Figure 1. Conventional Wallace Tree Multiplier

B. *Modified Wallace Tree Multiplier:*

The Modified Wallace multiplier is similar to that of Conventional Wallace multiplier in that it uses as so many full adders as possible, only different in that it only use half adders when necessary to ensure that the number of reduction stage is same as for Conventional Wallace Tree multiplier. This architecture helps in reducing the partial products with a rate of log3/2 N/2. The Modified Wallace Tree at first make the partial product formed into the pyramidal structure and divide the structure into tree rows of group and uses full adders for each group of three bits in a column. The modified Wallace tree multiplier is shown in Figure 2. A group of three bits in a column is not processed, it is passed on to the next stage [5]. Single bits are passed on to the next stage as in the conventional Wallace reduction. The Figure 3 explains the algorithm for the modified Wallace tree multiplier structure algorithm. The three main steps in the algorithm of Wallace tree multiplier design are:

1. The multiplication of the multiplier bits with the multiplicand generates a bit product stream.
2. The bit product matrix thus formed has been reduced into less number of rows with the help of half and full adders, this step persist till the last addition is done.
3. Last and final step is the final addition using adders and the final result can be obtained after this step.

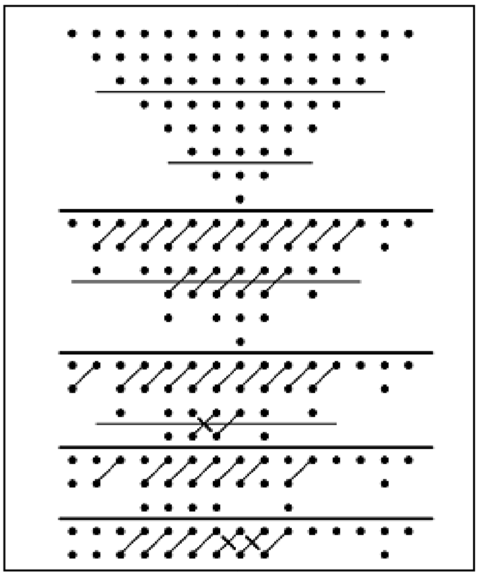

Figure 2. Modified Wallace Tree Multiplier

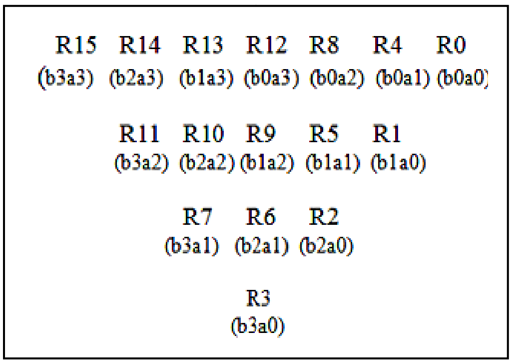

Figure 3. Modified Wallacce Tree Multiplier with pyramid structure

The Figure 3 explains the Wallace tree formation using partial products for 4-bits. Here R0, R1, R2,…R15 are the partial products of the multiplicand and multiplier.

III. MODIFIED WALLACE TREE MULTIPLIER USING RCA AND SQRT CSLA

A. Modified Wallace Tree Multiplier using RCA:

The basic architecture for Modified Wallace Tree Multiplier using ripple carry adder is shown in Figure 4. In this architecture the both multiplier and multiplicand are AND ed together and generates partial products and then an Wallace Tree is implemented.

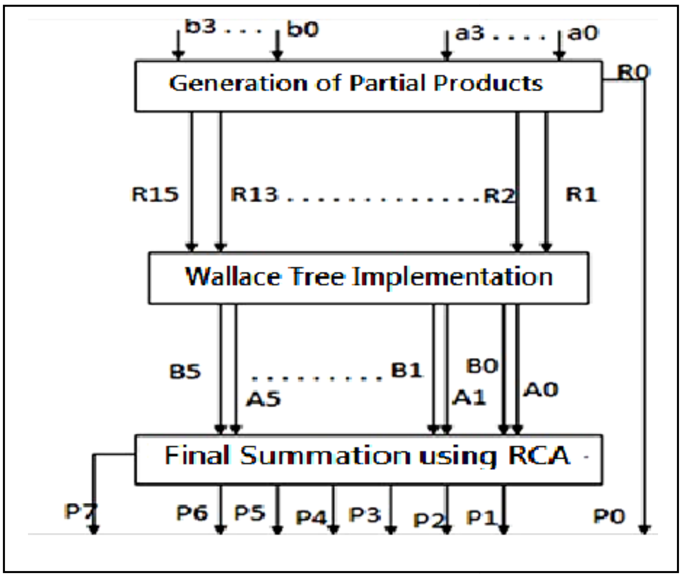

Figure 4. Modified Wallace Multiplier Architecture using RCA

In this arrangement the partial products with same weight are grouped together and written in a column. Here total six columns in the arrangement in accordance to the max weight carried by partial product term i.e. a3b3 has highest weight 6. Now the addition is applied in each column using half and full adder according to the need, if there are two numbers to be added then half adder is employed and if there are three numbers for addition then full adder has to be used. The main objective of Wallace tree implementation in this architecture is to generate the input terms for adders whether RCA. As we know the first partial product a0b0 doesn't need any computation, it is directly taken as the LSB of the product. Therefore R0 is equals to P0 [4]. Now the task we have to do is to extract two final bits from each remaining column after excluding the first column from right as it contains R0. Now carefully examining the columns we can see the second column from right has two partial products P4 and P1, which means it has only two bits in all so they can be taken directly and termed as A0 and B0. Moving further to the next column we are having three terms with us P8, P5 and P2, so here we need to apply adders to get final two bits for RCA. A half adder is applied with p8 and P5 as inputs which gives two outputs sum and carry, now from this column the sum obtained is taken as B1, the partial product term P2 as A1 and the carry so obtained as A2. Going ahead in this manner, we will get final six pairs of bits as A0B0, A1B1, A2B2, A3B3, A4B4, and A5B5. These numbers so obtained can be treated as two input numbers for the adder [5], [6]. The Wallace tree implementation with the RCA can be shown in Figure 5.

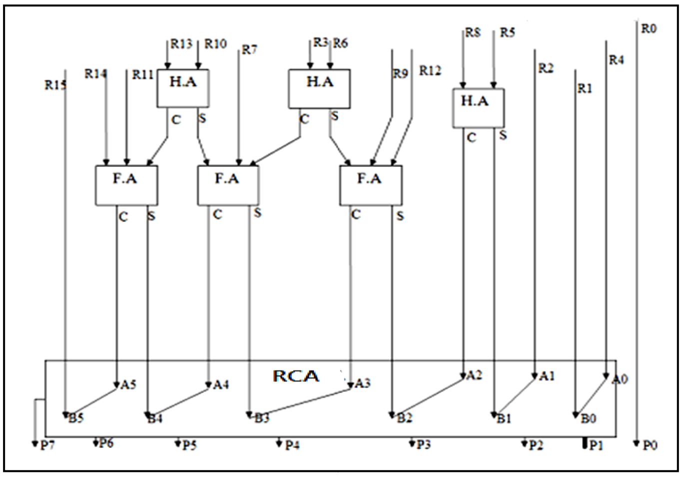

Figure 5. Wallace Tree Multiplier using RCA

Similarly the RCA is replaced with Square Root Carry Select adder and the architecture and the tree formation is shown in below Figure 6, 7.

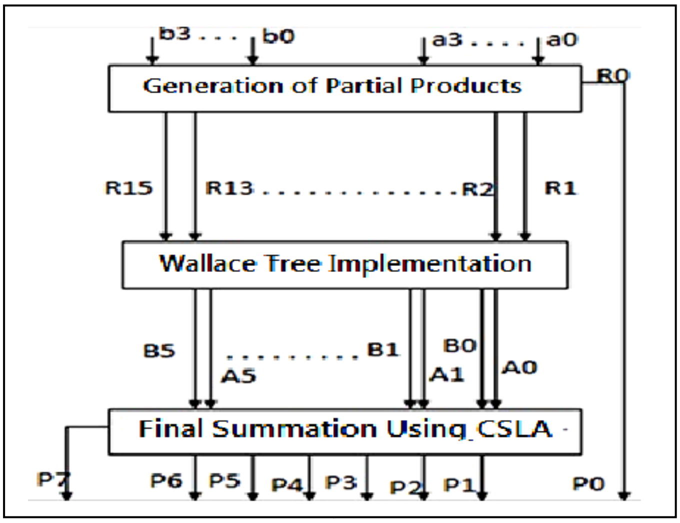

Figure 6. Modified Wallace Architecture using SQRT CSLA

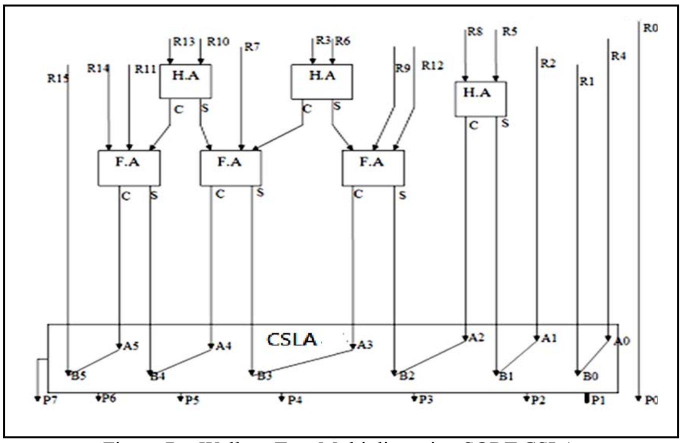

Figure 7. Wallace Tree Multiplier using SQRT CSLA

IV. Modified Wallace Tree Multiplier using CBL Based SQRT CSLA

In proposed work the normal SQRT CSLA is replaced with the Common Boolean logic based SQRT CSLA. This architecture of 16-bit CBL based SQRT CSLA is shown in Figure 8. And the area evaluations of internal structures are calculated by using the gate level simulation [2]. This architecture is implemented on the Wallace tree Multiplier and that final structure is shown in Figure 9.

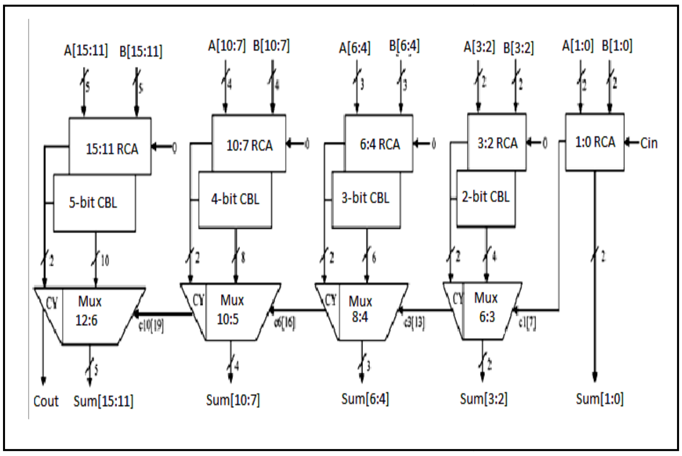

Figure 8. 16-bit CBL based Sqaure Root CSLA

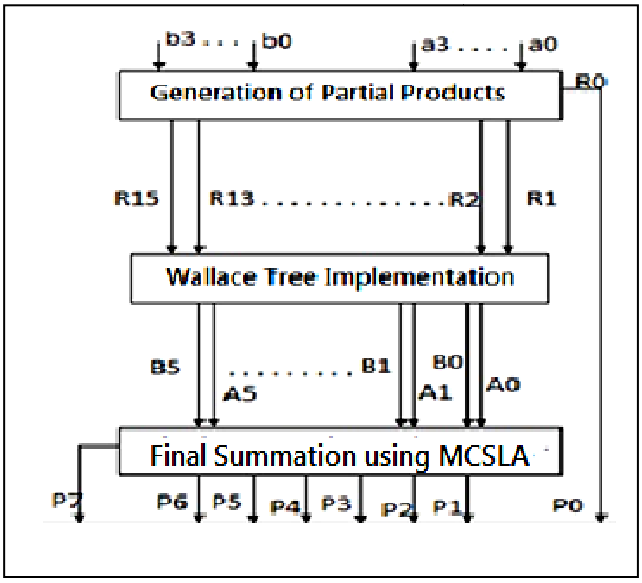

Figure 9. Wallace Architecture using CBL based SQRT CSLA

V. Result Summary

The comparison table for the 8-bit Wallace tree Multiplier using RCA, normal SQRT CSLA and Common Boolean Logic based SQRT CSLA are shown in Table 1. Similarly for 16-bit Wallace tree multiplier using different adder's topologies comparison is shown in Table 2. The total simulation done in Xilinx ISE 14.2 targeted Spartan 3E family. From the both tables the number of slices are reducing comparing with RCA to CBL based SQRT CSLA Wallace tree Multiplier. And slight increase in delay. So this gives an area efficient Wallace tree multiplier using CBL based SQRT CSLA.

TABLE I. Delay and area comparision of 8-bit Wallace tree multiplier

Wallace Multiplier	Delay (ns)	No. of Slices	Logic Levels
Using RCA	15.36	32	14
Using SQRT CSLA	17.05	28	12
Using CBL based SQRT CSLA	16.13	22	10

TABLE II. Delay and area comparision of 16-bit Wallace tree multiplier

Wallace Multiplier	Delay (ns)	No. of Slices	Logic Levels
Using RCA	35.62	57	28
Using SQRT CSLA	38.47	50	25
Using CBL based SQRT CSLA	36.73	46	23

VI. Conclusion

In this paper, an area efficient Wallace tree multiplier using Common Boolean logic (CBL) based square-root carry select adder is proposed. By sharing the common Boolean logic (CBL) term, the duplicated adder cells in the regular carry select adder is removed. The reduce number of gates of this work offers the great advantage in the reduction of delay and area. It would be interesting to test the design of the 32 and 64 bits. This work may helpful for designing of MAC unit.

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