Monday	EE 671: VLSI Design	Due on
Oct, 16 2017	Assignment 3	Oct. 27, 2017

Q–1 Using the design kit from SCL, design, layout, back extract and re-simulate a full adder, a half adder and a 2 to 1 mux using tri-stateable inverters. The circuits should be loaded with 4 minimum sized inverters. Inputs should be driven by buffers.

These are required for a multiplier, so sum should be independently generated from a, b and C_{in}.

Evaluate the worst case delay (slow/slow model, highest temperature, supply voltage = 1.7V) for the sum and carry outputs for the full and half adder.

Q–2 Using VHDL or verilog, write the structural description of an unsigned 8×8 multiplier using a Wallace tree without using Booth encoding. Use a carry select adder with square root tiling for the final adder.

Find the critical path of the tree (and carry select adder) and simulate the circuit using a test bench in VHDL/verilog with test vectors to excite the critical path. (Do not add delays at this stage).

Q–3 Repeat the above after adding worst case delays for half and full adders in the Wallace tree as well as the carry select adder.