Sherman Lam
E155
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Lab 2 Report: Multiplexed Display

1 Introduction

2 Design and Testing Methodology

2.1 Hardware

Notes on pin mapping:
switch 1: s1[0] = P54 s1[1] = P55 s1[2] = P53 s1[3] = P24
switch 2: s2[0] = P44 s2[1] = P49 s2[2] = P50 s2[3] = P51
display enable: on1 = P87 on2 = P86
clk = P88 reset = P60
seg[0] = a = P2 seg[1] = b = P1 seg[2] = c = P4 seg[3] = d = P10 seg[4] = e = P11 seg[5] = f = P3 seg[6] = g = P7
Other notes: Drop between base and emitter was measured to be 0.74-0.76 V. 0.7V approx okay. Drop between emitter and collector was 0.12-0.15V for 5.6k base resistor. 0.09V for 2.2k resistor. 0.05V for 1k resistor. Drop across 220 ohm resistors is 1V
reset switch works.

2.2 Software

2.2.1 Testing and Flashing

3 Technical Documentation

3.1 System Verilog Code

```
1  /* This is the main module. It selects which set of switch
2     outputs to use and then decodes the number of the selected
3     switch. This also sets the clock that time-multiplexes the
4     two 7 segment outputs.
5
6     Author: Sherman Lam
7     Email: slam@g.hmc.edu
8     Date: Sep 17, 2014
9  */
10 module lab2_SL(input logic clk, reset,
11                 input logic [3:0] s1,s2, //DIP switches
12                 output logic on1, on2,   //if on1 is pulled LOW, LED set 1 is on.
13                 output logic [6:0] seg); //segment states
14
15    // time multiplexing
16    multiplexer m1(.clk(clk), .on1(on1), .reset(reset));
17
18    // the segments always have opposite states.
19    assign on2 = ~on1;
20
21    // select the right set of switches.
```

```
22      // on1 -> s1 is used. on2 -> s2 is used
23      logic [3:0] s3;
24      // if on1 is pulled LOW, LED set 1 is on.
25      assign s3 = on1? s2 : s1;
26
27      // 7 segment decoder
28      led7Decoder decoder(.s(s3), .seg(seg));
29
30  endmodule
31
32
33  /* This module time multiplexes
34
35      Author: Sherman Lam
36      Email: slam@g.hmc.edu
37      Date: Sep 17, 2014
38  */
39  module multiplexer(  input logic clk, reset,
40                       output logic on1);
41      // time multiplexer for switching bewteen displays
42      logic [18:0] hPeriod = 19'd333333;  // 120Hz toggling
43      logic [18:0] counter = 'b0;
44
45      always_ff @(posedge clk, posedge reset) begin
46          if (reset)
47              on1 = 1'b0;
48          else begin
49              if (counter >= hPeriod) begin
50                  counter = 'b0;
51                  on1 = ~on1;
52              end
53              else
54                  //on1 = on1;
55                  counter <= counter + 1'b1;
56          end
57      end
58
59  endmodule
60
61
62  /* This module decodes the switch inputs into an output for the
63      7 segment display on the development board.
64      s[3:0] = [sw3, ... ,sw1]
65      seg[6:0] = [g,f, ... ,b,a]
66
67      Author: Sherman
68      Email: slam@g.hmc.edu
69      Date: Sep 9, 2014
70  */
71  module led7Decoder(  input logic [3:0] s,        //4 DIP switches
72                       output logic [6:0] seg);    //segments in 7-seg display
73
74      always_comb begin
75          //lookup table for s-seg relationship
76          case(s)
77              4'h0: seg = 7'b100_0000;        // 0x0
78              4'h1: seg = 7'b111_1001;        // 0x1
79              4'h2: seg = 7'b010_0100;        // 0x2
80              4'h3: seg = 7'b011_0000;        // 0x3
```

```
81              4'h4: seg = 7'b001_1001;        // 0x4
82              4'h5: seg = 7'b001_0010;        // 0x5
83              4'h6: seg = 7'b000_0010;        // 0x6
84              4'h7: seg = 7'b111_1000;        // 0x7
85              4'h8: seg = 7'b000_0000;        // 0x8
86              4'h9: seg = 7'b001_1000;        // 0x9
87              4'ha: seg = 7'b000_1000;        // 0xA
88              4'hb: seg = 7'b000_0011;        // 0xB
89              4'hc: seg = 7'b010_0111;        // 0xC
90              4'hd: seg = 7'b010_0001;        // 0xD
91              4'he: seg = 7'b000_0110;        // 0xE
92              4'hf: seg = 7'b000_1110;        // 0xF
93              default: seg = 7'b111_1110;       // default to a dash
94          endcase
95
96      end
97  endmodule
```

4 Results and Discussion

5 Conclusion

Time spent: so far, about 4.5hrs