Computer Architecture 2 Final Exam

ELE320, Hanyang University, 2020 Fall,

Department: ID: Name:

1. In HDD, the sector is the minimum unit to read and write. When a request from CPU arrives at HDD, what operations are required to read a sector in HDD? Explain them in terms of seek time, rotational latency, and data transfer.
2. Assume that the following HDD is given: 512B sector, 10,000 rpm, 5 ms average seek time, 50MB/s transfer rate, 0.5 ms controller overhead, idle disk. Compute the average read time. If the average seek time reduces to 1ms then what is the average read time?
3. In bus systems, there are two types of serial bus and parallel bus. Which shows higher performance (bandwidth) in general? Explain the reason.
4. In Flash memory, there are two types of NOR flash and NAND flash. Explain the difference between NOR and NAND flashes.
5. Compare ROM, PROM, EPROM, EEPROM, and flash memory in terms of the erase operation.
6. Compare “memory mapped I/O” vs. “I/O” instruction approaches.
7. Explain polling, interrupt, and DMA.
8. If DMA writes to a memory block that is cached then the cached copy becomes stale. Explain why it is happening and how to solve the stale problem.
9. In case that OS uses virtual addresses for memory, DMA blocks may not be contiguous in physical memory. How can we solve the scattered physical memory in DMA?
10. In RAID 5 system which uses distributed block-interleaved even parity. Note that the even parity means that all xored valued should be even. Assume E disk is out of order. Reconstruct E blocks. Note that p denotes a parity bit.

	A	B	C	D	E
0	1	1	1	0	0(p)
1	0	1	0	0(p)	?
2	1	0	1(p)	0	?
3	1	0(p)	0	0	?

11. What is Amdahl’s law?
12. Explain why a two-core processor can consume the half energy compared with a single core processor using voltage, current, power, time, and energy equations.
13. Write a code to sum 100,000 numbers on 10 processor UMA where each processor has ID, we partition 100 numbers per processor, and initial summation on each processor. Assume that the execution time for all operations except synch() is negligible, and synch() time requires 1ms. What is the total execution time to sum the 100,000 numbers on 10 processor UMA?
14. Explain SPMD (Single program multiple data) regarding to the conditional branch on multiple cores.
15. (10pt) Explain “Warp" in NVIDIA architecture.

16. Explain the ll (load linked) and sc (store conditional) instructions.