Computer Architecture 2 Final Exam

ELE320, Hanyang University, 2019 Fall,

Department: ID: Name:

1. (10pt) Compare “memory mapped I/O” vs. “I/O” instruction approaches.
2. (15pt) Explain polling, interrupt, and DMA.
3. (10pt) If DMA writes to a memory block that is cached then the cached copy becomes stale. Explain why it is happening and how to solve the stale problem.
4. (10pt) In case that OS uses virtual addresses for memory, DMA blocks may not be contiguous in physical memory. How can we solve the scattered physical memory in DMA?
5. (10pt) In RAID 5 system which uses distributed block-interleaved even parity. Note that the even parity means that all xored valued should be even.

(a) Assume E disk is out of order. Reconstruct E blocks. Note that p denotes a parity bit.

	A	B	C	D	E
0	0	1	1	0	0(p)
1	0	0	0	0(p)	?
2	1	1	1(p)	0	?
3	1	0(p)	1	1	?

(b) For requests to update blocks A0, B2, and C3, compute how many cycles are required. Assume that it takes a single cycle to update a single block in each HDD.

6. What is Amdahl’s law?

7. Explain the fine-grain, coarse-grain, and simultaneous multithreading.

8. (10pt) Explain “Warp" in NVIDIA architecture.

9. (10pt) For MESI snooping protocol, specify cache states in processors P1, P2, and P3 for each step. Assumes initial cache state is invalid.

step	P1 cache state	P2 cache state	P3 cache state
P1: read A1			
P1: write 1 to A1			
P3: read A1			
P2: write 2 to A1			
P1: read A1			
P2: write 3 to A1			
P2: write 0 to A1			
P3: read A1			
P1: write 1 to A1			

10. (10pt) The following code shows the implementation of lock by using ll (load linked) and sc (store conditional) instructions.

(a) Fill the blanks.

```
try: mov  R5, #1
     ll   R2,0(R4) ; load linked
     sc   _________ ; store conditional
     beqz _________ ; branch store fails (R5 = 0)
     bnez R2, try   ; already locked?
```

(b) The above code invalidates all other copies in caches, which generates considerable bus traffic. Fill the blanks to revise the above code to solve the problem.

```
try:    mov  R5, #1
lockit: lw   R2, 0(R4)
        bnez _________
        ll   R2,0(R4) ; load linked
        sc   _________; store conditional
        beqz _________; branch store fails
        bnez R2, try  ; already locked?
```

11. (10pt) Explain the directory cache coherent protocol.