Channel Vocoder on FPGA

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Vocoder Overview

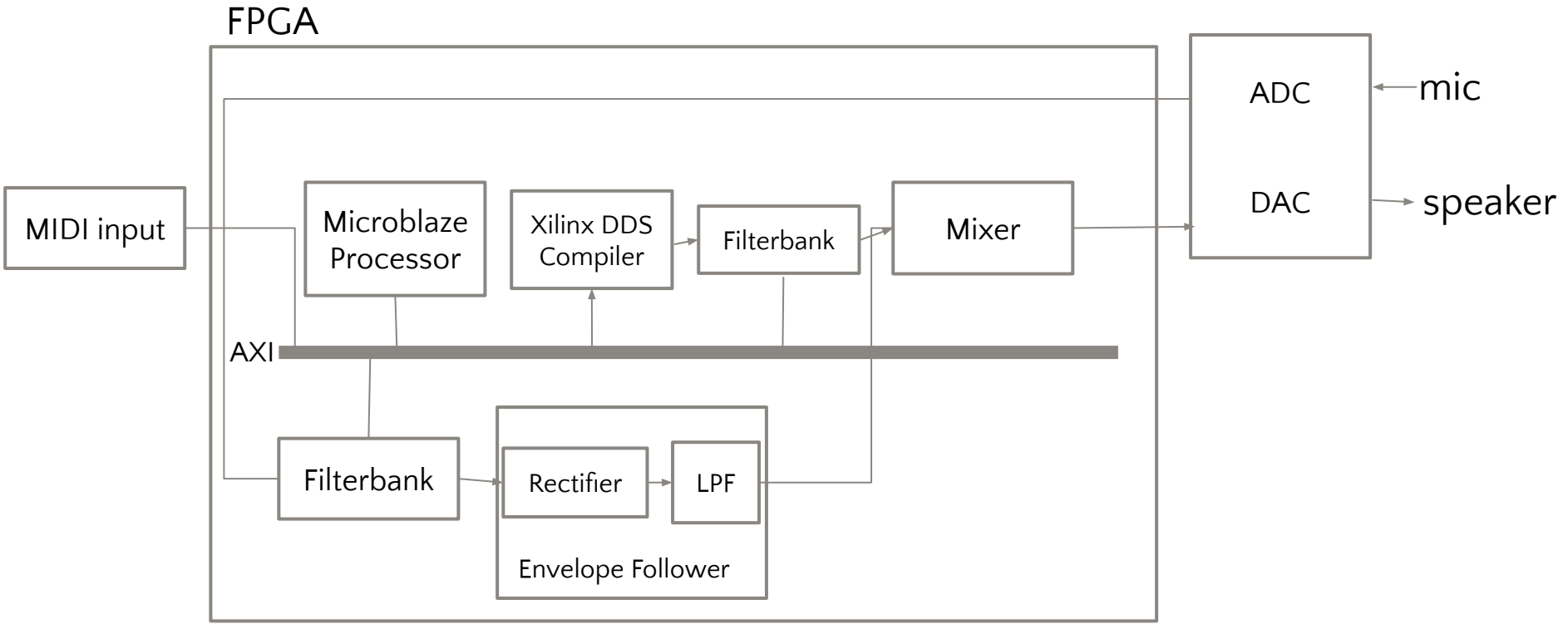
- Voice input, digital signal processing, synthesized audio output
  - Imposes input modulator signal (human voice) onto a carrier signal (often synthesized)

Initial Project Goals

- System:
  - Impose modulator signal input onto carrier signal
  - Support at least 1 carrier waveform

- Output:
  - At least 1 selected pitch at a time

Proposed System Block Diagram



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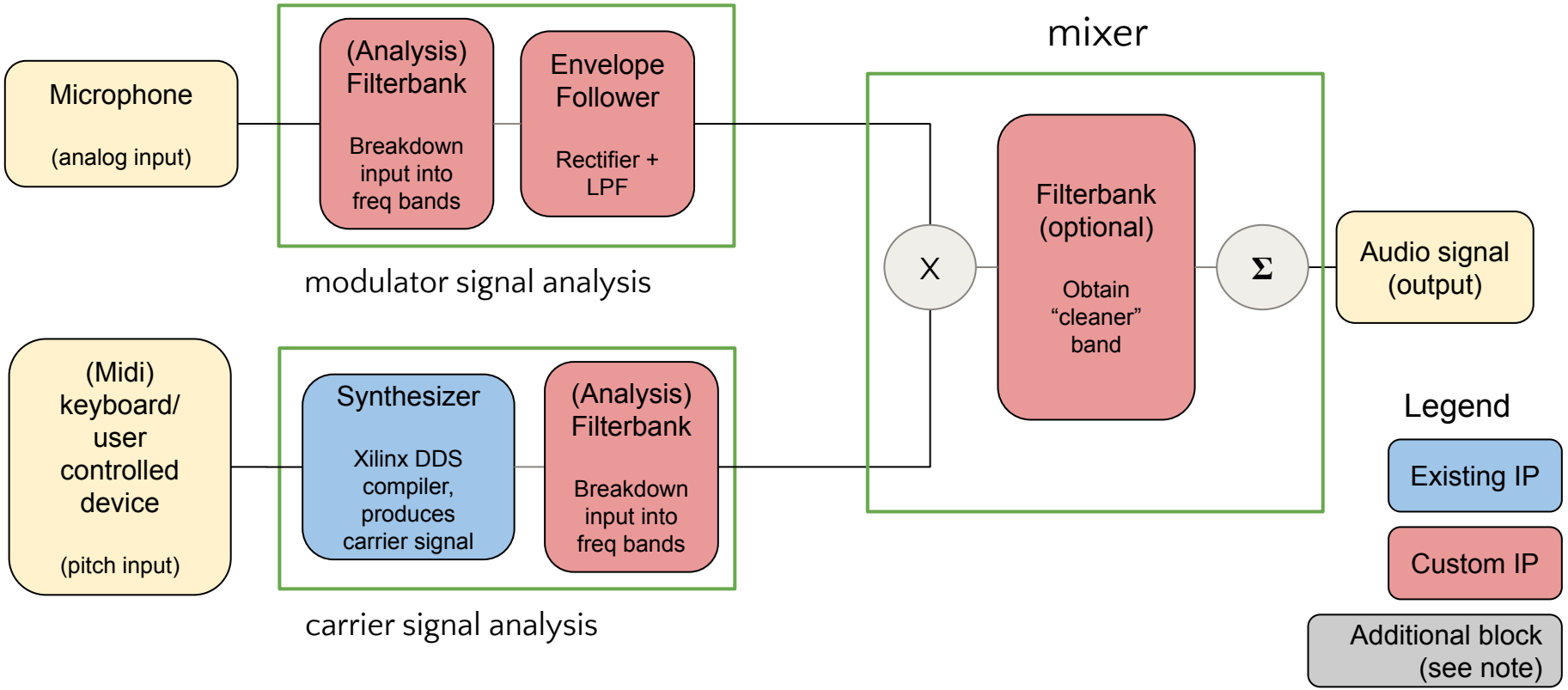
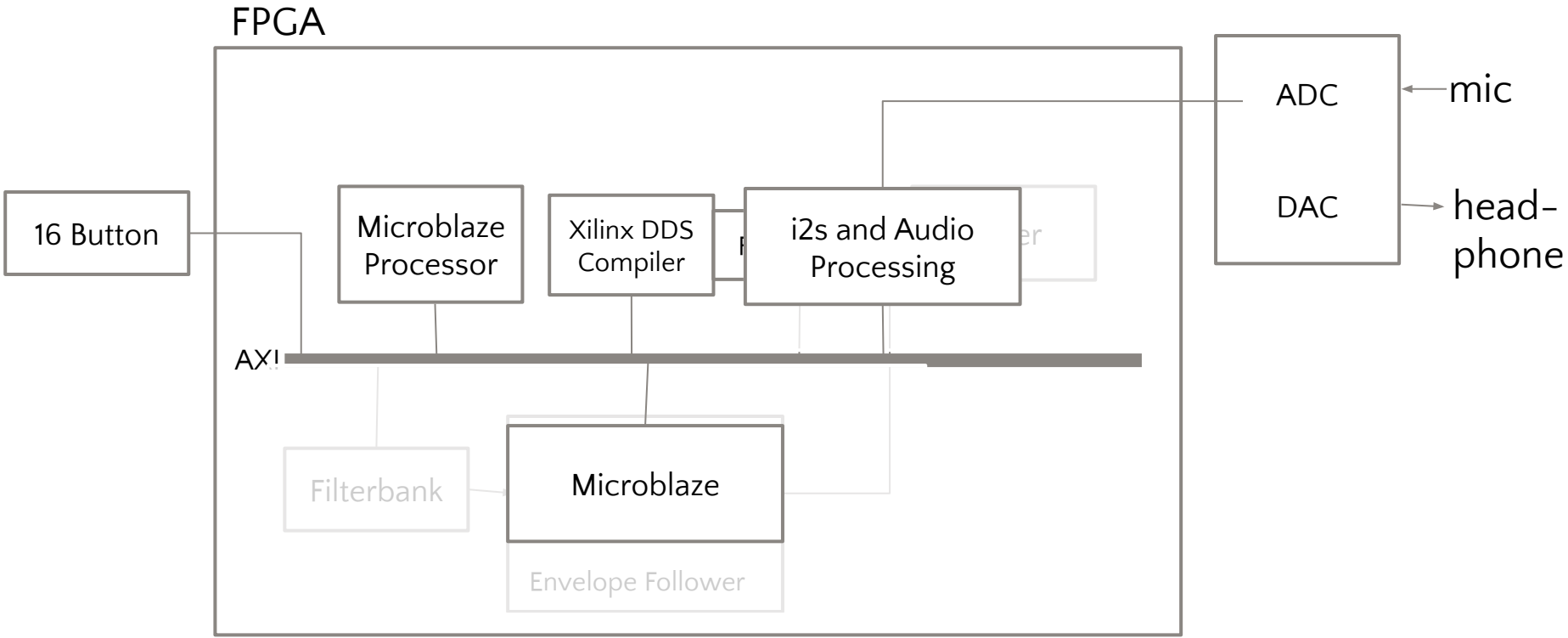


Final Implemented Project

- **Analog Input Handling:** A microphone to capture input audio
- **Pitch Input Handling:** 16 button keypad to select between various preset frequencies and/or carrier waveforms
- **Microblaze processor:**
  - Used for communicating 16 button to Xilinx DDS Compiler (to synthesize different carriers
- **Output:** headphone/earbud attached to hph jack

Final System Block Diagram

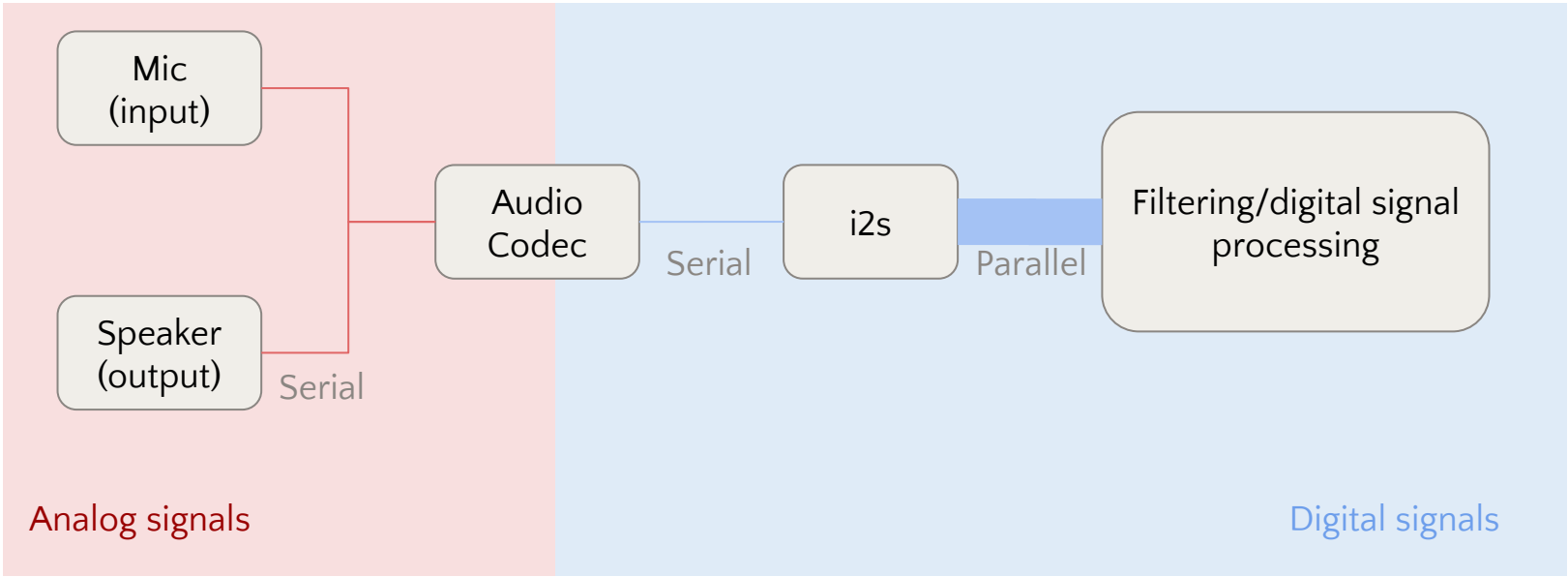


Major Components

- i2s and audio codec
  - Audio codec performs DAC/ADC for audio input/output ports on the board
  - i2s (inter-integrated circuit sound) transmits/receives digital audio data (from audio codec)
    - Converts parallel audio data (AXI stream) into serial format
    - Filters (when implemented) worked with the parallel audio data
  - Microphone/earbuds inserted into audio ports - handled by audio codec build into the board

Major Components

- i2s and audio codec



Major Components

- Button press interrupts
  - On board button: interrupt from button press event
  - 16 button keypad: input row, output col
    - 8 pins, 4 input, 4 output
    - All 1, 0 at location of press (see decoder)

```
// set columns, check rows
always @(posedge clk_100MHz)
    case(col_select)
        2'b00 : begin
                    col = 4'b0111;
                    if(scan_timer == LAG)
                       case(row)
                           4'b0111 : dec_out = 4'b0001;  // 1
                           4'b1011 : dec_out = 4'b0100;  // 4
                           4'b1101 : dec_out = 4'b0111;  // 7
                           4'b1110 : dec_out = 4'b0000;  // 0
                       endcase
                end
        2'b01 : begin
                    col = 4'b1011;
                    if(scan_timer == LAG)
                       case(row)
                           4'b0111 : dec_out = 4'b0010;  // 2
                           4'b1011 : dec_out = 4'b0101;  // 5
                           4'b1101 : dec_out = 4'b1000;  // 8
                           4'b1110 : dec_out = 4'b1111;  // F
                       endcase
```

Final Project Complexity

Description	Points
GPIO (16 button)	0.2 pts
On-board audio output port	0.5 pts
On-board microphone	0.5 pts
Total	1.2 pts

Project Improvements

- Debug and implement audio processing unit
  - Understand the filterbank/envelope detector components better
  - Implement it in 2023 version of Vivado instead of 2018
  - Handle clock/data width better
- Add multiple carrier options to make better use of 16 button
  - Multiple wave shapes
  - Different frequencies
- Redo certain modules/implementations (ex interrupt structure and sequence) to be cleaner and more responsive

Demo