

# **EEE 598: Co-Design and Modelling of Advanced Semiconductor Packaging**

**Professor Christopher Bailey**



## **Project Report**

### **Thermo-Mechanical Analysis of Solder Joint in 3D Chiplet Package with Varying Pitch Gap and Solder Joint Height**

#### **Submitted by:**

Sherry Daniel Sajan (1225838460)

Jonathan Reggie Ebenezer (1231742293)

Venkata Subrahmanya Krishna Vamshi Vemuri (1229568654)

Himanshu Parashar (1230162637)

Jay Hemal Nanavati (1229454137)

## **RESEARCH QUESTION**

The main question this project tries to answer is how the variation of pitch gap and height of solder joints influence thermal accumulation and solder joint performance, particularly in terms of failure mechanisms like thermal fatigue, void formation, and stress concentration. What role can thermo-mechanical and electrical analysis play in optimizing solder joint interconnects to mitigate these challenges and enhance the overall operational lifespan of the device? The Question aligns with the key topics covered in the course particularly about the thermal management and mechanical reliability of advanced packaging technologies and electronic components.

## **INTRODUCTION**

The semiconductor industry has been at the center of modern-day technological evolution, driving advancements in AI, computing, telecommunications, and consumer electronics. Over the decades, the pursuit of miniaturization, epitomized by Moore's Law, has been driving chip design, enabling faster, more efficient, and cost-effective devices. As industries transition from traditional two-dimensional planar architectures to three-dimensional packaging solutions like chiplets and system-on-chip (SoC) configurations, the need for smaller, more densely packed components has become imperative. This miniaturization demands innovations across design, material selection, and interconnect technologies.

Solder joints play a pivotal role in semiconductor manufacturing, serving as critical electrical and mechanical interconnects between chips and substrates. As chips shrink and their power density increases, solder joints are subjected to elevated thermal and mechanical stresses. These stresses exacerbate the risk of failure due to thermal fatigue, electromigration, or void formation, making reliability a central challenge in semiconductor packaging. Reliable solder joints are essential for ensuring device performance and for meeting industry standards for longevity and safety in applications such as automotive systems, telecommunications, and high-performance computing.

In light of these challenges, optimizing solder joint interconnects becomes critical. Though advantageous for chip miniaturization, the reduction in pitch gap and height of solder joints introduces complexities such as thermal accumulation and mechanical integrity. Understanding these dynamics through thermo-mechanical and electrical analysis is vital for improving solder joint reliability and prolonging the lifespan of semiconductor devices.

## LITERATURE REVIEW

A literature review is done to understand what research has been done related to the thermo-mechanical solder joint analysis, also including the electrical aspects such as the comparison between the electromigration behavior of Cu core solder balls (CCSBs) and Sn–Ag–Cu (SAC) solder joints under high current density and parasitic extraction of different conductor geometries in semiconductor packages for power applications. Various web sources such as Springer Nature, IEEE have been effectively used to review the existing literature.

### **Mechanical Analysis:**

The reliability of solder joints in 3D chiplet packaging is a critical concern, especially as electronic devices become smaller and more complex. Studies by Selvanayagam et al. (4) and Liu et al. (9) reveal how thermal expansion mismatches and repeated heating and cooling cycles can cause solder joints to degrade over time. These stresses lead to issues like fatigue and creep, especially in high-stress areas. Innovative solutions, such as adding underfill materials to reduce strain or designing elliptical pads and placing dummy solder balls to distribute stress more evenly, have shown promise. However, challenges like scaling down solder joints for finer pitches and addressing imperfections in fabrication remain significant hurdles.

Recent research highlights new ways to tackle these issues. Zhou et al. [2] found that smaller pitch gaps between chiplets increase heat build-up and thermal stress, but solutions like advanced bonding techniques and improved thermal interface materials (TIMs) can help manage heat more effectively. Liu et al. [3] explored how thermal cycling impacts solder joints, while Ahmed et al. [8] focused on how aging and the formation of intermetallic compounds (IMCs) influence joint performance under electrical stress. Their findings suggest that while IMCs can help reduce failures by acting as barriers to material diffusion, aging still weakens the joints. Together, these studies show the need for a balanced approach that combines smarter designs, better materials, and advanced simulations to ensure solder joints in 3D chiplet packaging remain reliable and durable.

The findings from these studies offer important insights into the complex factors that affect solder joint reliability. Selvanayagam et al. [4] showed that thermal expansion mismatches between materials and temperature cycling can cause significant stress and fatigue in solder joints. However, they found that adding underfill materials can drastically reduce this stress, improving reliability. Liu et al. [9] took this further by exploring how the geometry and layout of solder joints, like using elliptical pads and placing dummy solder balls in key areas, can help spread out stress and extend the life of the joints. Zhou et al. [2] highlighted the issue of thermal buildup in chiplet packaging, especially when the pitch gap is small, and found that advanced bonding methods, like bumpless hybrid bonding, could help reduce thermal stress while improving heat dissipation. Liu et al. [3] focused on thermal cycling and identified that solder

joints in the upper layers and along the edges are more likely to fail. Ahmed et al. [8] looked into how aging and the formation of intermetallic compounds (IMCs) impact solder joints, finding that while IMCs help reduce failures, aging can weaken the joints over time.

Looking ahead, there are plenty of opportunities to expand on these findings. Future research will need to focus on combining thermal, electrical, and mechanical simulations to better understand how these factors work together in real-world conditions. New materials that handle both thermal and mechanical stresses better, such as advanced thermal interface materials (TIMs) and improved solder alloys, could also enhance the durability of solder joints. As chiplet packaging continues to scale down, innovative design techniques and bonding methods will be needed to manage stress in tighter spaces. Long-term studies on aging and electromigration are essential for ensuring the longevity and performance of these advanced systems.

These results directly relate to our project, which focuses on how variations in pitch gap and height affect thermal accumulation, electromigration, and solder joint reliability in 3D chiplet packages. The studies provide a strong foundation for understanding how pitch gap affects thermal and electrical performance. By incorporating these insights, we aim to optimize solder joint designs to address both thermal management and mechanical reliability, ultimately contributing to the development of more robust and durable 3D chiplet packaging technologies.

### **Electrical Analysis:**

Electromigration (EM) phenomenon occurs when high-density electrical currents cause metal atom migration in solder joints, leading to reliability issues. Key effects include void formation near the cathode, increasing resistance and localized heating, and intermetallic compound (IMC) growth, which alters joint properties. Current crowding further intensifies EM by concentrating electrical stress at specific points, especially in smaller joints. These effects are particularly severe in SAC solder joints, where high current densities near the cathode edge accelerate void formation and reduce joint lifespan. The study [7] explores the performance of Cu core solder balls (CCSBs) in mitigating electromigration (EM) failures compared to traditional Sn–Ag–Cu (SAC) solder joints. The study employs a combination of finite element method (FEM) simulations and experimental analyses to investigate the reliability of these solder joints under high current density and elevated temperatures.

This paper [7] was chosen for review due to its direct alignment with the goals of our project, which investigates the influence of solder joint dimensions (pitch gap and height) on thermal and mechanical reliability. While our project emphasizes thermal modeling, this paper's focus on electromigration provides critical insights into the electrical behavior of solder joints. By integrating thermal and electromigration analyses, we aim to build a comprehensive understanding of the failure mechanisms affecting solder joint reliability in miniaturized semiconductor packaging.

Solder joints are essential interconnects in semiconductor packaging, enabling electrical conductivity and mechanical stability. As the industry moves toward denser and more compact designs, the reduction in solder joint dimensions—particularly pitch gap and height—presents significant challenges, such as increased susceptibility to thermal accumulation and electromigration (EM). This review highlights the impact of these factors, drawing on advancements in Cu core solder ball (CCSB) technology to mitigate failure mechanisms.

### **Electromigration: A Key Challenge in Solder Joints**

Electromigration (EM) is a critical phenomenon in which high-density electrical currents cause the movement of metal atoms within solder joints, leading to significant reliability challenges. One major effect of EM is void formation, where material depletion near the cathode interface results in voids that increase resistance and cause localized heating. Additionally, intermetallic compound (IMC) growth occurs at the anode and cathode, progressively altering the mechanical and electrical properties of the solder joint. Another significant issue is current crowding [10], where uneven current distribution creates concentrated electrical stress at specific points, exacerbating the effects of electromigration, particularly in smaller solder joints. These issues are especially severe in traditional SAC solder joints, where high current densities near the cathode edge accelerate void formation and significantly shorten the joint's lifespan.

### **Parasitic Elements - A Parallel Study**

Electrical parasitics - namely inductance, capacitance and resistance interfere with the true design motive of a semiconductor package. Parasitic resistance can cause additional Joule Heating and cause the package to heat abnormally - forming hotspots and wear out the traces, solder joints and chiplets earlier than predicted, especially in scenarios that involve high current and high voltage applications - like power modules. Parasitic Inductances and Capacitances on the other hand, interfere with signals in communication modules, and cause signal loss. Although completely eliminating parasitics is not possible, with accurate modeling they may be incorporated into the package design to prevent unwelcome characteristics.

The thesis document titled “Electrical Design Considerations and Packaging of Power Electronic Modules” [5] explores the variation of electrical parasitics (inductance and resistance) of semiconductor packages with changes in physical dimensions.

Although this study is not specifically done on solder joint geometry, it is quite relevant to the scope of the project, as terminal connector size can be correlated to solder joint size. The basic intuition obtained from this study - that “bigger” dimensions do not always lead to increased parasitics - can be used while planning solder joint geometry and spacing of a semiconductor package.

## **Advancements in Cu Core Solder Balls (CCSBs)**

Cu core solder balls (CCSBs) have gained attention as a superior alternative to traditional SAC joints, particularly for their enhanced performance under electromigration stress. The copper core's high conductivity enables more efficient distribution of electrical and thermal stress. Finite element method (FEM) simulations demonstrate that CCSBs reduce peak current density by approximately 10% compared to SAC joints, mitigating void formation and increasing joint durability. Experimental studies further reveal that CCSBs exhibit a time-to-failure (TTF) 1.73 times longer than SAC joints under identical conditions, with a current density of  $0.9 \times 10^4$  A/cm<sup>2</sup> and a temperature of 100°C. This improvement is due to the copper core's ability to effectively channel current, minimizing void formation at critical locations. Additionally, directing current through the copper core significantly reduces electromigration flux in the solder material, enhancing structural stability and decreasing void formation during stress testing. The copper core also maintains structural integrity by preventing joint collapse during reflow and preserving stand-off height, thereby improving mechanical stability.

## **Thermal Analysis and Its Interaction with Electromigration**

While electromigration is the primary failure mechanism under electrical stress, thermal effects play an equally critical role. High current densities result in localized heating, which accelerates atomic diffusion rates, thereby intensifying electromigration and causing thermal fatigue. One key thermal effect is hotspot formation, as identified by FEM contour plots in ANSYS simulations, which highlight regions prone to localized heating that align with areas of high current density. Another significant effect is thermal fatigue, where repeated thermal cycling generates mechanical stresses, increasing the likelihood of crack propagation and solder joint failure. Although the primary focus of the paper [7] is on electromigration, it also examines the interaction between thermal and electrical stresses. The findings reveal that Cu core solder balls (CCSBs) exhibit superior heat dissipation and reliability compared to SAC joints, making them more resilient under combined stress conditions.

## METHODOLOGY

### **Methodology used to answer Research Question-**

The methodology employed in this study begins with developing a comprehensive 3D model of a semiconductor chiplet, which incorporates essential components, including the substrate, silicon dies, solder joints, and micro bumps. This model is the foundation for executing a parametric analysis directed specifically at the solder joints.

The initial model is a quarter geometry constructed utilizing a standard pitch of 1.77 mm and a solder joint height of 0.37 mm. The geometric model is designed using Solidworks, taking advantage of its advanced CAD integration. Special attention is paid to accurately represent component dimensions and interconnections, particularly for the solder joints, depicted as hemispherical elements, to capture stress and thermal behavior. The Steady-State Thermal module of ANSYS is utilized to assess the thermal performance of the chip. This analysis encompasses the application of heat generation rates within the silicon die to emulate power dissipation, alongside the definition of thermal boundary conditions at the substrate and external interfaces, such as convection or fixed temperature. The thermal distribution is calculated, highlighting maximum and minimum temperature readings across the chip. Areas of thermal concentration are identified to evaluate potential hotspots. The results are visually represented as contour plots, providing insights into critical regions where heat accumulation may compromise solder joint integrity. The next step is Mechanical Analysis. The thermal load as input, a Static Structural analysis is performed to examine the thermo-mechanical behavior of the solder joints. Temperature distributions derived from the thermal analysis are mapped onto the structural model through imported temperature loads, ensuring a seamless transition between the analysis. The boundary conditions include fixed supports applied to the bottom face of the substrate to replicate PCB constraints and frictionless support in the symmetry planes along XZ and YZ, with additional constraints possibly imposed to emulate packaging conditions.

Thermal stresses and strains are computed based on temperature-induced material expansion. The ANSYS Mechanical solver assesses regions of high-stress concentration, particularly within the solder joints, which are susceptible to thermal fatigue and cracking under cyclic loading conditions. After the thermo-mechanical analysis of the base model is done, a parametric analysis is performed. The dimensions of the solder balls are systematically varied by reducing the pitch gap and height, thereby simulating trends associated with miniaturized semiconductor designs. For each configuration, Thermal and Structural Analysis are re-conducted to investigate variations in temperature distribution, stress concentration, and mechanical reliability. Our methodology uses ANSYS for mechanical and electrical analysis of hotspot formation and thermal stress due to varying pitch gaps, and for simulating thermal cycling to assess solder joint fatigue and predict failure risks.

**Relation of Methodology learned in class-** The methodology incorporates concepts such as **Chip Design**, **Thermal Analysis of Chips**, and the use of ANSYS Mechanical and **Electronics Desktop**, which were essential concepts in the course. In addition, chiplet design and advanced modeling in ANSYS Electronics Desktop represent new skills acquired and applied in this project.

**New Methods Used in Research-** ANSYS Workbench, ANSYS Mechanical Workbench (Static Structural and Transient Thermal).

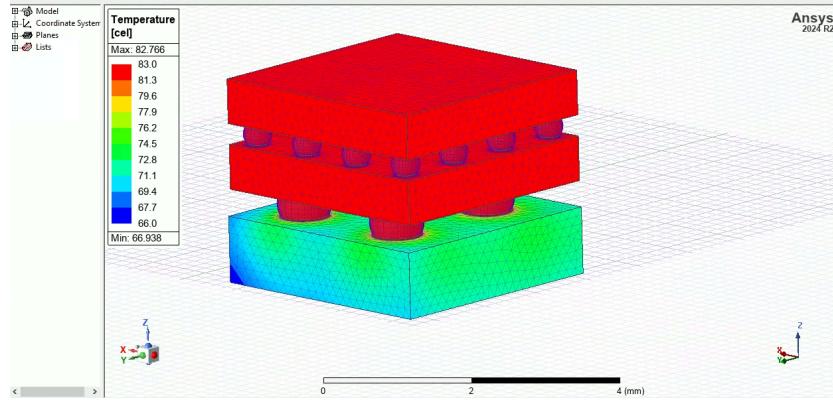
**Why are the above methodologies appropriate to solving the research question-** These tools were crucial for performing the Thermo-Mechanical analysis, addressing the research question by enabling the analysis of solder joint performance and thermal accumulation under varying geometries. This integration of coursework and new methods highlights the relevance and effectiveness of the approach.

## RESULTS OBTAINED

The primary objective of this study was to evaluate the thermal and mechanical performance of solder joints in a semiconductor chip under varying conditions. The analysis consists of thermal and mechanical ANSYS simulations focused on temperature distribution, stress-strain behavior, and their implications on solder joint performance. The results obtained from ANSYS simulations provided critical insights into the effects of reduced pitch gap and solder joint height.

### Thermal Analysis

Initially, a simple thermal analysis was performed on a quarter geometry model using ANSYS Electronics Desktop (ED). This provides an idea of how the heat is generated and is spread across the chip. It can be seen from the temperature contour plot that most of the dissipated heat is distributed to the substrate through the solder joints. So, the heat conduction of the solder joints is important in the chip's heat management process. The Ansys ED analysis was performed to understand how the heat flows in the chip. Ansys Workbench will be used to understand better and conduct a deeper thermal analysis.



*ANSYS Electronics Desktop Model*

In the Thermal Analysis, we utilized a simplified chip model designed in ANSYS Workbench to study the thermal performance of solder joints under varying pitch dimensions. The primary goal is to evaluate how changes in the pitch gap influence temperature distribution across the chip and within the solder joints. By systematically varying the pitch, we aimed to understand the impact of miniaturization on thermal behavior, mainly focusing on heat accumulation, hotspot formation, and temperature gradients. Initially, a pitch of 1.77mm and a solder joint height of 0.37mm is used and used as a reference to the parametric study. Consequently, the pitch is varied (0.9mm and 2.5mm) keeping the reference height to study the behaviour. Similarly, the height of the joint is varied (0.5mm and 1.5mm) keeping the pitch constant at 1.77mm. This parametric analysis allowed us to explore the relationship between reduced spacing and the thermal reliability of solder joints, providing insights critical for optimizing semiconductor packaging designs.

#### A) Varying of Pitch:

The parametric analysis is performed by varying the pitch. The temperature variation and distribution of each model can be seen here. The impact of varying solder joint pitch on thermal behavior was explored by analyzing three configurations: a reference pitch of 1.77 mm, a reduced pitch of 0.9 mm, and an increased pitch of 2.5 mm. The objective was to understand how these changes affect the chip's temperature distribution, heat accumulation, and overall thermal dynamics.

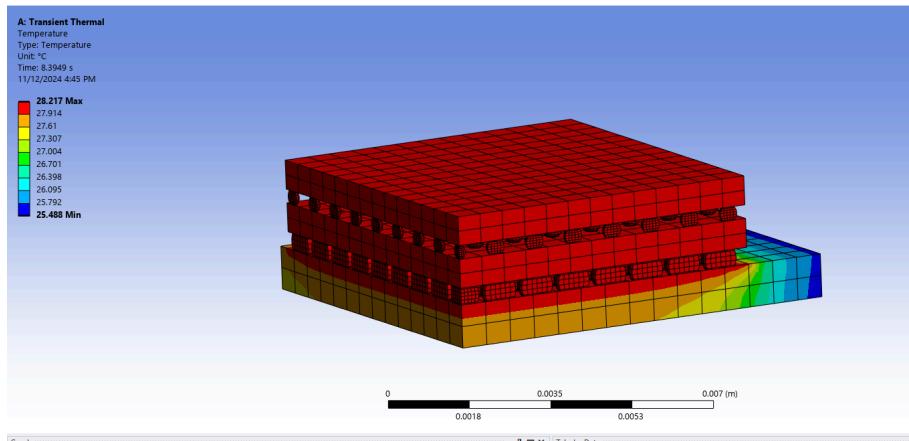
For the reference pitch of 1.77 mm, the temperature distribution appeared relatively balanced across the chip. Hotspots were observed near the solder joints and silicon die regions, but the thermal gradients were moderate, offering an effective baseline for comparison. This pitch dimension highlights the equilibrium between thermal performance and packaging density in conventional designs.

When the pitch was reduced to 0.9 mm, a noticeable intensification of thermal concentration occurred, particularly around the solder joints. The reduced spacing between adjacent joints

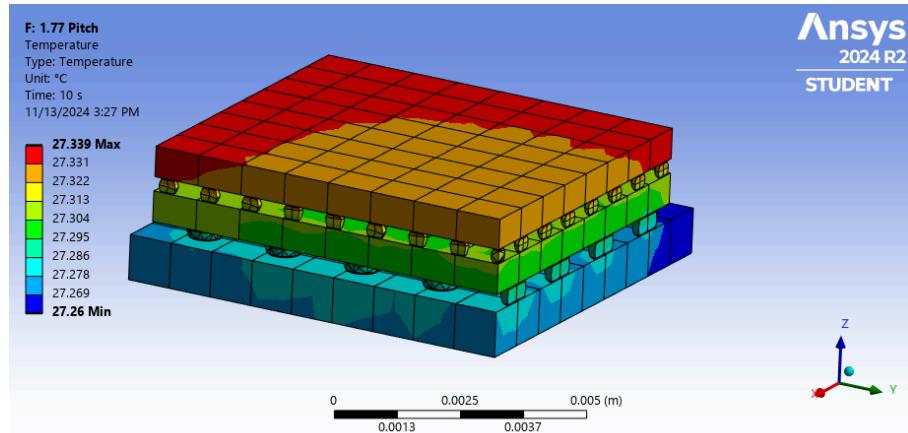
restricted efficient heat dissipation, resulting in elevated maximum temperatures and more localized hotspots. This phenomenon can be attributed to increased thermal coupling, where the heat flux from closely spaced solder joints overlaps, leading to higher thermal gradients. Such conditions indicate potential risks under prolonged operational loads, including solder joint fatigue or overheating. However, because of the more significant number of joints and the smaller spacing between them, the overall heat is distributed throughout the substrate.

Conversely, the thermal distribution improved significantly for the increased pitch of 2.5 mm. Hotspots became less pronounced, and the overall temperature gradients diminished. The wider spacing allowed for better heat spreading and reduced thermal interaction between adjacent solder joints. However, while thermally advantageous, this configuration might be less suitable for modern semiconductor designs prioritizing high packing density and miniaturization.

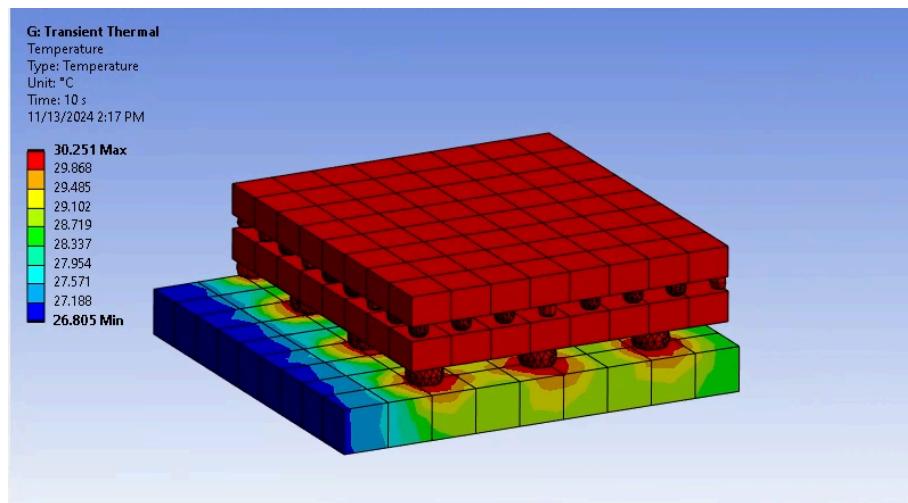
These results reveal the trade-offs inherent in pitch variations. Reduced pitch, while enabling greater packaging density, compromises thermal reliability due to heightened thermal accumulation. On the other hand, increased pitch enhances thermal performance but may be impractical in compact electronic designs. An optimal pitch is required to balance thermal management and spatial efficiency, supporting both reliability and design trends in the semiconductor industry.



*0.9mm Pitch Thermal Distribution Analysis- Temperature Plot*



1.77 mm Pitch Thermal Distribution Analysis - Temperature Plot



2.5 mm Pitch- Thermal Distribution Analysis- Temperature Plot

### B) Varying of Solder Height:

The effect of solder joint height on thermal behavior was analyzed by comparing three configurations: a reference height of 0.37 mm, an increased height of 0.5 mm, and a reduced height of 0.18 mm. This study aimed to understand how variations in joint height influence temperature distribution, thermal gradients, and heat dissipation efficiency in the chip.

The thermal analysis for the standard height of 0.37 mm demonstrated a balanced temperature distribution with moderate thermal gradients across the solder joints. As expected, hotspots were observed near the joints, but their intensity and spread were tolerable. This configuration served as a baseline for assessing the impact of height variations on thermal performance.

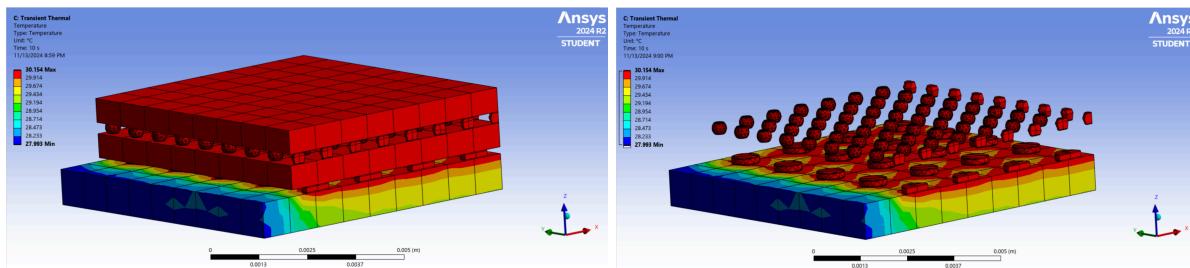
Increasing the solder joint height to 0.5 mm resulted in a more uniform temperature distribution and reduced thermal gradients. The taller joints provided an extended thermal path, allowing heat to dissipate more effectively through the joint. This led to a decrease in the maximum

temperature observed in the chip. However, excessively tall solder joints may introduce mechanical drawbacks, such as increased susceptibility to shear stress under thermal cycling, which must be considered in reliability studies.

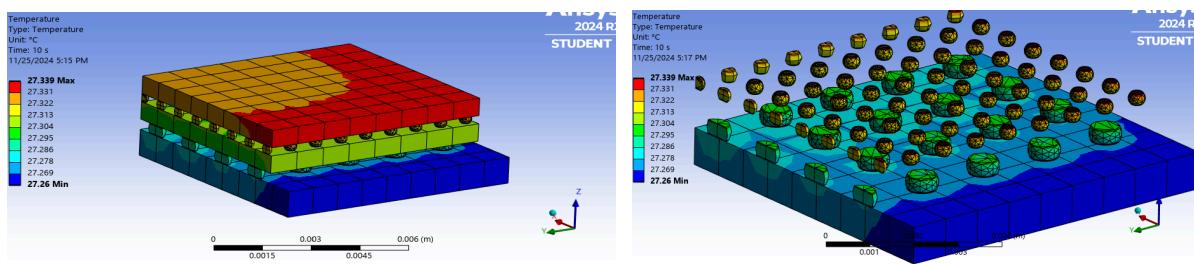
Decreasing the solder joint height to 0.18 mm significantly increased thermal concentration near the joint regions. The shorter thermal path reduced the heat dissipation ability, leading to higher localized temperatures and more pronounced hotspots. This configuration underscores the challenges of miniaturization, where reduced joint heights can exacerbate thermal issues and compromise the joint's ability to handle heat loads effectively.

**Impact of Increased Height:** Taller solder joints enhance thermal performance by providing better heat dissipation. However, while thermally beneficial, they may compromise mechanical reliability and conflict with industry trends of minimizing package height.

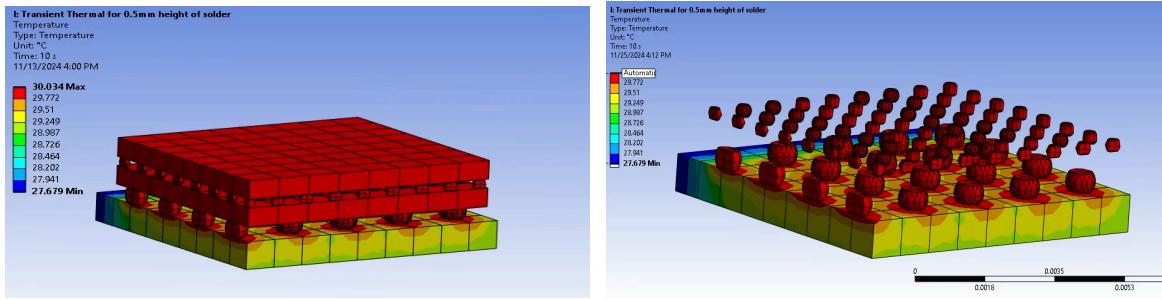
**Impact of Reduced Height:** Shorter solder joints result in higher thermal resistance, localized overheating, and increased risk of thermal fatigue or failure. While they support compact designs, the thermal trade-offs make them less reliable in high-performance applications. The analysis highlights the need for a balanced approach in determining solder joint height. While increased height improves thermal management, reduced height supports miniaturization goals. This study emphasizes that solder joint height optimization must account for thermal and mechanical considerations to enhance the reliability and longevity of semiconductor packages.



Solder Height of 0.18 mm- Thermal analysis



Solder Height of 0.37 mm- Thermal analysis

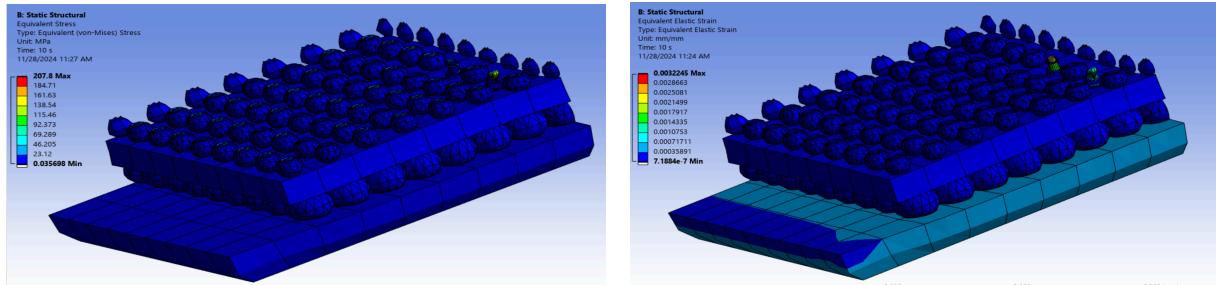


*Solder Height of 0.5 mm- Thermal analysis*

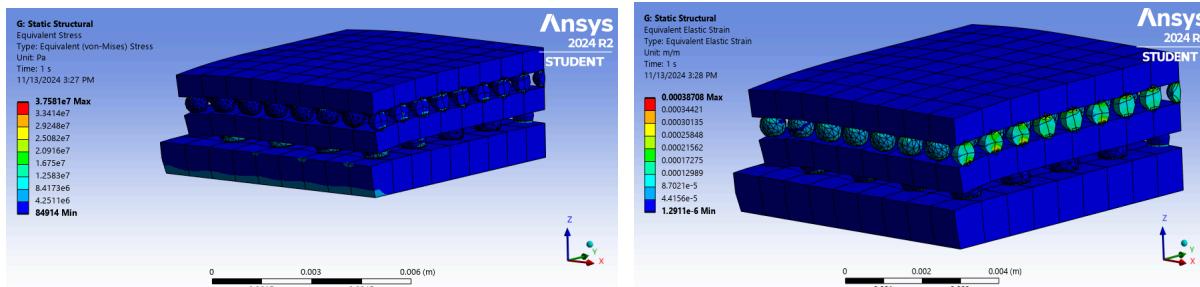
## Mechanical Analysis:

In the Mechanical Analysis, we utilized the same simplified chip model designed in ANSYS Workbench to study the mechanical performance of solder joints under varying pitch dimensions and solder heights. This is done to evaluate how changes in the pitch gap & Solder Height influence Stress and Strain distribution across the chip and within the solder joints.

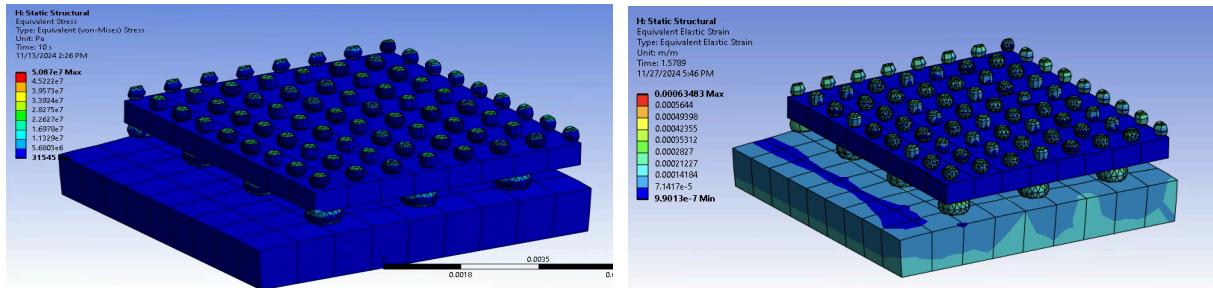
### A) Varying of Pitch:



*0.9 mm Pitch- Stress & Strain Distribution*

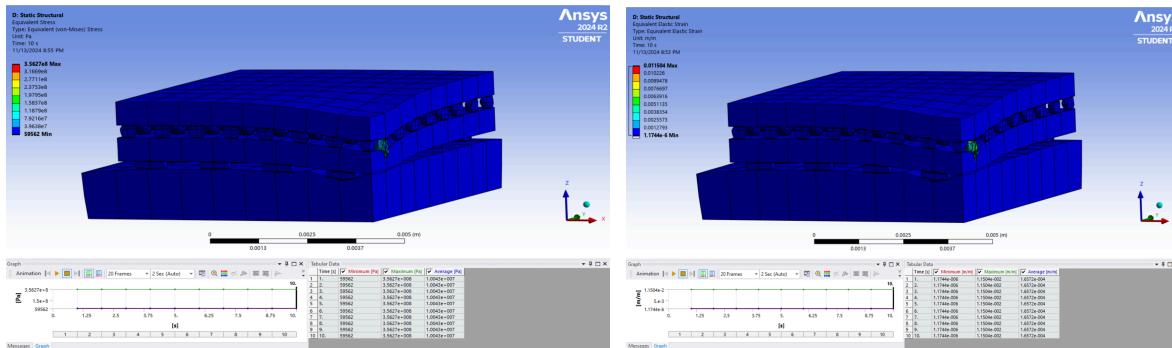


*1.7 mm Pitch- Stress & Strain Distribution*

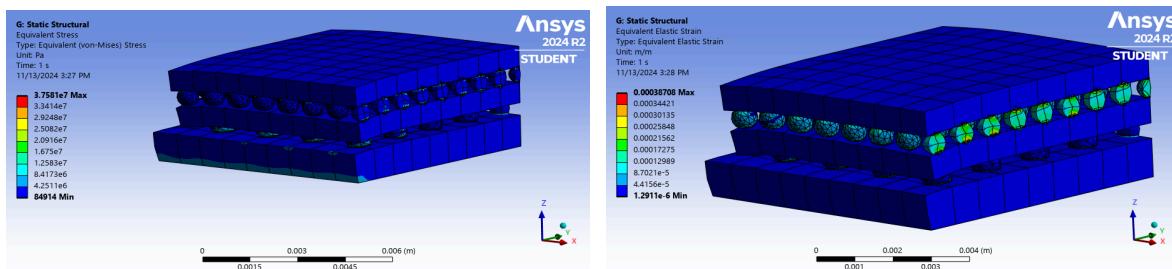


*2.5 mm Pitch- Stress & Strain Distribution*

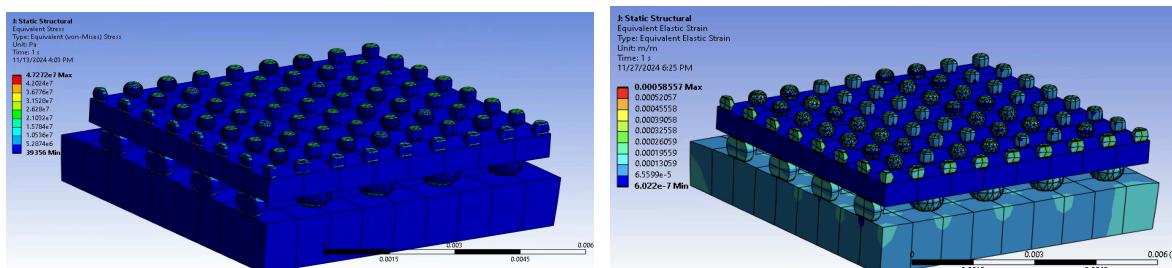
## B) Varying of Solder Height:



*Solder Height of 0.18 mm- Stress & Strain Distribution*



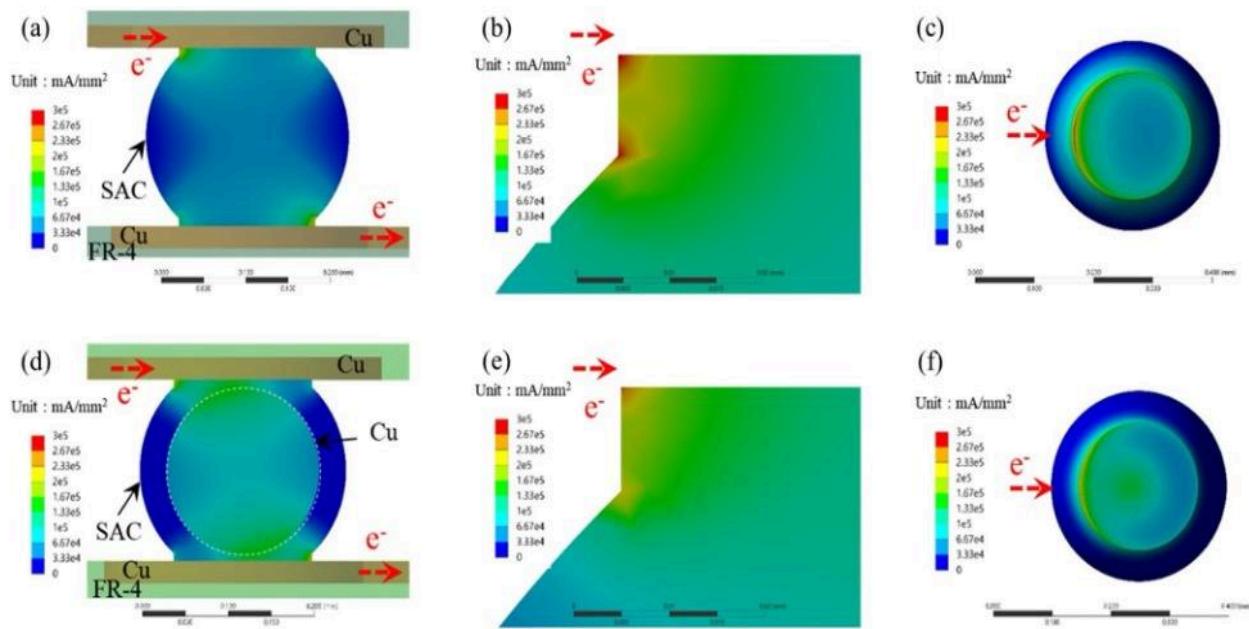
*Solder Height of 0.37 mm- Stress & Strain Distribution*



*Solder Height of 0.5 mm- Stress & Strain Distribution*

## Electrical Analysis:

The results analysed by Jeong, H., Lee, [7] highlight the superior performance of Cu core solder balls (CCSBs) over traditional SAC solder joints under combined electrical and thermal stress conditions. The figure below illustrates the localized heating and current distribution in SAC and CCSB solder joints, as observed through FEM contour plots using ANSYS simulations. These plots show that CCSBs experience reduced current density and lower hotspot formation compared to SAC joints, which correlates with improved thermal and electrical reliability. The lower peak current density in CCSBs mitigates void formation and enhances overall joint durability.



*Fig: Contour plots of the current density for a–c SAC and d–f CCSB solder joints with a current density of  $0.9 \times 10^4 \text{ A/cm}^2$ . a,d Whole solder joint, d,e current crowding region, and c,f top view of the solder joint [7]*

In addition to these thermal effects, the figure below presents the comparative time-to-failure (TTF) results for SAC and CCSB solder joints under identical stress conditions. The data clearly demonstrate that CCSBs have a significantly longer TTF, with a value 1.73 times greater than that of SAC joints, highlighting the effectiveness of the copper core in enhancing joint longevity. This extended TTF is attributed to the copper core's ability to effectively channel current, reducing void formation and improving structural stability.

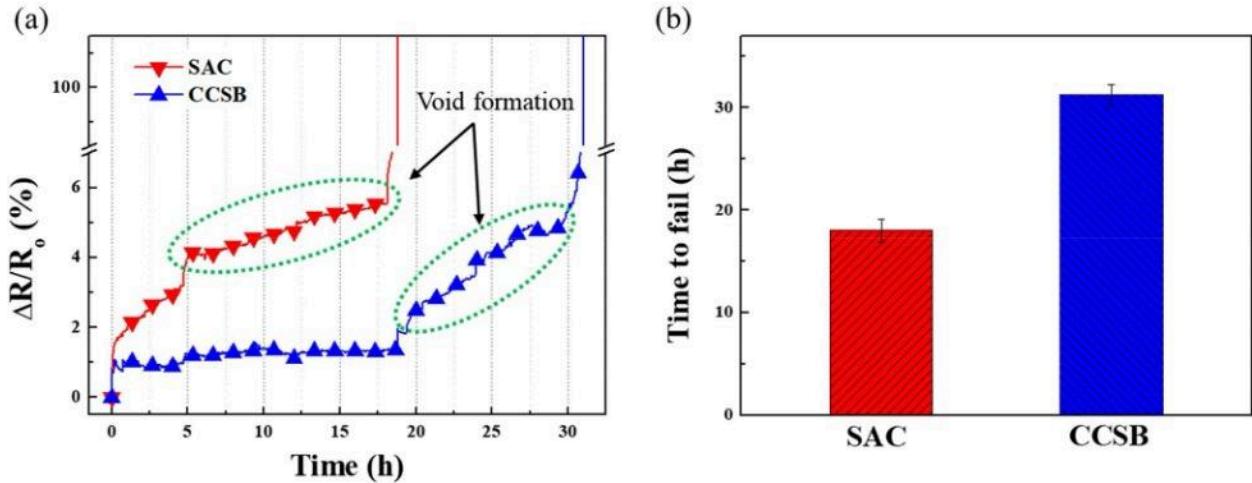


Fig: Result of electromigration of the SAC joint and CCSB joint. (a):  $\Delta R/R_0$  versus time of the solder joints at  $0.9 \times 10^4$  A/cm<sup>2</sup> at 100 °C (b): time to failure after the electromigration test [7]

Table below provides a concise comparison of key performance metrics for SAC and CCSB solder joints, which further emphasizes the advantages of CCSBs in miniaturized designs. As shown in the table, CCSBs exhibit a lower maximum current density ( $2.66 \times 10^6$  A/cm<sup>2</sup> compared to  $2.93 \times 10^6$  A/cm<sup>2</sup> for SAC joints) and a significantly longer time-to-failure (31.2 hours vs. 18.0 hours). Additionally, CCSBs demonstrate a reduced void formation rate and maintain better structural integrity post-reflow, making them more reliable under thermal cycling and electrical stress conditions.

Property	SAC Solder Joint	CCSB Solder Joint
Maximum Current Density (A/cm <sup>2</sup> )	$2.93 \times 10^6$	$2.66 \times 10^6$
Time-to-Failure (TTF) (hours)	18.0	31.2
Void Formation Rate	High	Low
Structural Integrity Post-Reflow	Reduced	Maintained

Table: Comparison of SAC and CCSB solder joint properties [7]

## **Importance of these Results/Findings:**

These findings highlight the potential effects of the dimensional aspects of the solder balls and help us mitigate the thermal and mechanical challenges, such as hotspot formation, fatigue, and stress concentration. Further, it helps in understanding CCSBs as a viable solution to address the challenges of electromigration and thermal fatigue in advanced solder joint designs, ensuring higher reliability in miniaturized and high-performance electronic applications.

## **CONCLUSION AND FUTURE WORK**

### **Conclusion:**

This study provides valuable insights into the influence of pitch gap and solder joint height on thermal accumulation and solder joint reliability. Key conclusions are as follows:

1. Impact of Reduced Pitch Gap and Height: Decreasing the pitch gap and solder joint height increases thermal accumulation and stress concentration, especially in the areas adjacent to solder joints. These changes amplify thermal fatigue risks and mechanical failure mechanisms, such as void formation and cracking.
2. Hotspot Identification and Mitigation: Thermal analysis revealed that hotspots are most pronounced at smaller pitch gaps due to restricted heat dissipation. Proper thermal management strategies, such as optimizing TIM (Thermal Interface Material) placement or using alternative materials with higher thermal conductivity, can mitigate these effects.
3. Thermo-Mechanical Coupling: The parametric analysis demonstrated that stress concentration within solder joints directly correlates with thermal loads. Higher stresses are observed in reduced-pitch configurations, which could shorten the operational lifespan of semiconductor devices through cyclic fatigue.
4. Design Implications: Findings highlight the need for a balanced design approach in semiconductor packaging, emphasizing the interplay between miniaturization and mechanical robustness.
5. Electro-Migration and Electrical Analysis: The study's focus on electromigration, particularly in Cu core solder balls (CCSBs), aligns with our project by examining how variations in solder joint dimensions, such as pitch gap and height, impact thermal accumulation and mechanical reliability. The comparative analysis of SAC and CCSB solder joints provides valuable insights into optimizing solder joint designs for improved electrical performance and material stability.

## **Future Work and Advice:**

To build on the insights gained in this project, future work should explore the following:

### 1. Advanced Material Characterization:

- Investigate alternative solder materials and novel interconnects, such as conductive adhesives or low-temperature solders for better thermal and mechanical performance.
- Explore the use of gradient or composite materials within solder joints to improve thermal cycling resilience.

### 2. Dynamic Loading and Reliability Testing:

- Incorporate dynamic loading scenarios, such as vibration or shock, to evaluate the combined effects of mechanical and thermal stresses on solder joints.
- Simulate real-world operational conditions, including power cycling and environmental variations, for enhanced reliability assessment.

### 3. Electro-Migration and Electrical Analysis:

- Extend the analysis to include electrical failure mechanisms like electro-migration under high current densities, particularly in miniaturized configurations.

### 4. Optimization of Cooling Strategies:

- To address heat accumulation in reduced-pitch designs, investigate advanced cooling solutions, such as micro-channel heat sinks or phase-change materials.

## **Research Methodology for the Study**

The methodology that can be followed to get started on this topic would be to understand the industry standards that are being used at the moment. Explore the influence of pitch gap and solder joint height on thermal accumulation and solder joint reliability, a research methodology combining simulation, experimental validation, and analytical techniques is recommended.

### 1. Simulation-Based Approach:

- Use finite element analysis (FEA) tools like **ANSYS Icepak** and **Mechanical** for thermal and structural simulations.
- Model solder joints with varying pitch gaps and heights, applying thermal loads, and assessing stress distribution.
- Perform coupled thermal-mechanical simulations to understand the interplay between heat accumulation and mechanical stress.

### 2. Experimental Validation:

- Prototype solder joints with controlled dimensions.
- Use thermal imaging and strain gauges to measure real-world temperature distributions and mechanical stress under operational conditions.

### 3. Parametric Analysis:

- Vary parameters systematically (pitch gap, solder joint height, material properties) to identify thermal and mechanical performance trends.

- Utilize Design of Experiments (DOE) to optimize factors influencing reliability.
4. Comparative Analysis:
- Compare SAC and CCSB solder joint performance in terms of thermal dissipation, electromigration resistance, and stress handling.
  - Conduct life-cycle assessments under accelerated testing conditions.

## **Importance of the Research**

The advised methodology is critical for several reasons:

- Understanding thermal accumulation and stress distribution is essential to mitigate reliability issues like solder fatigue and void formation as semiconductor devices continue to shrink.
- Insights from the research enable optimization of solder joint designs, balancing miniaturization with mechanical robustness and operational longevity.
- Identifying and mitigating hotspots through TIM optimization or alternative materials ensures better thermal dissipation, reducing the likelihood of device failure.
- By studying SAC and CCSB solder joints, the research can inform the development of new materials that combine superior thermal and mechanical performance with resistance to electromigration.
- The semiconductor industry demands higher power densities and reduced form factors. This research supports innovation in packaging technologies to meet these demands without compromising device reliability.
- Results can guide production processes by refining solder joint dimensions, improving quality control, and minimizing manufacturing defects.

This methodology advances theoretical understanding and has practical applications in the design and manufacturing of reliable semiconductor devices.

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