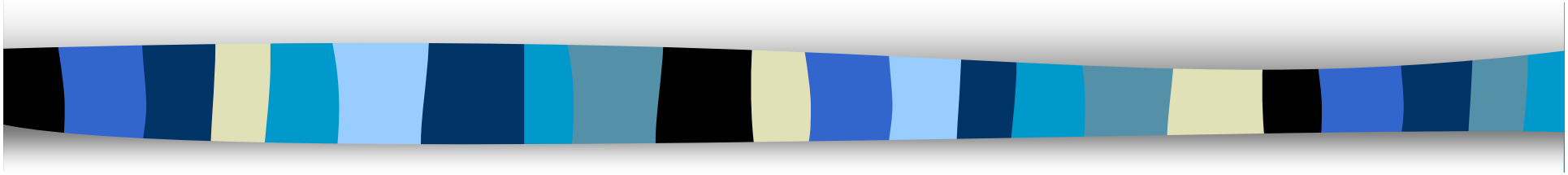
Micro . Computer System Lab.

Introduction

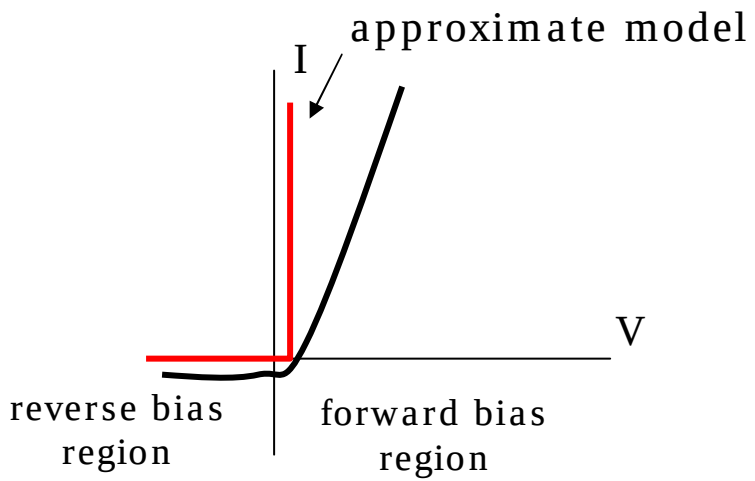


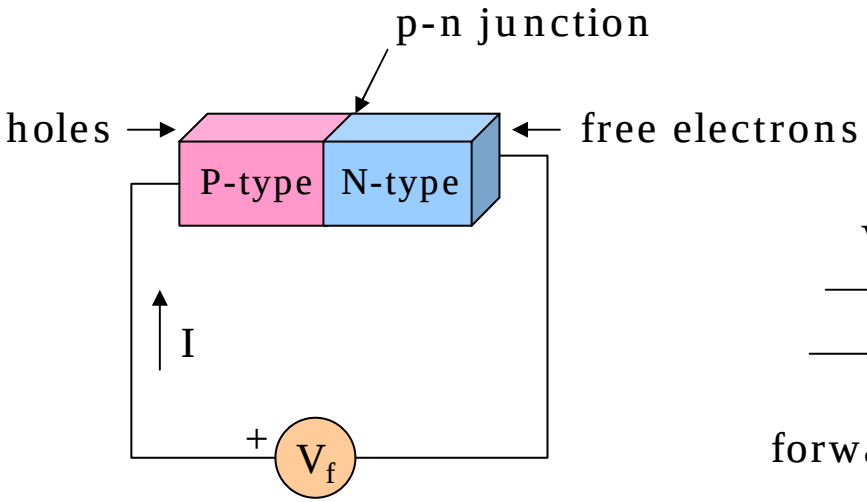
Outline

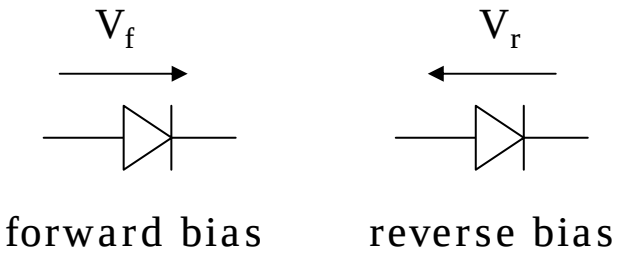
- From Diode to Micro Computer System
  - Technologies briefing
- Micro Computer System Basics

From Diode to Micro Computer System

- Diode switch

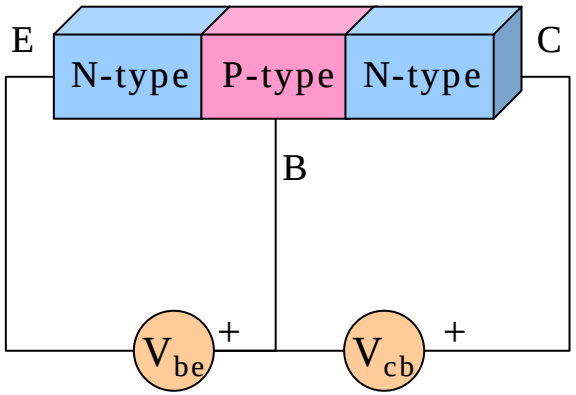


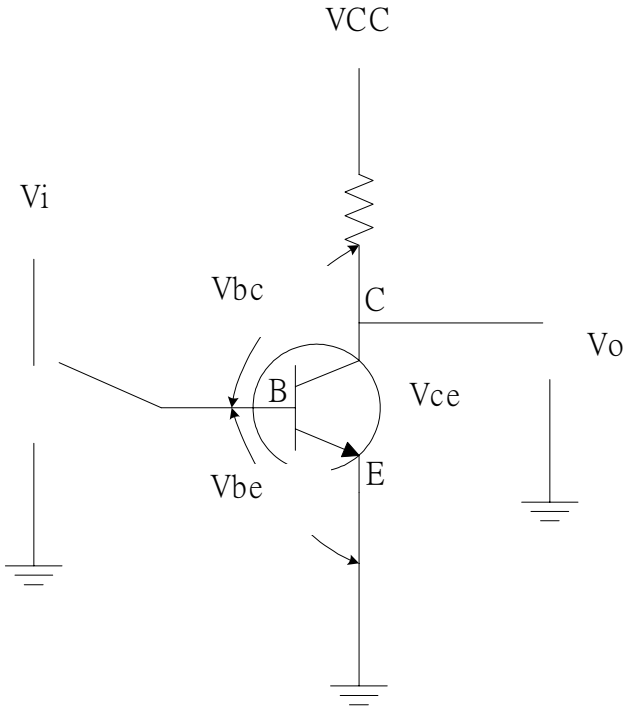




From Diode to Micro Computer System (Cont.)

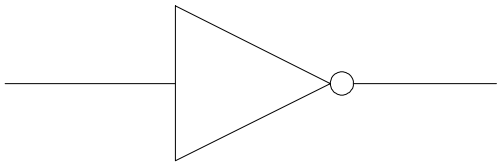
- Transistor switch
  - npn BJT



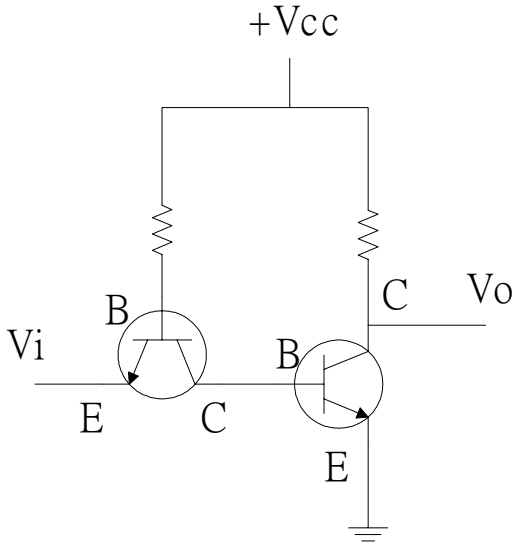


From Diode to Micro Computer System (Cont.)

- Transistor switch (Cont.)
  - Inverter

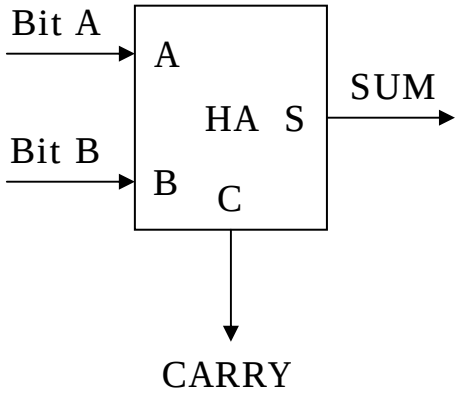


Xi	Xo
0	1(+V)
1(+V)	0



From Diode to Micro Computer System (Cont.)

- Combinational logic design
  - Half adder



A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

AB	0	1
0	0	1
1	1	0

S

AB	0	1
0	0	0
1	0	1

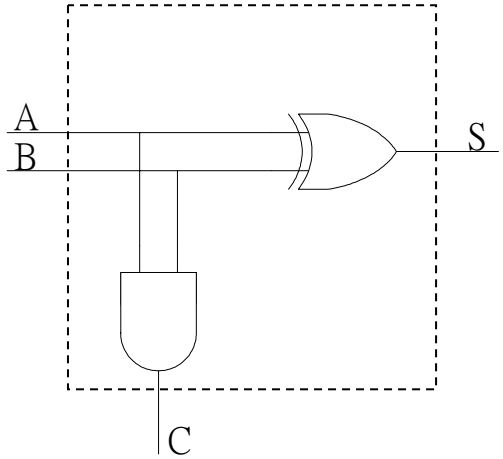
C

S=A⊕B

C=A•B

From Diode to Micro Computer System (Cont.)

- Combinational logic design
  - Half adder (Cont.)



From Diode to Micro Computer System (Cont.)

- Combinational logic design
  - Arithmetic and logic units (ALUs)

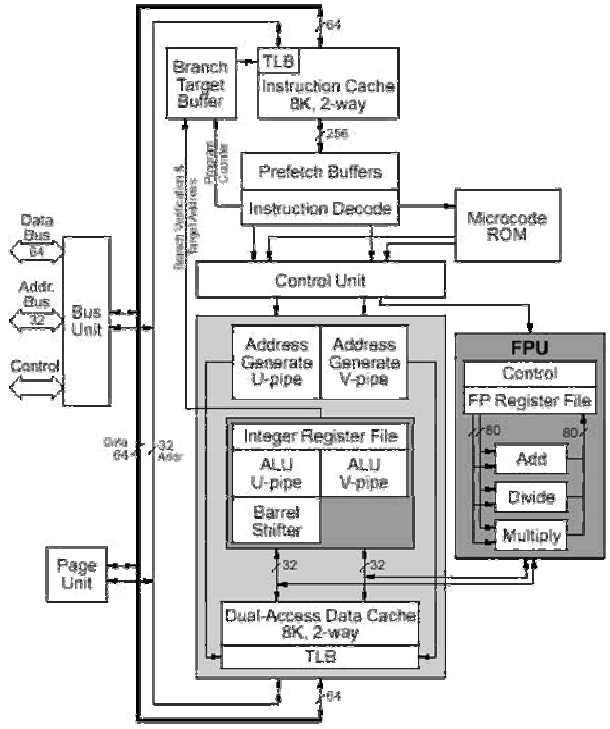
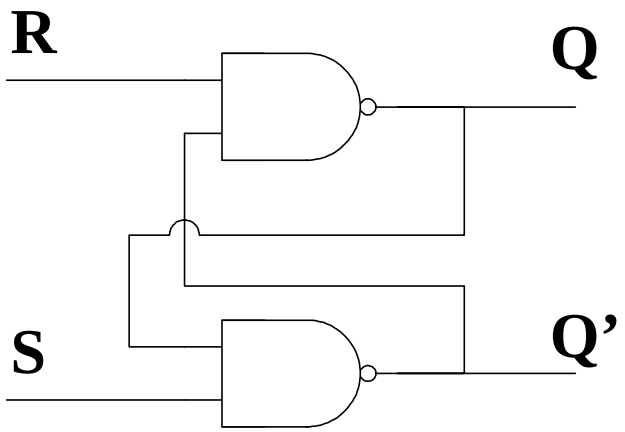


Figure 1. Pentium block diagram.

From Diode to Micro Computer System (Cont.)

- Combinational logic design
  - Flip-flop



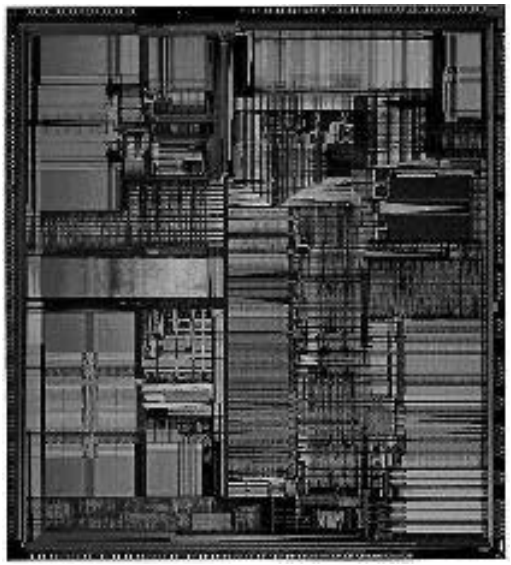
R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	X

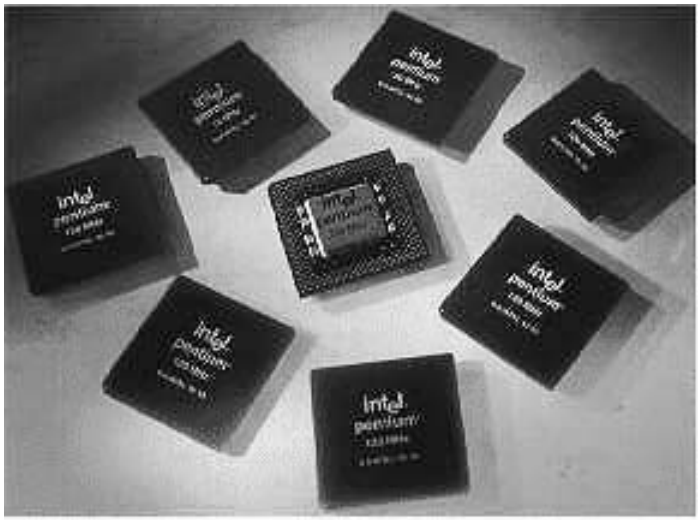
From Diode to Micro Computer System (Cont.)

- Combinational logic design
  - Memory
    - Register, cache, RAM, …

From Diode to Micro Computer System (Cont.)

- Processor
  - CPU, Microprocessor



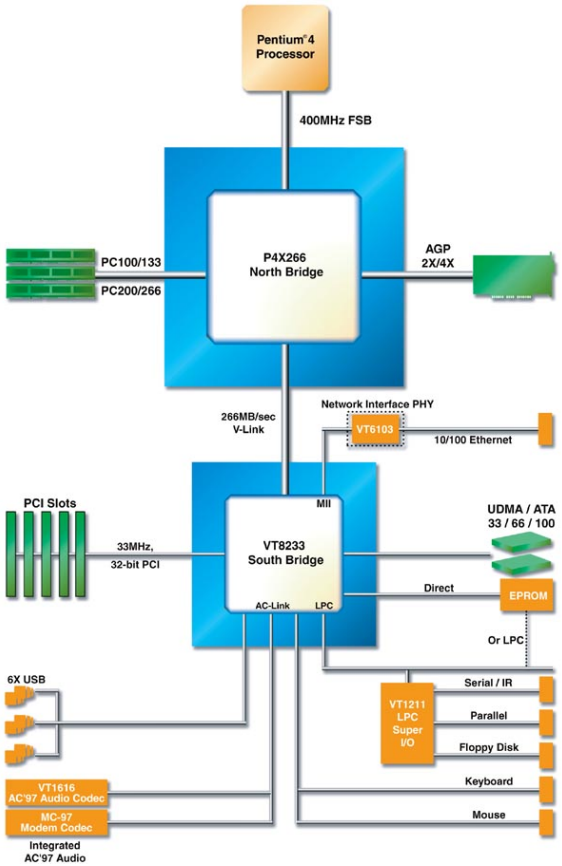


From Diode to Micro Computer System (Cont.)

- Processor vs. computer
  - Micro computer, mini computer, mainframe, super computer, ...
- Computer vs. controller
  - integrated circuit semiconductor chip that performs the bulk of the processing and controls the parts of a system; "a **microprocessor** functions as the central processing unit of a microcomputer"; "a disk drive contains a microprocessor to handle the internal functions of the drive"
  - A microprocessor on a single integrated circuit intended to operate as an embedded system. As well as a CPU, a **microcontroller** typically includes small amounts of RAM and PROM and timers and I/O ports (single chip computer)

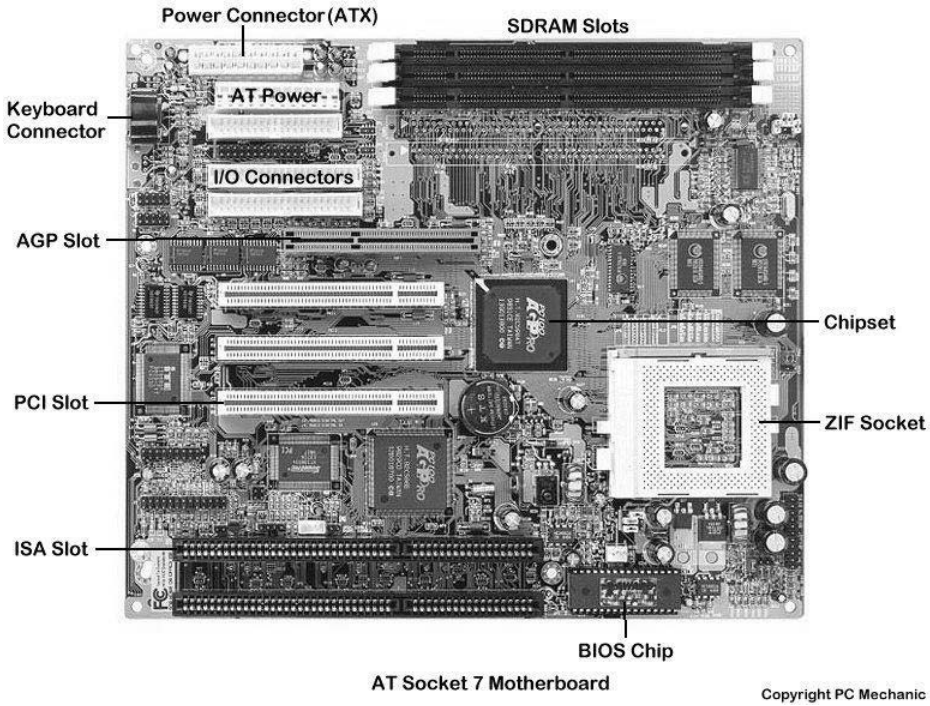
From Diode to Micro Computer System (Cont.)

- Micro processor ⇨ Micro computer system



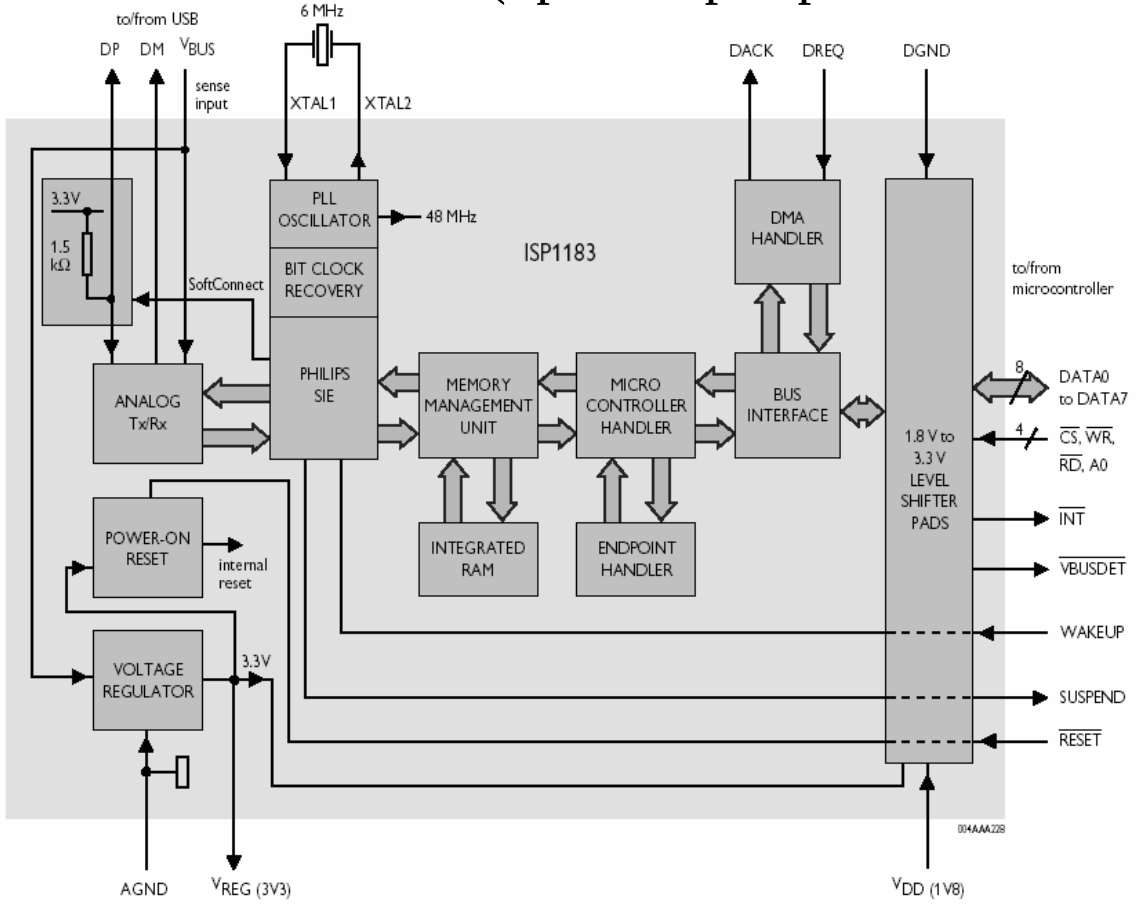
From Diode to Micro Computer System (Cont.)

- Micro processor ⇨ Micro computer system (Cont.)



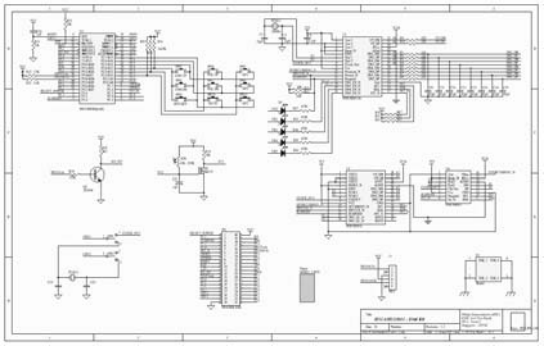
From Diode to Micro Computer System (Cont.)

- USB controller (special purpose micro controller)



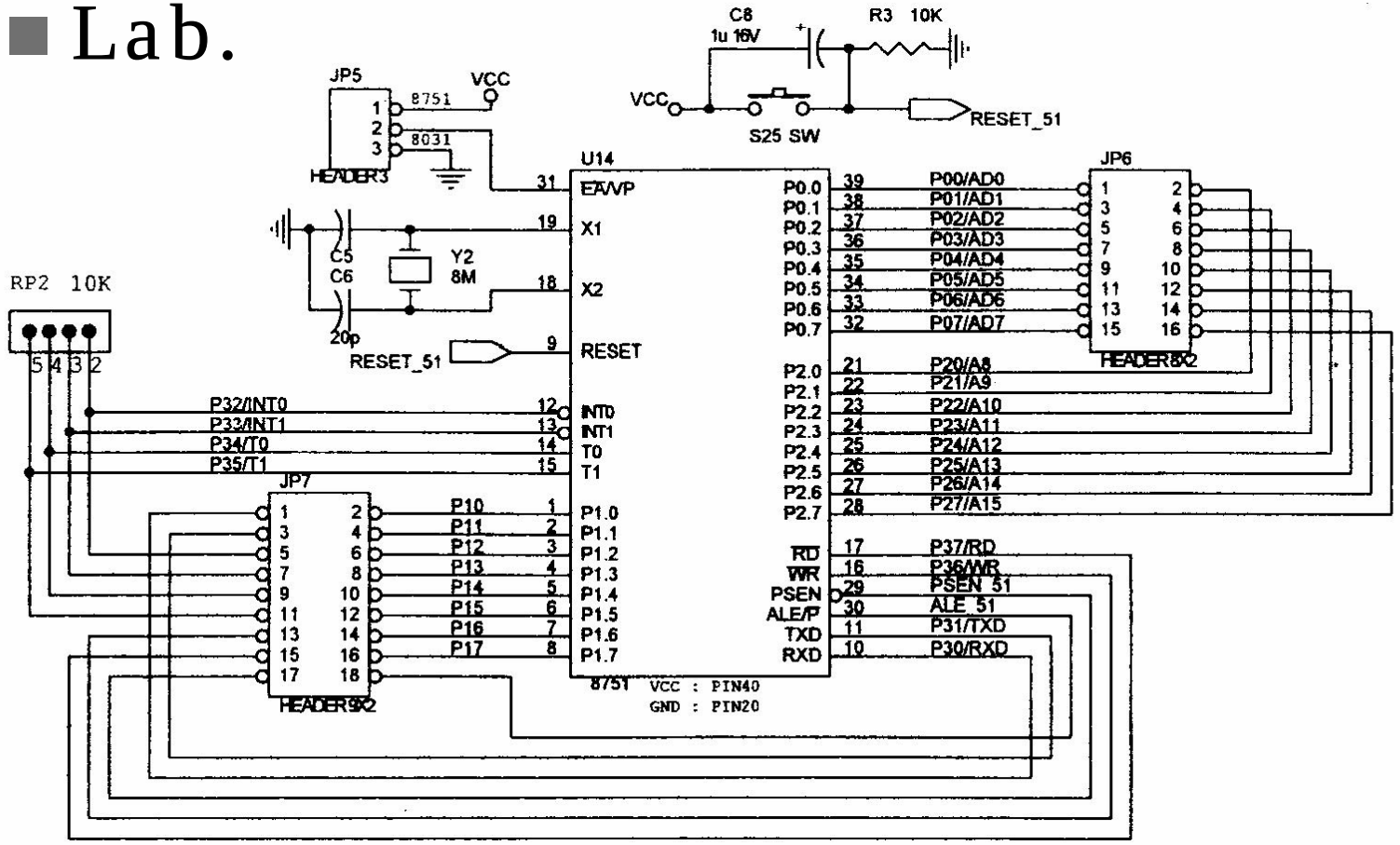
From Diode to Micro Computer System (Cont.)

- Microcontroller
  - Data sheet of the chip
  - Evaluation board and layout
  - Source code of the driver



Micro Computer System Basics (Cont.)

- Lab.

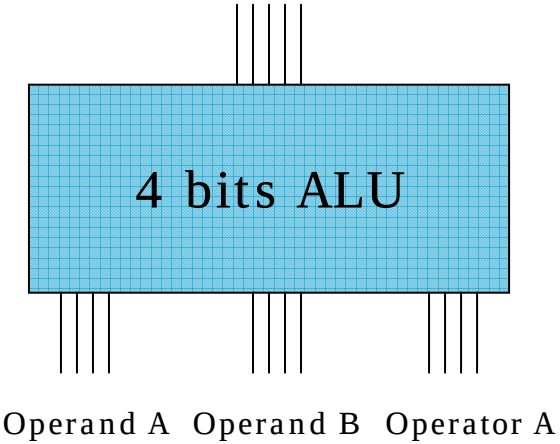


Review

- Diode (on-off circuit)
- Transistor (gate circuit)
- Logic gate
- Combination logic
- ALU
- Memory (Flip-flop)
- CPU(processor) (micro, mini, super)
  - Pentium
- Computer (micro, mini, super)
  - PC
- Single chip computer (controller)
  - 8051

8051 introduction

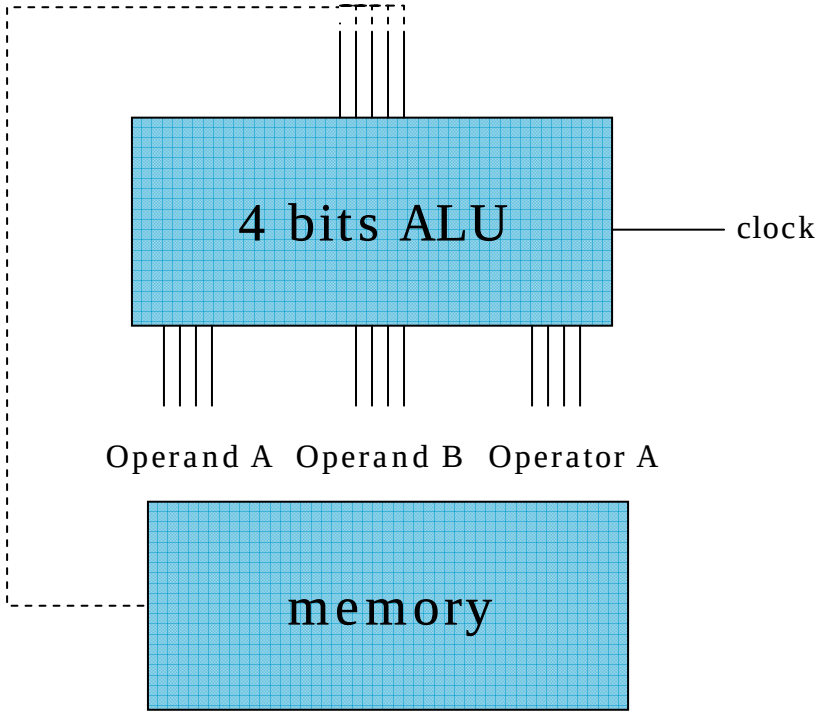
- Let's review computer architecture first
  - 4 bits ALU



OP code	
0000	+
0001	-
0010	X
0011	/
0100	DCL
0101	MOV

8051 introduction (Cont.)

- With memory



8051 introduction (Cont.)

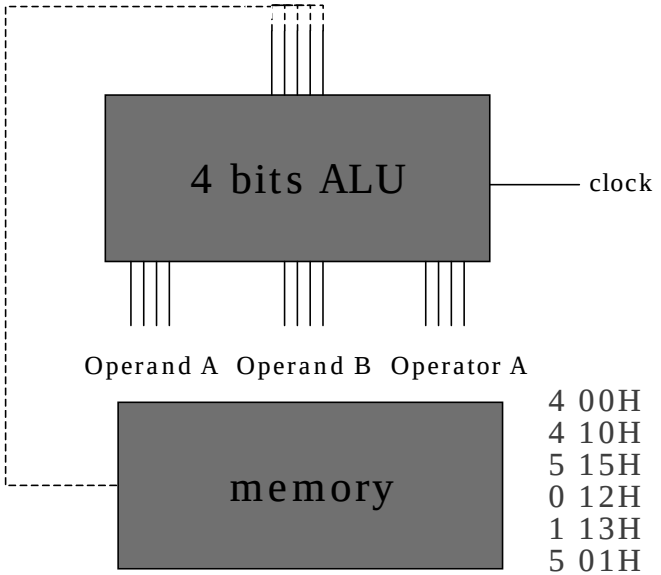
- Clock rate
  - The fundamental rate in cycles per second at which a computer performs its most basic operations such as adding two numbers or transferring a value from one register to another
- Machine cycle
  - The four steps which the CPU carries out for each machine language instruction: fetch, decode, execute, and store. These steps are performed by the control unit, and may be fixed in the logic of the CPU or may be programmed as microcode which is itself usually fixed (in ROM) but may be (partially) modifiable (stored in RAM)

8051 introduction (Cont.)

- A=5+2-3; (C language)

DCL A
DCL B
MOV B 5
ADD B 2
SUB B 3
MOV A B (assemble language)

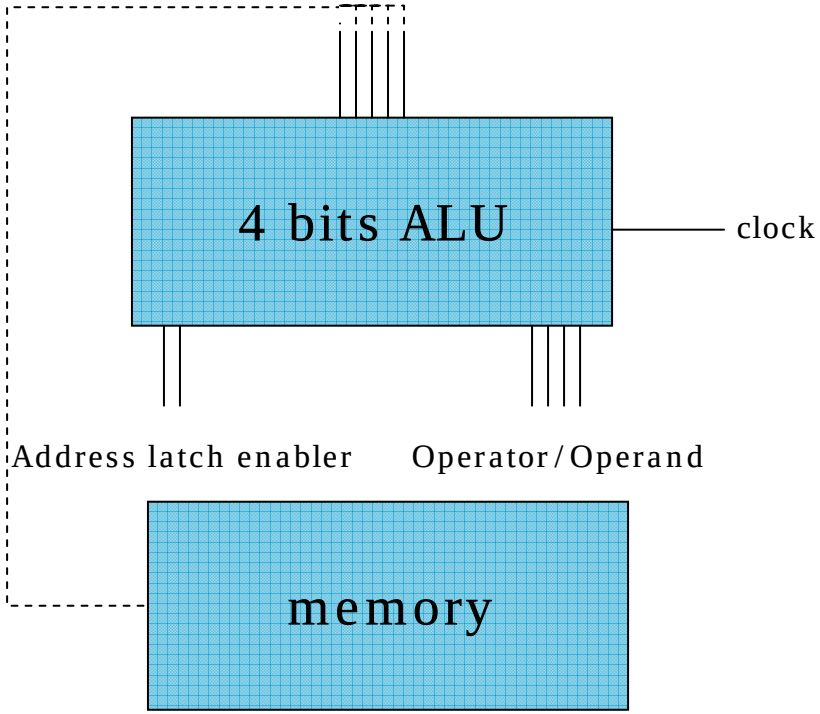
4 00H
4 10H
5 15H
0 12H
1 13H
5 01H (machine code)



8051 introduction (Cont.)

- Machine cycle
  - One machine cycle
  - fetch, decode, execute, and store
  - To improve the efficiency of instruction execution (pipeline)
- Reduce the number of pins
  - Multiplexer

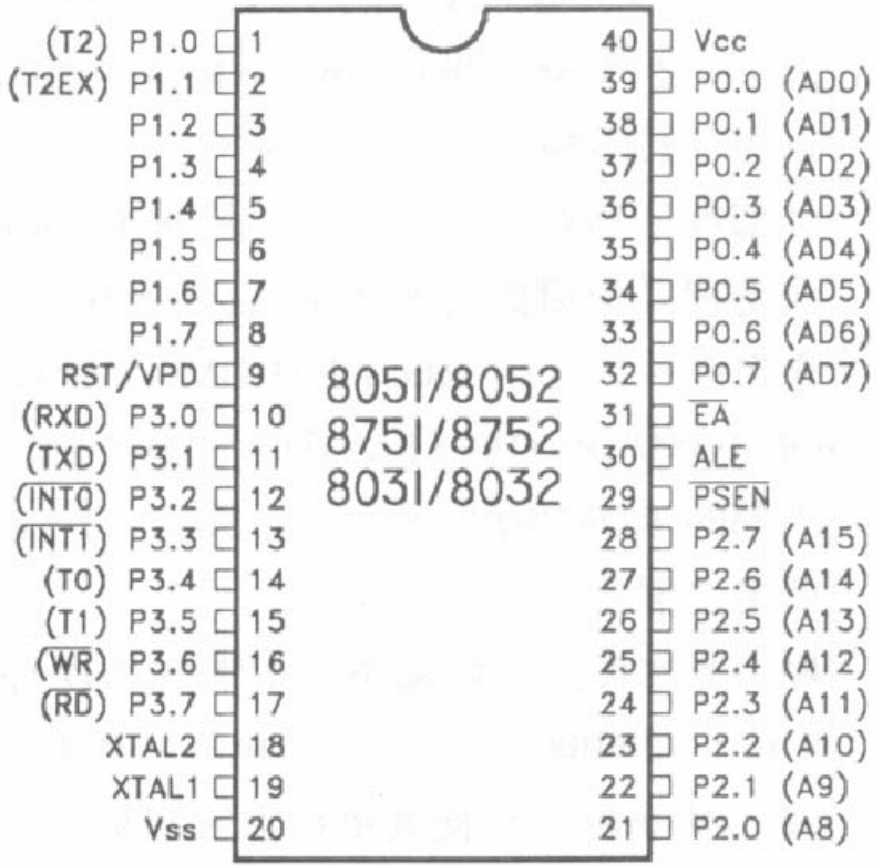
8051 introduction (Cont.)



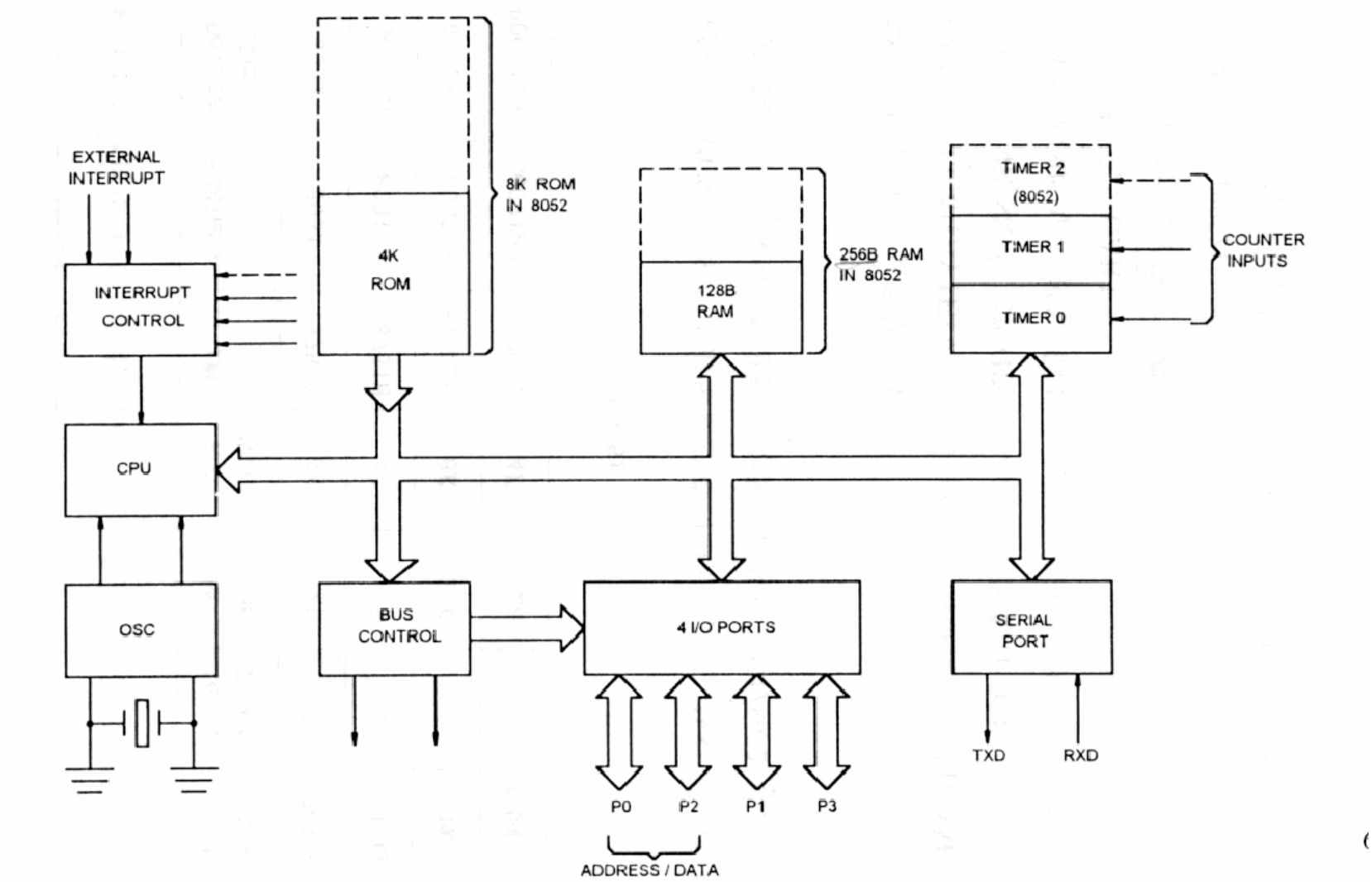
8051 introduction (Cont.)

- What else of CPU functions (pins) ?
  - IO control pins
    - Interrupt
    - Timer
    - Counter
    - …
  - Memory control pins
    - Selector
    - …
  - Power control pins
    - …
  - …

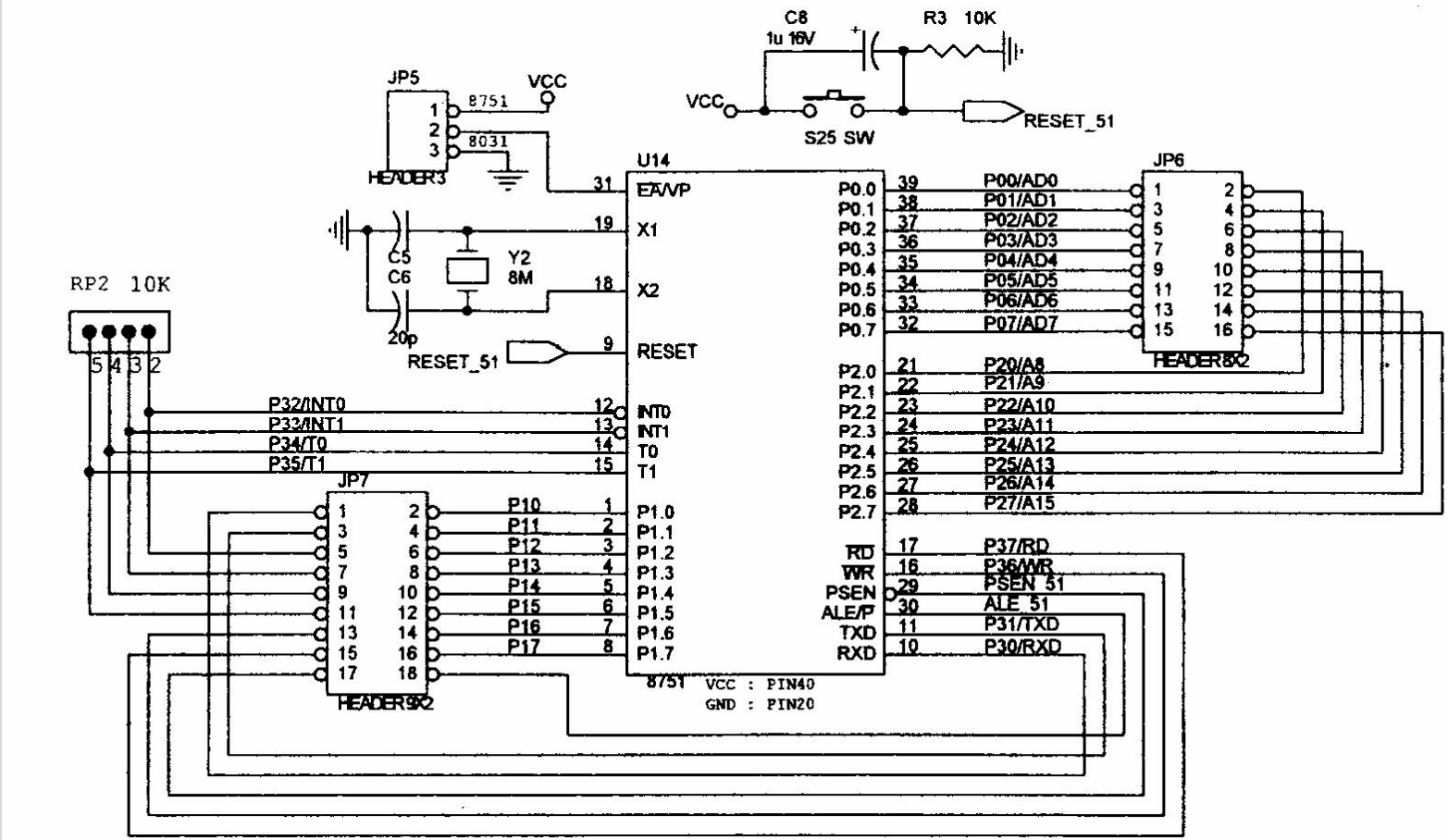
8051 introduction (Cont.)



8051 introduction (Cont.)



8051 introduction (Cont.)



8051 introduction (Cont.)

Pin Name	Description
Vcc (40)	Supply voltage
Vss (20)	Circuit ground
XTAL1 (19)	Input to the inverting oscillator (3.58MHz, 6MHz, 11.059MHz, 12MHz) amplifier.
XTAL2 (18)	Output from the inverting oscillator amplifier
RST (9)	Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.
EA/Vpp (31)	1. EA=low, access external program memory 2. EA=high, access internal program memory 3. This pin also receives the programming supply voltage (Vpp) during programming of the EPROM parts.

8051 introduction (Cont.)

Pin Name	Description
/PSEN (29)	1. Program Store Enable is the read strobe to external program memory. 2. /PSEN is activated twice each machine cycle when the 8051 is executing code from external memory, except that two /PSEN activations are skipped during each access to external data memory
ALE/PROG (30)	1. Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. 2. This pin is also the program pulse input during programming of the EPROM parts.
Port 0 P0.0~P0.7 (32~39)	1. Port 0 is an 8-bit open drain bi-directional I/O port. 2. As an output port each pin can sink 8 LS TTL inputs. 3. Having 1's written makes P0 float, and in that state P0 can be used as high-impedance inputs. 4. Multiplexed low-order address and data bus during accesses to the external program and data memory. 5. Port 0 receives the code bytes during programming of EPROM parts.

8051 introduction (Cont.)

Pin Name	Description
Port 2 P2.0~P2.7 (21~28)	1. Port 2 is an 8-bit bi-directional I/O port with internal pullups. 2. Port 2 output buffers can sink/source 4 LS TTL inputs. 3. Having 1's written makes Port 2 pulled high by the internal pullups, and in that state Port 2 can be used as inputs. 4. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). 5. Port 2 receives the high-order address bits during programming of the EPROM parts.

8051 introduction (Cont.)

Pin Name	Description
Port 3 P3.0~P3.7 (10~17)	1.Port 3 is an 8-bit bi-directional I/O port with internal pullups. 2.Port 3 output buffers can sink/source 4 LS TTL inputs. 3.Having 1's written makes Port 3 pulled high by the internal pullups, and in that state Port 3 can be used as inputs. 4.Port 3 serves the functions of various special features: a. P3.0: RXD (serial input port) b. P3.1: TXD (serial output port) c. P3.2: /INT0 (external interrupt 0) d. P3.3: /INT1 (external interrupt 1) e. P3.4: T0 (Timer 0 external input) f. P3.5: T1 (Timer 1 external input) g. P3.6: /WR (external data memory write strobe) h. P3.7: /RD (external data memory read strobe)