Cat Recognizer

Digital Design and Logical Synthesis
(361113611)
Course Project

Design Synthesis

Version 0.1

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Revision History

Rev	Change Description	Done By	Date
0.1	Initial document	Maor Assayag Refael Shetrit	22, Dec, 2018
0.2	Timing		27,Dec,2018
0.3	Gate-level		04,Jan,2019

Contents

1. Introduction

In the third part we will be required to perform a synthesis, analyze its result and perform a gate level simulation.
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2. Design Constraints

2.1. Constraints analysis

Our system is a part of a larger design and has the following constraints:

Constraint type	Description
Clock period	At least 30Mhz
Clock Max External Latency	0.2 ns
Clock Max Internal Latency	0.1
Clock uncertainty	0.6 ns
Clock transition time	0.7 ns
input delay	2.5 ns
output delay	1 ns
design area	Smallest
driving cell	Smallest not gate
output load	load of biggest DFF
Input transition	0.1
wire load model	tsmc18_wl50

table 1 general Timing Constraints.

False Path			
From Pin/Port	Through Pin	To Pin/Port	Comments

Clock Definitions		
Constraint Name	System clock	Comment
Period [Pico Seconds]	30,000	Pico seconds
Rising edge [Pico Seconds]	0	Pico seconds
Falling edge [Pico Seconds]	15,000	Pico seconds
Pin/Port name	CatRecognizr : clk	
Uncertainty	0.6	Nano seconds
Transition	0.7	Nano seconds
Constraint Name	Stimulus clock	Comment
Period [Pico Seconds]	60,000	Pico seconds
Rising edge [Pico Seconds]	0	Pico seconds
Falling edge [Pico Seconds]	30,000	Pico seconds
Pin/Port name	CatRecognizr : PENABLE	
Uncertainty	0.6	Nano seconds
Transition	0.7	Nano seconds

External Delay [Pico Seconds]		
Pin name	Value	Comment
PWDATA	0.2845	
clk	0.2845	

Load [Femto Farads]		
Pin name		
CatRecOut		

External Driver			
Pin name	Standard Cell Name	Cell Port name	Comment

	External Driver [standard cell name and port name]		

Multi-cycle Path			
From Pin/Port	Through Pin	To Pin/Port	Comments

table 2 Timing Constraints by pin names.

2.2. Implementation

Implement the above constraints on your design and perform an initial synthesis.

3. Design summary

Fill in cell internal power (gated clock+saif), cell internal power (without gated clock and without saif), Net Switching Power (gated clock+saif), Net Switching Power (without gated clock and without saif), total dynamic power (gated clock+saif), total dynamic power (without gated clock and without saif), Number of cells, Number of nets, Combinational area, Noncombinational area, maximum clock frequency, minimum clock cycle time in google docs at

https://docs.google.com/spreadsheets/d/1EsKUIfpHP0Jb4PmuaiM6lRvuo_H6tkhq3hAQu19Hdi0/edit?usp=sharing

Analyze the results you got from the synthesis and explain their connection to the strategy you were given.

3.1. Design Area, Number of Cells and Number of Nets

Show the **design area report**, suggest **how you could save more area** if you had more time to do your project.

```
****************************************
Report : area
Design : CatRecognizer
Version: J-2014.09-SP2
Date   : Mon Dec 31 13:12:08 2018
****************************************

Library(s) Used:

    slow (File: /users/agnon/year2016/maoryak/lab3/LibraryFiles/db/slow.db)

Number of ports:                        67
Number of nets:                        845
Number of cells:                       491
Number of combinational cells:         221
Number of sequential cells:            254
Number of macros/black boxes:            0
Number of buf/inv:                     124
Number of references:                   70

Combinational area:         4014376.029803
Buf/Inv area:             214915.384479
Noncombinational area:      9004701.336320
Macro/Black Box area:          0.000000
Net Interconnect area:    180528427.545090

Total cell area:          13019077.366123
Total area:             193547504.911212
```

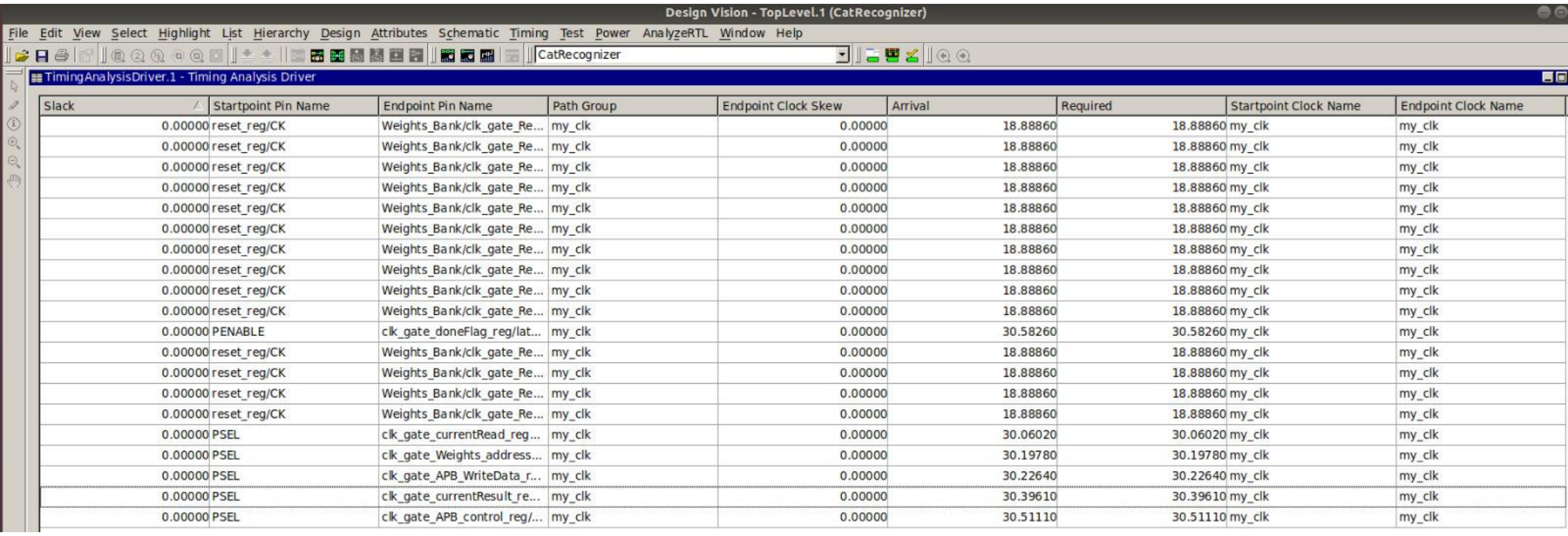
We design the system with the mind of save space. In the pixel register file, we stored 3 lines of pixel data (24bit) in 1 register and got 4096 registers instead of 12,288. In the computing module we decided to compute 1 register at a time (hence 3 neurons that compute weight * pixel 8bit), instead of computing all the register at once and generate 4096 multipliers. In conclusion, we put a lot of work t make this design space efficient as possible. If we had more time, we would look into maybe combining the weights register file and the pixel register file, although it will only save some logic and not actual registers (or bytes) needed.

3.2. Timing analysis

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : CatRecognizer
Version: J-2014.09-SP2
Date   : Mon Dec 31 13:12:08 2018
****************************************
# A fanout number of 1000 was used for high fanout net computations.
Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: rst (input port clocked by my_clk)
  Endpoint: clk_gate_APB_control_reg/latch
            (negative level-sensitive latch clocked by my_clk)
  Path Group: my_clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  CatRecognizer      tsmc18_wl50           slow

  Point                                   Incr       Path
  ---------------------------------------------------------------------------
  clock my_clk (rise edge)                0.00       0.00
  clock network delay (ideal)             1.00       1.00
  input external delay                   27.45      28.45 r
  rst (in)                                0.00      28.45 r
  U302/Y (CLKINVX3)                       1.08      29.53 f
  U297/Y (OAI21X4)                        0.64      30.17 r
  U280/Y (OR2X4)                          0.31      30.48 r
  clk_gate_APB_control_reg/EN (SNPS_CLOCK_GATE_HIGH_CatRecognizer_6)
                                          0.00      30.48 r
  clk_gate_APB_control_reg/latch/D (TLATNX4)
                                          0.00      30.48 r
  data arrival time                                 30.48

  clock my_clk (fall edge)               15.00      15.00
  clock network delay (ideal)             1.00      16.00
  clock uncertainty                      -0.15      15.85
  clk_gate_APB_control_reg/latch/GN (TLATNX4)
                                          0.00      15.85 f
  time borrowed from endpoint            14.63      30.48
  data required time                                30.48
  ---------------------------------------------------------------------------
```

```
data required time                              30.48
data arrival time                              -30.48
--------------------------------------------------------------------------
slack (MET)                                      0.00

Time Borrowing Information
--------------------------------------------------------------
my_clk nominal pulse width                       15.00
library setup time                          -0.10
--------------------------------------------------------------
max time borrow                              14.90
--------------------------------------------------------------
actual time borrow                           14.63
clock uncertainty                           -0.15
--------------------------------------------------------------
time given to startpoint                     14.48
--------------------------------------------------------------
```

Figure 3.2.1 – Timing report



Slack	Startpoint Pin Name	Endpoint Pin Name	Path Group	Endpoint Clock Skew	Arrival	Required	Startpoint Clock Name	Endpoint Clock Name
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	PENABLE	clk_gate_doneFlag_reg/lat...	my_clk	0.00000	30.58260	30.58260	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	reset_reg/CK	Weights_Bank/clk_gate_Re...	my_clk	0.00000	18.88860	18.88860	my_clk	my_clk
0.00000	PSEL	clk_gate_currentRead_reg...	my_clk	0.00000	30.06020	30.06020	my_clk	my_clk
0.00000	PSEL	clk_gate_Weights_address...	my_clk	0.00000	30.19780	30.19780	my_clk	my_clk
0.00000	PSEL	clk_gate_APB_WriteData_r...	my_clk	0.00000	30.22640	30.22640	my_clk	my_clk
0.00000	PSEL	clk_gate_currentResult_re...	my_clk	0.00000	30.39610	30.39610	my_clk	my_clk
0.00000	PSEL	clk_gate_APB_control_reg/...	my_clk	0.00000	30.51110	30.51110	my_clk	my_clk

Figure 3.2.2 – Timing Analysis Driver

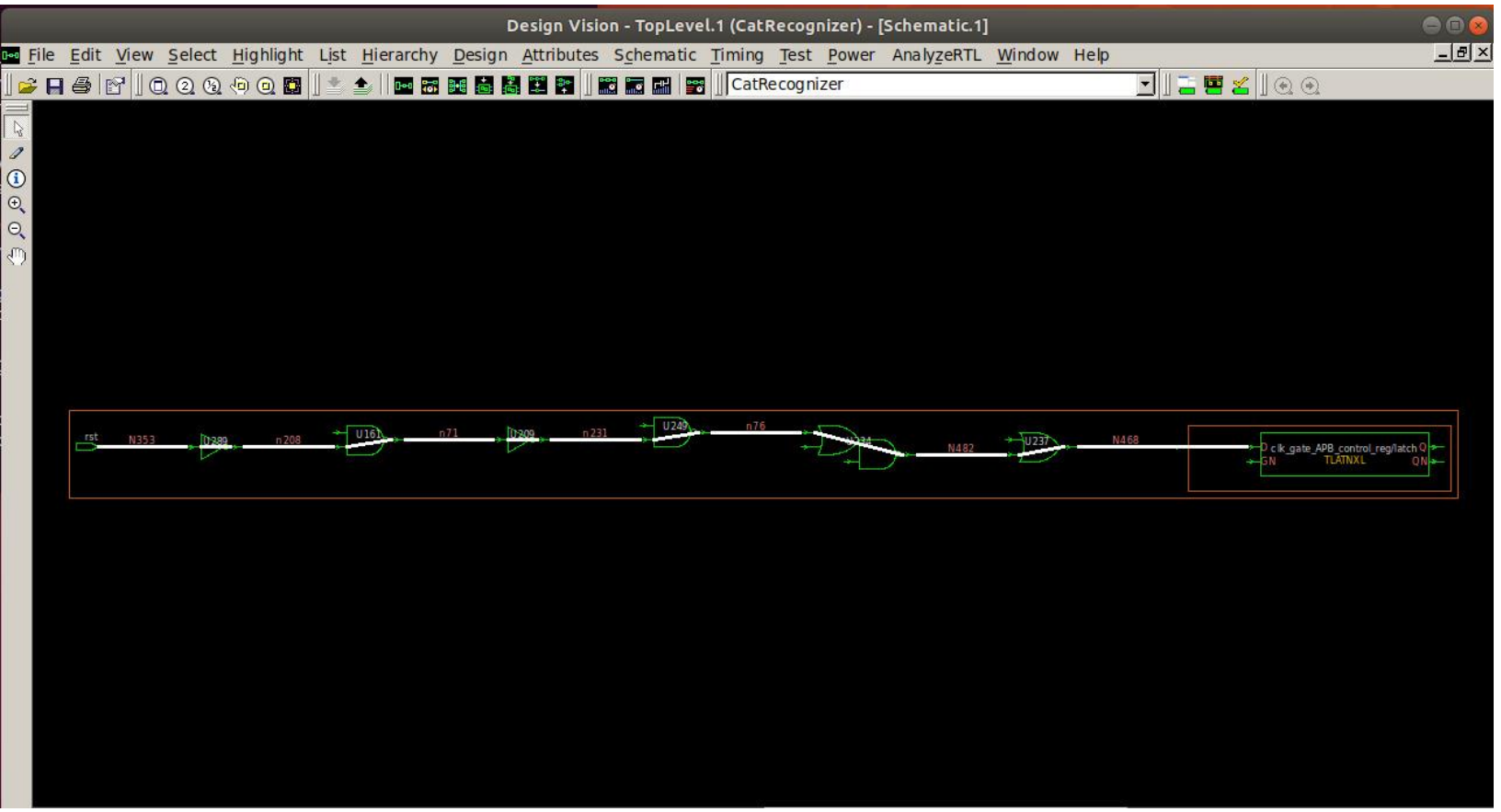


Figure 3.2.3 – Critical path

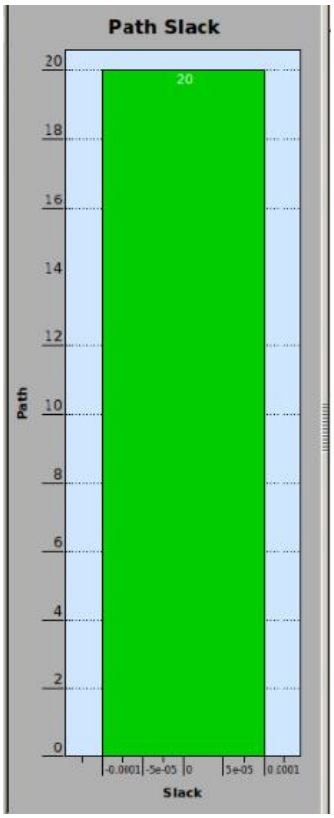


Figure 3.2.3 – Path Slack

3.3. Power refinement

3.3.1. Power report without the SAIF input file and without gated clock

```
****************************************
Report : power
        -analysis_effort low
Design : CatRecognizer
Version: J-2014.09-SP2
Date   : Mon Dec 31 14:50:46 2018
****************************************
Library(s) Used:
    slow (File: /users/agnon/year2016/maoryak/lab3/LibraryFiles/db/slow.db)

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design        Wire Load Model           Library
------------------------------------------------
CatRecognizer          tsmc18_wl50       slow

Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 302.3504 mW   (89%)
  Net Switching Power  =  37.0312 mW   (11%)
                         ---------
Total Dynamic Power    = 339.3816 mW  (100%)

Cell Leakage Power     = 534.9120 uW

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad           0.0000           0.0000            0.0000           0.0000  (   0.00%)
memory           0.0000           0.0000            0.0000           0.0000  (   0.00%)
black_box        0.0000           0.0000            0.0000           0.0000  (   0.00%)
clock_network    0.0000           0.0000            0.0000           0.0000  (   0.00%)
register         301.6539         5.3222e-02        2.9409e+08       301.9720  (  88.89%)
sequential       0.0000           0.0000            0.0000           0.0000  (   0.00%)
combinational    0.5031           36.9891           2.4083e+08       37.7275  (  11.11%)
--------------------------------------------------------------------------------------------------
Total            302.1569 mW      37.0424 mW        5.3491e+08 pW    339.6995 mW
1
```

3.3.2. Power report with the SAIF input file and without gated clock

```
****************************************
Report : power
        -analysis_effort low
Design : CatRecognizer
Version: J-2014.09-SP2
Date   : Tue Jan  1 20:48:40 2019
****************************************
Library(s) Used:
   slow (File: /users/agnon/year2016/maoryak/lab3/LibraryFiles/db/slow.db)

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design       Wire Load Model          Library
------------------------------------------------
CatRecognizer         tsmc18_wl50       slow

Global Operating Voltage = 1.62
Power-specific unit information :
   Voltage Units = 1V
   Capacitance Units = 1.000000pf
   Time Units = 1ns
   Dynamic Power Units = 1mW    (derived from V,C,T units)
   Leakage Power Units = 1pW
  Cell Internal Power  =   2.2605  W   (97%)
  Net Switching Power  =  64.0888 mW    (3%)
                  ---------
Total Dynamic Power    =   2.3246  W  (100%)

Cell Leakage Power     = 534.9120 uW

               Internal         Switching          Leakage            Total
Power Group      Power            Power             Power             Power   (   %    )  Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000           0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000           0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000           0.0000           0.0000  (   0.00%)
clock_network      0.0000           0.0000           0.0000           0.0000  (   0.00%)
register       2.2571e+03       6.0774e-02       2.9409e+08       2.2575e+03  (  97.18%)
sequential         0.0000           0.0000           0.0000           0.0000  (   0.00%)
combinational      1.2054           64.0274       2.4083e+08           65.4377  (   2.82%)
---------------------------------------------------------------------------------------------------
Total          2.2583e+03 mW        64.0881 mW     5.3491e+08 pW     2.3229e+03 mW
1
```

3.3.3. Power report without the SAIF input file and with gated clock

```
****************************************
Report : power
        -analysis_effort low
Design : CatRecognizer
Version: J-2014.09-SP2
Date   : Mon Dec 31 18:20:37 2018
****************************************
Library(s) Used:
   slow (File: /users/agnon/year2016/maoryak/lab3/LibraryFiles/db/slow.db)

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design       Wire Load Model          Library
------------------------------------------------
CatRecognizer         tsmc18_wl50       slow

Global Operating Voltage = 1.62
Power-specific unit information :
   Voltage Units = 1V
   Capacitance Units = 1.000000pf
   Time Units = 1ns
   Dynamic Power Units = 1mW    (derived from V,C,T units)
   Leakage Power Units = 1pW
  Cell Internal Power  =  85.5021 mW   (31%)
  Net Switching Power  = 192.3105 mW   (69%)
                       ---------
Total Dynamic Power    = 277.8125 mW  (100%)

Cell Leakage Power     = 365.0787 uW

                Internal         Switching           Leakage            Total
Power Group     Power            Power               Power              Power   (  %    ) Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000           0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000           0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000           0.0000           0.0000  (   0.00%)
clock_network     16.6708          181.5567        2.1429e+07          198.2604  (  71.26%)
register          68.5826        3.3345e-02        2.9021e+08          68.8996  (  24.76%)
sequential         0.0000           0.0000           0.0000           0.0000  (   0.00%)
combinational      0.2855          10.7244        5.3443e+07          11.0652  (   3.98%)
---------------------------------------------------------------------------------------------------
Total            85.5389 mW       192.3145 mW      3.6508e+08 pW       278.2253 mW
1
```

3.3.4. Power report with the SAIF input file and with gated clock

```
****************************************
Report : power
        -analysis_effort low
Design : CatRecognizer
Version: J-2014.09-SP2
Date   : Tue Jan  1 22:50:29 2019
****************************************
Library(s) Used:
   slow (File: /users/agnon/year2016/maoryak/lab3/LibraryFiles/db/slow.db)

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design       Wire Load Model          Library
------------------------------------------------
CatRecognizer         tsmc18_wl50       slow

Global Operating Voltage = 1.62
Power-specific unit information :
   Voltage Units = 1V
   Capacitance Units = 1.000000pf
   Time Units = 1ns
   Dynamic Power Units = 1mW    (derived from V,C,T units)
   Leakage Power Units = 1pW
  Cell Internal Power  =  79.2246 mW   (97%)
  Net Switching Power  =   2.1151 mW    (3%)
                         ---------
Total Dynamic Power    =  81.3397 mW  (100%)

Cell Leakage Power     = 365.0787 uW

                Internal         Switching           Leakage            Total
Power Group      Power           Power               Power              Power   (   %    ) Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000           0.0000           0.0000  (   0.00%)
memory             0.0000           0.0000           0.0000           0.0000  (   0.00%)
black_box          0.0000           0.0000           0.0000           0.0000  (   0.00%)
clock_network     78.1620           0.6510        2.1429e+07          78.8523  (  96.50%)
register           0.7103        8.0289e-03        2.9021e+08           1.0085  (   1.23%)
sequential         0.0000           0.0000           0.0000           0.0000  (   0.00%)
combinational      0.3387           1.4560        5.3443e+07           1.8484  (   2.26%)
---------------------------------------------------------------------------------------------------
Total            79.2110 mW        2.1150 mW     3.6508e+08 pW        81.7092 mW
1
```

We can see that the gating the clock improve the register power group timing significantly, hence improve the overall timing. In the other hand, we can see that the dynamic power is larger when we used gating on the clock, as shown in class.

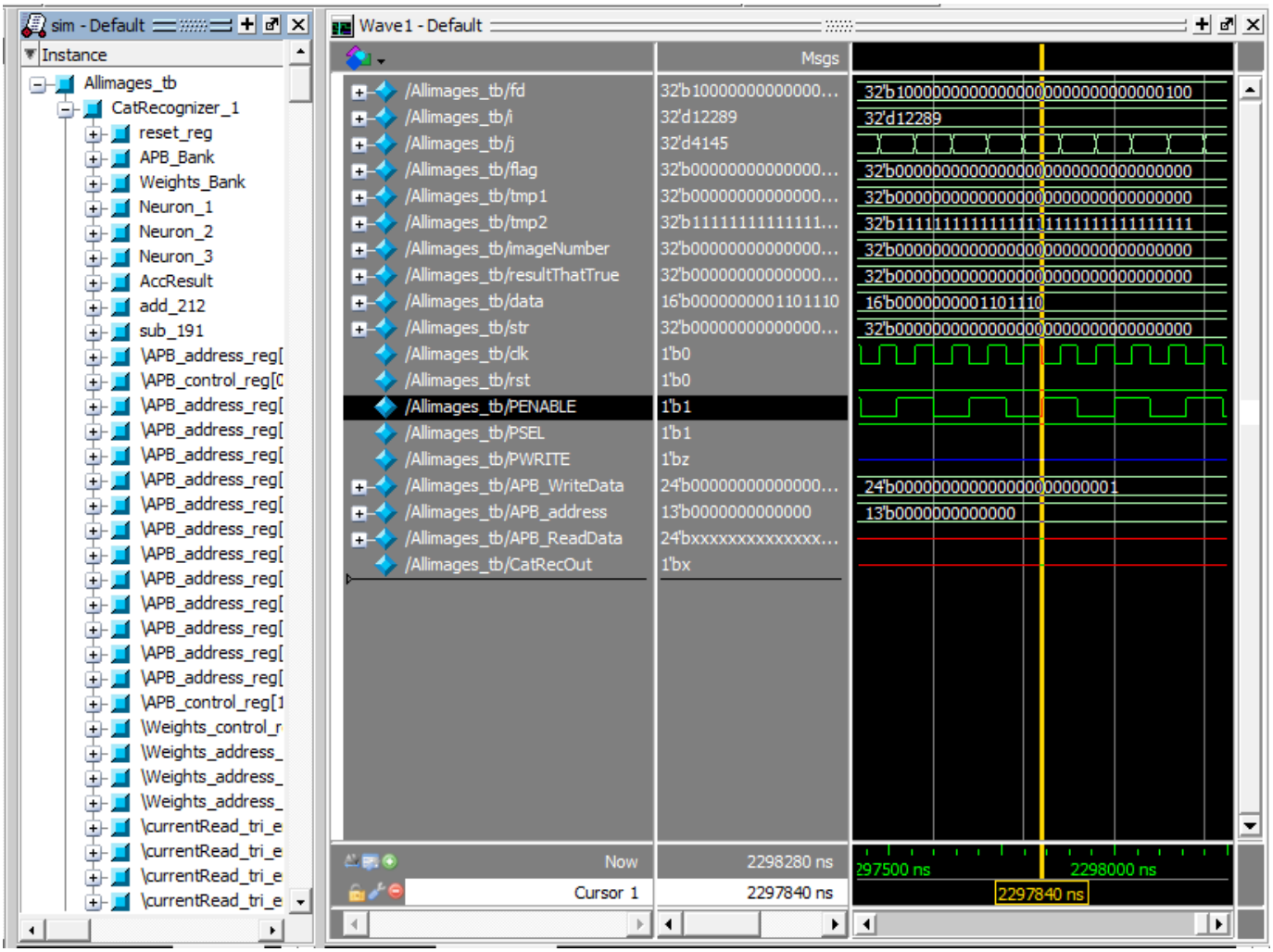
4. Gate level simulation

4.1. Input to simulator

Input the synthesis output file – verilog and SDF into the verification simulation from part 2 (black box approach).

What kind of errors you got in the initial run (before you fixed them)?

1. Accumulator – the synthesis didn't like that we used the same reg for accumulator, so we design another module to take care of the accumulation instead of being inside CatRecognizer Gate-level.
2. Timing – in the basic test bench we updated the clock to 30MHZ, for the gate level test.
3. SDF is not complete – due to memory override on the servers, we need to run a couple of times the script run.tcl to produce a proper sdf file.
4. Passing parameters – the synthesis didn't like that we passed parameters to the Register file module. The fix for this is changing the design to get the parameters from the global file Parameters.v as we did in PART 2 – verification.



If we had more time, we would keep testing the gate level and figure out why it doesn't produce a result (1 or 0). The compile seem alright and the test bench start regulary.