Characterization of a Novel Nine-Transistor SRAM Cell

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Characterization of a Novel Nine-Transistor SRAM Cell

Zhiyu Liu and Volkan Kursun

***Abstract*—Data stability of SRAM cells has become an important issue with the scaling of CMOS technology. Memory banks are also important sources of leakage since the majority of transistors are utilized for on-chip caches in today's high performance microprocessors. A new nine-transistor (9T) SRAM cell is proposed in this paper for simultaneously reducing leakage power and enhancing data stability. The proposed 9T SRAM cell completely isolates the data from the bit lines during a read operation. The read static-noise-margin of the proposed circuit is thereby enhanced by 2× as compared to a conventional six-transistor (6T) SRAM cell. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption by 22.9% as compared to the standard 6T SRAM cells in a 65-nm CMOS technology. The leakage power reduction and read stability enhancement provided with the new circuit technique are also verified under process parameter variations.**

***Index Terms*—Cache memory, data stability, leakage power, process variations, static noise margin, super cutoff sleep mode.**

I. Introduction

In modern high performance integrated circuits, more than 40% of the total active mode energy is consumed due to leakage currents [2], [3]. Furthermore, leakage is the only source of energy consumption in an idle circuit. SRAM arrays are important sources of leakage since the majority of transistors are utilized for on-chip memory in today's high performance microprocessors and systems-on-chips (SoCs). The design of a low leakage SRAM cell is, therefore, highly desirable.

In addition to the leakage power issues, the degradation of data stability in SRAM cells is another growing concern with the scaling of device dimensions and voltages in each new technology generation. The SRAM cell stability is further degraded due to process variations in deeply scaled CMOS technologies.

A new nine-transistor (9T) SRAM cell with reduced leakage power consumption and enhanced data stability is proposed in this paper. The leakage power consumption of the new SRAM cell is reduced by 22.9% as compared to the conventional six-transistor (6T) SRAM cells. The 9T SRAM cell provides two separate data access mechanisms for the read and write operations. During a read operation, the data storage nodes are completely isolated from the bit lines. The read static-noise-margin (SNM) of the proposed 9T SRAM cell is thereby enhanced by 2× as compared to the standard 6T SRAM cells.

This paper is organized as follows. The new 9T SRAM cell is presented in Section II. Circuit area, data stability, and leakage power of the 6T and 9T SRAM cells are compared for the nominal set of circuit and technology parameters in Section III. The new memory circuit is characterized under process parameter variations in Section IV. Finally, some conclusions are offered in Section V.

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The authors are with the Department of Electrical and Computer Engineering, University of Wisconsin—Madison, Madison, WI 53706-1691 USA (e-mail: zhiyuliu@wisc.edu).

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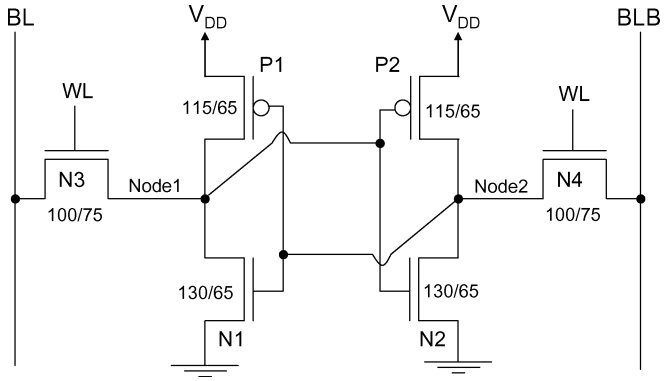

Fig. 1. Standard 6T SRAM cell in a 65-nm CMOS technology.

II. SRAM Cells

The operation and design of the conventional 6T and the new 9T SRAM circuits are presented in this section. The standard 6T SRAM cell is discussed in Section II-A. The new 9T SRAM cell is introduced in Section II-B.

A. Conventional 6T SRAM Cell

A typical 6T SRAM cell in a 65-nm CMOS technology is shown in Fig. 1 [1]. In a conventional 6T SRAM cell, the stored data is disturbed due to the voltage division between the cross-coupled inverters and the access transistors during a read operation. The data is most vulnerable to external noise during this intrinsic disturbance produced by the direct-data-read-access mechanism of a standard 6T SRAM cell.

There are strict constraints on the sizing of transistors to be able to maintain the data stability and functionality of a standard 6T SRAM cell, as shown in Fig. 1. In order to maintain the read stability, the current produced by N1 and N2 must be higher as compared to the access transistors N3 and N4. Alternatively, for write ability, the current conducting capability of N3 and N4 must be stronger as compared to P1 and P2. For read stability, write ability, and sufficient feedback pull-up strength, typically none of the devices in a standard SRAM cell are sized minimum ($W \neq W_{\min} = 65$ nm), as illustrated in Fig. 1.

B. 9T SRAM Cell

A novel 9T SRAM cell with enhanced data stability and reduced leakage power consumption is presented in this section. The schematic of the new 9T SRAM cell, with transistors sized for a 65-nm CMOS technology, is shown in Fig. 2. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized devices (composed of N1, N2, N3, N4, P1, and P2 with $W = W_{\min}$ and $L = L_{\min}$). The two write access transistors (N3 and N4) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD).

During a write operation, WR signal transitions high while RD is maintained low, as shown in Fig. 2(a). N7 is cutoff. The two write access transistors N3 and N4 are turned on. In order to write a "0" to Node1, BL and BLB are discharged and charged, respectively. A "0"

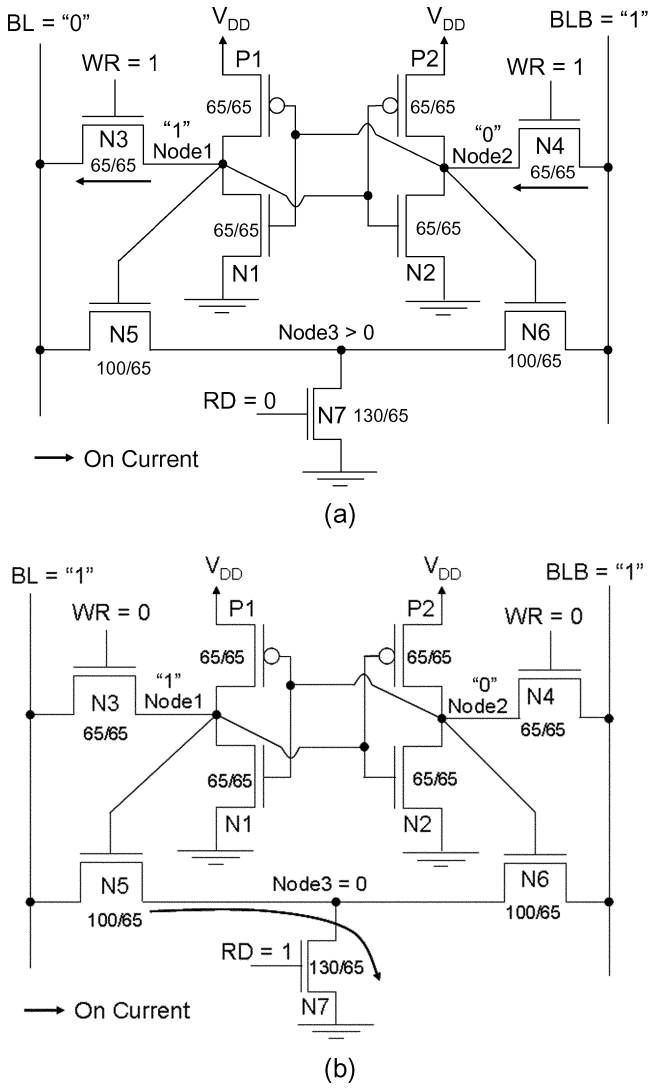

Fig. 2. 9T SRAM cell in the active mode. (a) The 9T SRAM cell during a write operation. (b) The 9T SRAM cell during a read operation. The transistors are sized for a 65-nm CMOS technology.

is forced into the SRAM cell through N3. Alternatively, for writing a "0" to Node2, BL and BLB are charged and discharged, respectively. A "0" is forced onto Node2 through N4.

During a read operation, RD signal transitions high while WR is maintained low, as illustrated in Fig. 2(b). The read access transistor N7 is activated. Provided that Node1 stores "1" [as assumed in Fig. 2(b)], BL is discharged through N5 and N7. Alternatively, provided that Node2 stores "1", the complementary bitline (BLB) is discharged through N6 and N7.

Since N3 and N4 are cutoff, the storage nodes Node1 and Node2 are completely isolated from the bitlines during a read operation. Unlike the 6T SRAM cell, the voltage of the node which stores "0" is strictly maintained at the ground level during a read operation with the proposed circuit technique. The read stability of the 9T SRAM cell is thereby enhanced as compared to a standard 6T SRAM cell.

III. Simulation Results

The read stability, leakage power, and area of the 6T and 9T SRAM cells for the nominal set of device and circuit parameters are compared in this section. 32 bit × 32 bit memory arrays are designed to operate

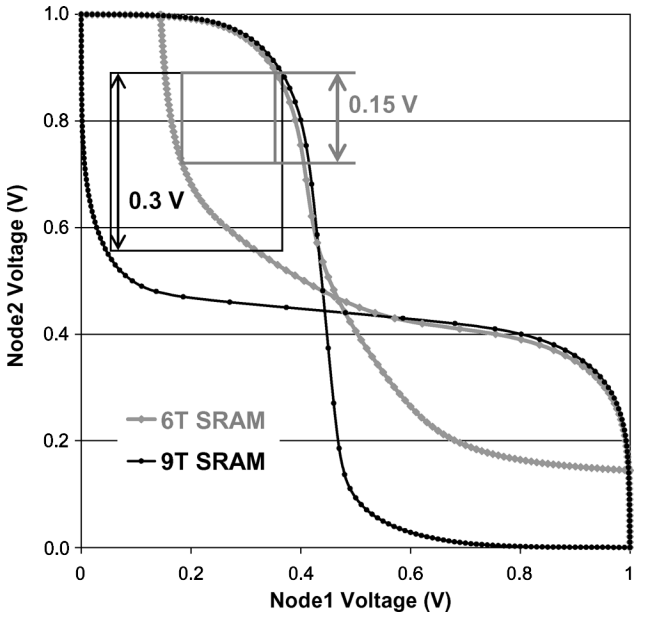

Fig. 3. Static voltage transfer characteristics and SNM of 6T and 9T SRAM cells during a read operation.

at a clock frequency of 2 GHz with the standard 6T and the proposed 9T SRAM cells. SRAM circuits are simulated in a 65-nm CMOS technology ($V_{\rm tn} = |V_{\rm tp}| = 0.22$ V and $V_{\rm DD} = 1$ V) [7]. The transistor sizing of the 6T and 9T SRAM cells is shown in Figs. 1 and 2, respectively. Data are measured at 70 °C.

A. Read Stability

Static noise margin (SNM) is the metric used in this paper to chdcaracterize the read stability of the SRAM cells. The SNM is defined as the minimum noise voltage necessary to flip the state of an SRAM cell [4]–[6]. The static voltage transfer characteristics of the 6T and 9T SRAM cells during a read operation are shown in Fig. 3. The read SNM is the side length of the maximum nested square between voltage transfer characteristics of the two data storage nodes during a read access, as shown in Fig. 3 [5].

As illustrated in Fig. 3, when Node1 of the 6T SRAM cell is at $V_{\rm DD}$, Node2 rises to a higher steady-state voltage of 146 mV due to the voltage division between the access transistor and the pull-down transistor in the inverter. Data is more vulnerable to external noise due to this intrinsic disturbance produced by the direct read-access mechanism of a conventional 6T SRAM cell. Alternatively, the data is completely isolated from the bit lines, thereby significantly enhancing the data stability during a read operation with the proposed technique. When Node1 of the 9T SRAM cell is at $V_{\rm DD}$, Node2 is maintained strictly at 0 V since the data storage nodes are decoupled from the bitlines. As illustrated in Fig. 3, the read SNM of the 9T SRAM cell is 2× higher as compared to the 6T SRAM cell.

B. Leakage Power Consumption

The proposed 9T SRAM cell also lowers the total leakage power. For the 6T and 9T SRAM cells in the standby mode, the access transistors are cutoff and the bitlines are charged to $V_{\rm DD}$. In a 9T SRAM cell, the transistors which produce the leakage current have either minimum width or smaller drain-to-source voltage ($V_{\rm DS}$) as compared to a conventional 6T cell. Therefore, if WL, WR, and RD signals are all maintained at zero volts in the standby mode, the leakage power consumed by the 9T SRAM cell is 7.7% lower as compared to the standard 6T SRAM cell.

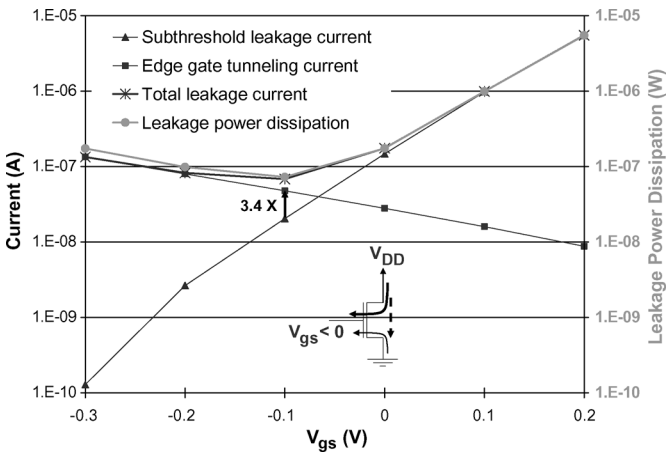

Fig. 4. Subthreshold and edge-tunneling gate-oxide leakage currents of a super cutoff nMOS transistor in a 65-nm CMOS technology. Transistor width $= 1\ \mu$m. Transistor length $= 65$ nm. $V_{\rm DD} = 1$ V.

In order to further suppress the leakage current when the memory circuits are idle, the super cutoff scheme [11] is also explored for the two memory arrays. The subthreshold leakage current is exponentially dependent on the gate-to-source voltage of a MOSFET [3]. Applying negative gate-to-source voltage $(V_{\rm GS})$ to an nMOS transistor suppresses the subthreshold leakage current. However, the negative $V_{\rm GS}$ also increases the gate tunneling current due to the higher gate-oxide voltage, as illustrated in Fig. 4. In the deeply scaled nanometer CMOS technologies with ultra-thin gate-oxide layers, the super cutoff scheme can increase the total leakage current produced by a MOSFET due to the enhanced tunneling of the carriers at negative $V_{\rm GS}$. As shown in Fig. 4, the edge tunneling gate-oxide leakage current of an nMOS transistor is 3.4× higher than the subthreshold leakage current for $V_{\rm GS} = -100$ mV. The increasing gate-oxide leakage starts to dominate the total leakage power dissipation for $V_{\rm GS} < -100$ mV, as shown in Fig. 4.

The super cutoff 6T and 9T SRAM cells are shown in Fig. 5. The access transistors N3 and N4 are not the widest transistors in a 6T SRAM cell. N3 and N4 also have longer channel length to reduce the bitline leakage. The majority of leakage power in a conventional 6T SRAM cell is, therefore, consumed by the inverters. Reducing the voltage of WL $(V_{\rm WL})$ increases the gate-oxide leakage currents conducted by N3 and N4 while lowering only the subthreshold leakage current produced by N4, for the data storage condition shown in Fig. 5(a). Applying the super cutoff scheme to the access transistors, therefore, does not provide a noticeable leakage reduction in a conventional 6T SRAM cell as shown in Fig. 6.

WR and RD signals are both maintained below zero volts in order to lower the leakage current of the 9T SRAM cell with a super cutoff sleep mode as shown in Fig. 5(b). Subthreshold leakage currents of the 9T SRAM cell are produced by N1, P2, N4, N6, and N7, for the data storage condition shown in Fig. 5(b). The total current conducted by N5 and N6 is equal to the leakage current produced by N7. Node3 is maintained at approximately $0.9\times V_{\rm DD}$ in the standby mode. The subthreshold leakage current produced by the extra transistor N7 is significantly reduced since $V_{\rm GS}$ is negative and $V_{\rm DS}$ is less than $V_{\rm DD}$. Furthermore, the transistors in the cross-coupled inverters are sized minimum with the proposed technique. Alternatively, the inverters need to be sized considerably larger for read stability, write ability, and sufficient feedback pull-up strength in a 6T SRAM cell, thereby producing higher leakage current. The total leakage power consumed by the super cutoff 9T SRAM cell is thereby further reduced as compared to the 6T SRAM cell.

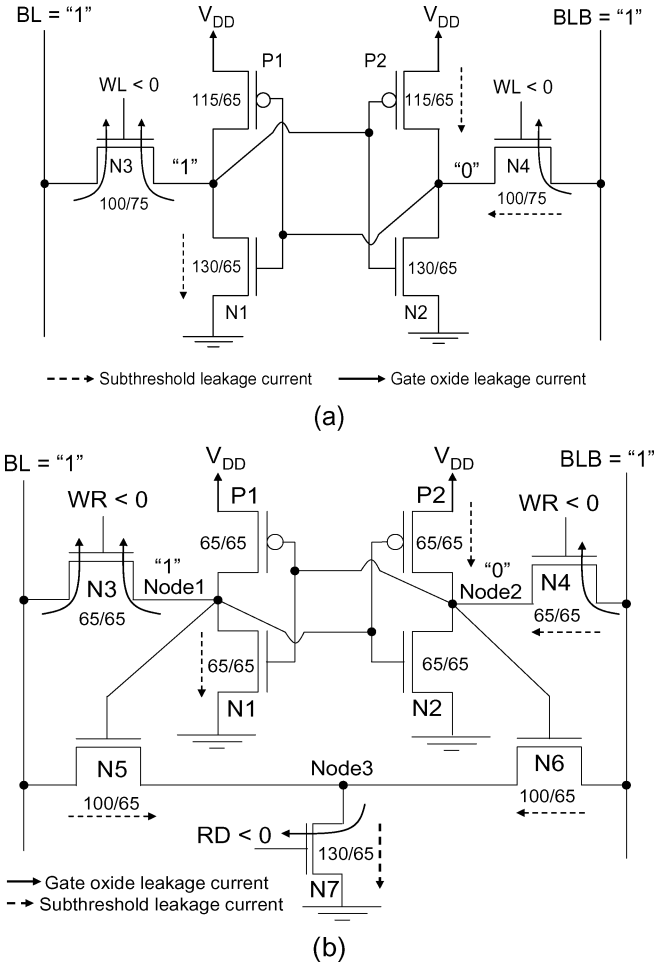

Fig. 5. Super cutoff 6T and 9T SRAM cells in the sleep mode. (a) The super cutoff 6T SRAM cell. (b) The super cutoff 9T SRAM cell. The transistors are sized for a 65-nm CMOS technology.

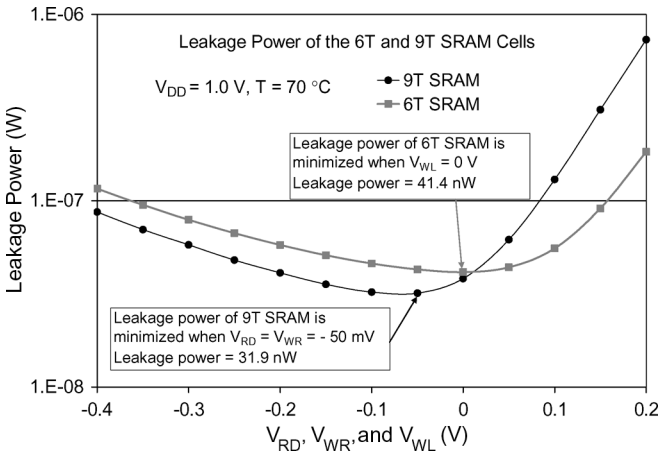

Fig. 6. Leakage power of the 6T and 9T SRAM cells in the standby mode.

The leakage power of the 9T SRAM cell varies with $V_{\rm RD}$ and $V_{\rm WR}$, as shown in Fig. 6. The $V_{\rm RD}$ and $V_{\rm WR}$ are assumed to be equal in the standby mode. The subthreshold leakage currents conducted by the access transistors are reduced by lowering $V_{\rm WR}$ and $V_{\rm RD}$. The total leakage power of the 9T cell is minimized for $V_{\rm RD} = V_{\rm WR} = -50$ mV. Further reduction of $V_{\rm RD}$ and $V_{\rm WR}$ increases the total leakage power consumption due to the higher gate tunneling current of N3, N4, and

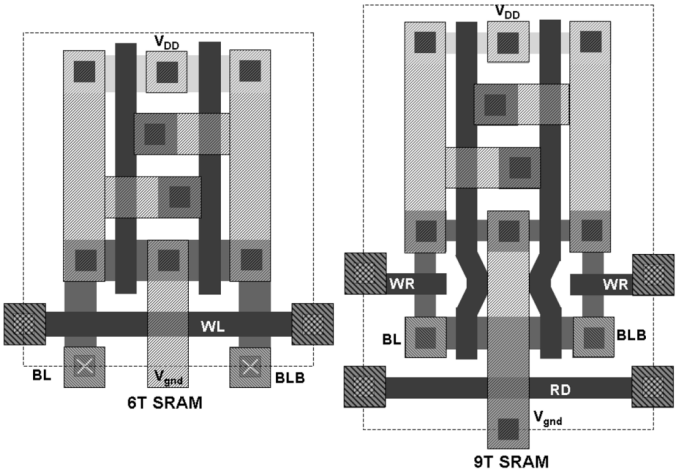

Fig. 7. Layouts of the 6T and 9T SRAM cells. 6T SRAM cell: 0.75 μm^2. 9T SRAM cell: 1.01 μm^2.

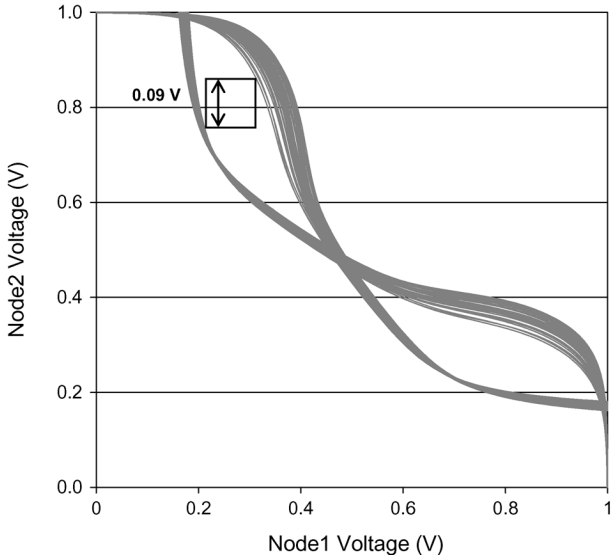

Fig. 8. Static voltage transfer characteristics and worst-case SNM of the 6T SRAM cells during a read operation under process variations.

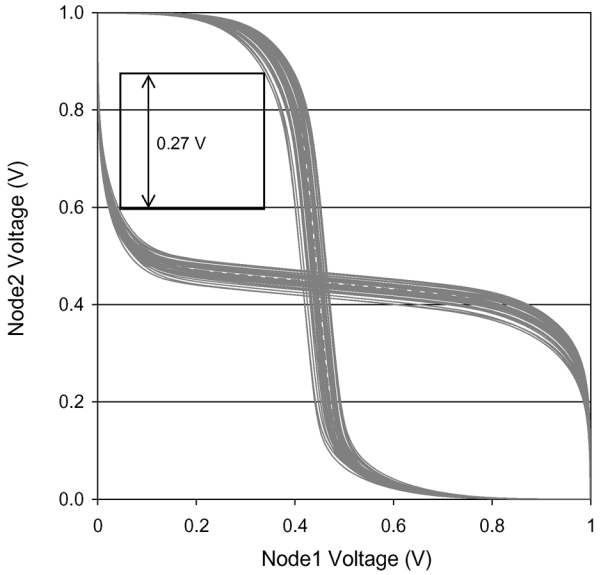

Fig. 9. Static voltage transfer characteristics and worst-case SNM of the 9T SRAM cells during a read operation under process variations.

N7. When $V_{\rm RD} = -50$ mV, the leakage power of the 9T SRAM cell is 22.9% lower than the minimum leakage power achieved with the conventional 6T SRAM cell.

C. Area Comparison

The layouts of the 6T and 9T SRAM cells are drawn based on MOSIS scalable CMOS design rules [10] as shown in Fig. 7. The area of the 9T SRAM cell is increased by 37.8% as compared to the conventional 6T SRAM cell.

IV. Process Variations

Random and systematic fluctuations in channel length, doping concentration, and gate-oxide thickness cause variations in MOSFET characteristics. The read stability of a 6T SRAM cell is determined by the ratio of the current produced by the access transistors (N3 and N4 in Fig. 1) and the nMOS transistors in the cross-coupled inverters (N1 and N2 in Fig. 1). The relative strength of the nMOS transistors in the inverters can vary as compared to the access transistors due to process parameter fluctuations. The read stability, therefore, fluctuates with the process parameters.

From a read stability point of view, the worst-case process variations would strengthen the access transistors N3 and N4 while weakening N1 and N2 as compared to the nominal design corner. With this worst-case variation scenario, the read stability is further degraded since the node which stores "0" is raised to an even higher voltage level as compared to the circuits operating at the nominal process parameter corner. Furthermore, the subthreshold and gate-oxide leakage currents vary with the fluctuations of the threshold voltage and the gate-oxide thickness, inducing variations in the leakage power consumption of the SRAM cells [8], [9].

In this section, read stability and leakage power variations of the SRAM cells due to process fluctuations in gate length ($L_{\rm gate}$), channel doping concentration ($N_{\rm ch}$), and gate-oxide thickness ($t_{\rm ox}$) are evaluated. $L_{\rm gate}$, $N_{\rm ch}$, and $t_{\rm ox}$ are assumed to have normal Gaussian statistical distributions. Each parameter is assumed to have a three sigma (3σ) variation of 10% [9]. Monte Carlo simulations are run to evaluate the read stability and leakage power distributions. The static voltage transfer characteristics and the worst-case SNM of the 6T and the 9T SRAM cells for a read operation are shown in Figs. 8 and 9, respectively.

Process parameter variations degrade the read SNMs of the standard 6T and the proposed 9T cells. The worst-case read SNM of the conventional 6T SRAM cells is degraded by up to 40% as compared to the SNM at the nominal design corner as shown in Fig. 8. Alternatively, the worst-case read SNM of the 9T SRAM cells is 10% lower as compared to the nominal process corner. The proposed 9T SRAM cells provide 3× higher worst-case SNM as compared to the conventional 6T SRAM cells under process parameter fluctuations, as shown in Figs. 8 and 9.

The leakage power distributions due to process parameter variations of the idle 6T and 9T SRAM cells are shown in Fig. 10. For producing the data in Fig. 10, the $V_{\rm WL}$ of the conventional 6T SRAM cells is maintained at 0 V while the $V_{\rm RD}$ and $V_{\rm WR}$ of the 9T SRAM cells are maintained at -50 mV to minimize the leakage power consumption of the two memory arrays. The leakage power distribution curves of the 6T and 9T SRAM cells cross at 34 nW, as shown in Fig. 10. Leakage

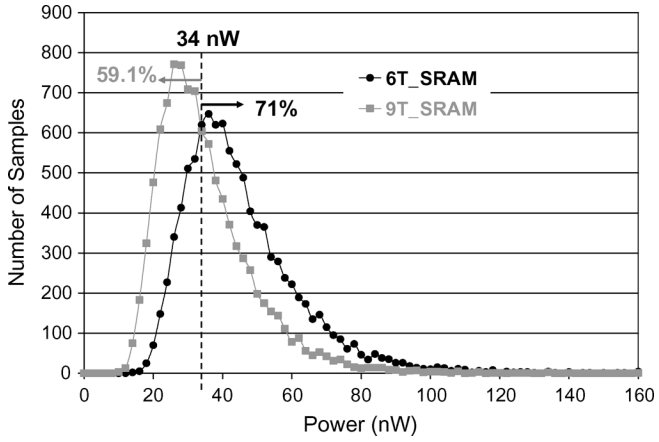

Fig. 10. Idle mode leakage power distributions of the 6T and 9T SRAM cells under process variations.

power consumption of 59.1% of the samples with the proposed technique is lower than 34 nW. Alternatively, 71% of the samples with the conventional 6T SRAM technique consume leakage power higher than 34 nW. The average leakage power consumption of the 6T and the 9T SRAM cells are 45.3 and 35.1 nW, respectively. The standard deviations of leakage power with the 6T and 9T SRAM cells are 16.7 and 13.9 nW, respectively. A 22.6% reduction in average leakage power is provided with the 9T SRAM cells as compared to the 6T cells under process parameter variations.

V. Conclusion

A new 9T SRAM cell is presented in this paper for enhancing the read SNM while reducing the leakage power consumption as compared to the conventional 6T SRAM circuits. The proposed static memory circuit provides two separate data access mechanisms for the read and write operations. During a read operation, the stored data is isolated from the bit lines, thereby enhancing the read SNM by 2× as compared to the conventional 6T SRAM cells. Due to the enhanced stability of the stored data, the transistors in a 9T SRAM cell are sized significantly smaller as compared to the corresponding transistors in a standard 6T SRAM cell. Leakage power consumption of a super cutoff 9T SRAM cell is reduced by 22.9% as compared to a standard 6T SRAM cell. The effectiveness of the 9T SRAM cell for providing significant data stability enhancement and leakage power reduction is also verified under process parameter variations.

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