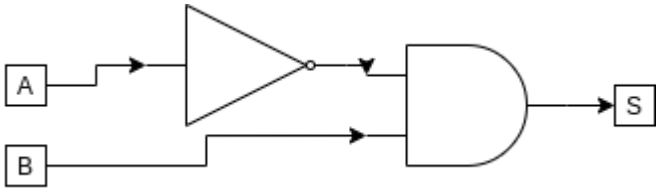
INSTITUTO FEDERAL
Paraíba

Curso Superior de Bacharelado em Engenharia Elétrica

Disciplina: Sistemas Digitais
Professor: Lincoln Machado de Araújo

Lista de Exercícios para primeira semana de atividades remotas

1 -(4 pontos) Desenvolva uma descrição de hardware em VHDL para os circuitos digitais abaixo. Para o desenvolvimento do testbench, teste todas as possibilidades de entradas possíveis para cada circuito. (Apenas cole o seu código do EDA Playground)
a)



Após encontrar a solução de forma simplificada através do mapa K, temos que
S=A*.B

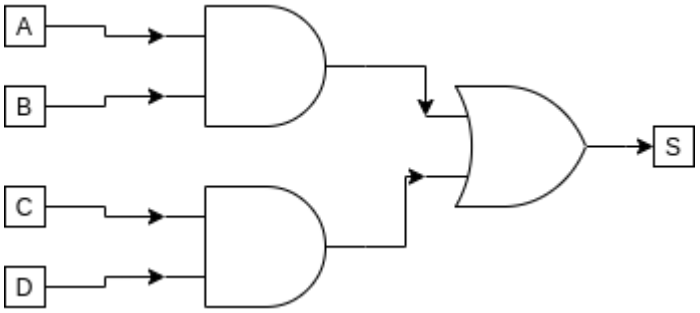
Link do código
https://www.edaplayground.com/x/WPLE

```
library IEEE;
use IEEE.std_logic_1164.all;

entity circuitoA is
port(N: in std_logic_vector (1 downto 0);
    S:  out std_logic      );
end circuitoA;

architecture miolo of circuitoA is begin

  S <= (not N(0)) and N(1);

end miolo;
```

……

```
library IEEE;
use IEEE.std_logic_1164.all;

entity testbench is
end testbench;

architecture test of testbench is

component circuitoA is
port(N: in std_logic_vector (1 downto 0);
    S:  out std_logic      );
end component;

signal N: std_logic_vector (1 downto 0);
signal S: std_logic;

begin

dut: circuitoA port map(N,S);

N <= "00",
    "01" after 5 ns,
    "10" after 10 ns,
    "11" after 15 ns,
    "00" after 20 ns;

end test;
```

b)



Após encontrar a solução de forma simplificada através do mapa K, temos que S=(A.B)+(C.D)

Link do código
https://www.edaplayground.com/x/AFP4

```
library IEEE;
use IEEE.std_logic_1164.all;

entity circuitoB is
port(N: in std_logic_vector (3 downto 0);
    S:  out std_logic      );
end circuitoB;

architecture miolo of circuitoB is begin

  S <= (N(0) and N(1)) or (N(2) and N(3));

end miolo;
……..
library IEEE;
use IEEE.std_logic_1164.all;

entity testbench is
end testbench;

architecture test of testbench is

component circuitoB is
port(N: in std_logic_vector (3 downto 0);
    S:  out std_logic      );
end component;

signal N: std_logic_vector (3 downto 0);
signal S: std_logic;

begin

dut: circuitoB port map(N,S);

N <= "0000",
    "0001" after  5 ns,
    "0010" after 10 ns,
    "0011" after 15 ns,
    "0100" after 20 ns,
    "0101" after 25 ns,
    "0110" after 30 ns,
    "0111" after 35 ns,
    "1000" after 40 ns,
    "1001" after 45 ns,
    "1010" after 50 ns,
    "1011" after 55 ns,
```

```
    "1100" after 60 ns,
    "1101" after 65 ns,
    "1110" after 70 ns,
    "1111" after 75 ns,
    "0000" after 80 ns;


end test;
```