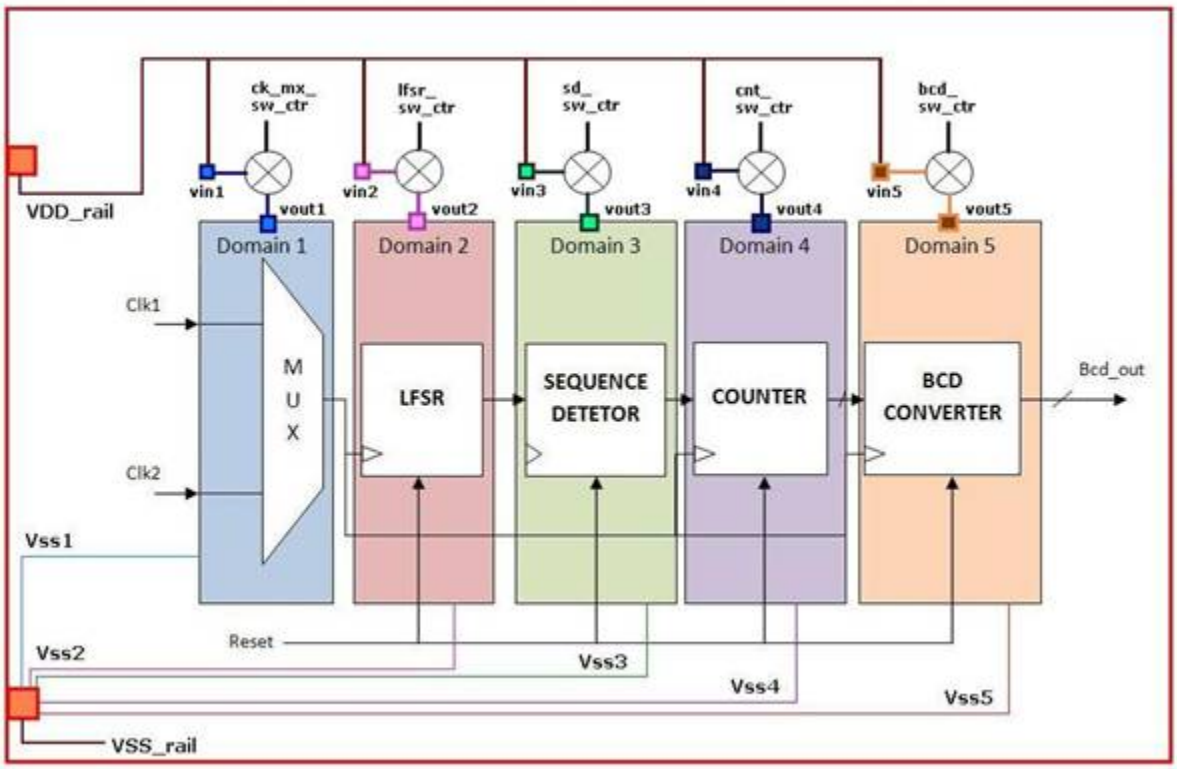
EEM216A Design of VLSI Circuits and Systems **Fall 2015**
Prof. Dejan Marković Lab #3

Due: Monday, Nov 30 at 4pm

The goal of this lab is to introduce you to the Unified Power Format, which is used to specify multiple clock and power domains, as well as power and clock gating. This lab will cover the basics of simulating and synthesizing a design with multiple power domains for power gating. Below is a power plan of the design we will be working with.



To begin, you will need to source the included setup file (different from your tool-setup file you usually use):

```
tcsh
source tool-setup_lab3
```

Included files: lab3_tb.sv, lab3.upf, top.v, 1_clk_mux.v, 2_lfsr.v, 3_seqdet.v, 4_counter.v, 5_bcd_convert.v, lab3_synthesis.tcl, tool-setup_lab3

Part 1: Simulating UPF in ModelSim

The Verilog-2001 standard was created before the UPF format, so it does not support it. However, SystemVerilog is an extension of Verilog-2001 and does support UPF. The testbench (lab3_tb.sv) is written in SystemVerilog (as a reference for you) and does not need to be modified. However, before you can simulate it you will need to complete lab3.upf.

Your first task is to create the power switch for the Counter (power domain 4). You should use the other power switches in lab3.upf as a guideline.

The line(s) of code added to lab3.upf for power switch:

Your second task is to create the isolation strategy for the Counter (power domain 4). You should use the other isolation strategies in lab3.upf as a guideline. Note that the "isolation control" and "isolation cells" are different in power domain 4.

The line(s) of code added to lab3.upf for isolation:

In ModelSim, you will need to add the UPF and Power Aware libraries:

```
vmap mtiUPF /w/apps3/Mentor/ModelsimSE/v6.6a/modeltech/upf_lib
vmap mtiPA /w/apps3/Mentor/ModelsimSE/v6.6a/modeltech/pa_lib
```

Now you can compile all of the Verilog files.

To simulate with your lab3.upf, you will need to create a power aware simulation:

```
vopt lab3_tb -pa_upf lab3.upf
```

And to run the simulation, you will need to include the power aware library:

```
vsim -pa work.lab3_tb -L mtiPA
```

Your lab3.upf is correct if you see (after you type “quit -sim"):

```
# ================================================================
#        TEST CASE PASSED     :)        time:2300
# ================================================================
```

Part 2: Synthesis

Before you can synthesize the design you will need to edit the included tcl file. For UPF synthesis, Synopsys Design Compiler needs to know the operating voltage of each power domain. Add these definitions to lab3_synthesis.tcl.

The line(s) of code added to lab3_synthesis.tcl for operating voltages:

Multiple power domains also require the use of isolation cells. By default, the library tells the synthesis tool not to use or touch these cells. Find and uncomment the necessary lines in lab3_synthesis.tcl to enable the isolation cells. Run Synopsys Design Compiler:

```
dc_shell -f lab3_synthesis.tcl
```

Report the synthesized design area here:

Combinational	Buf/Inv	Noncombinational	Net Interconnect

Report the synthesized design power here:

Switch Power	Int. Power	Leak Power	Total Power