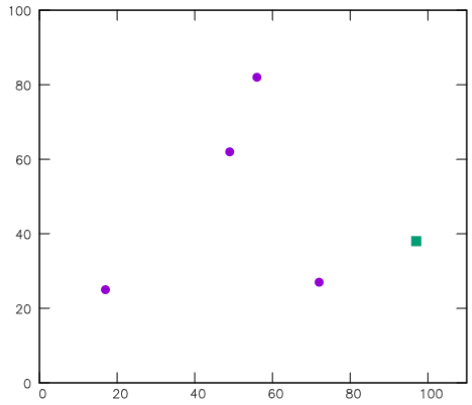
CAD Design Project 2 – Clock Tree Synthesis
Due: 23:59, Oct. 9, 2024

Clock Tree Synthesis (CTS) plays a pivotal role in the design of synchronous digital integrated circuits. In this project, you are required to develop a rectilinear clock tree algorithm with a minimal skew ratio and wire length ratio. Your program would be evaluated in a Linux environment (e.g., WSL) according to the following requirements.

1. Read a CTS input file and generate the output CTS line segment file.
2. For simplicity, the chip dimension is (0, 0) to (dimX, dimY), and all coordinates are integers.
3. The output clock tree must be rectilinear (horizontal and vertical line segments) without incurring a cycle. These line segments connect two nodes ranging from the source node, sink nodes, bend nodes, and Steiner nodes (i.e., branch nodes, if applicable).
4. The arrival time of clock sink i is the total lengths of line segments from the clock source node to the clock sink node i, which are contained within the path set of line segments P_i.
$$T_i = \sum_{l_k \in P_i} l_k$$
5. The skew ratio is the ratio of the maximum arrival time to the minimum arrival time.
$$R_{skew} = \frac{T_{max}}{T_{min}}$$
6. The total wire length of the clock tree is the length summation of all line segments.
$$W_{CTS} = \sum_{l_k \in CTS} l_k$$
7. The wire length ratio is the ratio of the CTS wire length to an RSMT wire length reported from the open-source tool, FLUTE.
$$R_w = \frac{W_{CTS}}{\sum_{l_k \in FLUTE} l_k}$$
8. Upload a tarball (*.tgz) of your program source code and a text ReadMe file, which illustrates how your program is to be compiled and executed in a Linux environment
(NOTE: The uploaded file name should be the same as your student ID.)

Input File Example: input.cts

```
.p 5          # number of pins
.dimx 110     # chip dimension in x-axis
.dimy 100     # chip dimension in y-axis
97 38         # clock source coordinates
49 62         # #1 clock sink coordinates
17 25         # #2 clock sink coordinates
56 82         # #3 clock sink coordinates
72 27         # #4 clock sink coordinates
.e
```

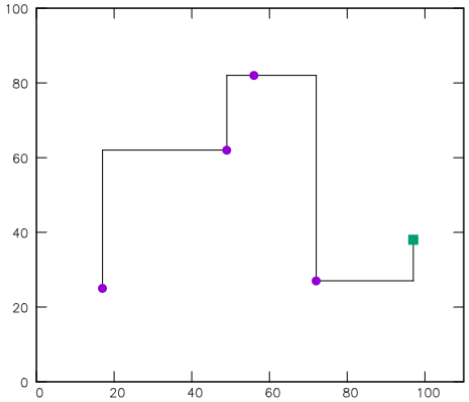


SYNOPSIS for CTS

%> cts INPUT_FILE OUTPUT_FILE

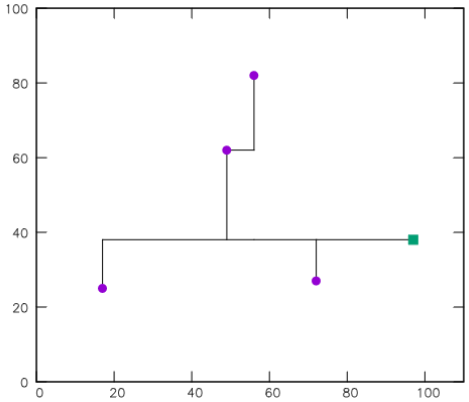
Run-time Examples:

```
%> cts input.cts output1.cts
%> cat output1.cts

.l 8          # number of line segments
.dimx 110     # chip dimension in x-axis
.dimy 100     # chip dimension in y-axis
17 25 17 62   # line segment coordinates
17 62 49 62
72 82 72 27
72 27 97 27
49 62 49 82
49 82 56 82
56 82 72 82
97 27 97 38
.e
```



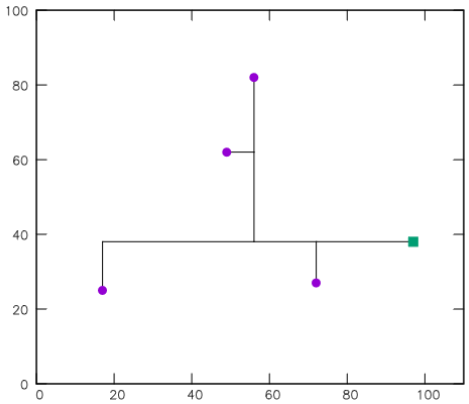
T_max: 203, T_min: 36, Skew ratio: 5.64
W_cts: 203, W_FLUTE: 155, Wire length ratio: 1.31

```
%> cts input.cts output2.cts
%> cat output2.cts

.l 8
.dimx 110
.dimy 100
49 62 56 62
56 62 56 82
72 27 72 38
72 38 97 38
49 62 49 38
49 38 72 38
17 25 17 38
17 38 49 38
.e
```



T_max: 99, T_min: 36, Skew ratio: 2.75
W_cts: 155, W_FLUTE: 155, Wire length ratio: 1.0

```
%> cts input.cts output3.cts
%> cat output3.cts

.l 8
.dimx 110
.dimy 100
49 62 56 62
56 62 56 82
72 27 72 38
72 38 97 38
56 62 56 38
56 38 72 38
17 25 17 38
17 38 56 38
.e
```



T_max: 93, T_min: 36, Skew ratio: 2.58
W_cts: 155, W_FLUTE: 155, Wire length ratio: 1.0