CAD Design Project 3 – Standard Cell Placement Legalization
Due: 23:59, Nov. 6, 2024

In the standard cell IC design flow, placement is the stage that comes after logic synthesis and before routing. During this step, logic gates and other modules are assigned to specific locations on the chip. Good placement is crucial for improving circuit performance, routing feasibility, thermal distribution, and power consumption. The placement process typically includes three major steps: (1) Global placement generates an eagle-eye rough layout result where gate positions may overlap. (2) Legalization adjusts the global placement to ensure that all gate positions are legal and non-overlapping. (3) Detailed placement fine-tunes the legalized placement to optimize wirelength, routability, and miscellaneous performance metrics. In this project, you are required to develop a placement legalization algorithm that simultaneously minimizes both total cell displacement and maximum cell displacement. Your program would be evaluated in a Linux environment (e.g., WSL) according to the following requirements.

1. Read a global placement result based on the GSRC Bookshelf file format.
2. For simplicity, there are no macro block, and all logic gates have the same row height.
3. Output a legalized placement result in GSRC Bookshelf file format and report the total displacement and maximum displacement.
4. The displacement of cell *i* is derived in Manhattan distance, where *gp* indicates the X/Y coordinates of global placement and *legal* indicates the X/Y coordinates after legalization.
$$d_i = \left|x_i^{gp} - x_i^{legal}\right| + \left|y_i^{gp} - y_i^{legal}\right|$$
5. The total displacement is the summation of all cell displacements, where G is the set of all logic gates.
$$D_{total} = \sum_{i \in G} d_i$$
6. The maximum cell displacement is the maximum displacement distance among all logic gates.
$$D_{max} = \underset{i \in G}{\text{Max}} \left(d_i\right)$$
7. Upload a tarball (*.tgz) of your program source code and a text ReadMe file, which illustrates how your program is to be compiled and executed in a Linux environment
(NOTE: The uploaded file name should be the same as your student ID.)

Reference

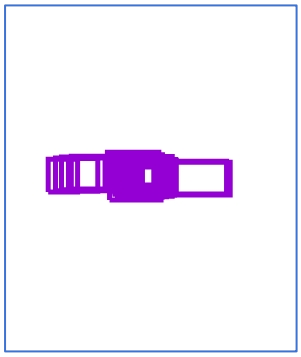
[1] http://vlsicad.eecs.umich.edu/BK/ISPD06bench/BookshelfFormat.txt

SYNOPSIS for legalizer

```
%> legalizer INPUT_FILE OUTPUT_FILE
```

Run-time Examples:

```
%> ls toy.*
toy.aux  toy.nets  toy.nodes
toy.pl   toy.scl   toy.wts
```



```
%> legalizer toy output
Total displacement: 62531.2
Maximum displacement: 5219.7

%> ls output.*
output.aux  output.nets  output.nodes
output.pl   output.scl   output.wts
```