# Neuromorphic System Using Memcapacitors and Autonomous Local Learning

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***Abstract*— Artificial intelligence is used for various applications and is promising as an indispensable infrastructure in future societies. Neural networks are representative technologies that imitate human brains and exhibit various advantages. However, the size is bulky, the power is huge, and some advantages are not demonstrated because they are executed on Neumann-type computers. Neuromorphic systems are biomimetic systems from the hardware level to implement neuron and synapse elements, and the size is compact, the power is low, and the operation is robust. However, because the conventional ones are not composed of fully optimized hardware, the power is not yet minimal, and extra control circuits must be used. In this article, we developed a neuromorphic system using memcapacitors and autonomous local learning. By using memcapacitors, the power can be minimal, and by using autonomous local learning, the control circuits to handle the synapse elements can be deleted. First, the memcapacitors are completed in a cross-bar array, where the ferroelectric layers are sandwiched between the horizontal and perpendicular electrodes. The polarization and capacitance exhibit hysteresis due to the dielectric polarization. Next, autonomous local learning is introduced as follows. During the training phase, associative patterns to be memorized are directly sent, relatively high voltages are applied, and dielectric polarizations are induced. During the operation phase, relatively low voltages are applied, and input signals are weighted with the capacitances of the memcapacitors, summed, and transferred as the output signals. Finally, the experimental system is set up, and the experimental results are acquired. The memorized patterns during the training phase, distorted patterns as the input signals during the operation phase, and retrieved patterns as the output signals in the operation phase are shown. Researchers found that the retrieved patterns are completely the same as the memorized patterns. This means that the neuromorphic system works as an associative memory.**

***Index Terms*— Autonomous local learning, cross-bar array, ferroelectric layer, memcapacitor, neuromorphic system.**

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## I. Introduction

ARTIFICIAL intelligence is used for various applications, such as information retrieval and provision, language translation and caption composition, expert system, handwriting letter and image recognition, autonomous driving, and artificial brain [1], [2], and it is also promising as an indispensable infrastructure to create novel concepts in future smart societies [3]. Neural networks are typical representative technologies of artificial intelligence that imitate human brains, mimic biological functions, and demonstrate various advantages, such as self-organization, self-learning, parallel-distributed computing, and fault tolerance [4]–[6]. However, because the traditional ones are composed of complicated and lengthy software executed on high-spec and super-performance hardware, which is not customized, the computer size is incredibly bulky, and the power consumption is unbelievably huge. For example, one of the most illustrious cognitive systems exhibits the computer size of several refrigerators and power consumption of several hundred kW [7], [8]. Moreover, some abovementioned advantages, such as parallel-distributed computing and fault tolerance, are not demonstrated because they are still executed on old-fashioned Neumann-type computers [9]. Although parallel-distributed computing is executed on some systems, such as multiple cores, GPUs, systolic arrays, and multiple instruction multiple data, because they are parallel-connected Neumann-type computers, the effect is limited [10].

Neuromorphic systems are biomimetic systems from the more basic hardware level to implement neuron and synapse elements, which is customized from device, circuit, and architecture viewpoints, and they demonstrate the same advantages as human brains, namely, the system size is excellently compact, the power consumption is extremely low, and the system operation is dramatically robust [11]–[13]. However, because

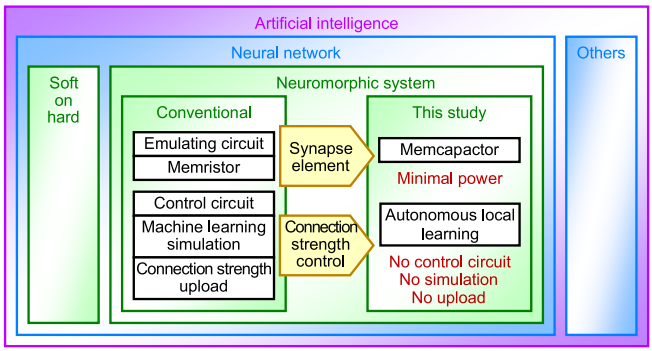


Fig. 1. Neuromorphic system using memcapacitors and autonomous local learning.

the conventional ones are not composed of fully optimized hardware, the abovementioned advantages are only partially got [14]–[18]. We worry that two serious issues are present, which need to be resolved. First, the power consumption is not yet minimal, when cumbersome emulating circuits of a certain scale or memristors are used, especially for the synapse elements because direct current (dc) is consumed there. Second, extra control circuits of a large scale to handle connection strength of synapse elements must be used, which are sometimes larger than neural networks themselves, when machine learning is simulated elsewhere, such as on server computers, and connection strength is uploaded to neuromorphic systems.

In this article, we developed a neuromorphic system using memcapacitors [19], [20] and autonomous local learning. The neuromorphic system using memcapacitors and autonomous local learning is shown in Fig. 1. Instead of using emulating circuits or memristors, by using memcapacitors, the power consumption can be minimal because the direct current is saved there. By using autonomous local learning, the control circuits to handle the synapse elements can be deleted, the machine learning is not required to be simulated elsewhere, and the connection strength does not need to be uploaded to the neuromorphic systems, which make the neuromorphic systems the simplest structure. In this article, we will explain the device structure and ferroelectric characteristic of the memcapacitors, the working principle of the autonomous local learning, and the experimental result of the neuromorphic system as an associative memory [21].

## II. Memcapacitors

The memcapacitors are shown in Fig. 2 [22]. The device structure is shown in Fig. 2(a). First, a Pt thin film is deposited on a quartz glass substrate using dc sputtering of a Pt metal target, which is used as bottom electrodes. Next, a $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) thin film is deposited using the sol–gel process, namely, dissolution of a BLT precursor in 1-butanol at 10 wt.%, spin coating of the source solution, furnace hot-plate annealing at 300 °C for 5 min, and at 400 °C for 10 min, and rapid thermal annealing (RTA) in $O_2$ at 750 °C for 30 min, sequentially, whose thickness is 320 nm, and which is used as ferroelectric layers. Finally, an Au film is deposited using vacuum evaporation, which is used as top electrodes. As a result, the memcapacitors are completed in a cross-bar array, where the ferroelectric layers of the BLT thin film are sandwiched between the top electrodes of the Au thin film as the perpendicular electrodes and bottom electrodes of the Pt thin film as the horizontal electrodes, and the dimension of the memcapacitors is $1.2 \times 1.2$ mm$^2$. The ferroelectric characteristic is shown in Fig. 2(b). The electric field ($E$) is scanned, the polarization ($P$) is measured, and the capacitance ($C$) is calculated, both of which exhibit hysteresis due to the dielectric polarization. The remanent $P$ is 1.2 $\mu$C/cm$^2$, and the coercive $E$ is 130 kV/cm, when $E$ is scanned in $\pm$300 kV/cm. Here the scan frequency is 1 kHz, the measurement time is 10 s or so, and the ferroelectric characteristic is stable. Therefore, it is concluded that the repeatability of 10 000 times or more is ensured, which is sufficient for the application in this article, neuromorphic systems.

## III. Autonomous Local Learning

The autonomous local learning is shown in Fig. 3. The training phase is shown in Fig. 3(a), and the operating-point analysis is shown in Fig. 3(c). During the training phase, associative patterns to be memorized are directly sent as input signals. Relatively high voltages are applied to both the horizontal and perpendicular electrodes. For the cross-bar points where the voltages are different between the horizontal and perpendicular electrodes, a high $E$ is applied to the memcapacitors, and the dielectric polarizations are induced, whose operating points are indicated by dark purple circle dots in Fig. 3(c). Conversely, for the cross-bar points where the voltages are the same between the horizontal and perpendicular electrodes, no E is applied to the memcapacitors, and no dielectric polarizations are induced, whose operating point is indicated by a bright purple rhombus dot on the ferroelectric characteristic in Fig. 3(c). The operation phase is shown in Fig. 3(b), and the operating-point analysis is again shown in Fig. 3(c). During the operation phase, relatively low voltages are applied to only the horizontal electrodes. For the cross-bar points where the dielectric polarizations are induced during the training phase, the capacitances are higher, whose operating points move to dark purple arrowheads in Fig. 3(c). Conversely, for the cross-bar points where no dielectric polarizations are induced during the training phase, the capacitances are lower, whose operating point remains at the bright purple rhombus dot in Fig. 3(c). As a result, the capacitances of the memcapacitors during the operation phase depend on the history of the voltage application during the training phase. The input signals are weighted with the capacitances of the memcapacitors, summed, and transferred as the output signals. The output signals of analog voltage from the perpendicular electrodes are binarized and returned to the input signals of digital voltage to the horizontal electrodes. By repeating these dynamics, the final values of the output signals are obtained. This learning is autonomous because the associative patterns to be memorized are directly sent, and no intentional and pre-processed teaching is performed. Furthermore, the learning is local because the capacitances of the memcapacitors change depending only on the voltages between the top and bottom electrodes of themselves. The actual photograph is shown

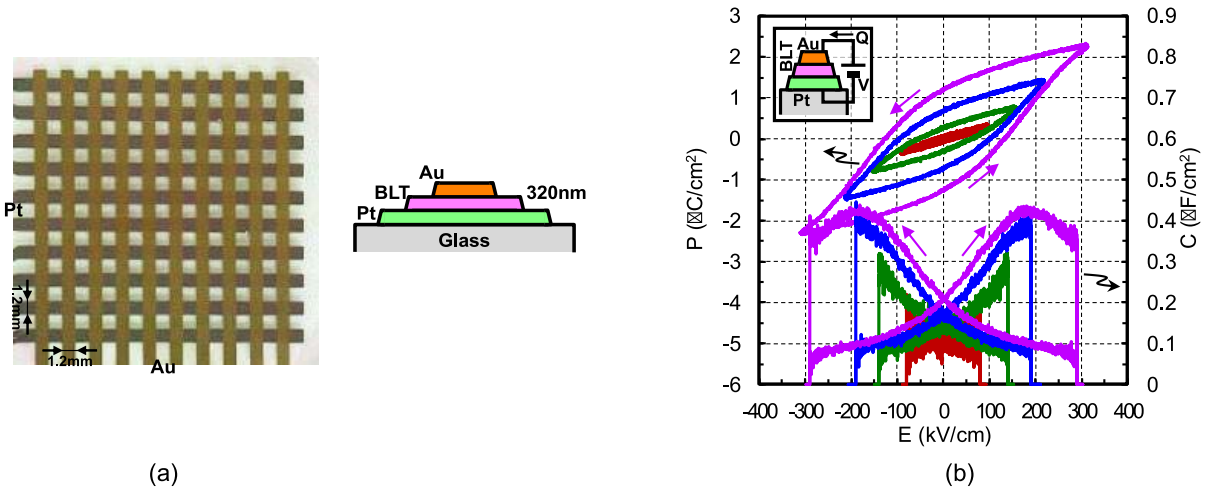


Fig. 2. Memcapacitors. (a) Device structure: The memcapacitors are completed in a cross-bar array, where the ferroelectric layers are sandwiched between the top and bottom electrodes. (b) Ferroelectric characteristic: $E$ is scanned, $P$ is measured, and $C$ is calculated, both of which exhibit hysteresis. The remanent $P$ is 1.2 $\mu$C/cm$^2$, and the coercive $E$ is 130 kV/cm, when $E$ is scanned in $\pm$300 kV/cm.

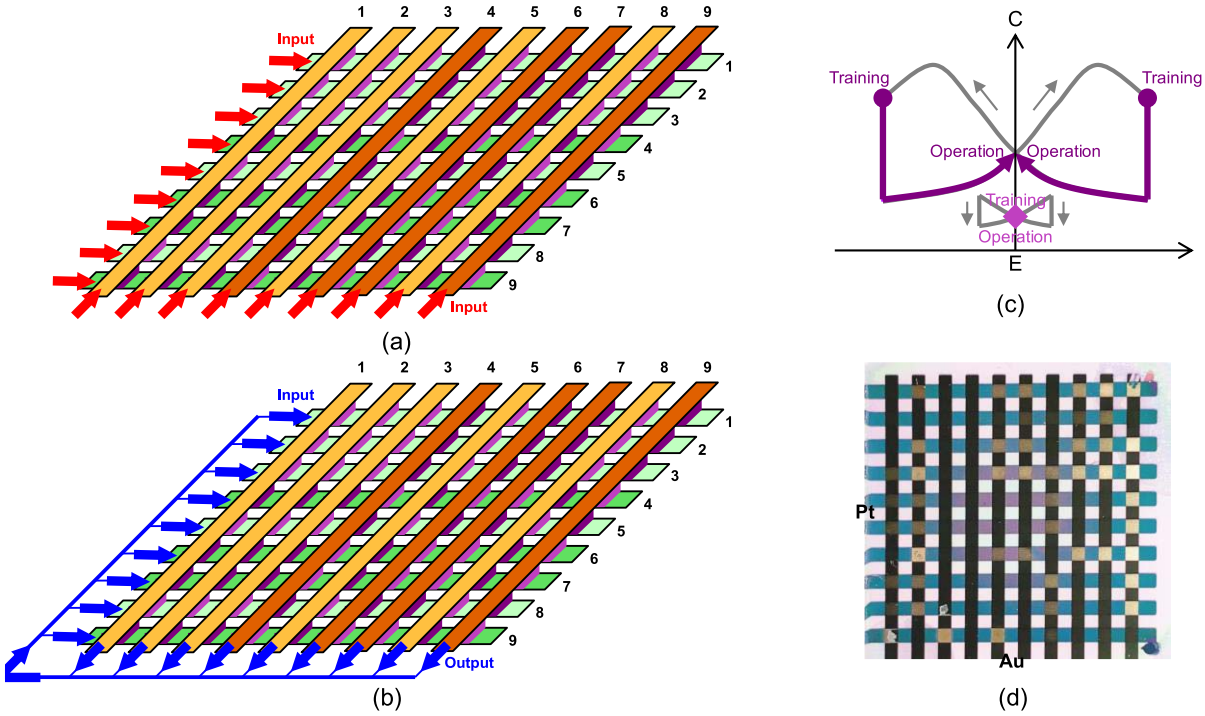


Fig. 3. Autonomous local learning. (a) Training phase: Associative patterns to be memorized are directly sent as input signals. High voltages are applied to both the horizontal and perpendicular electrodes. For the cross-bar points where the voltages are different between both the electrodes, the dielectric polarizations are induced. For the other cross-bar points, no dielectric polarizations are induced. (b) Operation phase: Low voltages are applied to only the horizontal electrodes. The capacitances of the memcapacitors during the operation phase depend on the history of the voltage application during the training phase. The input signals are weighted with the capacitances, summed as the output signals, binarized, and returned to the input signals. By repeating these dynamics, the final values of the output signals are obtained. (c) Operating-point analysis: During the training phase, for the cross-bar points where the voltages are different between both the electrodes, the operating points are indicated by dark purple circle dots. For the other cross-bar points, the operating point is indicated by a bright purple rhombus dot. During the operation phase, for the former points, the operating points move to dark purple arrowheads. For the latter points, the operating point remains at the bright purple rhombus dot. (d) Actual photograph: The color pattern is a visualization of the dielectric polarization pattern.

in Fig. 3(d). In comparison with the initial photograph shown in Fig. 2(a), the final photograph shown in Fig. 3(d) shows that the color changes at some cross-bar points because the BLT thickness also changes due to the inverse piezoelectric effect when the dielectric polarizations are induced. In other words, the color pattern is a visualization of the dielectric polarization pattern.

## IV. Experimental System

The experimental system is shown in Fig. 4. The actual photograph is shown in Fig. 4(a). Here, a full-connection neural network is actually assembled by combining nine neuron elements in a field-programmable gate array (FPGA) chip and $9 \times 9 = 81$ synapse elements in the cross-bar array. The schematic model of the whole network is shown in Fig. 4(b).

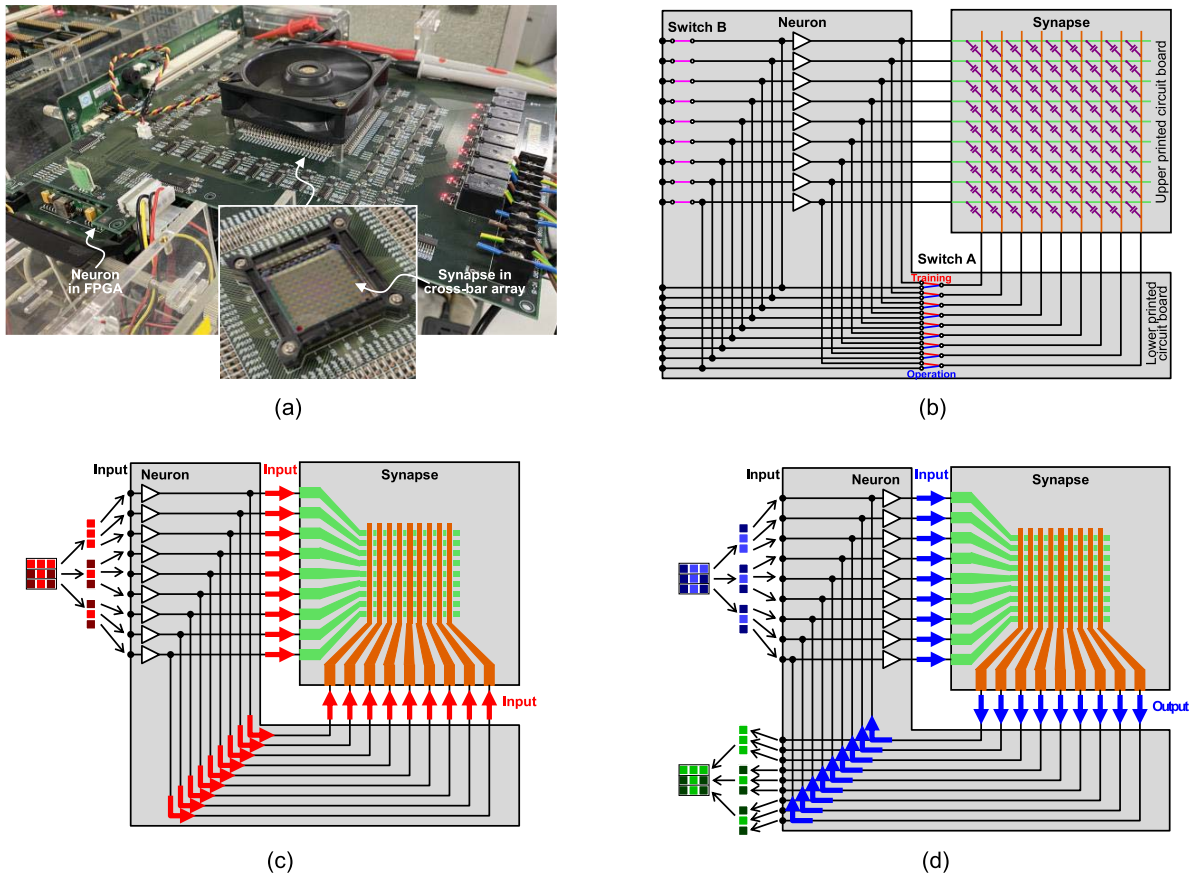


Fig. 4. Experimental system. (a) Actual photograph: A full-connection neural network is actually assembled by combining nine neuron elements in an FPGA chip mounted on the lower printed circuit board and $9 \times 9 = 81$ synapse elements in the cross-bar array set on the upper printed circuit board. (b) Schematic model: The wiring connections are switched between the training and operation phases. (c) Training phase: The neuron elements are connected so that signals are applied to both the horizontal and perpendicular electrodes. Associative patterns to be memorized are directly sent. The voltages of $\pm 10$ V are applied for the on and off pixels, respectively. (d) Operation phase: The neuron elements are connected so that signals are applied to only the horizontal electrodes. Distorted patterns are momentarily sent, and the voltages of $\pm 0.1$ V are applied. The input signals are weighted, summed as the output signals, binarized, and returned to the input signals, and the final values of the output signals are obtained, where the positive and negative voltages are recognized as on and off pixels, respectively.

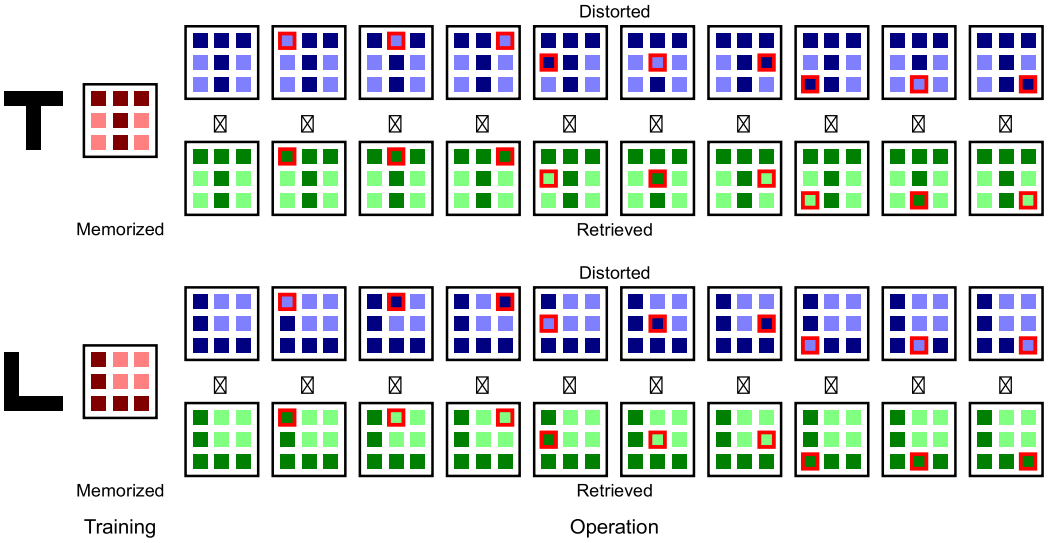


Fig. 5. Experimental results. The memorized patterns during the training phase, namely, "**T**" and "**L**", distorted patterns as the input signals during the operation phase, namely, one-pixel-flipped patterns, and retrieved patterns as the output signals in the operation phase, namely, the final values of the output signals, are shown. The retrieved patterns are completely the same as the memorized patterns.

The neuron element consists of a digital voltage buffer that outputs a binary voltage depending on whether the input voltage exceeds the threshold voltage. The wiring connections are switched between the training and operation phases. Switch A toggles the wire connection between the training and operation phases, and switch B turns the wiring connection on and

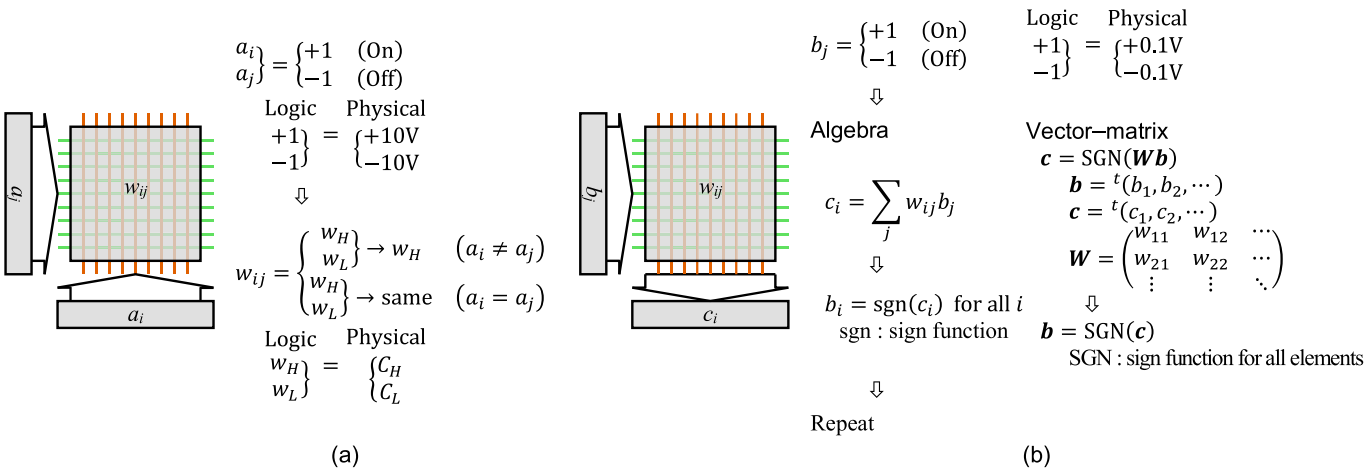


Fig. 6. Mathematical formulation of our neuromorphic system. (a) Training phase: The associative patterns to be memorized, $A_i$, are sent as input signals to both the horizontal and perpendicular electrodes, and the connection strengths of the synapse elements, $w_{ij}$, become higher, $w_H$, for $a_i = a_j$, whereas they remain the same for $a_i = a_j$. (b) Operation phase: The distorted patterns different from the memorized patterns, $b_i$, are sent as input signals to only the horizontal electrodes, weighted with the connection strengths, $w_{ij}$, summed as the output signals, $c_j$, binarized with the sign function, and returned to the input signals, and the final values of the output signals are obtained.

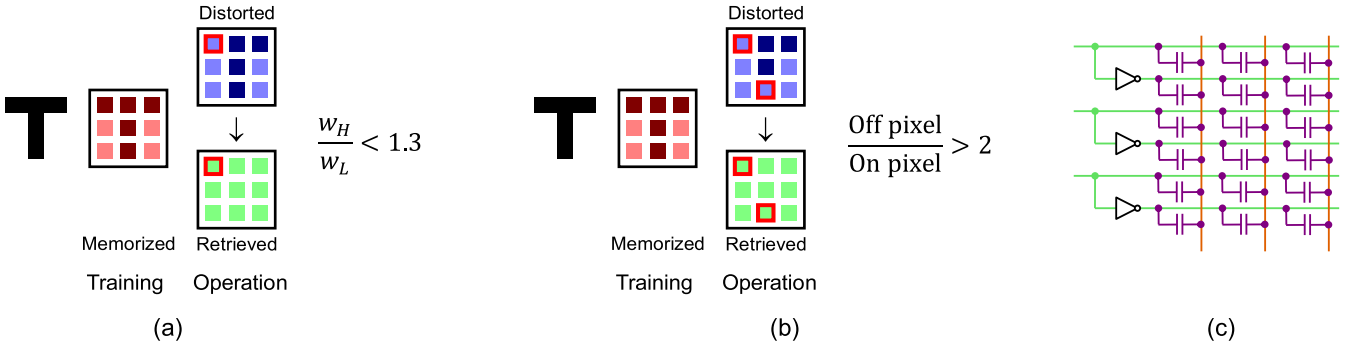


Fig. 7. Performance limits of our neuromorphic system and countermeasure. The retrieved pattern is not the same as the memorized pattern for some cases. The common reason is that our neuromorphic system takes a simple weighted majority vote. (a) One example: When $w_H/w_L$ is small, the difference in connection strengths is not sufficient to reverse the difference in the numbers of on and off pixels. (b) Another example: When the balance between the on and off pixels is far from equal, it is not easy to reverse the relationship by the weighted majority vote. (c) Countermeasure: The countermeasure is to use positive and negative logic as the input signals.

off. The training phase is shown in Fig. 4(c). Here, the neuron elements are connected so that signals to the neuron elements are applied to both the horizontal and perpendicular electrodes of the synapse elements. During the training phase, associative patterns to be memorized, namely, one-1-D patterns of nine signals rearranged from two-dimensional patterns of $3 \times 3 = 9$ pixels, are directly sent as input signals. Relatively high voltages, namely, the voltages of $\pm 10$ V corresponding to $E$ of $\pm 300$ kV/cm, are applied to both the horizontal and perpendicular electrodes. In the input signals, the voltages of 10 V are applied for the on pixels, whereas the voltages of $-10$ V are applied for the OFF pixels. The operation phase is shown in Fig. 4(d). Here, the neuron elements are connected so that signals from the synapse elements to the neuron elements are applied to only the horizontal electrodes of the synapse elements. During the operation phase, distorted patterns, namely, slightly different patterns from the memorized patterns, are momentarily sent as input signals. Relatively low voltages, namely, the voltages of $\pm 0.1$ V, are applied to only the horizontal electrodes. The input signals are weighted with the synapse elements, summed, and transferred as the output signals. The output signals of analog voltage are binarized by the neuron elements and returned to the input signals of digital voltage, and the final values of the output signals are obtained. In the output signals, the positive voltages are recognized as ON pixels, whereas the negative voltages are recognized as OFF pixels.

## V. Experimental Results

The experimental results are shown in Fig. 5. Here, the memorized patterns during the training phase, namely, the two-dimensional patterns for "**T**" and "**L**", distorted patterns as the input signals during the operation phase, namely, one-pixel-flipped patterns, and retrieved patterns as the output signals in the operation phase, namely, the final values of the output signals, are shown. Researchers found that the retrieved patterns are completely the same as the memorized patterns. This means that the neuromorphic system works as an associative memory.

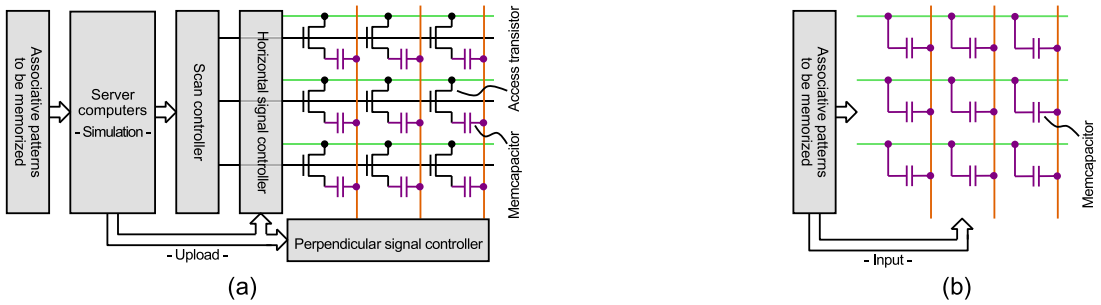


Fig. 8. Architecture comparison of neuromorphic systems. (a) Machine learning simulated on server computers and connection strength uploaded to neuromorphic system: The associative patterns to be memorized are inputted into the server computer, the machine learning is simulated on a server computer, the connection strength is computed, and they are uploaded to the memcapacitors through a scan controller, horizontal signal controller, perpendicular signal controller, etc. Access transistors are also needed to avoid crosstalk. (b) Autonomous local learning: The associative patterns to be memorized are directly inputted into the memcapacitors in the cross-bar array.

Based on an elementary theory for the Hopfield associative memory, $m = n / 4 \log n$, where $n$ is the number of the pixels and $m$ is the maximum of letters that can be memorized [23], by substituting $n = 9$, $m = 1.02$ is obtained. Therefore, even considering that our full-connection neural network is slightly more complex than the Hopfield network, the maximum of letters that can be memorized is one or two at most. In this article, in fact, no more letters can be memorized. In the future, the number of pixels needs to be increased and the learning algorithm needs to be improved so that more letters can be memorized.

## VI. Conclusion

In conclusion, we developed a neuromorphic system using memcapacitors and autonomous local learning. By using memcapacitors, the power can be minimal, and by using autonomous local learning, the control circuits can be deleted. First, the memristors were completed in a cross-bar array, where the polarization and capacitance exhibit hysteresis due to the dielectric polarization. Next, the autonomous local learning was introduced, where during the training phase, the dielectric polarizations are induced, whereas during the operation phase, the input signals are weighted with the capacitances of the memcapacitors, summed, and transferred as the output signals. Finally, the experimental system was set up, and the experimental results were acquired, where researchers found that the retrieved patterns are completely the same as the memorized patterns. As noted in the Appendix, the retrieved pattern is not the same as the memorized pattern for some cases, but we can solve the problem with a countermeasure. Once researchers confirmed that the neuromorphic system works as an associative memory, it can be applied to general use in artificial intelligence because most of the problems in machine learning can be reduced to appropriate problems related to associative memories. Finally, we would like to emphasize that necessary functions are realized only by the memcapacitors in our study, whereas they are realized by combining capacitors and something, such as other electron devices and circuits, in the previous studies [24], [25]. This is because autonomous local learning is also skillfully utilized in our study.

In this article, in order to fundamentally confirm the working principle, the size is far from compact, and the power is not evaluated. The ultimate size and power can be evaluated as follows by assuming advanced semiconductor technologies. Here since the number of the synapse elements is overwhelmingly larger than the number of the neuron elements, we will evaluate the size and power of the synapse elements only. It has been reported that a ferroelectric capacitor can be fabricated using 28 nm semiconductor technologies [26]. The synapse size can be (28 nm line + 28 nm space)$^2$ $\cong$ 3,000 nm$^2$. Even if $10^{14}$ synapse elements are implemented, which are the same number as a human brain, the total size is approximately 3000 cm$^2$ $\cong$ 50 $\times$ 50 cm$^2$, which can be excellently compact by stacking multiple chips. On the other hand, the ferroelectric capacitance can be 30 aF [27]. By supposing the charge–discharge voltage of $\pm$0.1 V and working frequency of 100 kHz, the synapse power can be 30 aF $\times$ (0.2 V)$^2$ $\times$ 100 kHz = 120 fW. Even if $10^{14}$ synapse elements are implemented, the total power is 12 W, which is approximately the same as 20 W in a human brain.

## Appendix

### A. Mathematical Formulation of Our Neuromorphic System

The mathematical formulation of our neuromorphic system is shown in Fig. 6. As shown in Fig. 6(a), during the training phase, the associative patterns to be memorized, $a_i$, are sent as input signals to both the horizontal and perpendicular electrodes. The connection strengths of the synapse elements, $w_{ij}$, become higher, $w_H$, for $a_i = a_j$, whereas they remain the same for $a_i = a_j$. On the other hand, as shown in Fig. 6(b), during the operation phase, the distorted patterns different from the memorized patterns, $b_j$, are sent as input signals to only the horizontal electrodes. They are weighted with the connection strengths, $w_{ij}$, summed as the output signals, $c_i$, binarized with the sign function, and returned to the input signals, and the final values of the output signals are obtained. The mathematical formulation is written in algebra and vector–matrix representations in Fig. 6(b). As physical quantities for circuit implementation, $a_i$ and $a_j$ of $\pm$1 correspond to the voltages of $\pm$10 V, $b_j$ of $\pm$1 corresponds to the voltages of $\pm$0.1 V, $c_i$ corresponds to an analog voltage generated in the circuit working, and $w_{ij}$ of $w_H$ and $w_L$ corresponds to $C_H$ of the high capacitance and $C_L$ of the low capacitance of the memcapacitors.

The performance limits of our neuromorphic system are evaluated based on the abovementioned mathematical formulation by logic simulation because it is difficult to attain the analytical solution. Examples of the performance limits of our neuromorphic system and countermeasure are shown in Fig. 7. The retrieved pattern is not the same as the memorized pattern for some cases. The common reason is that our neuromorphic system takes a simple weighted majority vote. As shown in Fig. 7(a), when $w_H/w_L$ is small, the difference in connection strengths is not sufficient to reverse the difference in the numbers of on and off pixels. Alternatively, as shown in Fig. 7(b), when the balance of the large and small relationship between the numbers of on and off pixels is far from equal, it is not easy to reverse the relationship by the weighted majority vote shown in the equations in Fig. 6(b). As shown in Fig. 7(c), the countermeasure is to use the positive and negative logics simultaneously as the input signals, which solves the abovementioned problem in principle.

### *B. Architecture Comparison of Neuromorphic Systems*

An example of an architecture comparison of neuromorphic systems is shown in Fig. 8. Here, it is assumed that memcapacitors are used for the synapse elements in the cross-bar array, and the capacitance is set to a binary state, namely, either higher or lower state, during the training phase. In the case shown in Fig. 8(a), the associative patterns to be memorized are inputted into a server computer, the machine learning is simulated on it, the connection strength is computed, and they are uploaded to the memcapacitors through a scan controller, horizontal signal controller, perpendicular signal controller, etc. Access transistors are also needed to avoid crosstalk. On the other hand, as shown in Fig. 8(b), in the case of autonomous local learning, the associative patterns to be memorized are directly inputted into the memcapacitors in the cross-bar array. This explains why local autonomous learning yields the simplest structure.

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## REFERENCES

[1] J. McCarthy, M. L. Minsky, N. Rochester, and C. E. Shannon, "A proposal for the Dartmouth summer research project on artificial intelligence," in *Proc. Dartmouth Conf.*, 1956. [Online]. Available: https://ojs.aaai.org/index.php/aimagazine/article/download/1904/1802

[2] S. Russell and P. Norvig, *Artificial Intelligence: A Modern Approach*. London, U.K.: Pearson, 2009.

[3] *Society 5.0*. Accessed: Apr. 19, 2020. [Online]. Available: https://www8.cao.go.jp/cstp/english/society5_0/index.html

[4] W. S. McCulloch and W. Pitts, "A logical calculus of the ideas immanent in nervous activity," *Bull. Math. Biophys.*, vol. 5, no. 4, pp. 115–133, 1943.

[5] P. D. Wasserman, *Neural Computing: Theory and Practice*. Scottsdale, AZ, USA: Coriolis Group, 1989.

[6] J. E. Dayhoff, *Neural Network Architectures, an Introduction*. New York, NY, USA: Van Nostrand Reinhold, 1990.

[7] D. Ferrucci *et al.*, "Building Watson: An overview of the DeepQA project," *AI Mag.*, vol. 31, no. 3, pp. 59–79, 2010.

[8] *IBM Watson*. Accessed: Apr. 19, 2020. [Online]. Available: https://www.ibm.com/watson/index.html

[9] J. Von Neumann, *First Draft of a Report on the EDVAC*. Philadelphia, PA, USA: Univ. Pennsylvania, 1945.

[10] B. Chapman, F. Desprez, G. R. Joubert, A. Lichnewsky, and F. Peters, *Parallel Computing: From Multicores and GPU's to Petascale*. Amsterdam, The Netherlands: IOS Press, 2010.

[11] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA, USA: Addison-Wesley, 1989.

[12] T. S. Lande, *Neuromorphic Systems Engineering, Neural Networks in Silicon*. New York, NY, USA: Springer, 2013.

[13] M. Suri, *Advances in Neuromorphic Hardware Exploiting Emerging Nanoscale Devices*. New Delhi: Springer, 2017.

[14] P. A. Merolla *et al.*, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, Aug. 2014.

[15] J. Hsu, "IBM's new brain," *IEEE Spectr.*, vol. 51, no. 10, pp. 17–19, Oct. 2014.

[16] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, pp. 61–64, May 2015, doi: 10.1038/nature14441.

[17] A. Neckar *et al.*, "Braindrop: A mixed-signal neuromorphic architecture with a dynamical systems-based programming model," *Proc. IEEE*, vol. 107, no. 1, pp. 144–164, Jan. 2019.

[18] *IBM Brain Power*. Accessed: Apr. 19, 2020. [Online]. Available: http://www.ibm.com/smarterplanet/jp/ja/brainpower/

[19] Y. V. Pershin and M. Di Ventra, "Neuromorphic, digital, and quantum computation with memory circuit elements," *Proc. IEEE*, vol. 100, no. 6, pp. 2071–2080, Jun. 2012.

[20] Y. Chen, J. Zhang, Y. Zhang, R. Zhang, M. Kimura, and Y. Nakashima, "A programmable calculation unit employing memcapacitor-based neuromorphic circuit," in *Proc. NEWCAS*, 2019, pp. 1–4.

[21] T. Kohonen, *Self-Organization and Associative Memory*. Berlin, Germany: Springer, 1989.

[22] K.-I. Haga and E. Tokumitsu, "Fabrication and characterization of ferroelectric-gate thin-film transistors with an amorphous oxide semiconductor, amorphous In–Ga–Zn–O," *Jpn. J. Appl. Phys.*, vol. 53, no. 11, Nov. 2014, Art. no. 111103.

[23] R. McEliece, E. Posner, E. Rodemich, and S. Venkatesh, "The capacity of the Hopfield associative memory," *IEEE Trans. Inf. Theory*, vol. IT-33, no. 4, pp. 461–482, Jul. 1987.

[24] O. Kavehei *et al.*, "An associative capacitive network based on nanoscale complementary resistive switches for memory-intensive computing," *Nanoscale*, vol. 5, no. 11, pp. 5119–5128, 2013.

[25] Z. Wang *et al.*, "Capacitive neural network with neuro-transistors," *Nature Commun.*, vol. 9, no. 1, p. 3208, Dec. 2018.

[26] M. Trentzsch *et al.*, "A 28 nm HKMG super low power embedded NVM technology based on ferroelectric FETs," in *IEDM Tech. Dig.*, Dec. 2016, p. 11.

[27] C. H. Diaz *et al.*, "32 nm gate-first high-k/metal-gate technology for high performance low power applications," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

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