Analog Memcapacitor by Ferroelectric Capacitor and Its Application to Spiking Neuromorphic System

Yuma Ishisaki, Reon Oshio, *Graduate Student Member, IEEE*, Takumi Kuwahara, Michihiro Shintani, *Senior Member, IEEE*, Eisuke Tokumitsu, *Member, IEEE*, Tokiyoshi Matsuda, *Member, IEEE*, Hidenori Kawanishi, *Member, IEEE*, Yasuhiko Nakashima, *Senior Member, IEEE*, and Mutsumi Kimura, *Senior Member, IEEE*

***Abstract*— An analog memcapacitor has been created by a ferroelectric capacitor. Since the memcapacitor is a capacitor, the power consumption is not dissipated at all in principle. The device structure is that a ferroelectric layer is sandwiched between the bottom electrode and the top electrode. The analog memcapacitor characteristic is realized, namely, varying Vmax is applied, and the capacitance is strongly dependent on it. The working principle can be explained by the operating point analysis for the intrinsic property of the ferroelectric layer. If the memcapacitors are implemented in neuromorphic systems, it is expected that the power consumption will be remarkably reduced. It has been simulated that the spiking neuromorphic system dissipates only 6.24 nJ/Inference for MNIST inference with acceptable accuracy, which is much lower than other systems.**

***Index Terms*— Analog memcapacitor, ferroelectric capacitor, spiking neuromorphic system.**

Manuscript received 21 February 2024; revised 27 April 2024; accepted 29 May 2024. Date of publication 7 June 2024; date of current version 25 July 2024. This work was supported in part by the Japan Society for the Promotion of Science (JSPS) KAKENHI (C) under Grant 19K11876, Grant 22H00515, and Grant 22K11954; in part by the Japan Science and Technology Agency (JST) Strategic International Collaborative Research Program (SICORP) Taiwan; in part by the Artificial Intelligence Research Promotion Foundation; in part by KDDI Foundation; in part by the High-Tech Research Center in Ryukoku University; in part by the Laboratory for Materials and Structures in Tokyo Institute of Technology; in part by the Research Institute of Electrical Communication in Tohoku University; and in part by Mitsubishi Materials Corporation. The review of this article was arranged by Editor P. Narayanan. *(Corresponding author: Mutsumi Kimura.)*

Yuma Ishisaki was with the Graduate School of Science and Technology, Ryukoku University, Otsu 520-2194, Japan. He is now with the Research and Development Department, SK-Electronics Company Ltd., Koka 528-0068, Japan.

Reon Oshio, Takumi Kuwahara, and Yasuhiko Nakashima are with the Graduate School of Science and Technology, Nara Institute of Science and Technology (NAIST), Ikoma 630-0192, Japan.

Michihiro Shintani is with the Graduate School of Science and Technology, Kyoto Institute of Technology, Kyoto 606-8585, Japan.

Eisuke Tokumitsu is with the Graduate School of Advanced Science and Technology, Japan Advanced Institute of Science and Technology (JAIST), Nomi 923-1292, Japan.

Tokiyoshi Matsuda is with the Faculty of Science and Engineering, Kindai University, Higashiosaka 577-8502, Japan.

Hidenori Kawanishi is with the Innovative Materials and Processing Research Center, Ryukoku University, Otsu 520-2194, Japan, and also with the Graduate School of Science and Technology, Nara Institute of Science and Technology (NAIST), Ikoma 630-0192, Japan.

Mutsumi Kimura is with the Faculty of Advanced Science and Technology, Ryukoku University, Otsu 520-2194, Japan, and also with the Graduate School of Science and Technology, Nara Institute of Science and Technology (NAIST), Ikoma 630-0192, Japan (e-mail: mutsu@rins.ryukoku.ac.jp).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2024.3408783.

Digital Object Identifier 10.1109/TED.2024.3408783

I. Introduction

A MEMRISTOR is a resistor whose resistance is dependent on the history of the applied voltage and flowing current [1], and a historic report triggered aggressive research and development that extends even until now [2]. Moreover, an analog memristor, whose resistance is continuously controlled, has been presented, which is promising especially for neuromorphic applications [3]. However, since the memristor is a resistor in any case, the power consumption is dissipated in principle. On the other hand, a memcapacitor is a capacitance whose capacitance is dependent on the history of the applied voltage [4], but research and development has not yet spread widely.

In this article, an analog memcapacitor, whose capacitance is continuously controlled, has been created by a ferroelectric capacitor, which will be promising also, especially for neuromorphic applications [5]. Moreover, since the memcapacitor is a capacitor, the power consumption is not dissipated at all in principle. The device structure, analog memcapacitor characteristics, and the working principle will be explained. If the memcapacitors are implemented in neuromorphic systems, it is expected that the power consumption will be remarkably reduced [6]. Circuit simulation will be executed to prove that the spiking neuromorphic system dissipates extremely low energy consumption.

II. Device Structure

The device structure is shown in Fig. 1. The overall view is shown in Fig. 1(a), and the cross-sectional view is shown in Fig. 1(b). A ferroelectric layer is sandwiched between the bottom electrode and the top electrodes. The fabrication process is shown in Fig. 1(c) [7]. First, a Ti thin film and

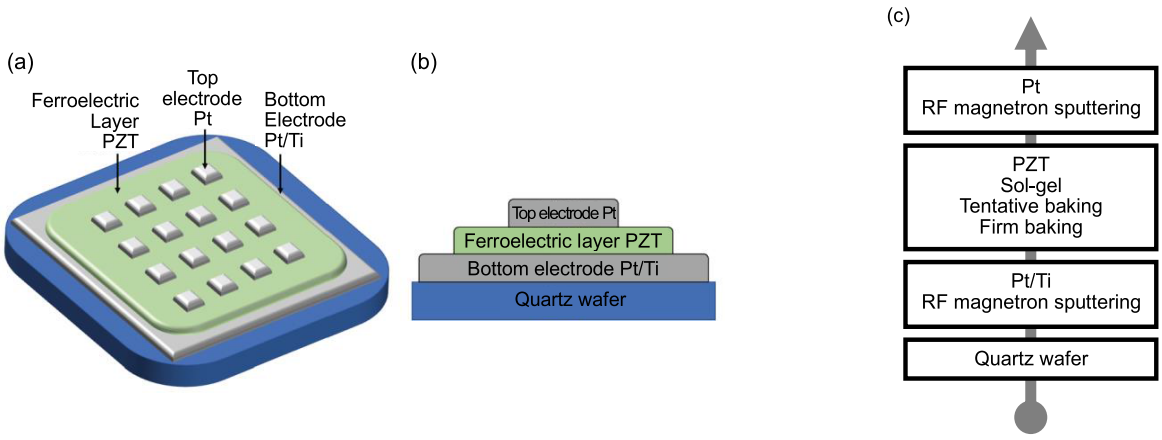

Fig. 1. Device structure. (a) Overall view. (b) Cross-sectional view. (c) Fabrication process. A ferroelectric layer is sandwiched between the bottom electrode and the top electrode. A PZT thin film is deposited using a sol–gel method, where a precursor solution is coated using a spin-coating method, tentatively baked, which are repeated to the target thickness, and firmly baked.

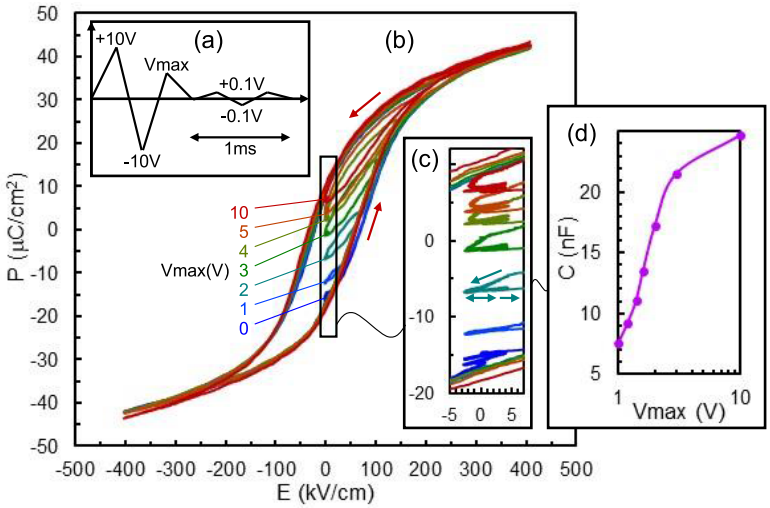

Fig. 2. Analog memcapacitor characteristic. (a) Applied voltage. (b) *P*–*E* characteristic. (c) Enlarged graph. (d) *C*-Vmax characteristic. First, positive and negative large voltages are consecutively applied to initialize the spontaneous polarization, next, varying Vmax is applied to obtain the analog memcapacitor characteristic, and finally, positive and negative small voltages are iteratively applied to evaluate it. It is found that the *P*–*E* characteristic is different depending on Vmax, and it should be noted that *C* is strongly dependent on Vmax.

Pt thin film are stacked and deposited on a quartz wafer using a radio frequency (RF) magnetron sputtering method as a bottom electrode. Next, a Pb(Zr, Ti)O_3 (PZT) thin film is deposited using a sol–gel method, where a precursor solution is coated using a spin-coating method as a ferroelectric layer, tentatively baked at 300 °C for 5 min, which is repeated to the required thickness, firmly baked at 700 °C for 1 min, and the final thickness of the PZT thin film is also 240 nm. Finally, a Pt thin film is deposited again using an RF magnetron sputtering method and patterned through a metal mask as top electrodes. Incidentally, it is intended that the ferroelectric memcapacitors can be integrated into Si CMOS chips because the fabrication temperature is not so high as to damage the underlying structure. The maximum fabrication temperature is 700 °C for the PZT in this article, and it is low enough to be integrated after the CMOS process and before the BEOL process. However, to avoid unfavorable contamination and be integrated easily, it is better to be integrated as the BEOL process, whose fabrication temperature must be below 500 °C. In this case, it is useful that the temperature can be lowered to 450 °C for PZT [8] and 500 °C for $Hf_{0.5}Zr_{0.5}O_2$ (HZO) [9], which can be alternatives to the ferroelectric layer.

III. Analog Memcapacitor Characteristic

The analog memcapacitor characteristic is shown in Fig. 2. The applied voltage is shown in Fig. 2(a). First, +10 V and −10 V are consecutively applied to initialize the spontaneous polarization. Next, Vmax varying from 1 to 10 V is applied to obtain the analog memcapacitor characteristic. Finally, +0.1 V and −0.1 V are iteratively applied to evaluate the analog memcapacitor characteristic. The polarization vs electric field (P–E) characteristic is measured using the Sawyer-Tower circuit [10]. The P–E characteristic and its enlarged graph are shown in Fig. 2(b) and (c). It is found that the P–E characteristic is different depending on Vmax. The capacitance (C) is calculated from the derivative of the P–E characteristic when + 0.1 V and −0.1 V are applied. The C-Vmax characteristic is shown in Fig. 2(d). It should be noted that

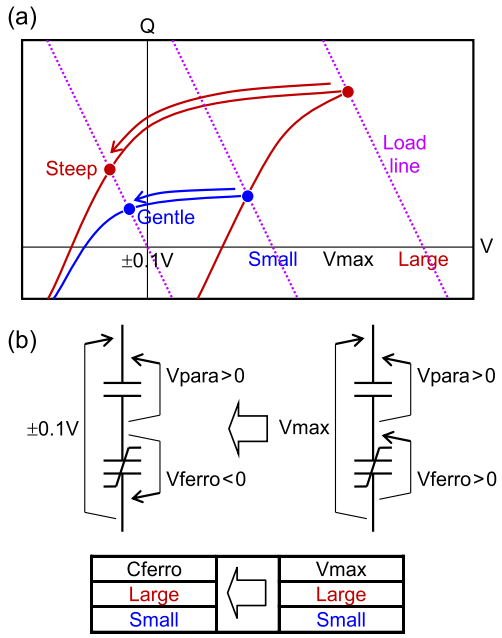

Fig. 3. Working principle. (a) Operating point analysis. (b) Equivalent circuit. The operating point analysis is done by Q–V characteristic and load line. When Vmax is large, the operating point is the red intersection point on the red major loop. On the other hand, when Vmax is small, the operating point is the blue intersection point on the blue minor loop.

C is strongly dependent on Vmax. Incidentally, parameter variations such as C are suppressed within a few percent in commercial products [11].

IV. Working Principle

The working principle is shown in Fig. 3. The operating point analysis is shown in Fig. 3(a), and the equivalent circuit is shown in Fig. 3(b). Here, as shown in Fig. 3(b), it is assumed that a parasitic capacitor is connected to the ferroelectric capacitor in series, and as shown in Fig. 3(a), the operating point analysis is done by the charge versus voltage (Q–V) characteristic, which corresponds to the P–E characteristic for the intrinsic property of the ferroelectric layer, and load line, which corresponds to $Q = CV$ for the parasitic capacitor. First, when Vmax is large, a large amount of the spontaneous polarization is aligned in the ferroelectric capacitor, and the operating point is the red intersection point for the red major loop of the Q–V characteristic and the purple load line. The internal voltage of the ferroelectric capacitor (Vferro) and that of the parasitic capacitor (Vpara) are both positive. Next, when ±0.1 V is applied, it moves to the left, and the slope is steep, which means that the ferroelectric capacitance (Cferro) is large, and C is also large. Vferro is negative, whereas Vpara is positive, and these absolute values are roughly the same. On the other hand, when Vmax is small, a small amount of the spontaneous polarization is aligned, and the operating point is the blue intersection point for the blue minor loop. Next, when ±0.1 V is applied, it also moves to the left, and the slope is gentle, which means that Cferro and C are small. These are the working principles of the analog memcapacitor.

V. Neuromorphic System

The spiking neuromorphic system is shown in Fig. 4. Circuit simulation is executed to prove that the spiking neuromorphic system dissipates extremely low energy consumption. The neuron circuit is shown in Fig. 4(a). The subtracted signals of the input spikes between the excitatory postsynaptic potential (EPSP) circuit and inhibitory postsynaptic potential (IPSP) circuit are accumulated, and once it reaches the threshold voltage, the spike generator generates an output spike. The Si CMOS technology is 180 nm, and the supply voltage is standard, 1.8 V, which is supplied only to the Si CMOS circuits and not to the analog memcapacitors. The synapse array is shown in Fig. 4(b). The analog memcapacitors (Cam) and switching transistors are implemented in each cell, where an electrode of Cam is charged through the switching transistors, whereas another electrode is connected to a common voltage. First, upload operation is done, where it is supposed that the word lines (WLs) are sequentially scanned, the common voltage of Cam (Vam0) is set to 0.65 V, and voltage waveforms with varying Vmax as shown in Fig. 2(a) added to Vam0 are applied as the individual voltage of Cam through bit lines (BL + and BL−), namely, ±10 V and Vmax from 1 to 10 V are consecutively applied to Cam, to make the analog capacitances to the desired ones. (We are not sure whether 10 V is available ON-chip, but some kinds of BEOL transistors are available for high-voltage applications at least [12].) This signifies that synaptic weights can be continuously controlled in infinity levels. It should be noted that only some parts of the existing circuits for inference operation are used. Next, an inference operation is done, where the multiplied signals of the input spikes from the WL and analog capacitance are transferred to BL + and BL− as output signals. The voltage charged to Cam (Vam) is optimized to a enough low voltage so that the applied voltage is under 0.1 V to avoid the unintentional disappearance of the analog memcapacitor characteristic, namely, the individual voltage of the Cam (Vam+) is set to Vam0 + 0.1 V and the initial voltage of the BL + and BL− (Vam−) is set to Vam0 − 0.1 V through the EPSP and IPSP circuit. The reason why Vam0 is optimized to 0.65 V is so that the applied voltage is under 0.1 V for Cam and simultaneously the supply voltage is 1.8 V for Si CMOS circuits. Although a memcapacitor model should be used in the circuit simulation, because there is no circuit model for the analog memcapacitors, a normal model for fixed capacitors is used, where the capacitances are set to the desired ones that the analog memcapacitors should have so that the fixed capacitors emulate the analog memcapacitors. The system architecture is shown in Fig. 4(c). A two-layer neural network is built, the input signals are 196, and the output signals are 10. The detailed information such as those on the peripheral circuits are described elsewhere [13], except that the analog memcapacitors and their characteristics are employed in this simulation.

The simulated waveform is shown in Fig. 5. Here, MNIST inference is tried, the label is “0” as an example, all output spikes are shown, and the spike numbers are counted. It is found that the spike number for output “0” is more than those for other outputs, which is the same as the label, and therefore the inference is successful. Incidentally, as shown in Fig. 5,

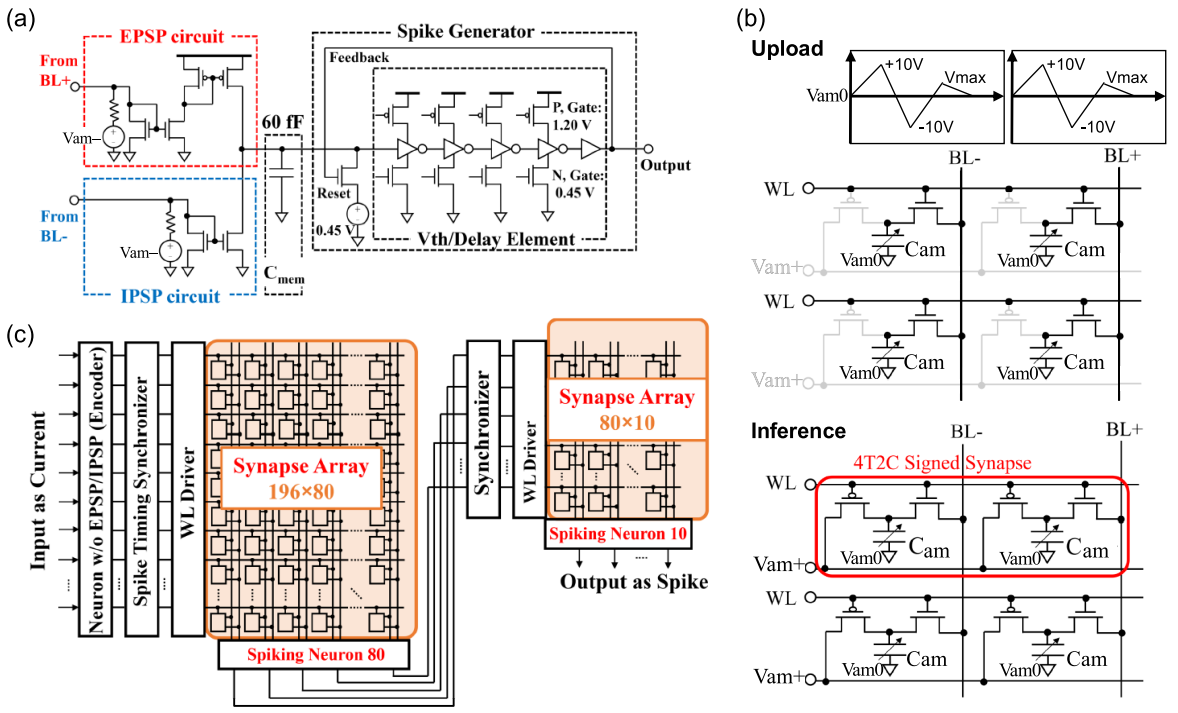

Fig. 4. Spiking neuromorphic system. (a) Neuron Circuit. (b) Synapse Array. (c) System Architecture [12]. Circuit simulation is executed to prove that the spiking neuromorphic system dissipates extremely low power consumption.

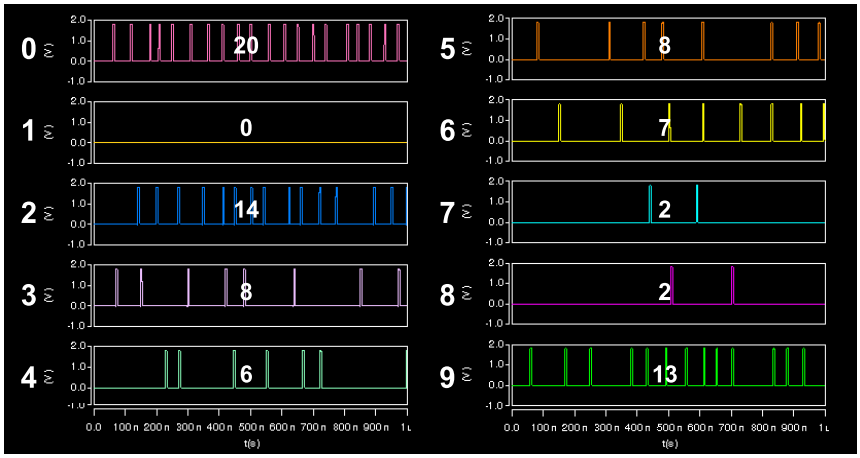

Fig. 5. Simulated waveforms. MNIST inference is tried, the label is “0” as an example, all output spikes are shown, and the spike numbers are counted. The spike number for output “0” is more than those for other outputs, and therefore the inference is successful.

one inference takes 1 μs to count the spike numbers, which is sufficiently speedy, although the operation voltage is as low as $\pm$0.1 V, in comparison with the inference time of 1.02 μs when the operation voltage is as high as 1.8 V [13].

The inference performance is shown in Fig. 6. It has been confirmed that the MNIST accuracy is 95%, which is acceptable in comparison with other similar systems. It should be particularly highlighted that the spiking neuromorphic system dissipates only 6.24 nJ/Inference, which is much lower than the other systems and surprising because the semiconductor technology is 180 nm, which is very rough. The reason why the neuromorphic system dissipates extremely low energy is because the memcapacitor is a capacitor, and the power consumption is not dissipated at all in principle, as aforementioned. Moreover, Vam is optimized to a low voltage, and spiking neuromorphic systems generally dissipate low energy consumption. The reason why the spiking neuromorphic system in this article has different energy efficiency from our previous paper [13] is that a lower voltage is used, which is enabled by demonstrating that the analog memcapacitor can work at the lower voltage in this article.

The accuracy tolerance against the capacitance variation is shown in Fig. 7. Here, random variation is added to Cam. It is found that the MNIST accuracy is maintained when the capacitance variation is suppressed below 10%. This excellence in accuracy tolerance is attributed to the inherent nature of

	[14]	[15]	[16]	This paper
Type	Digital	Digital	SRAM	Analog memC
Technology (nm)	40	65	40	180
MNIST Accuracy (%)	91.7	97	94.73	95
Energy /Inference (nJ)	308	74	202.3	6.24

Fig. 6. Inference performance. The spiking neuromorphic system in this study dissipates only 6.24 nJ/Inference, which is much lower than the other similar systems and surprising because the semiconductor technology is 180 nm, which is very rough.

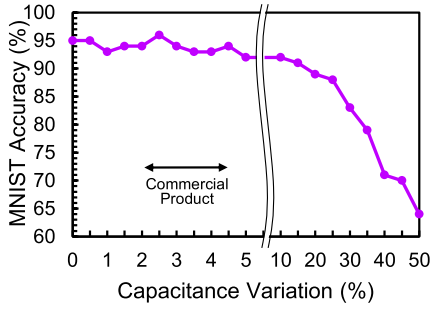

Fig. 7. Accuracy tolerance against the capacitance variation. The MNIST accuracy is maintained when the capacitance variation is suppressed below 10%. This excellence in accuracy tolerance is attributed to the inherent nature of robustness in neuromorphic systems [16].

robustness in neuromorphic systems [17], which play specific functions in the entire system. Therefore, the capacitance variation does not matter because it is suppressed within a few percent in commercial products, as aforementioned.

The memcapacitor area is estimated as follows. As shown in Fig. 2(d), the maximum C is roughly 25 nF/mm^2, and during the upload operation, the maximum C is assumed to be at most 100 fF. Therefore, the memcapacitor area is estimated at 4 μm^2, which is sufficiently small to be integrated on synapse arrays in Si CMOS chips with 180-nm technology. Moreover, if the semiconductor technology is miniaturized, the memcapacitors are also miniaturized with the same ratio based on the scaling rule, the area is still sufficiently small to be integrated into the chips. It should be noted that our claim is not that the area of the synapse is small compared to the memristor-based synapses, but that the area is sufficiently small to be integrated into synapse arrays in Si CMOS chips. The memcapacitor area is generally larger than the memristor area. The advantage is not that the memcapacitor area is smaller than the memristor area, but that the power consumption is remarkably reduced.

VI. Conclusion

An analog memcapacitor has been created by a ferroelectric capacitor. Since the memcapacitor is a capacitor, the power consumption is not dissipated at all in principle. The device structure is that a ferroelectric layer is sandwiched between the bottom electrode and top electrodes. It was found that the analog memcapacitor characteristic is realized, namely, varying Vmax is applied, and the capacitance is strongly dependent on it. The working principle can be explained by the operating point analysis for the intrinsic property of the ferroelectric layer. If the memcapacitors are implemented in neuromorphic systems, it is expected that the power consumption will be remarkably reduced. It has been simulated that the spiking neuromorphic system dissipates only 6.24 nJ/Inference for MNIST inference with acceptable accuracy, which is much lower than other systems.

Acknowledgment

The authors would like to thank Dr. Toshihiro Doi of Mitsubishi Materials Corporation.

References

[1] L. O. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, pp. 507–519, 1971, doi: 10.1109/TCT.1971.1083337.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[3] D. Makioka, S. Shiomi, and M. Kimura, "Ga-Sn-O thin-film memristor and analog plasticity characteristic," *IEEE J. Electron Devices Soc.*, vol. 11, pp. 174–178, 2023, doi: 10.1109/JEDS.2023.3253465.

[4] Z. Yin, H. Tian, G. Chen, and L. O. Chua, "What are memristor, memcapacitor, and meminductor?" *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 4, pp. 402–406, Apr. 2015, doi: 10.1109/TCSII.2014.2387653.

[5] M. Kimura et al., "Neuromorphic system using memcapacitors and autonomous local learning," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 34, no. 5, pp. 2366–2373, May 2023, doi: 10.1109/TNNLS.2021.3106566.

[6] R. Oshio, T. Sugahara, A. Sawada, M. Kimura, R. Zhang, and Y. Nakashima, "A memcapacitive spiking neural network with circuit nonlinearity-aware training," in *Proc. IEEE Symp. Low-Power High-Speed Chips (COOL CHIPS)*, Apr. 2022, pp. 1–6.

[7] T. Doi, T. Noguchi, J. Fuji, N. Soyama, and H. Sakurai, "The orientation and grain texture effect on life time reliability of sol–gel derived $PbZr_{0.52}Ti_{0.48}O_3$ films," *Jpn. J. Appl. Phys.*, vol. 51, no. 9S1, Sep. 2012, Art. no. 09LA15.

[8] L. Song, S. Glinsek, and E. Defay, "Toward low-temperature processing of lead zirconate titanate thin films: Advances, strategies, and applications," *Appl. Phys. Rev.*, vol. 8, no. 4, Dec. 2021, Art. no. 041315, doi: 10.1063/5.0054004.

[9] K. Tahara et al., "Strategy toward HZO BEOL-FeRAM with low-voltage operation (= 1.2 V), low process temperature, and high endurance by thickness scaling," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.

[10] C. B. Sawyer and C. H. Tower, "Rochelle salt as a dielectric," *Phys. Rev.*, vol. 35, no. 3, pp. 269–273, Feb. 1930.

[11] A. Nishiyama, "Mass production of 8 PZT thin film by sol-gel deposition," in *Proc. PiezoMEMS*, Oct. 2014.

[12] H. Sunamura et al., "High-voltage complementary BEOL-FETs on Cu interconnects using N-type IGZO and P-type SnO dual oxide semiconductor channels," in *Proc. Symp. VLSI Technol.*, Jun. 2013, pp. T250–T251.

[13] R. Oshio, T. Sugahara, A. Sawada, M. Kimura, R. Zhang, and Y. Nakashima, "A compressed spiking neural network onto memcapacitive in-memory computing array," *IEEE Micro*, vol. 44, no. 1, pp. 8–16, Jan./Feb. 2024, doi: 10.1109/MM.2023.3285529.

[14] J. Stuijt, M. Sifalakis, A. Yousefzadeh, and F. Corradi, "μBrain: An event-driven and fully synthesizable architecture for spiking neural networks," *Frontiers Neurosci.*, vol. 15, May 2021, Art. no. 664208, doi: 10.3389/fnins.2021.664208.

[15] D.-A. Nguyen, X.-T. Tran, K. N. Dang, and F. Iacopi, "A low-power, high-accuracy with fully on-chip ternary weight hardware architecture for deep spiking neural networks," *Microprocessors Microsystems*, vol. 90, Apr. 2022, Art. no. 104458, doi: 10.1016/j.micpro.2022.104458.

[16] C. Liu, Z. Xuan, and Y. Kang, "A 40-nm 202.3 nJ/classification neuromorphic architecture employing in-SRAM charge-domain compute," in *Proc. IEEE ASICON*, Oct. 2021, pp. 1–4.

[17] C. Mead, "Neuromorphic electronic systems," *Proc. IEEE*, vol. 78, no. 10, pp. 1629–1636, Oct. 1990, doi: 10.1109/5.58356.