

2022-1-60-051

Assignment - B

(a)

Device name: HP LAPTOP - MSJH8KQO

CPU: AMD Ryzen 7 5700U featuring Radeon Graphics

Architecture: Constructed on the AMD Zen 2 architecture utilizing 7 nm process technology.

Cores / Threads: Comprising 8 cores and 16 threads

Base clock frequency:

1. 80 GHz (This denotes the fundamental operating frequency of the operation).

Maximum Boost Clock:

Reaching upto 4.3 GHz

Round 1 Ques

Cache :

L1 Cache : 512 KB

L2 Cache : 4 MB

L3 Cache : 8 MB

Integrated Graphics : Equipped with Radeon Vega

8 Graphics, proficient in managing light gaming.

media, play back.

Compute Units : 8 Graphics clock frequency.

Capable of reaching up to 1.9 GHz.

GPU Architecture : Vega thermal design power.

TDP : 15 W

Installed RAM (main memory) :

8.00 GB (7.33 GB accessible)

Type: It is highly probable that, the memory type is DDR4, operating at a frequency of 3200 MHz on an equivalent rate.

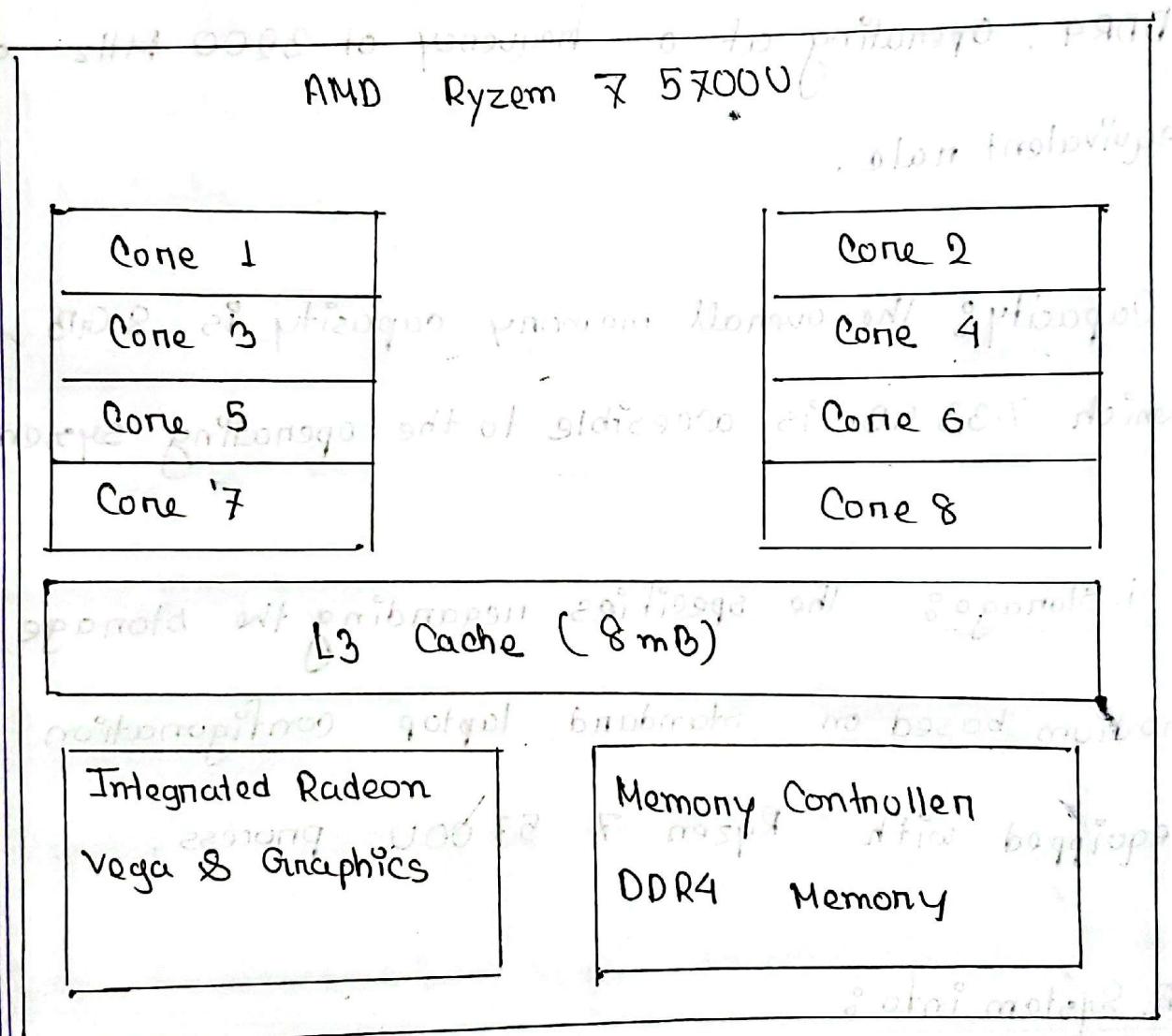
Capacity: The overall memory capacity is 8 GB, of which 7.33 GB is accessible to the operating system.

4. Storage: The specifies regarding the storage medium based on standard laptop configuration equipped with Ryzen 7 5700U processor.

5. System info:

The device operates on a 64-bit architecture (X64-based processor) signifying its capacity to accommodate larger memory address and deliver superior performance in comparison to 32 bit.

Block diagram of AMD Ryzen 7 5700U



* instruction set details :

- * X86 - 64 - ISA : Standard 64 bit instruction set architecture used in modern processors.
- * SSE : For vectorized operations on multiple data points.
- * AVX2 : 256-bit wide vector operations for floating-point calculations.
- * FMA : Single instructions that performs both multiplication and addition.
- * AMD-V : Virtualization technology that allows the processor to efficiently run multiple machine.

* Pipelining Details :

- i) The Ryzen 7 5700U implements a superclean pipeline, allowing multiple instruction to be fetched and decoded.

1) out-of-order execution allows the processor

to avoid bottlenecks and hazards.

3) The processor has deep pipeline that allows

higher speeds, improving performance.

~~* Multiple Issue~~

1) The Ryzen 5 5700G is capable of issuing

multiple instructions per clock cycle.

2) Each core can handle up to 4 instructions

per clock cycle.

~~* Cache memory details~~

L1 cache: 64 kB per core

L2 cache: 512 kB per core

L3 cache: 8 MB shared across all cores.

Processor has 16 cores and 32 threads.

16 GB RAM

* Bus System:

The Ryzen 7 5700U utilizes the Infinity fabric architecture to connect CPU Cores, GPU, memory controllers and I/O.

* Interrupts:

The processor supports maskable and non-maskable interrupts (NMIs).

* I/O:

- * PCIe for high-speed peripheral connection.
- * USB 3.1 / 3.2 for fast data transfer.
- * SATA for traditional hard drive connection.
- * HDMI / Display for display output.

* Direct Memory Access (DMA):

The Ryzen processor features a DMA controller, allowing peripheral like network cards or disk drives to transfer data directly to and from memory without involving the CPU.

(b)

The Samsung Galaxy S0+ is powered by the Qualcomm Snapdragon 675 processor. This processor is part of Qualcomm's mid-range 600 series.

Processor Specifications

Chipset: Qualcomm SDM675 Snapdragon 675 (4nm)

CPU: * Octa-Core

* 2x 2.0 GHz Kryo 460 Gold

* 6x 1.76 Hz 460 Silver

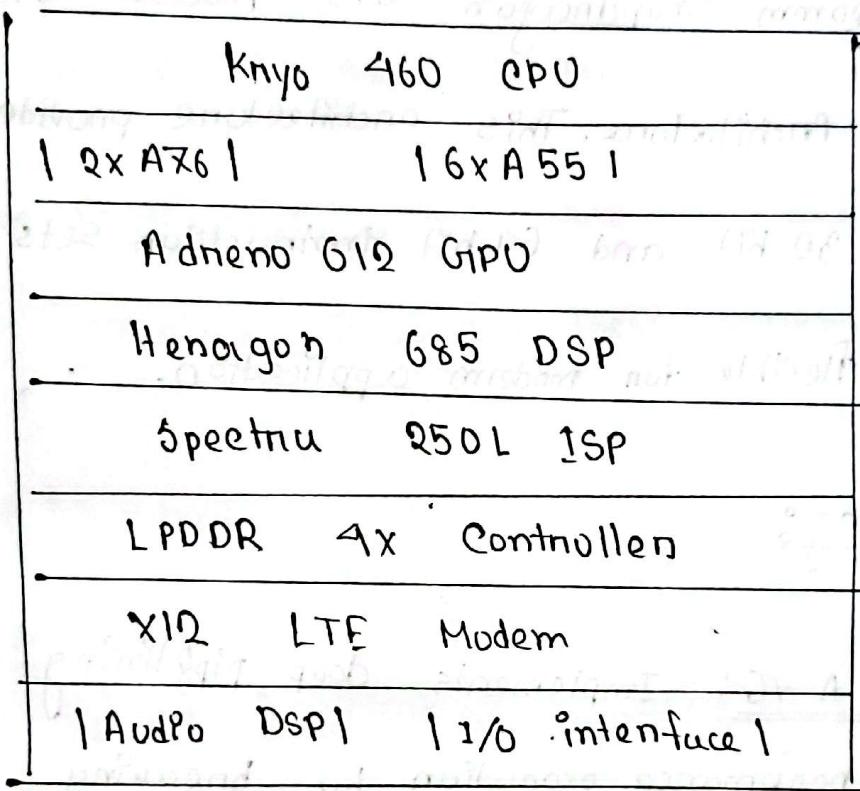
GPU: Adreno 612

Main Memory: 8GB of RAM

Storage: 128 GB of internal storage

SD Card (Upto 1TB)

* Block diagram :



* Processor specification :

Cone Architecture : ARM Cortex-A76 and Cortex-A55

Cores.

Configuration : 8 cores (2x Cortex-A76 @ 2.0 GHz for

high performance.

* ISA related info:

The Qualcomm Snapdragon 675 processor uses the ARM-8-A architecture. This architecture provides support for both 32-bit and 64-bit instruction sets, making it highly flexible for modern application.

* Pipelining:

Context A76: Implements deep pipelining, allowing for high-performance execution by breaking instruction into smaller stages.

Context A55:

Small pipeline (8-10) stages, focusing on energy-efficient execution.

*Multiple issue:

- 1) Superscalar architecture with multiple issue out-of-order execution for the Cortex A76 cores.
- 2) The Cortex-A55 cores are in-order processors, so no multiple issue for these cores.

*Cache Memory:

L1 Cache:

32KB instruction cache

32KB data cache, per core.

L2 Cache:

512 KB shared L2 cache for the 2 cortex-

A76 cores.

256 KB shared L2 caches for the cortex-

A55 cores.

L3 cache:

16-32 MB system level cache shared across the entire CPU cluster, improving data sharing among the cores.

Bus system:

AXI Bus: The snapdragon 675 uses the advanced interface (AXI) bus protocol to connect the various components like CPU, GPU and memory controller.

Network on chip: Manage data flow both within the SoC by efficiently connecting the different components.

Interrupts:

The ARM architecture supports both FIQ and IRQ for handling hardware interrupts.

The ~~then~~ snapdragon 675 use GIC to manage
interrupts. in a flexible manner.

I/O:

USB: Supports USB 3.1 for fast data transfer.

Display interface: Support 1080p full HD display.

I/O Controller:

The snapdragon 675 SOC support
multiple I/O operation such as USB, I2C, UART
and SPI.

DMA (Direct Memory access):

DMA controller is available
within the snapdragon 675 SOC allowing peripherals to
directly read from or write to the memory without
burdening the CPU. It helps fast data transfer.

application of IoT (C) IoT application part 3

One of the recent and popular embedded

microcontroller is the ESP 32 by Espressif

systems. It is widely used in IoT (Internet of

Things) application due to its low costs,

integrated WiFi, Bluetooth and robust performance.

* Application of the ESP32:

1) IOT Devices: Smart home devices, sensors and actuators.

2) Wearable devices: Smart watches, fitness trackers and health monitoring devices.

3) Home automation: Controlling appliances like fans, lights and security systems over WiFi.

4) Industrial Automation: Data logging, process control

and remote monitoring.

5) Wireless Sensors networks: Using Bluetooth or

WiFi sensors communication in environment on industrial monitoring system.

Programming the ESP32 microcontroller:

Using Arduino IDE

Step 01: Install Arduino IDE

Step 02: Install the ESP32 Board support in

Arduino IDE

Step 03: Select the ESP32 Board

Step 04: Connect ESP32 to my computer

Step 05: Example code

```
// Define the LED pin number  
int ledPin;  
void setup () {  
    // initialize the digital pin as an output  
    Pin Mode (led Pin OUTPUT);  
}  
void loop () {  
    digital write (ledPin , HIGH);  
    delay (1000);  
    digital write (ledPin , LOW);  
    delay (1000);  
}
```

Step 06: Upload the code