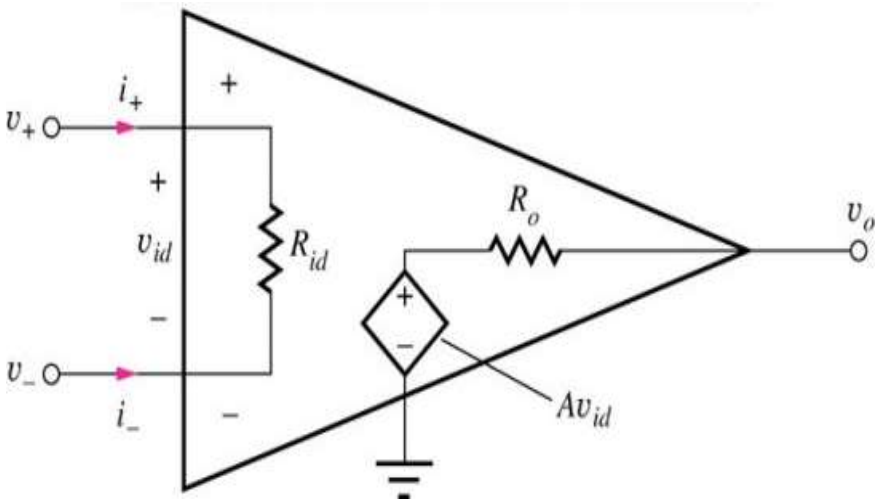
Operational Amplifiers and Applications

Differential Amplifier Model: Basic



Represented by:

A = open-circuit voltage gain

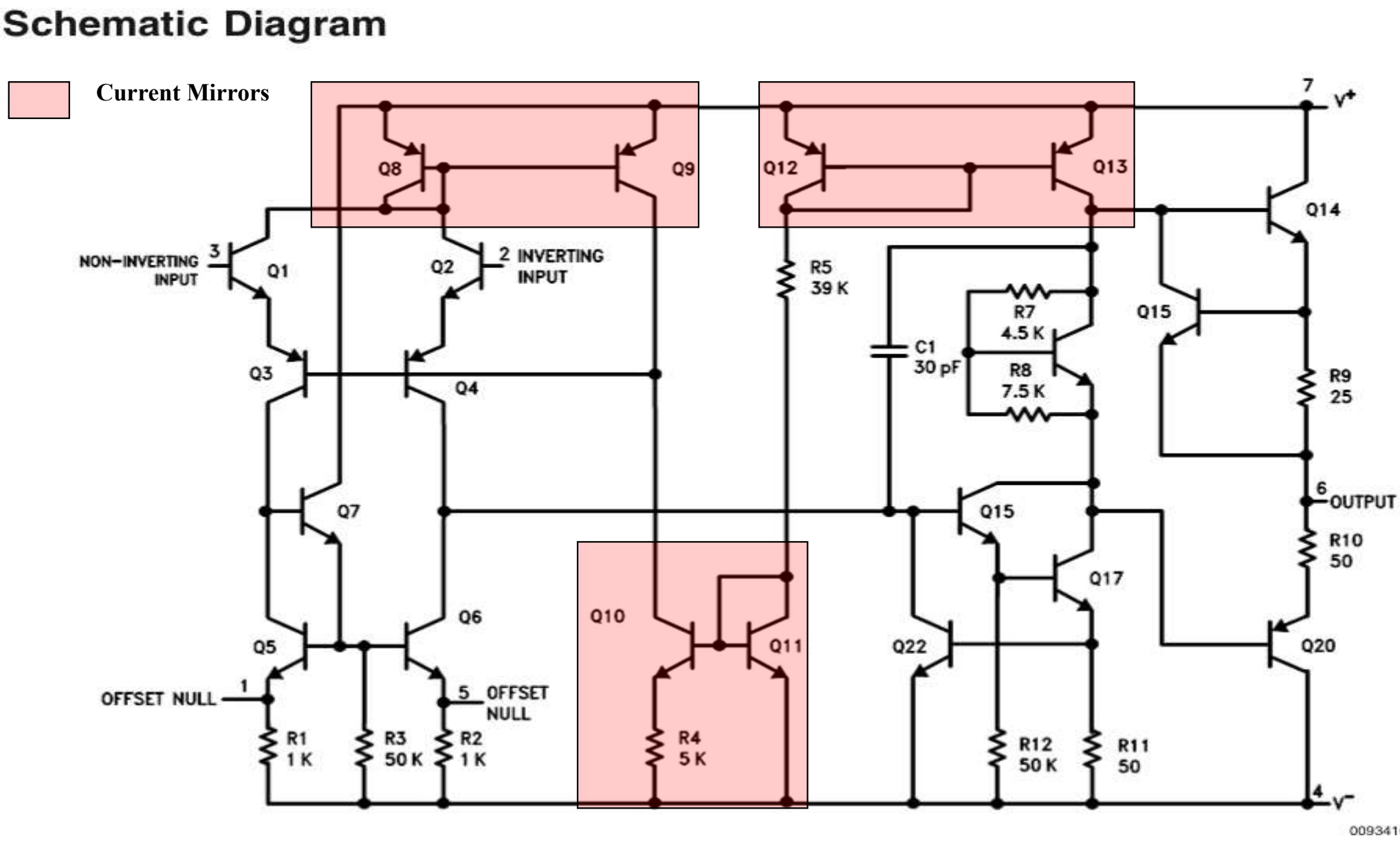
$v_{id} = (v^+ - v^-)$ = differential input signal voltage

R_{id} = amplifier input resistance

R_o = amplifier output resistance

The signal developed at the amplifier output is in phase with the voltage applied at the + input (non-inverting) terminal and 180° out of phase with that applied at the - input (inverting) terminal.

LM741 Operational Amplifier: Circuit Architecture



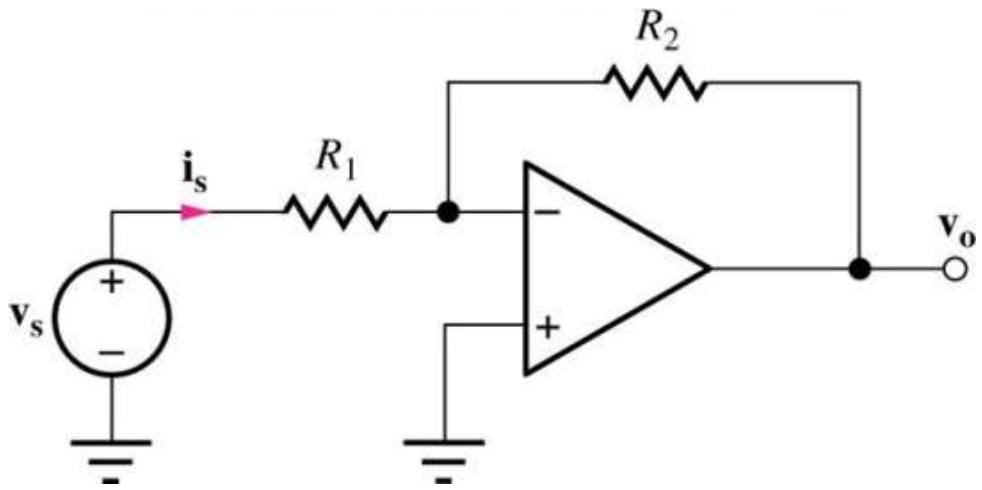
Ideal Operational Amplifier

- The "ideal" op amp is a special case of the ideal differential amplifier with infinite gain, infinite R_{id} and zero R_o .

$$v_{id} = \frac{v_o}{A} \quad \text{and} \quad \lim_{A \to \infty} v_{id} = 0$$

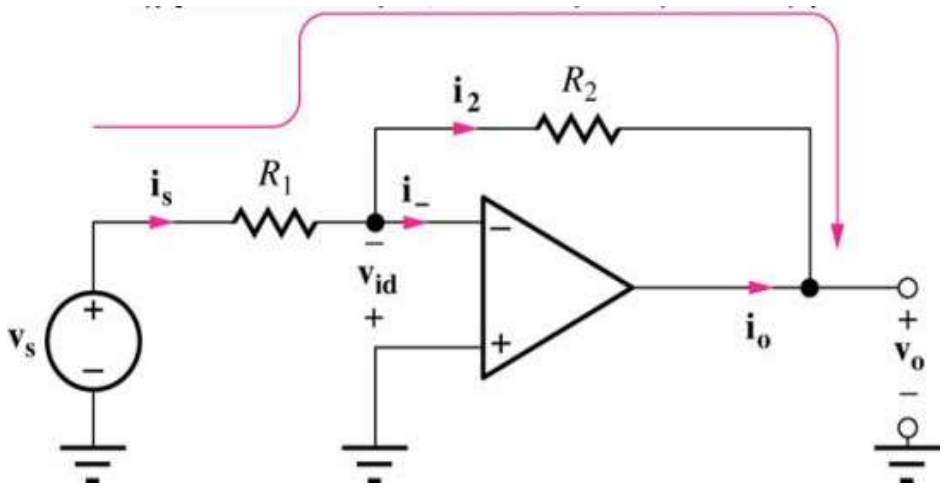
  - If A is infinite, v_{id} is zero for any finite output voltage.
  - Infinite input resistance R_{id} forces input currents i_+ and i_- to be zero.
- The ideal op amp operates with the following assumptions:
  - It has infinite common-mode rejection, power supply rejection, open-loop bandwidth, output voltage range, output current capability and slew rate
  - It also has zero output resistance, input-bias currents, input-offset current, and input-offset voltage.

The Inverting Amplifier: Configuration



- The positive input is grounded.
- A "feedback network" composed of resistors R_1 and R_2 is connected between the inverting input, signal source and amplifier output node, respectively.

Inverting Amplifier:Voltage Gain



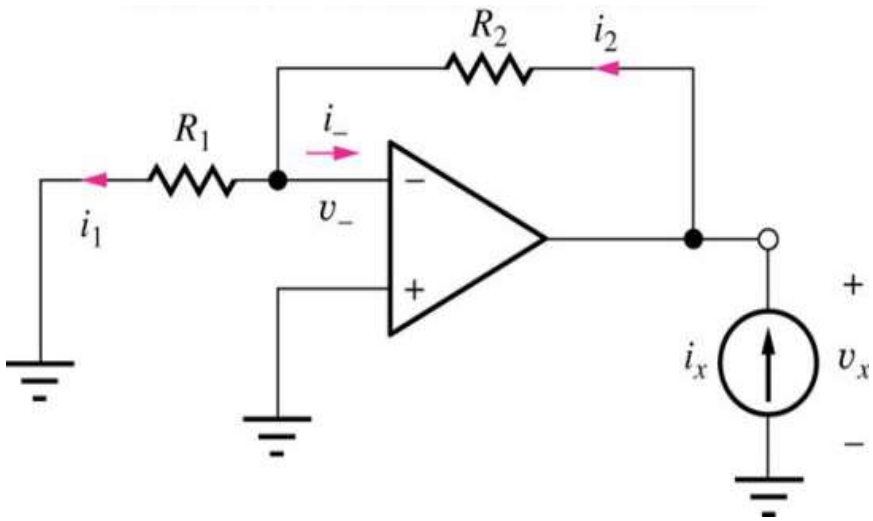
$$v_s - i_s R_1 - i_2 R_2 - v_o = 0$$

But $i_s = i_2$ and $v_- = 0$ (since $v_{id} = v_+ - v_- = 0$)

$$\therefore i_s = \frac{v_s}{R_1} \quad \text{and} \quad A_v = \frac{v_o}{v_s} = -\frac{R_2}{R_1}$$

- The negative voltage gain implies that there is a 180^0 phase shift between both dc and sinusoidal input and output signals.
- The gain magnitude can be greater than 1 if $R_2 > R_1$
- The gain magnitude can be less than 1 if $R_1 > R_2$
- The inverting input of the op amp is at ground potential (although it is not connected directly to ground) and is said to be at **virtual ground.**

Inverting Amplifier: Input and Output Resistances



R_{out} is found by applying a test current (or voltage) source to the amplifier output and determining the voltage (or current) after turning off all independent sources. Hence, $v_s = 0$

$$v_x = i_2 R_2 + i_1 R_1$$

But $i_1 = i_2$

$$\therefore v_x = i_1 (R_2 + R_1)$$

$$R_{in} = \frac{v_s}{i_s} = R_1 \quad \text{since } v_- = 0$$

Since $v_- = 0$, $i_1 = 0$. Therefore $v_x = 0$ irrespective of the value of i_x .

$$\therefore R_{out} = 0$$

Inverting Amplifier: Example

- **Problem**: Design an inverting amplifier
- **Given Data**: A_v= 20 dB, R_{in} = 20kΩ,
- **Assumptions:** Ideal op amp
- **Analysis**: Input resistance is controlled by R_1 and voltage gain is set by R_2 / R_1.

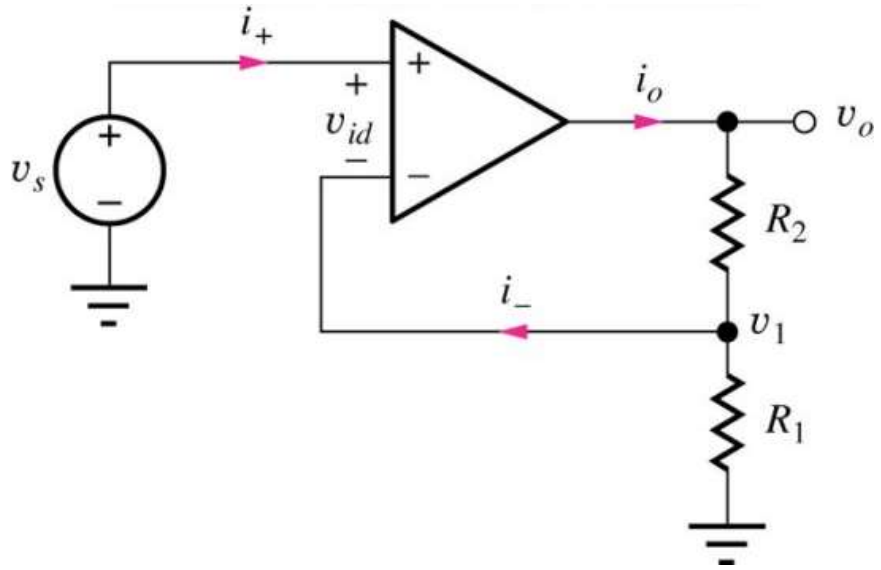
$$A_v(dB) = 20\log_{10}(|A_v|), \quad \therefore |A_v| = 10^{40\text{dB}/20\text{dB}} = 100 \quad \text{and } A_v = -100$$

A minus sign is added since the amplifier is inverting.

$$R_1 = R_{in} = 20\text{k}\Omega$$

$$A_v = -\frac{R_2}{R_1} \Rightarrow R_2 = 100R_1 = 2M\Omega$$

The Non-inverting Amplifier: Configuration



- The input signal is applied to the non-inverting input terminal.
- A portion of the output signal is fed back to the negative input terminal.
- Analysis is done by relating the voltage at v_1 to input voltage v_s and output voltage v_o .

Non-inverting Amplifier: Voltage Gain, Input Resistance and Output Resistance

Since $i_-=0$ $\quad v_1 = v_o \dfrac{R_1}{R_1+R_2}$ $\quad$ and $\quad v_s - v_{id} = v_1$

But $v_{id}=0$ $\quad \therefore v_s = v_1$

$$v_o = v_s \frac{R_1+R_2}{R_1}$$

$$\therefore A_v = \frac{v_o}{v_s} = \frac{R_1+R_2}{R_1} = 1+\frac{R_2}{R_1}$$

Since $i_+=0$ $\quad R_{in} = \dfrac{v_s}{i_+} = \infty$

R_{out} is found by applying a test current source to the amplifier output after setting $v_s = 0$. It is identical to the output resistance of the inverting amplifier i.e. $R_{out} = 0$.

Non-inverting Amplifier: Example

- **Problem**: Determine the output voltage and current for the given non-inverting amplifier.
- **Given Data**: $R_1 = 3\text{k}\Omega$, $R_2 = 43\text{k}\Omega$, $v_s = +0.1$ V
- **Assumptions:** Ideal op amp
- **Analysis**:

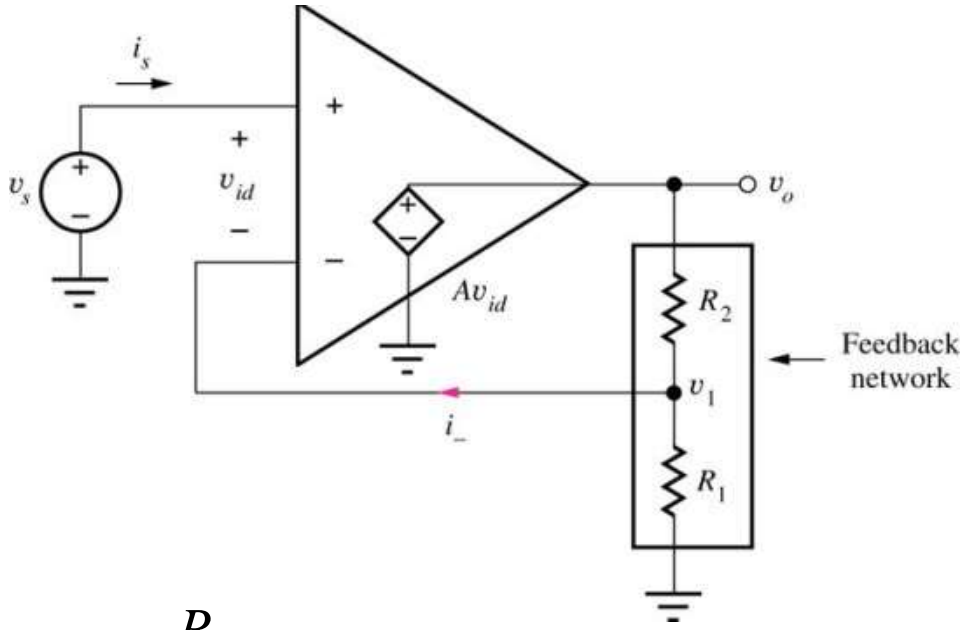
$$A_v = 1 + \frac{R_2}{R_1} = 1 + \frac{43\text{k}\Omega}{3\text{k}\Omega} = 15.3$$

$$\text{v}_\text{o} = A_v \text{v}_\text{s} = (15.3)(0.1\text{V}) = 1.53\text{V}$$

Since $i_- = 0$,

$$\text{i}_\text{o} = \frac{\text{v}_\text{o}}{R_2 + R_1} = \frac{1.53\text{V}}{43\text{k}\Omega + 3\text{k}\Omega} = 33.3\mu\text{A}$$

Finite Open-loop Gain and Gain Error



$$v_o = Av_{id} = A(v_s - v_1) = A(v_s - \beta v_o)$$

$$A_v = \frac{v_o}{v_s} = \frac{A}{1 + A\beta}$$

$A\beta$ is called loop gain.

For $A\beta >> 1$,

$$A_v \cong \frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

This is the "ideal" voltage gain of the amplifier. If $A\beta$ is <u>not</u> >>1, there will be "Gain Error".

$$v_1 = \frac{R_1}{R_1 + R_2} v_o = \beta v_o$$

$$\beta = \frac{R_1}{R_1 + R_2}$$ is called the **feedback factor.**

Gain Error

- Gain Error is given by

GE = (ideal gain) - (actual gain)

For the non-inverting amplifier,

$$GE = \frac{1}{\beta} - \frac{A}{1+A\beta} = \frac{1}{\beta(1+A\beta)}$$

- Gain error is also expressed as a fractional or percentage error.

$$FGE = \frac{\frac{1}{\beta} - \frac{A}{1+A\beta}}{\frac{1}{\beta}} = \frac{1}{1+A\beta} \cong \frac{1}{A\beta}$$

$$PGE \cong \frac{1}{A\beta} \times 100\%$$

Gain Error: Example

- **Problem**: Find ideal and actual gain and gain error in percent
- **Given data**: Closed-loop gain of 100,000, open-loop gain of 1,000,000.
- **Approach**: The amplifier is designed to give ideal gain and deviations from the ideal case have to be determined. Hence, $\beta = \frac{1}{10^5}$

  .

  Note: R_1 and R_2 aren't designed to compensate for the finite open-loop gain of the amplifier.
- **Analysis**: $A_v = \frac{A}{1+A\beta} = \frac{10^6}{1+\frac{10^6}{10^5}} = 9.09x10^4$

$$\text{PGE} = \frac{10^5 - 9.09x10^4}{10^5} \times 100\% = 9.09\%$$

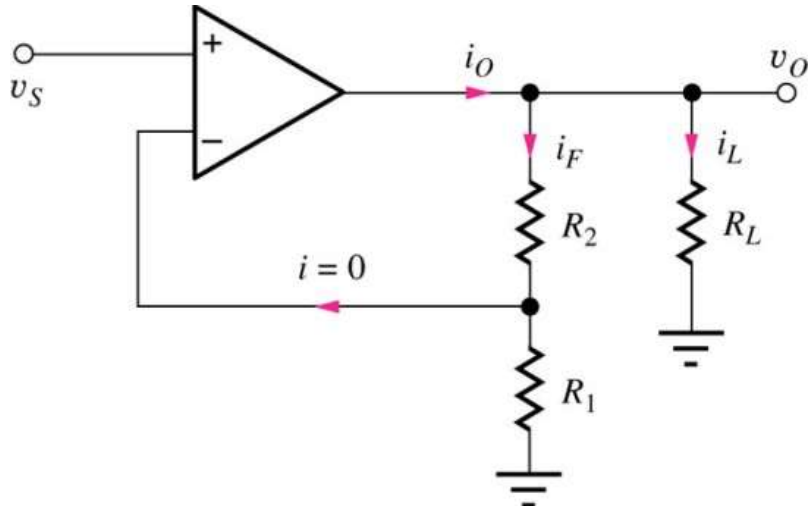
Output Voltage and Current Limits

Practical op amps have limited output voltage and current ranges.

Voltage: Usually limited to a few volts less than power supply span.

Current: Limited by additional circuits (to limit power dissipation or protect against accidental short circuits).

The current limit is frequently specified in terms of the minimum load resistance that the amplifier can drive with a given output voltage swing. Eg: $|i_o| = \frac{5\text{V}}{500\Omega} = 10\text{mA}$



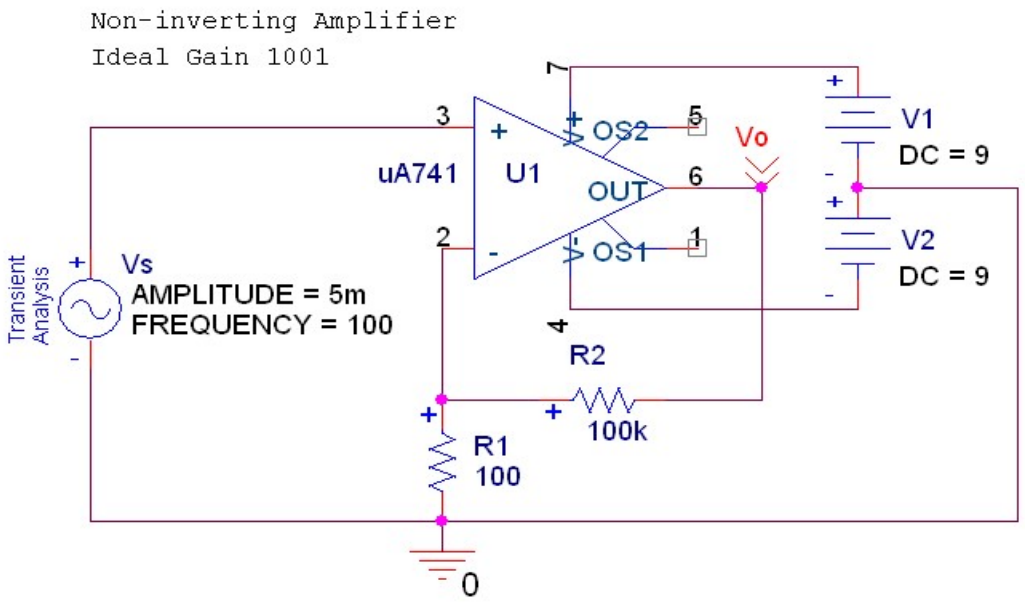
$$i_o = i_L + i_F = \frac{v_o}{R_L} + \frac{v_o}{R_2 + R_1} = \frac{v_o}{R_{EQ}}$$

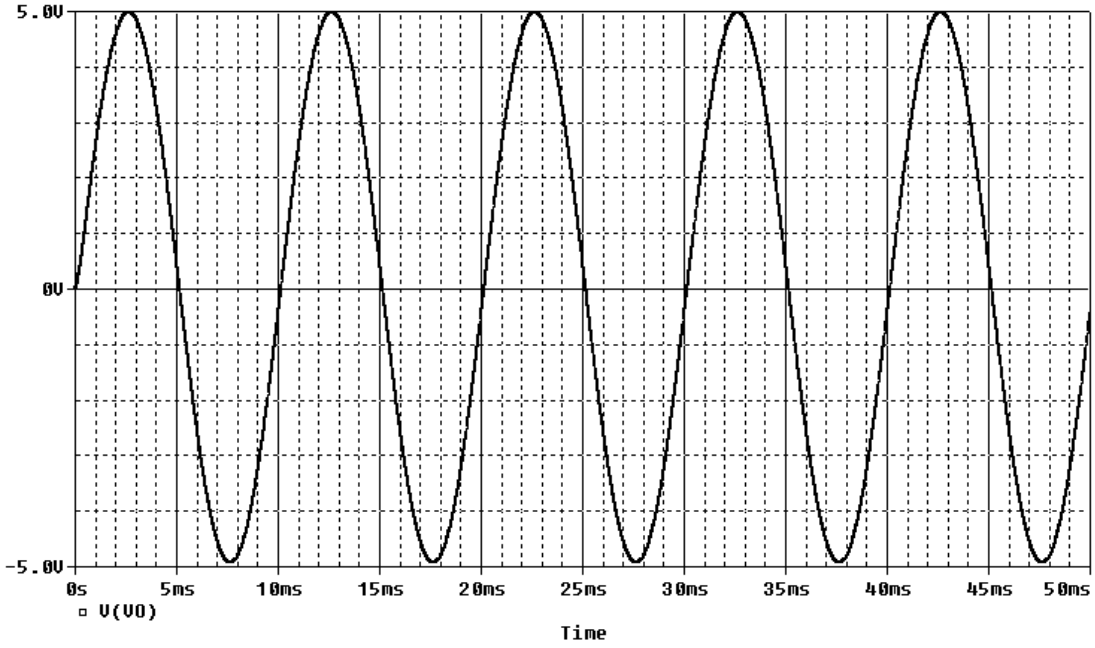
$$R_{EQ} = R_L \| (R_1 + R_2)$$

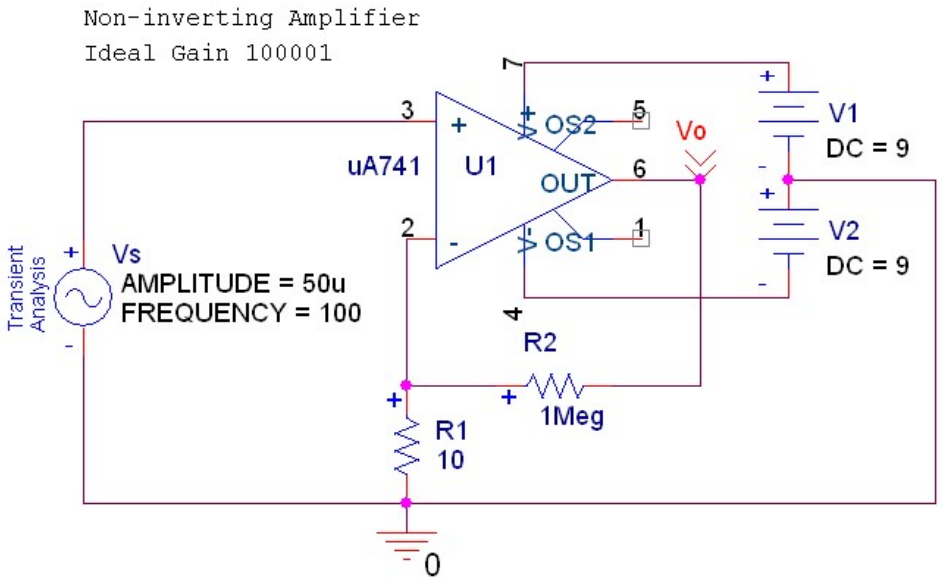
For the inverting amplifier,

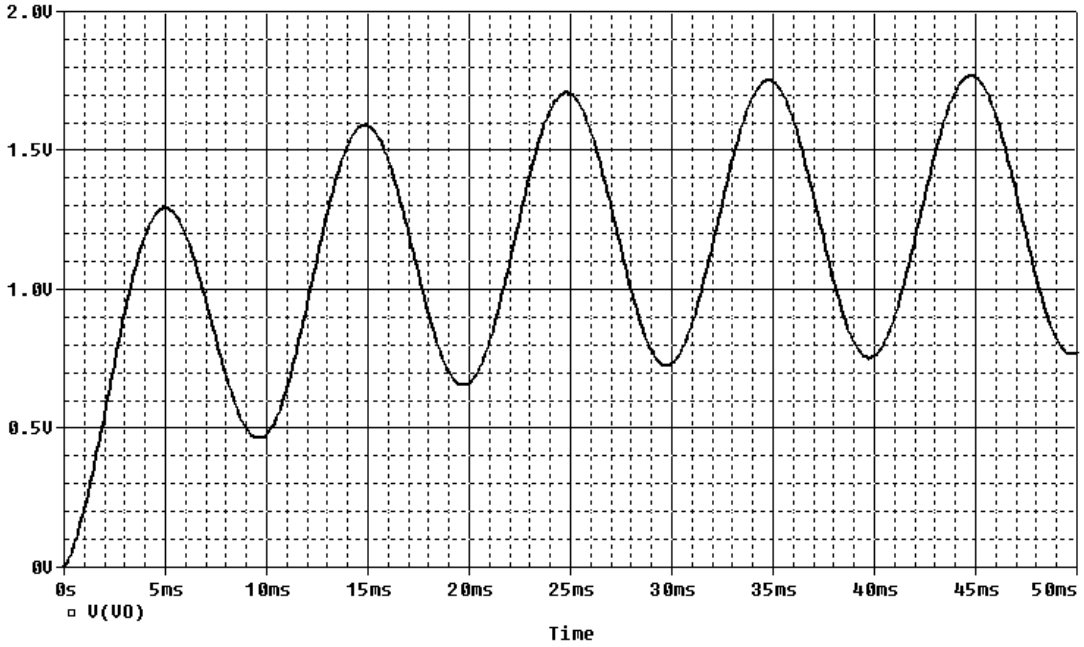
$$R_{EQ} = R_L \| R_2$$

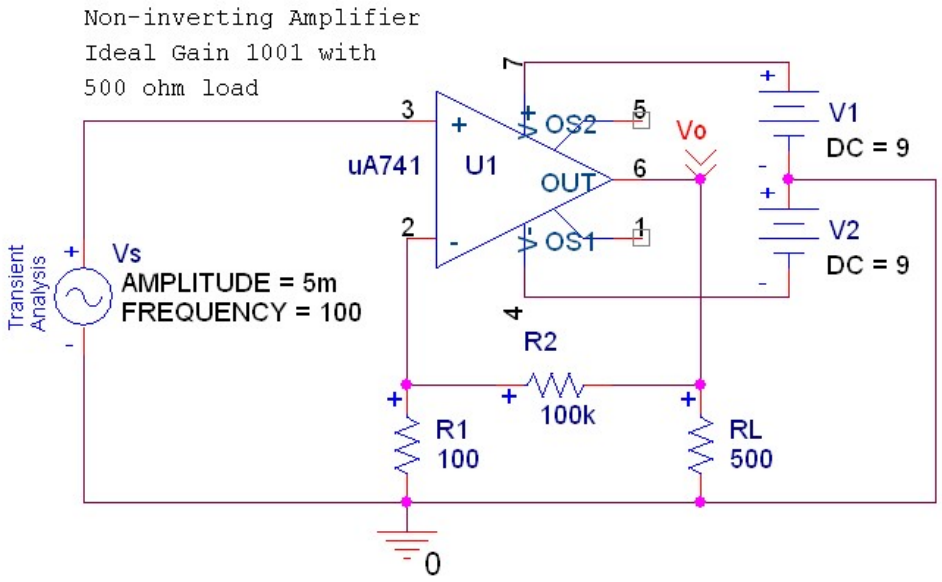
Example PSpice Simulations of Non-inverting Amplifier Circuits

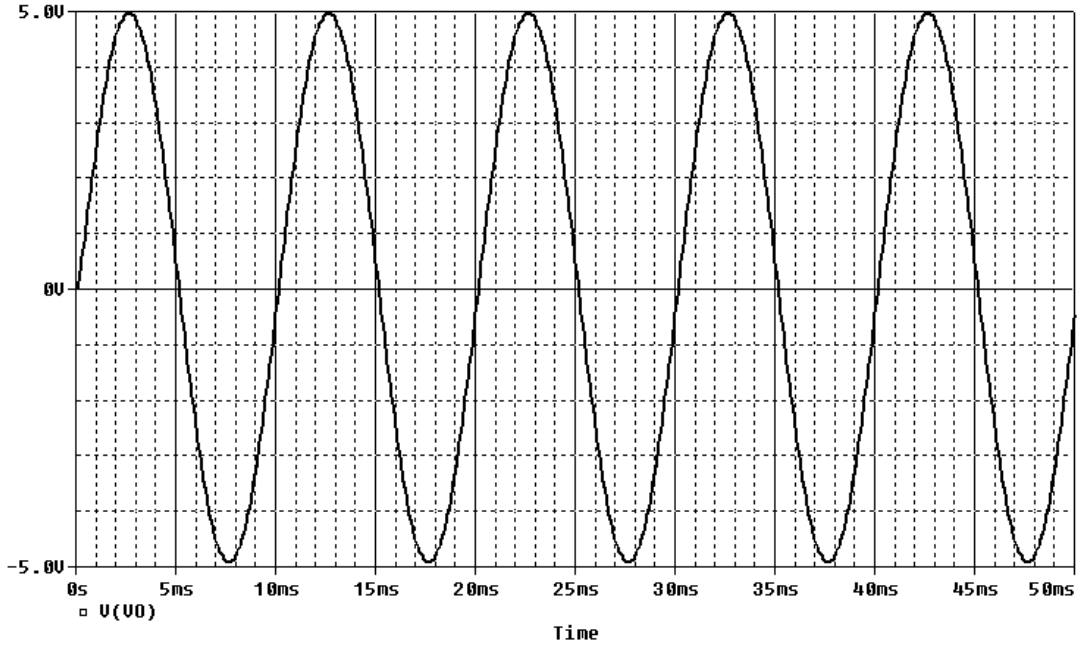

Non-inverting Amplifier
Ideal Gain 1001
uA741
U1
OS2
OS1
OUT
Vo
V1
DC = 9
V2
DC = 9
Vs
AMPLITUDE = 5m
FREQUENCY = 100
Transient Analysis
R2
100k
R1
100
0

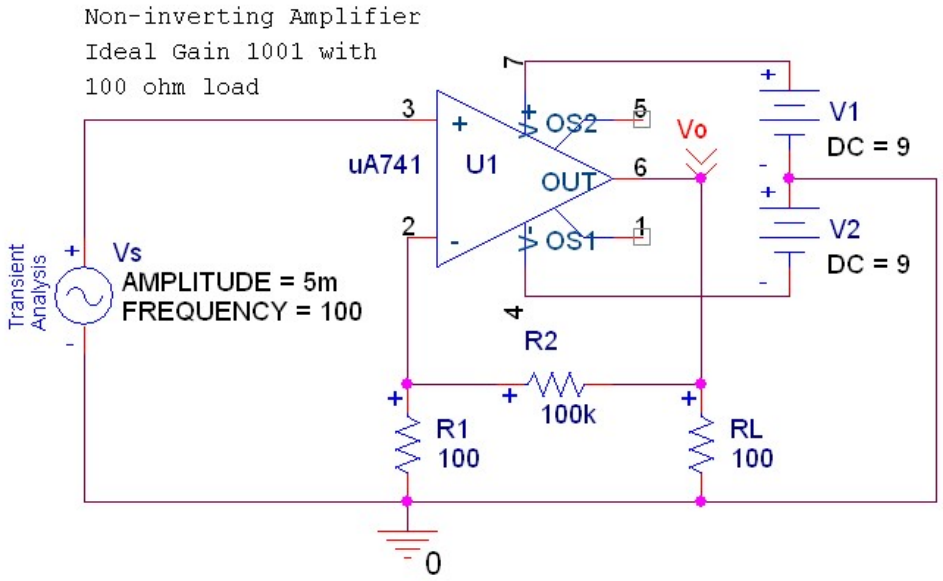

5.0V
0V
-5.0V
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
V(VO)
Time

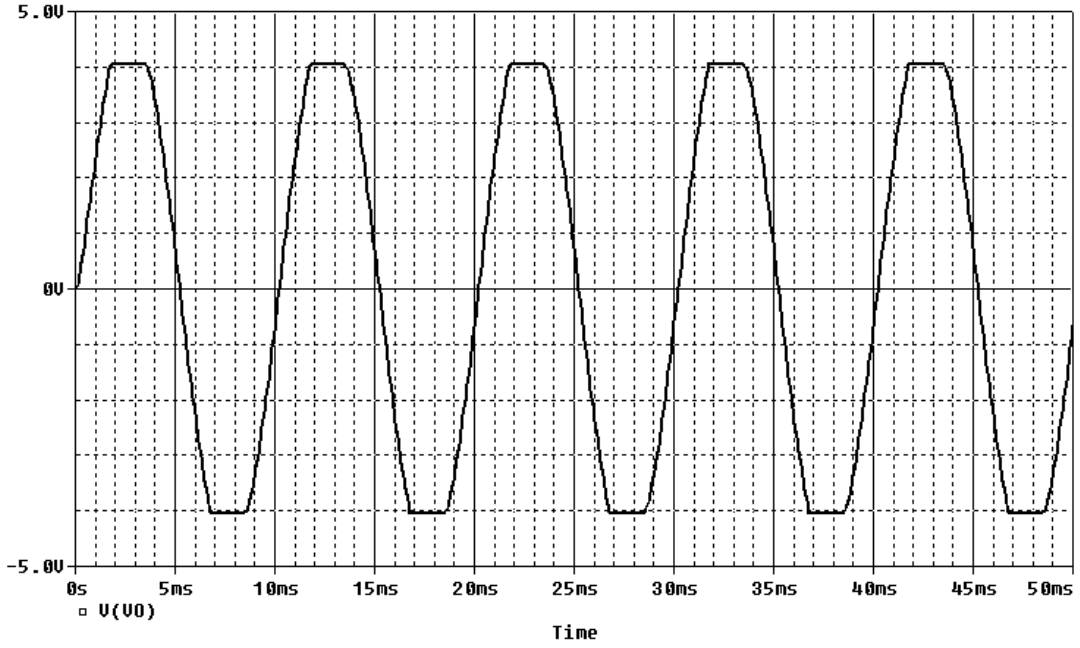

Non-inverting Amplifier
Ideal Gain 100001
Transient Analysis
Vs
AMPLITUDE = 50u
FREQUENCY = 100
uA741
U1
OS2
OS1
OUT
Vo
V1
DC = 9
V2
DC = 9
R2
1Meg
R1
10
0


2.0V
1.5V
1.0V
0.5V
0V
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
V(VO)
Time

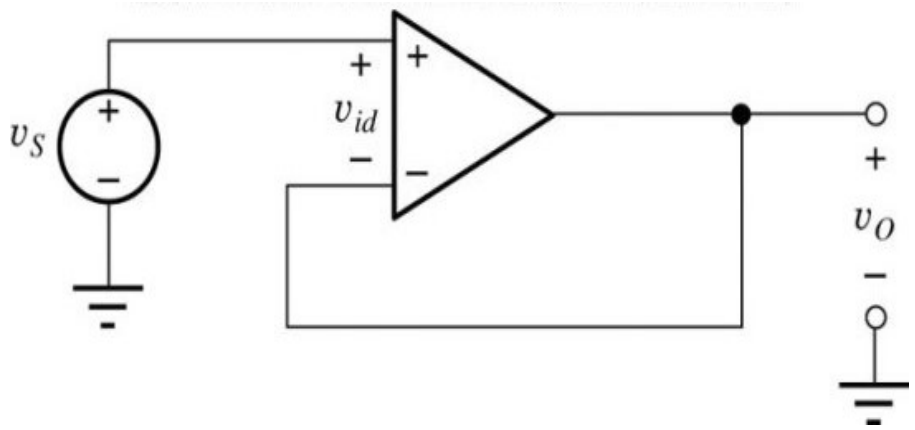

Non-inverting Amplifier
Ideal Gain 1001 with
500 ohm load
3
2
7
4
5
6
1
uA741
U1
OS2
OS1
OUT
Vo
V1
DC = 9
V2
DC = 9
Vs
AMPLITUDE = 5m
FREQUENCY = 100
Transient Analysis
R2
100k
R1
100
RL
500
0


5.0V
0V
-5.0V
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
V(VO)
Time


Non-inverting Amplifier
Ideal Gain 1001 with
100 ohm load
uA741
U1
OS2
OS1
OUT
Vo
V1
DC = 9
V2
DC = 9
Vs
AMPLITUDE = 5m
FREQUENCY = 100
Transient Analysis
R2
100k
R1
100
RL
100
0

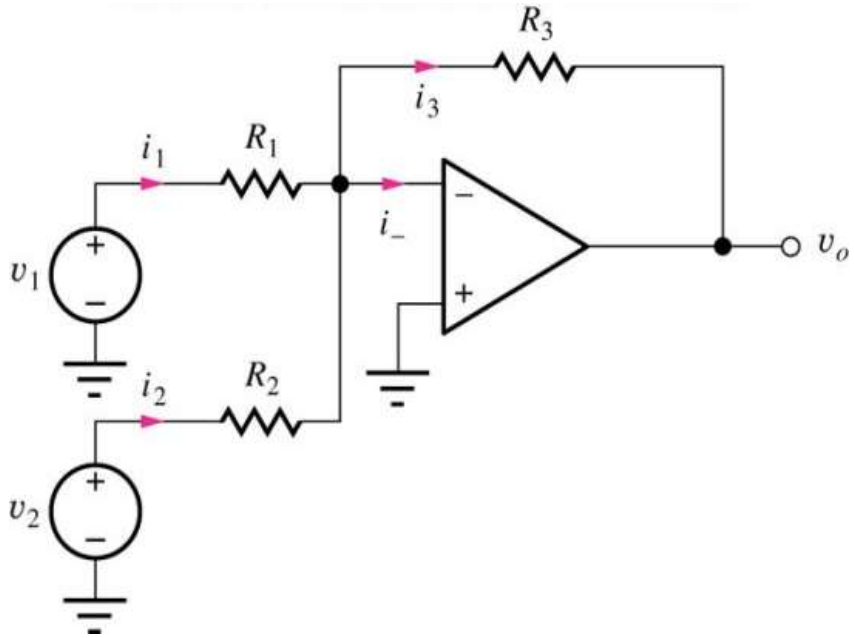

5.0V
0V
-5.0V
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
V(VO)
Time

The Unity-gain Amplifier or "Buffer"



- This is a special case of the non-inverting amplifier, which is also called a voltage follower, with infinite R_1 and zero R_2. Hence $A_v = 1$.
- It provides an excellent impedance-level transformation while maintaining the signal voltage level.
- The "ideal" buffer does not require any input current and can drive any desired load resistance without loss of signal voltage.
- Such a buffer is used in many sensor and data acquisition system applications.

The Summing Amplifier



Since the negative amplifier input is at virtual ground,

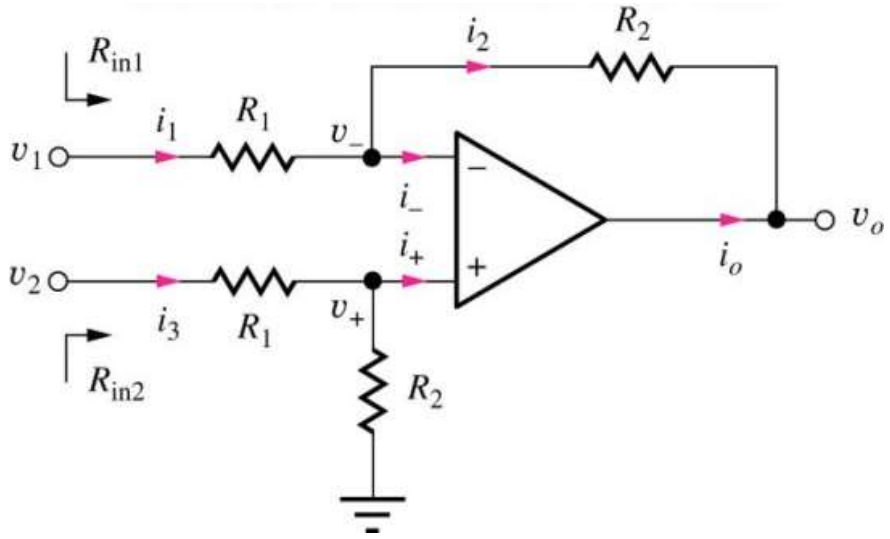
$$i_1 = \frac{v_1}{R_1} \quad i_2 = \frac{v_2}{R_2} \quad i_3 = -\frac{v_o}{R_3}$$

Since $i_- = 0$, $i_3 = i_1 + i_2$,

$$\therefore v_o = -\frac{R_3}{R_1} v_1 - \frac{R_3}{R_2} v_2$$

- Scale factors for the 2 inputs can be independently adjusted by the proper choice of R_2 and R_1.
- Any number of inputs can be connected to a summing junction through extra resistors.
- This circuit can be used as a simple digital-to-analog converter. This will be illustrated in more detail, later.

The Difference Amplifier



$$v_o = v_- - i_2 R_2 = v_- - i_1 R_2$$

$$= v_- - \frac{R_2}{R_1}(v_1 - v_-) = \left(\frac{R_1 + R_2}{R_1}\right) v_- - \frac{R_2}{R_1} v_1$$

Also, $$v_+ = \frac{R_2}{R_1 + R_2} v_2$$

Since $v_- = v_+$ $$v_o = -\frac{R_2}{R_1}(v_1 - v_2)$$

For $R_2 = R_1$ $$v_o = -(v_1 - v_2)$$

- This circuit is also called a differential amplifier, since it amplifies the difference between the input signals.
- R_{in2} is series combination of R_1 and R_2 because i_+ is zero.
- For v_2=0, $R_{in1} = R_1$, as the circuit reduces to an inverting amplifier.
- For general case, i_1 is a function of both v_1 and v_2.

Difference Amplifier: Example

- **Problem**: Determine v_o
- **Given Data**: R_1= 10kΩ, R_2 =100kΩ, v_1=5 V, v_2=3 V
- **Assumptions:** Ideal op amp. Hence, v_-= v_+ and i_-= i_+= 0.
- **Analysis:** Using dc values,

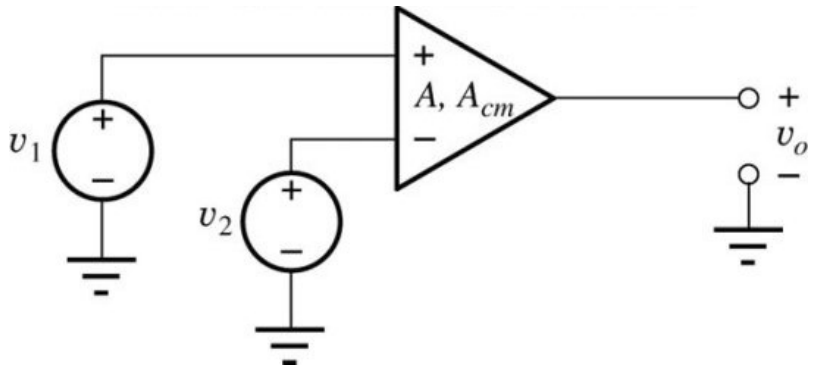
$$A_{dm} = -\frac{R_2}{R_1} = -\frac{100\text{k}\Omega}{10\text{k}\Omega} = -10$$

$$V_o = A_{dm}\left(V_1 - V_2\right) = -10(5-3)$$

$$V_o = -20.0 \text{ V}$$

Here A_{dm} is called the "differential mode voltage gain" of the difference amplifier.

Finite Common-Mode Rejection Ratio (CMRR)



A(or A_{dm}) = differential-mode gain

A_{cm} = common-mode gain

v_{id} = differential-mode input voltage

v_{ic} = common-mode input voltage

$$v_1 = v_{ic} + \frac{v_{id}}{2} \qquad v_2 = v_{ic} - \frac{v_{id}}{2}$$

A real amplifier responds to signal common to both inputs, called the common-mode input voltage (v_{ic}). In general,

$$v_o = A_{dm}(v_1 - v_2) + A_{cm}\left(\frac{v_1 + v_2}{2}\right)$$

$$v_o = A_{dm}(v_{id}) + A_{cm}(v_{ic})$$

An ideal amplifier has $A_{cm} = 0$, but for a real amplifier,

$$v_o = A_{dm}\left(v_{id} + \frac{A_{cm} v_{ic}}{A_{dm}}\right) = A_{dm}\left(v_{id} + \frac{v_{ic}}{\text{CMRR}}\right)$$

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right|$$

and $\text{CMRR(dB)} = 20\log_{10}(\text{CMRR})$

Finite Common-Mode Rejection Ratio: Example

- **Problem**: Find output voltage error introduced by finite CMRR.
- **Given Data**: A_{dm}= 2500, CMRR = 80 dB, v_1 = 5.001 V, v_2 = 4.999 V
- **Assumptions:** Op amp is ideal, except for CMRR. Here, a CMRR in dB of 80 dB corresponds to a CMRR of 10^4.
- **Analysis:**

$$v_{id} = 5.001\text{V} - 4.999\text{V}$$

$$v_{ic} = \frac{5.001\text{V} + 4.999\text{V}}{2} = 5.000\text{V}$$

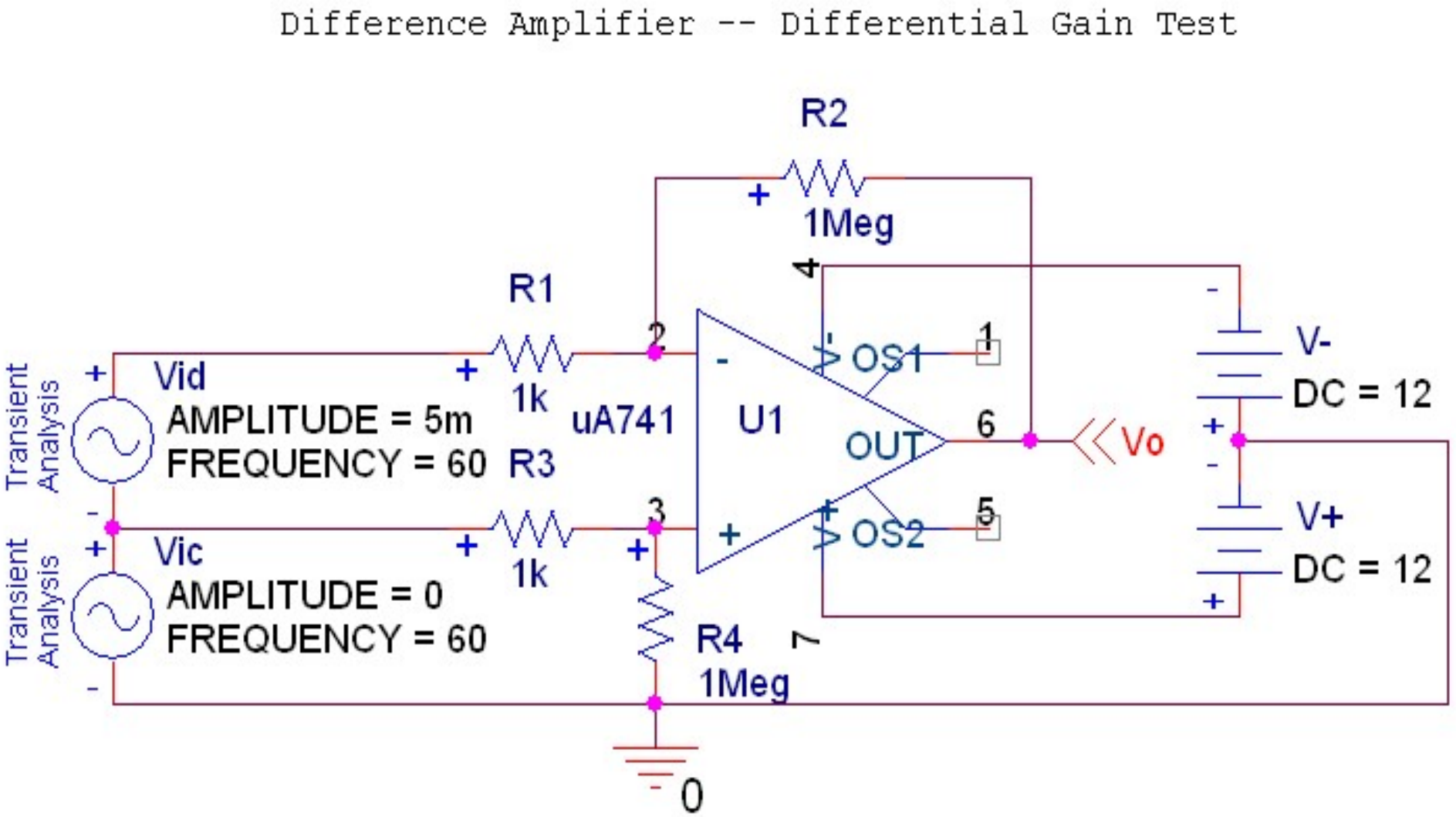
$$v_o = A_{dm}\left(v_{id} + \frac{v_{ic}}{\text{CMRR}}\right) = 2500\left(0.002 + \frac{5.000}{10^4}\right)\text{V} = 6.25\text{V}$$

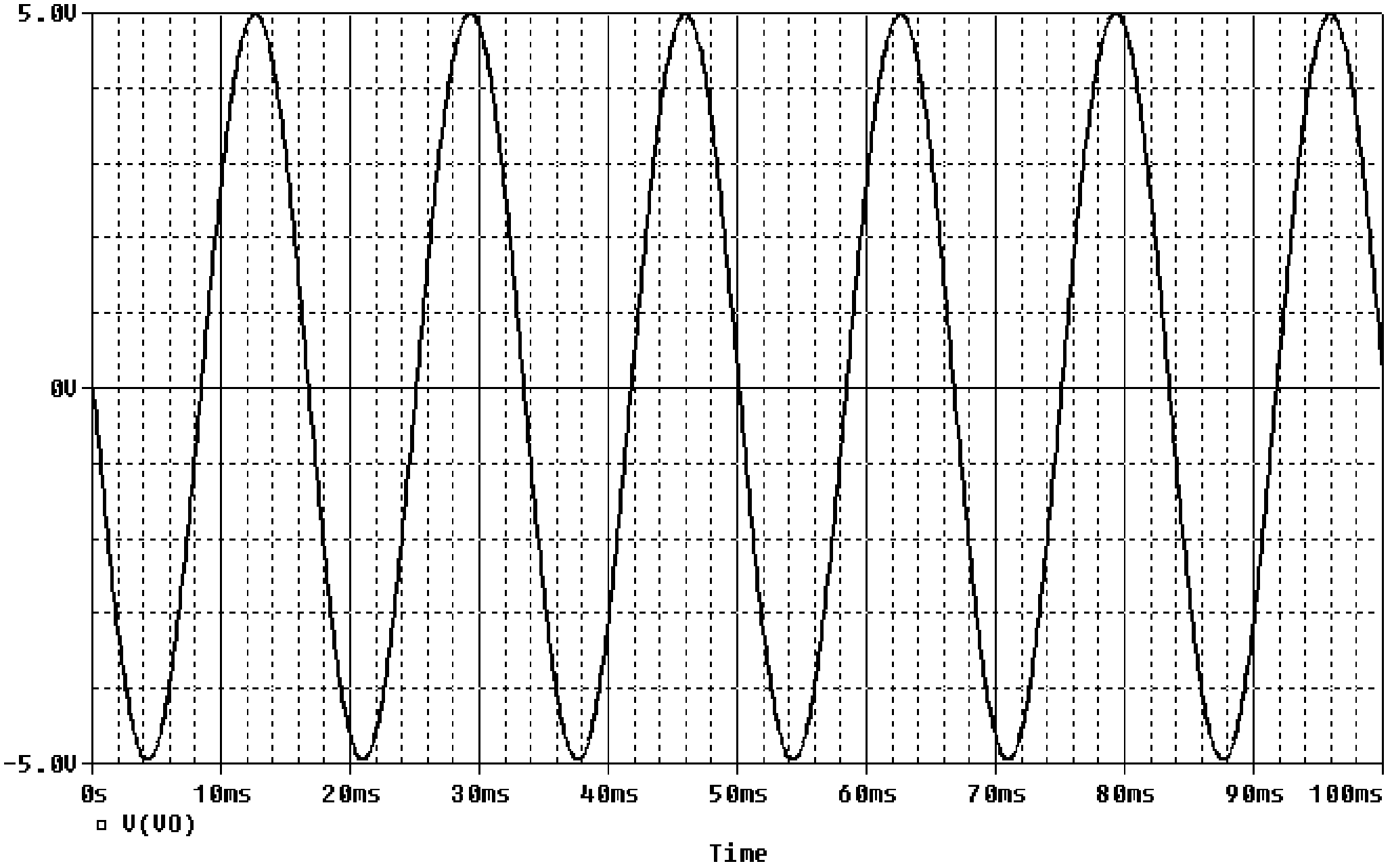
In the "ideal" case, $v_o = A_{dm} v_{id} = 5.00$ V

$$\%\ \text{output error} = \frac{6.25 - 5.00}{5.00} \times 100\% = 25\%$$

The output error introduced by finite CMRR is 25% of the expected ideal output.

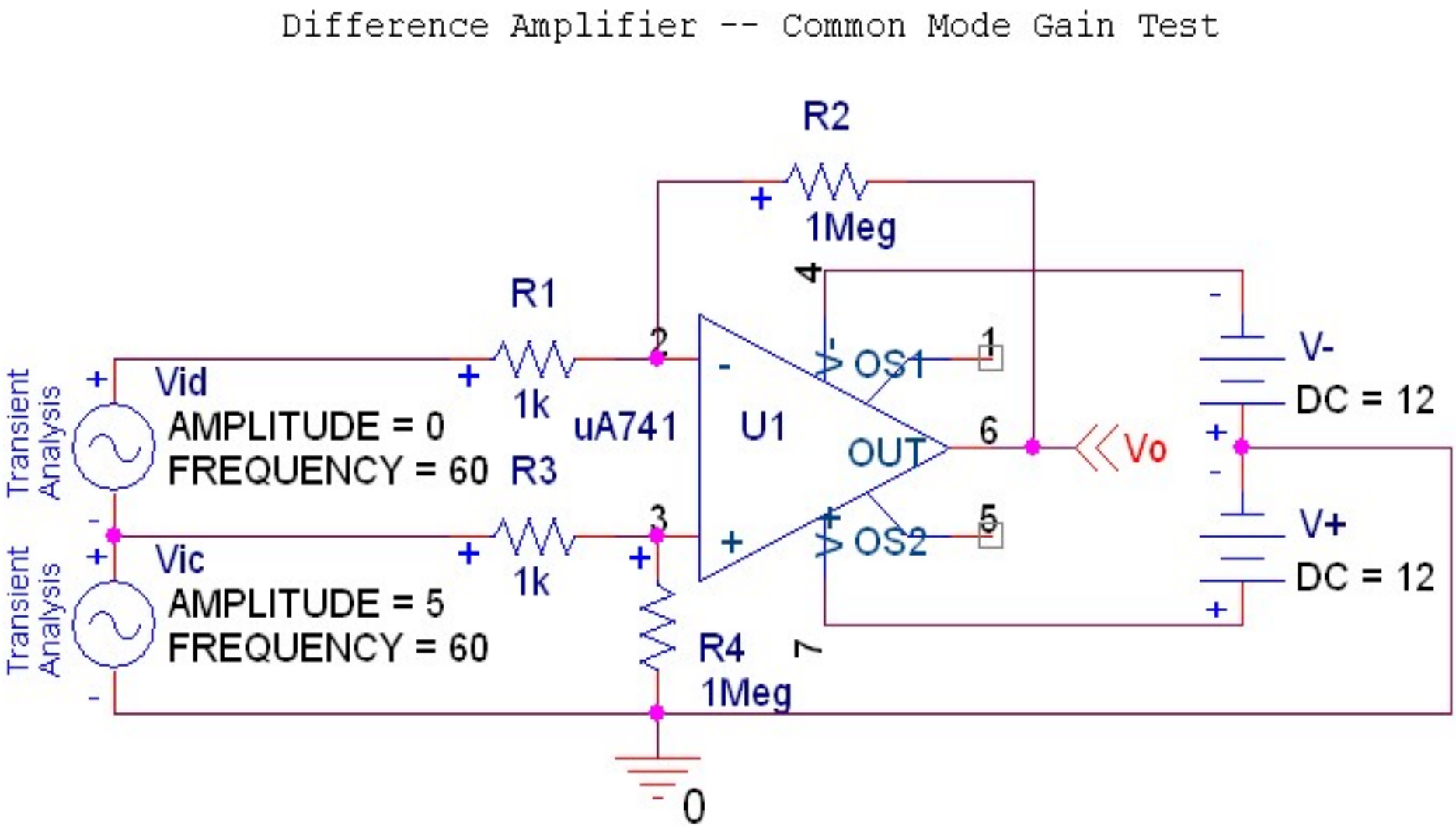
uA741 CMRR Test: Differential Gain

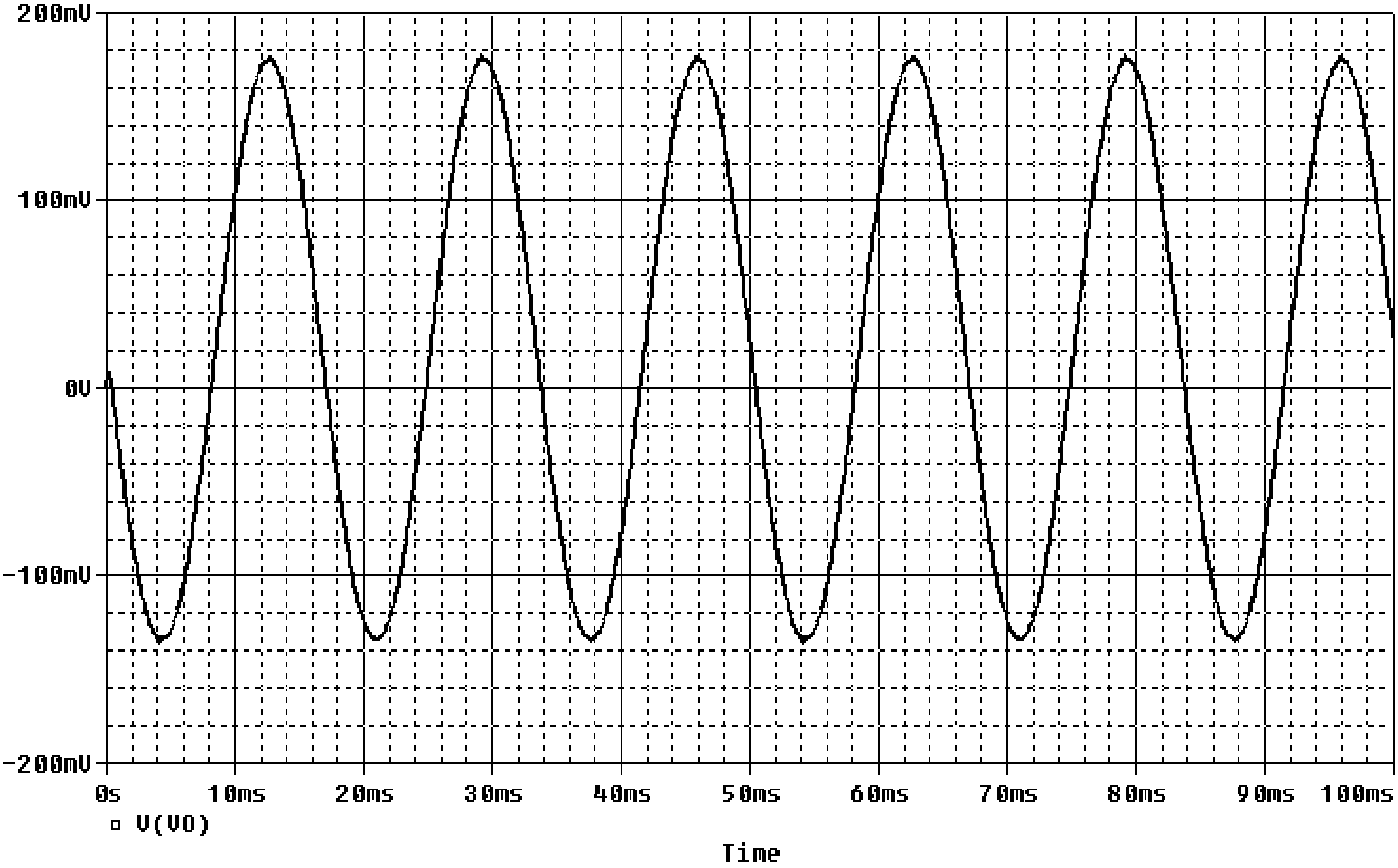




Differential Gain A_{dm} = 5 V/5 mV = 1000

uA741 CMRR Test: Common Mode Gain





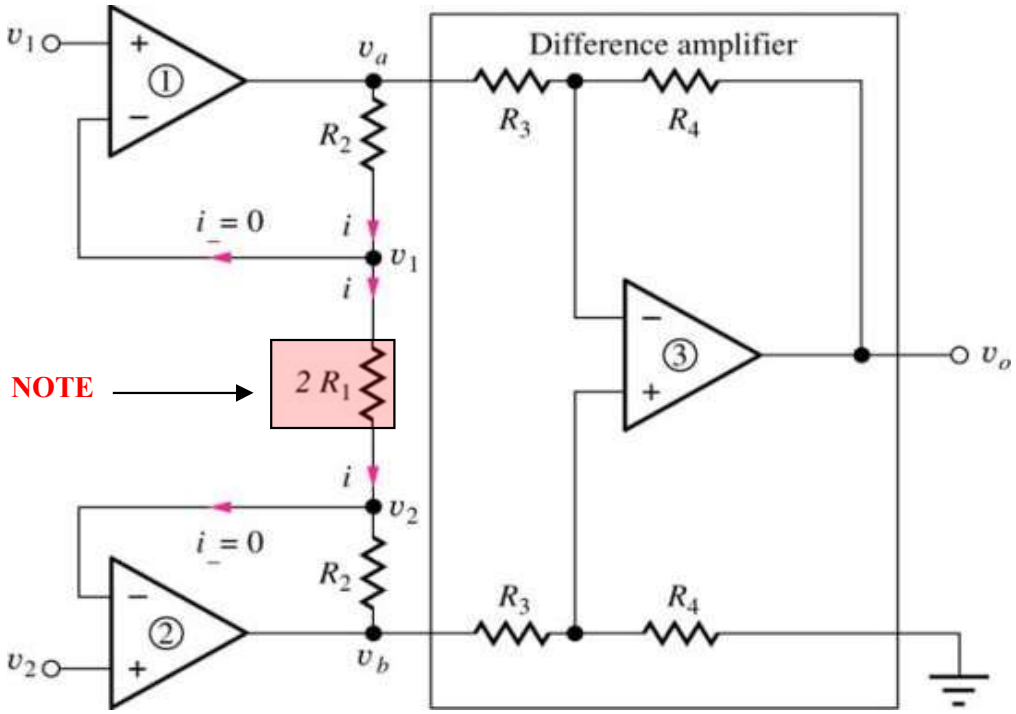
Common Mode Gain A_{cm} = 160 mV/5 V = .032

CMRR Calculation for uA741

$$\text{CMRR} = \frac{|A_{dm}|}{|A_{cm}|} = \frac{1000}{.032} = 3.125x10^4$$

$$\text{CMRR(dB)} = 20\log_{10}(\text{CMRR}) = 89.9 \text{ dB}$$

Instrumentation Amplifier



$$v_o = -\frac{R_4}{R_3}(v_a - v_b)$$

$$v_a - iR_2 - i(2R_1) - iR_2 = v_b$$

$$i = \frac{v_1 - v_2}{2R_1}$$

$$\therefore v_o = -\frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)(v_1 - v_2)$$

Combines 2 non-inverting amplifiers with the difference amplifier to provide higher gain and higher input resistance.

Ideal input resistance is infinite because input current to both op amps is zero. The CMRR is determined only by Op Amp 3.

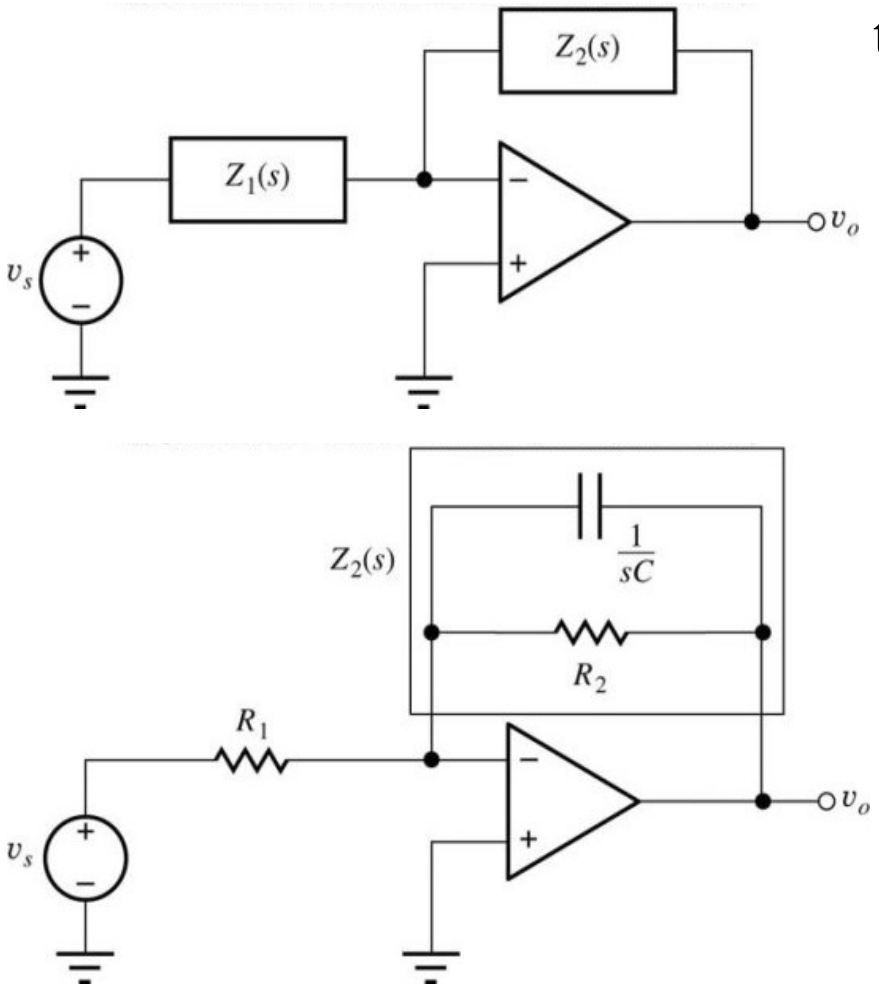
Instrumentation Amplifier: Example

- **Problem**: Determine V_o
- **Given Data**: $R_1 = 15\ \text{k}\Omega$, $R_2 = 150\ \text{k}\Omega$, $R_3 = 15\ \text{k}\Omega$, $R_4 = 30\ \text{k}\Omega$ $V_1 = 2.5$ V, $V_2 = 2.25$ V
- **Assumptions:** Ideal op amp. Hence, $v_- = v_+$ and $i_- = i_+ = 0$.
- **Analysis:** Using dc values,

$$A_{dm} = -\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right) = -\frac{30\text{k}\Omega}{15\text{k}\Omega}\left(1+\frac{150\text{k}\Omega}{15\text{k}\Omega}\right) = -22$$

$$V_o = A_{dm}(V_1 - V_2) = -22(2.5-2.25) = -5.50\text{V}$$

The Active Low-pass Filter



Use a phasor approach to gain analysis of this inverting amplifier. Let s = jω.

$$A_v = \frac{\tilde{v}_o(j\omega)}{\tilde{v}(j\omega)} = -\frac{Z_2(j\omega)}{Z_1(j\omega)} \qquad Z_1(j\omega) = R_1$$

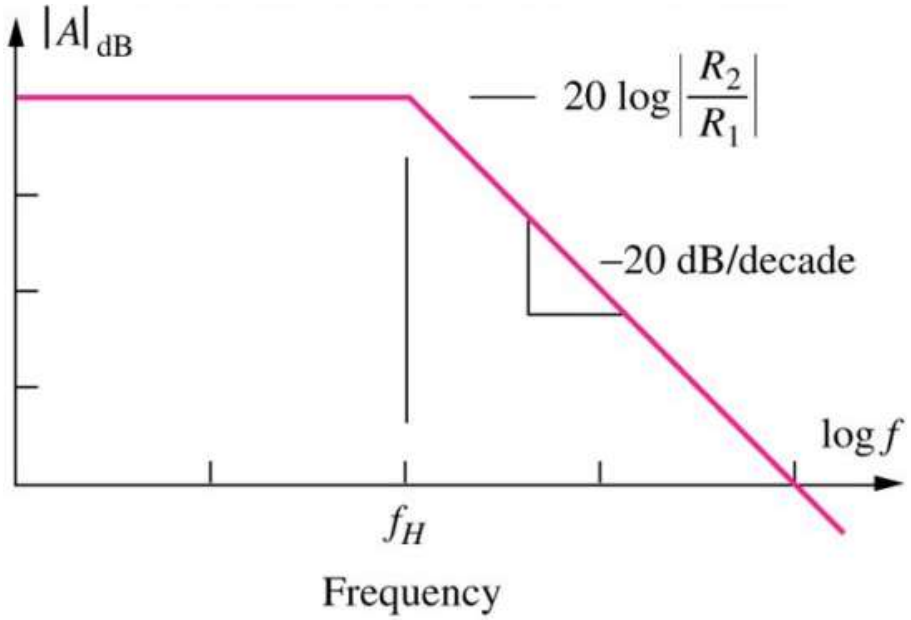
$$Z_2(j\omega) = \frac{R_2 \frac{1}{j\omega C}}{R_2 + \frac{1}{j\omega C}} = \frac{R_2}{j\omega C R_2 + 1}$$

$$A_v = -\frac{R_2}{R_1}\frac{1}{(1 + j\omega C R_2)} = \frac{R_2}{R_1}\frac{e^{j\pi}}{(1 + \frac{j\omega}{\omega_c})}$$

$$\omega_c = 2\pi f_c = \frac{1}{R_2 C} \quad \therefore f_c = \frac{1}{2\pi R_2 C}$$

f_c is called the high frequency "cutoff" of the low-pass filter.

Active Low-pass Filter (continued)



- At frequencies below f_c (f_H in the figure), the amplifier is an inverting amplifier with gain set by the ratio of resistors R_2 and R_1.
- At frequencies above f_c, the amplifier response "rolls off" at -20dB/decade.
- Notice that cutoff frequency and gain can be independently set.

$$A_v = \frac{R_2}{R_1}\left(\frac{e^{j\pi}}{(1+\frac{j\omega}{\omega_c})}\right) = \frac{R_2}{R_1\sqrt{1^2+\left(\frac{\omega}{\omega_c}\right)^2}}\left(\frac{e^{j\pi}}{e^{j\tan^{-1}(\omega/\omega_c)}}\right) = \frac{R_2}{R_1\sqrt{1+\left(\frac{\omega}{\omega_c}\right)^2}} e^{j[\pi-\tan^{-1}(\omega/\omega_c)]}$$

magnitude phase

Active Low-pass Filter: Example

- **Problem**: Design an active low-pass filter
- **Given Data**: A_v= 40 dB, R_{in}= 5 kΩ, f_H = 2 kHz
- **Assumptions:** Ideal op amp, specified gain represents the desired low-frequency gain.
- **Analysis**: $|A_v| = 10^{40\text{dB}/20\text{dB}} = 100$

  Input resistance is controlled by R_1 and voltage gain is set by R_2 / R_1.

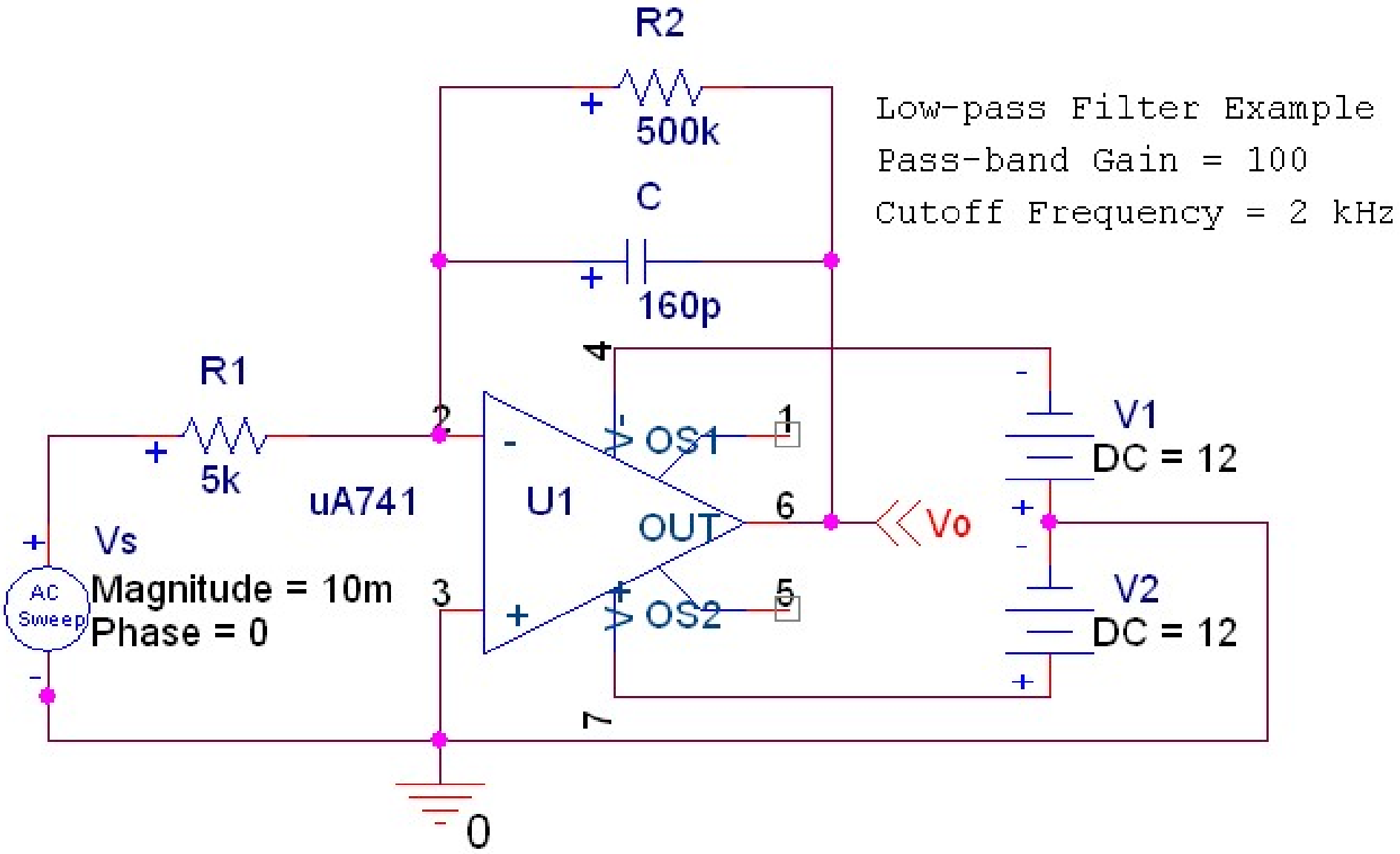
  The cutoff frequency is then set by C.

$$R_1 = R_{in} = 5\text{k}\Omega \quad \text{and} \quad |A_v| = \frac{R_2}{R_1} \Rightarrow R_2 = 100R_1 = 500\text{k}\Omega$$

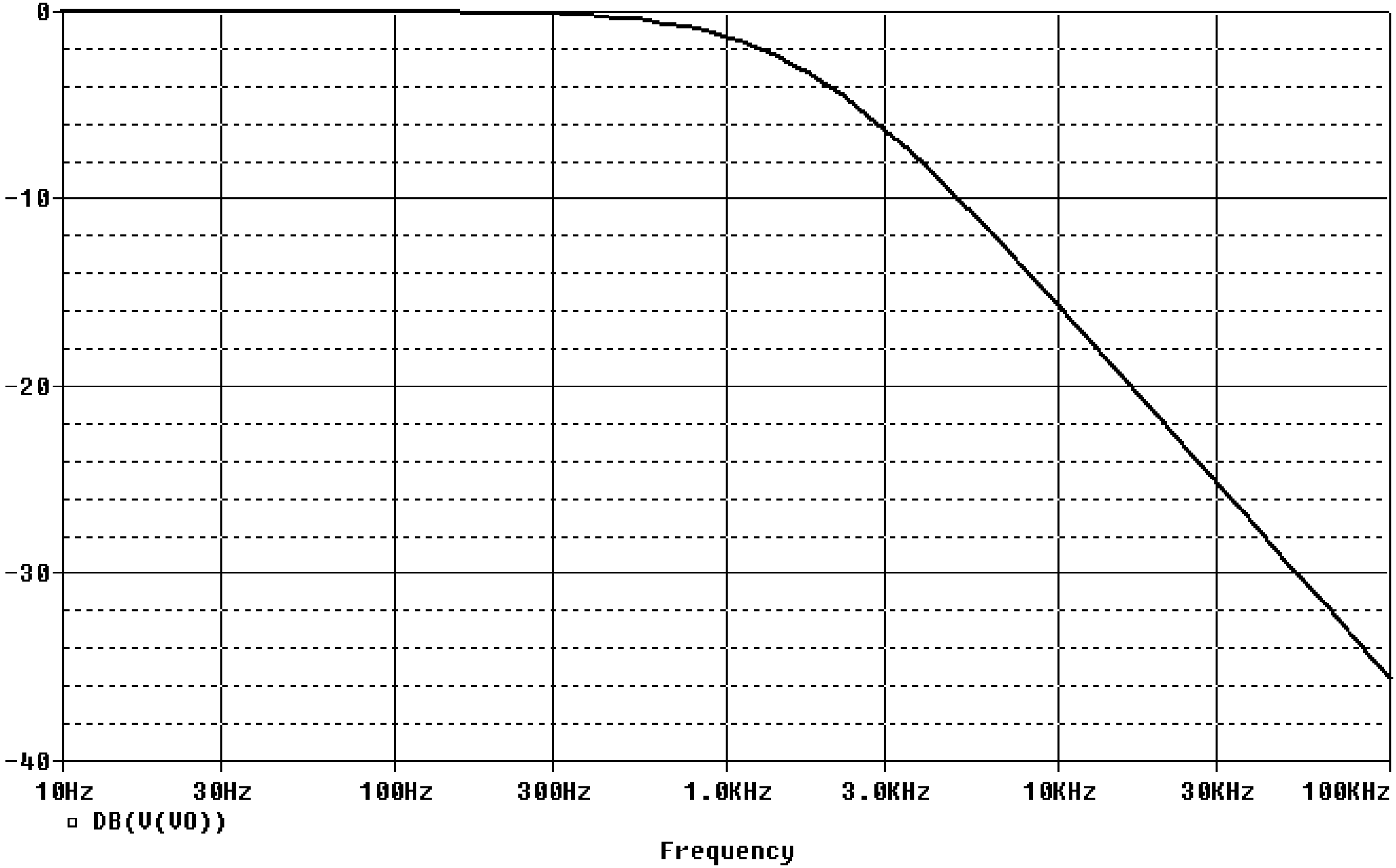
$$C = \frac{1}{2\pi f_H R_2} = \frac{1}{2\pi(2\text{kHz})(500\text{k}\Omega)} = 159\text{pF}$$

  The closest standard capacitor value of 160 pF lowers cutoff frequency to 1.99 kHz.

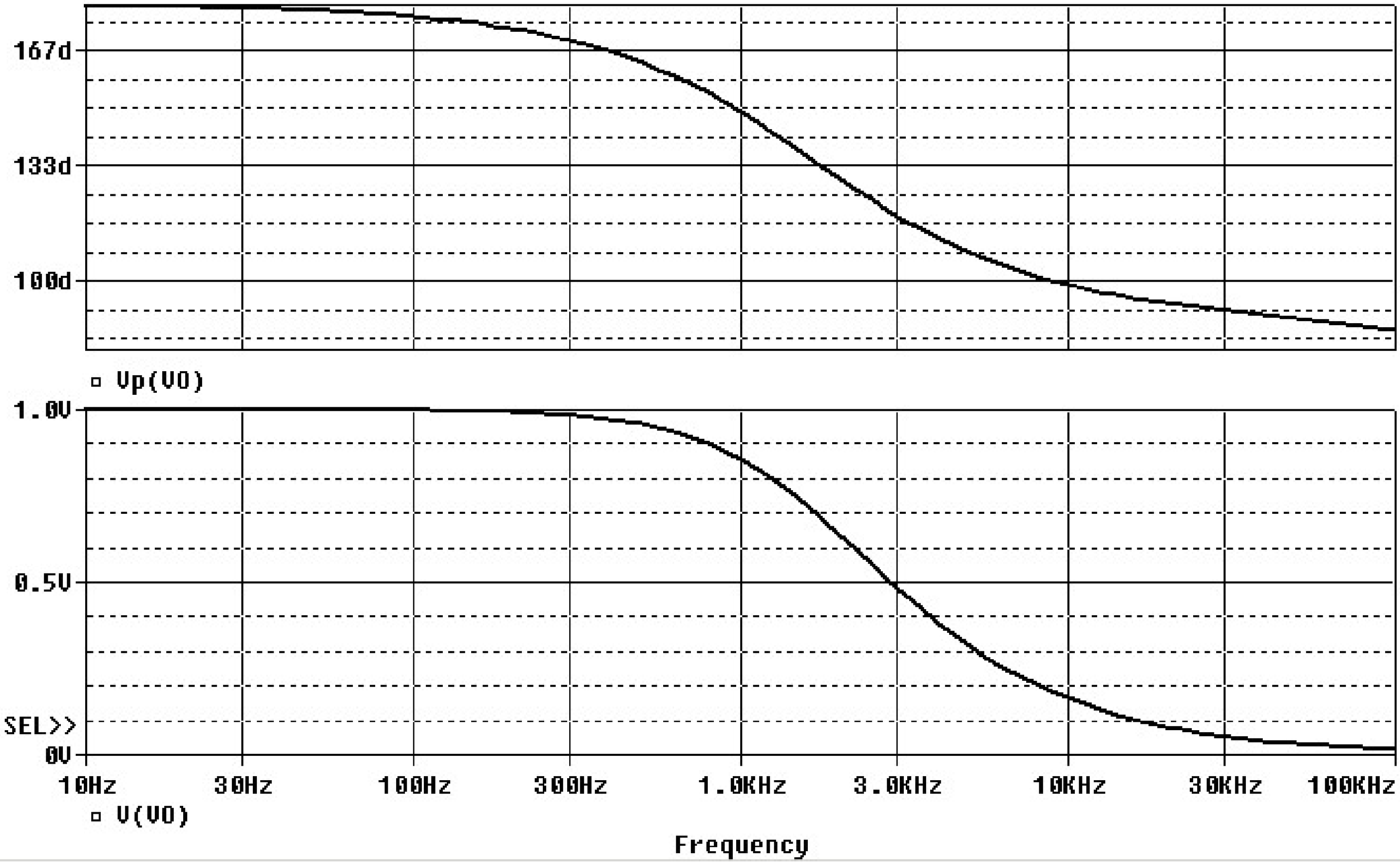
Low-pass Filter Example PSpice Simulation



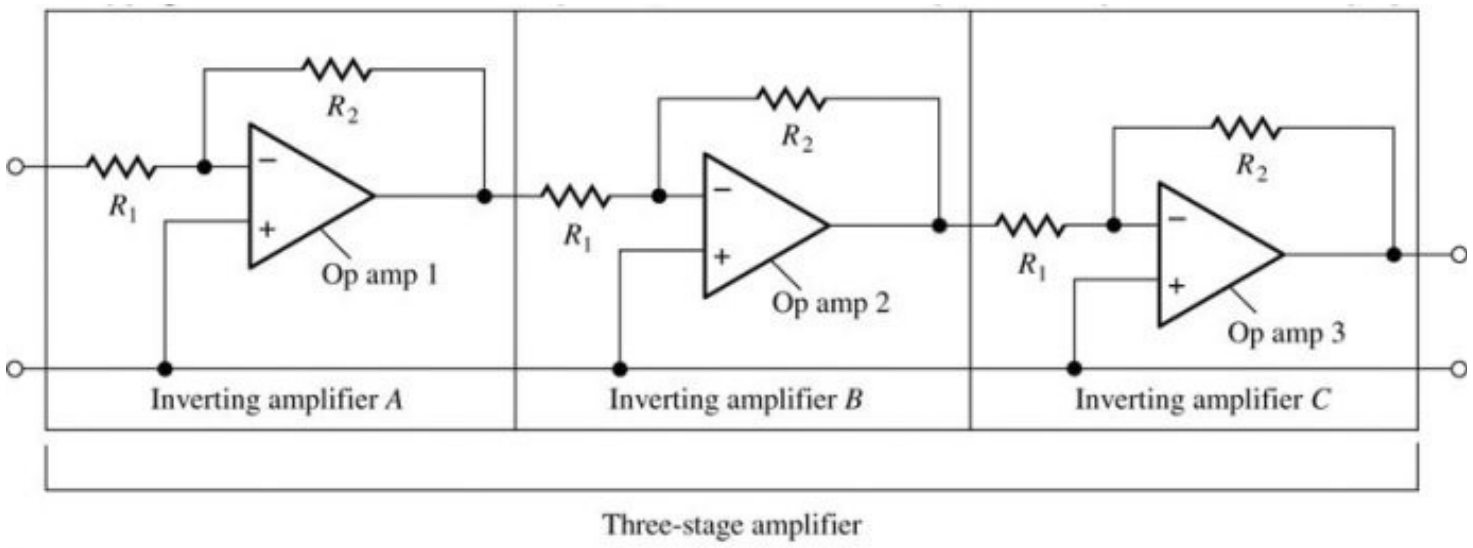
Output Voltage Amplitude in dB



Output Voltage Amplitude in Volts (V) and Phase in Degrees (d)

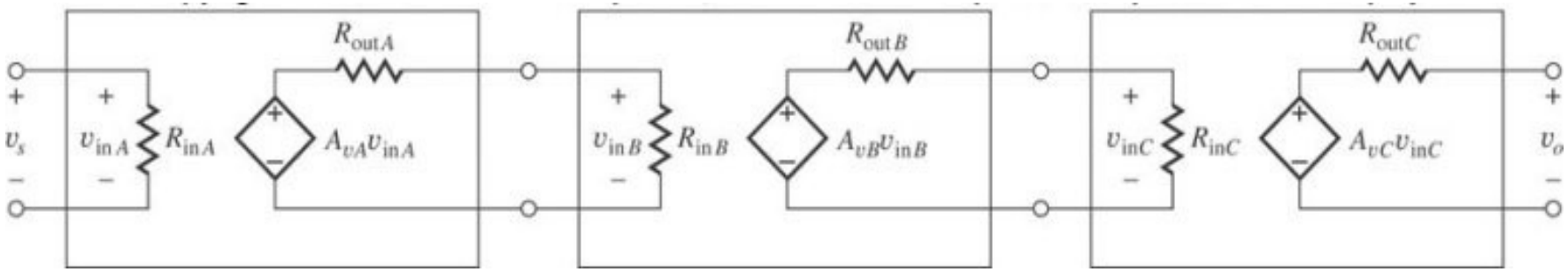


Cascaded Amplifiers



- Connecting several amplifiers in cascade (output of one stage connected to the input of the next) can meet design specifications not met by a single amplifier.
- Each amplifer stage is built using an op amp with parameters A, R_{id}, R_o, called open loop parameters, that describe the op amp with no external elements.
- A_v, R_{in}, R_{out} are closed loop parameters that can be used to describe each closed-loop op amp stage with its feedback network, as well as the overall composite (cascaded) amplifier.

Two-port Model for a 3-stage Cascade Amplifier



- Each amplifier in the 3-stage cascaded amplifier is replaced by its 2-port model.

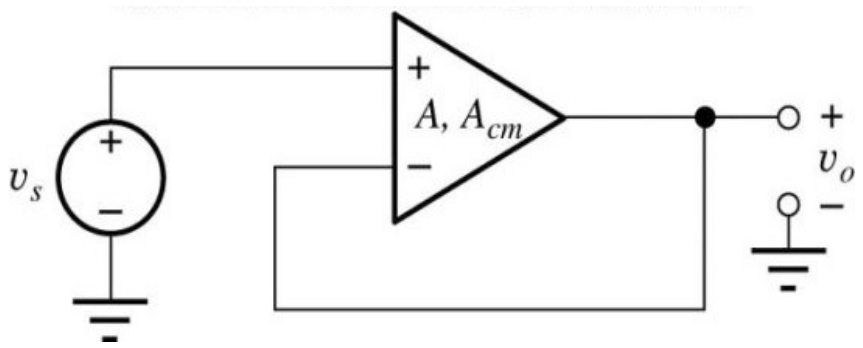
$$v_o = A_{vA} v_s \left(\frac{R_{inB}}{R_{outA} + R_{inB}} \right) A_{vB} \left(\frac{R_{inC}}{R_{outB} + R_{inC}} \right) A_{vC}$$

Since $R_{out} = 0$

$$A_v = \frac{v_o}{v_s} = A_{vA} A_{vB} A_{vC}$$

$$R_{in} = R_{inA} \quad \text{and} \quad R_{out} = R_{outC} = 0$$

A Problem: Voltage Follower Closed Loop Gain Error due to A and CMRR



$$v_{id} = v_s - v_o \qquad v_{ic} = \frac{v_s + v_o}{2}$$

$$v_o = A\left((v_s - v_o) + \frac{(v_s + v_o)}{2(CMRR)}\right)$$

$$A_v = \frac{v_o}{v_s} = \frac{A\left(1 + \frac{1}{2(CMRR)}\right)}{1 + A\left(1 - \frac{1}{2(CMRR)}\right)}$$

The ideal gain for the voltage follower is unity. The gain error here is:

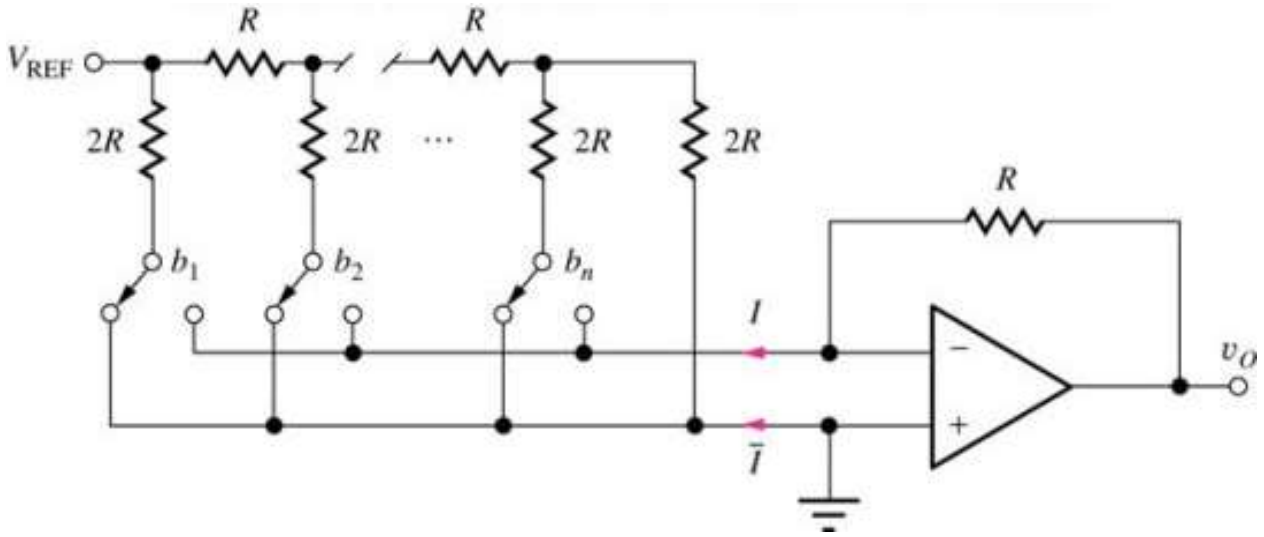
$$GE = 1 - A_v = \frac{1 - \frac{A}{CMRR}}{1 + A\left(1 - \frac{1}{2(CMRR)}\right)}$$

Since, both A and CMRR are normally >>1,

$$GE \cong \frac{1}{A} - \frac{1}{CMRR}$$

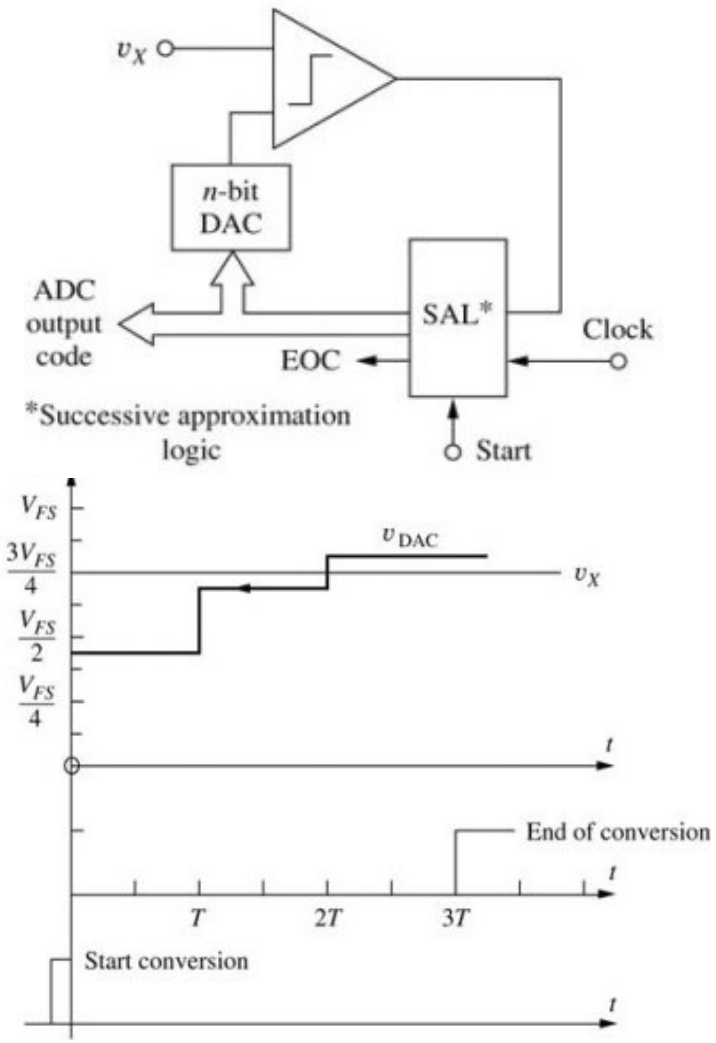
Since $A \sim 10^6$ and CMRR $\sim 10^4$ at low to moderate frequency, the gain error is quite small and is, in fact, usually negligible.

Inverted R-2R Ladder DAC



- A very common DAC circuit architecture with good precision.
- Currents in the ladder and the reference source are independent of digital input. This contributes to good conversion precision.
- Complementary currents are available at the output of inverted ladder.
- The “bit switches” need to have very low on-resistance to minimize conversion errors.

Successive Approximation ADC



- Binary search is used by the SAL to determine v_X.
- n-bit conversion needs n clock periods. Speed is limited by the time taken by the DAC output to settle within a fraction of an LSB of V_{FS}, and by the comparator to respond to input signals differing by small amounts.
- Slowly varying input signals, not changing by more than 0.5 LSB ($V_{FS}/2^{n+1}$) during the conversion time ($T_T = nT_C$) are acceptable.
- For a sinusoidal input signal with p-p amplitude = V_{FS}, $f_o \leq \dfrac{f_c}{2^{n+2}(n+1)\pi}$
- To avoid this frequency limitation, a high speed sample-and-hold circuit is used ahead of the successive approximation ADC.
- This is a very popular ADC with fast conversion times, used in 8- to 16- bit converters.

SAADC: Block Diagram

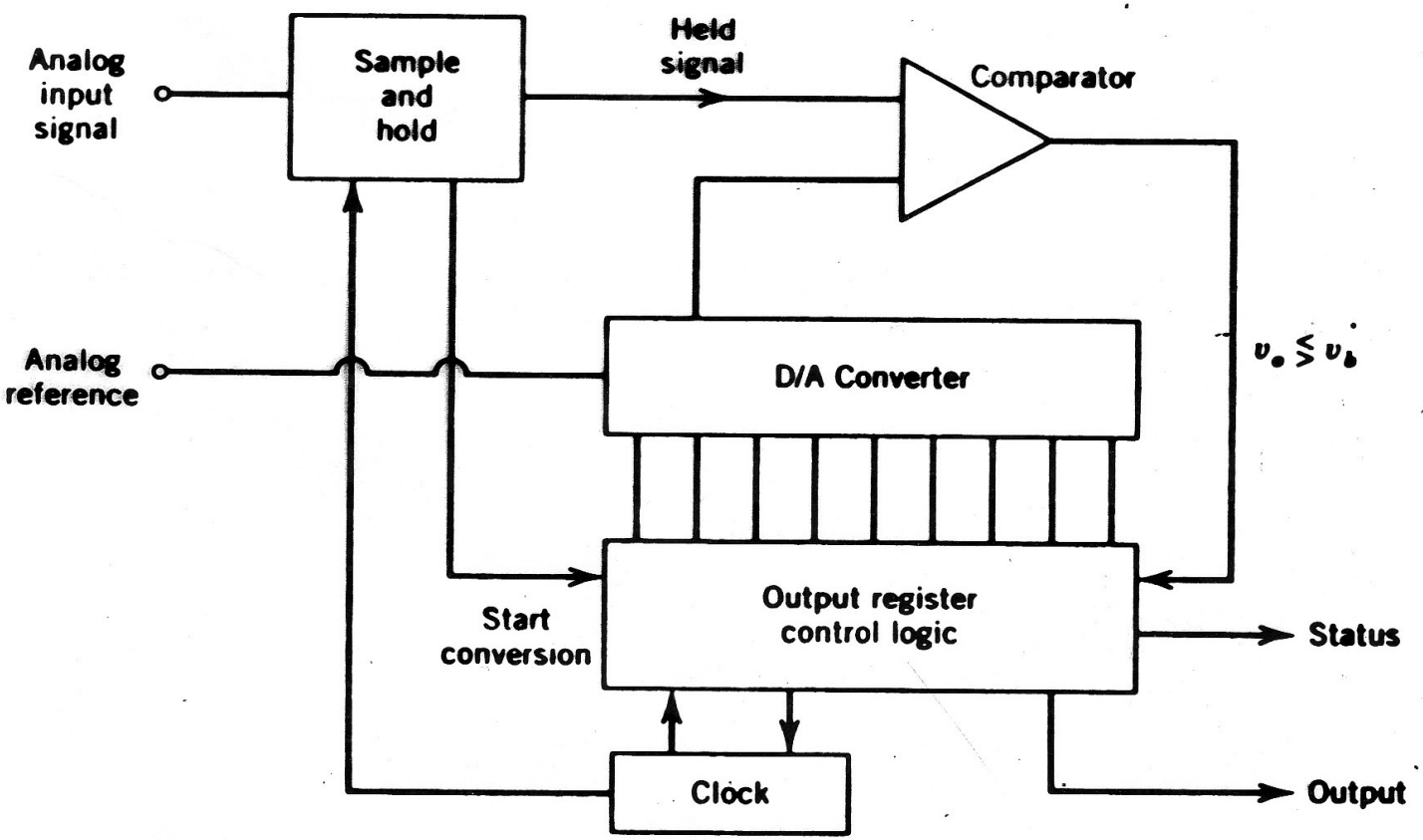


Figure 4.8 Successive-approximation converter with a sample-and-hold device

SAADC: Method of Operation

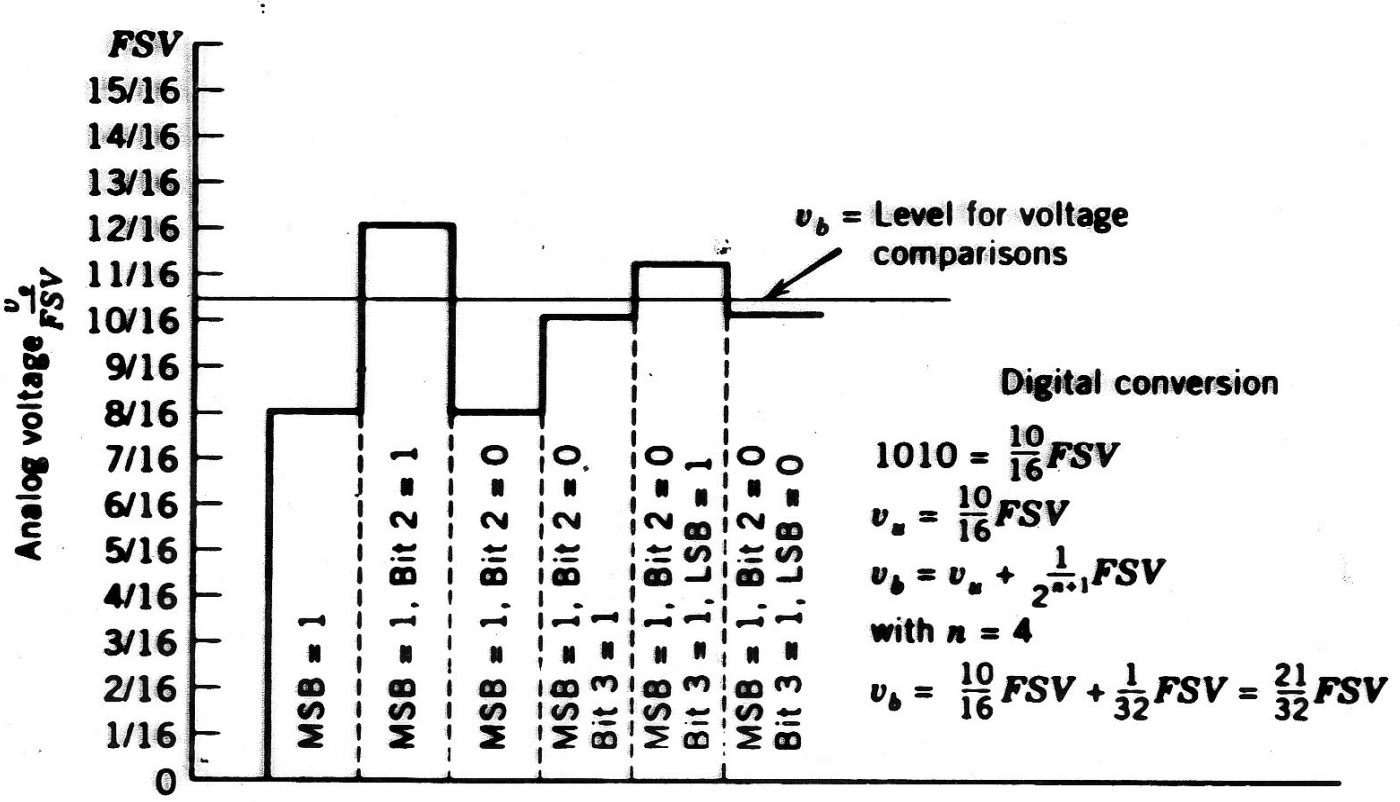


Figure 4.7 Successive-approximation method for analog-to-digital conversion.