EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term I Examination, Summer 2021

Course: CSE360 – Computer Architecture, Section-3
Instructor: Md. Nawab Yousuf Ali, PhD, Professor, CSE Department
Full Mark: 25
Time: 1 Hour and 20 Minutes

Note: There are FIVE questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

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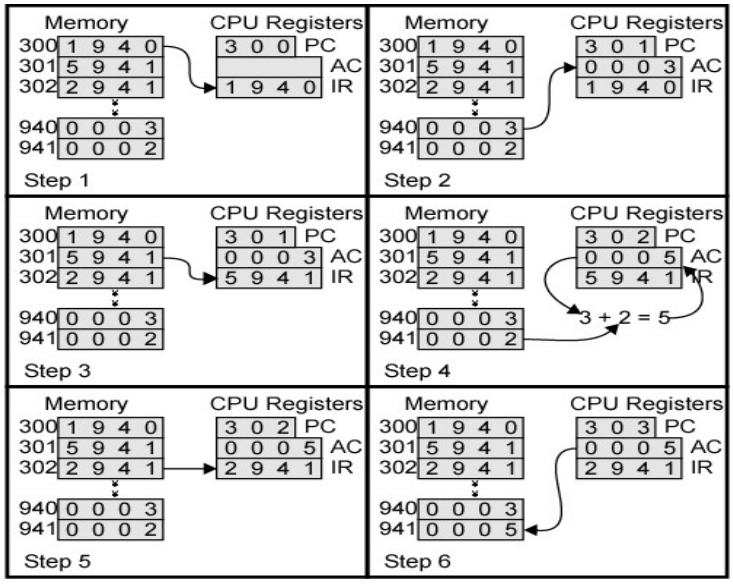
1. The hypothetical machine has two instructions: [CO1, C2, Mark: 7]
   0011 = Load AC from I/O
   0111 = Store AC to I/O
   In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:
   a) Load AC from device 11
   b) Add contents of memory location 940
   c) Store AC to device 13
   Assume that the next value retrieved from device 11 is 15 and that location 940 contains a value of 16



2. Consider a hypothetical microprocessor generating a 128-bit address (for example, assume that the program counter and the address registers are 128 bits wide) and having a 64-bit data bus. [CO1, C2, Mark: 2+3]
   a. What is the maximum memory address space that the processor can access directly if it is connected to a "128-bit memory"?
   b. What is the maximum memory address space that the processor can access directly if it is connected to an "64-bit memory"?

3. When a CPU operates at a clock frequency of 12.1GHz, requires an average of 17 CPI for executing one instruction, **what** is the performance (in MIPS) of the CPU? [CO1, C3, Mark: 3]

4. Consider a 64-bit microprocessor, with a 64-bit external data bus, driven by an 32-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. [CO1, C3, Mark: 2+ 3]
   a) **What** is the maximum data transfer rate across the bus?
   b) To increase its performance, would it be better to make its external data bus 128 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make and explain.

5. Consider a hypothetical 64-bit microprocessor having 64-bit instructions composed of two fields: the first two bytes contains the opcode and the remainder the immediate operand or an operand address. [CO2, C3 Mark: 2+3]
   a. **What** is the size of the main memory?
   b. How many bits are needed for the program counter and the instruction register?