

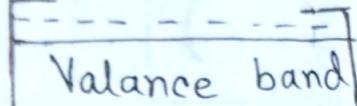
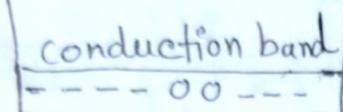
C.W
22/10/2024

CSE251

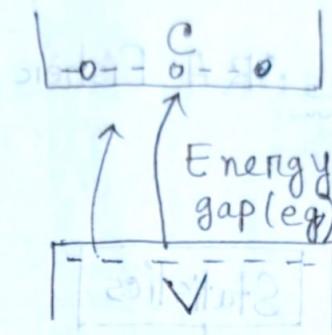
Root-ME

Diode

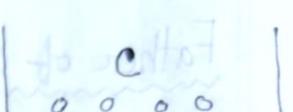
Conductor



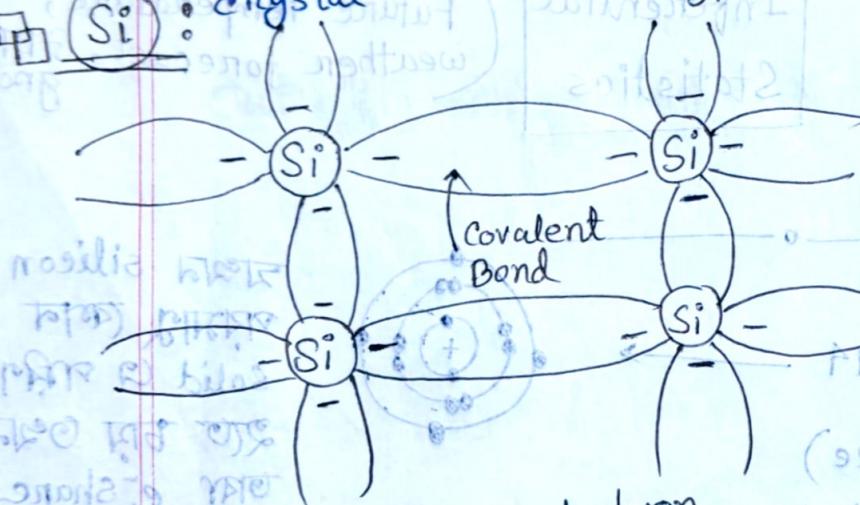
Semi-Conductor



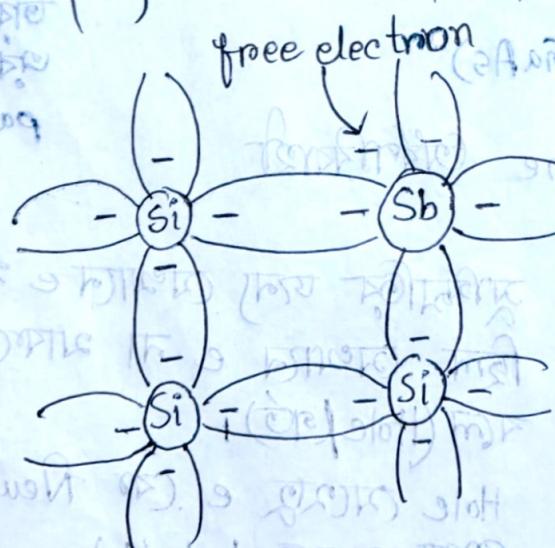
Insulator



Si: crystal



Dope:

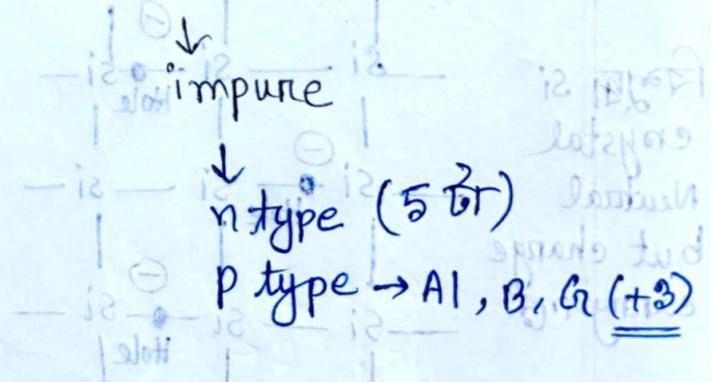


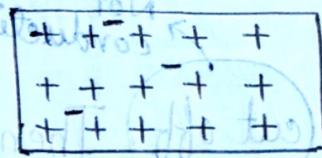
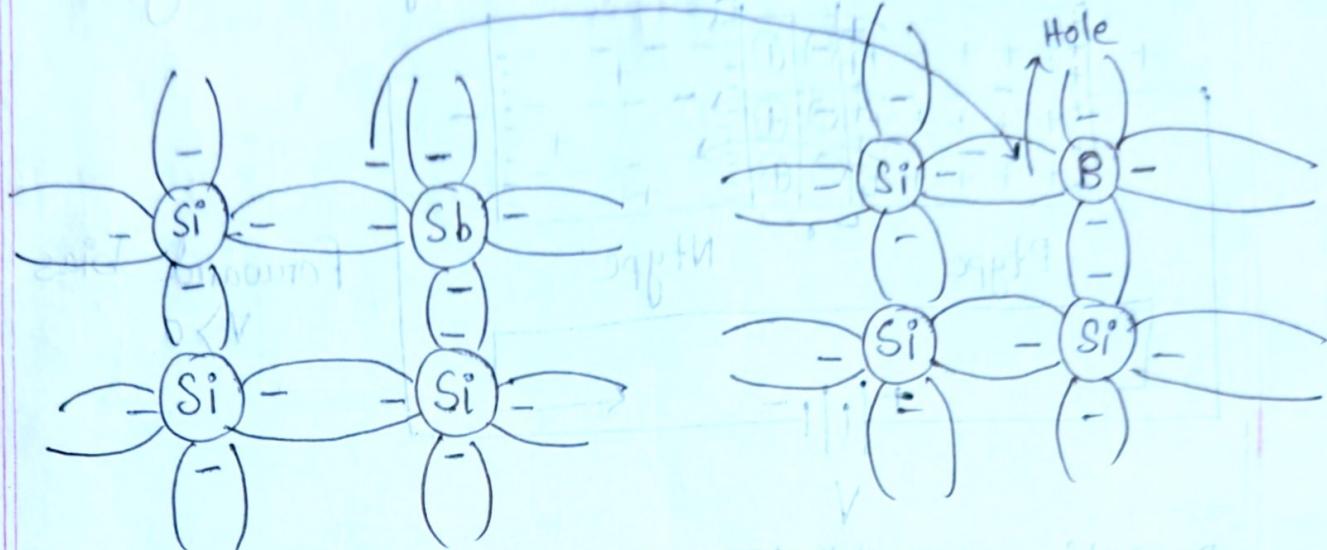
Intrinsic material: No impurity or pure

(all silicone)

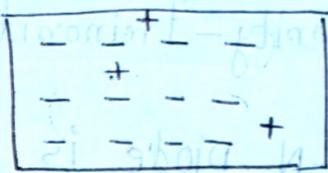
Dope Intrinsic material

Extrinsic material





P type



N-type

Hole \rightarrow +ve \rightarrow Majority carrier

Electron \rightarrow -ve \rightarrow Minority carrier

Electron \rightarrow -ve \rightarrow Majority carrier

Hole \rightarrow +ve \rightarrow Minority carrier

P-N Diode :

$+++ +$	$(-)$	$(+)$	$-- -$
$++ + +$	$(-)$	$(+)$	$-- -$
$++ + +$	$(-)$	$(+)$	$-- -$

Ptype

(Junction)

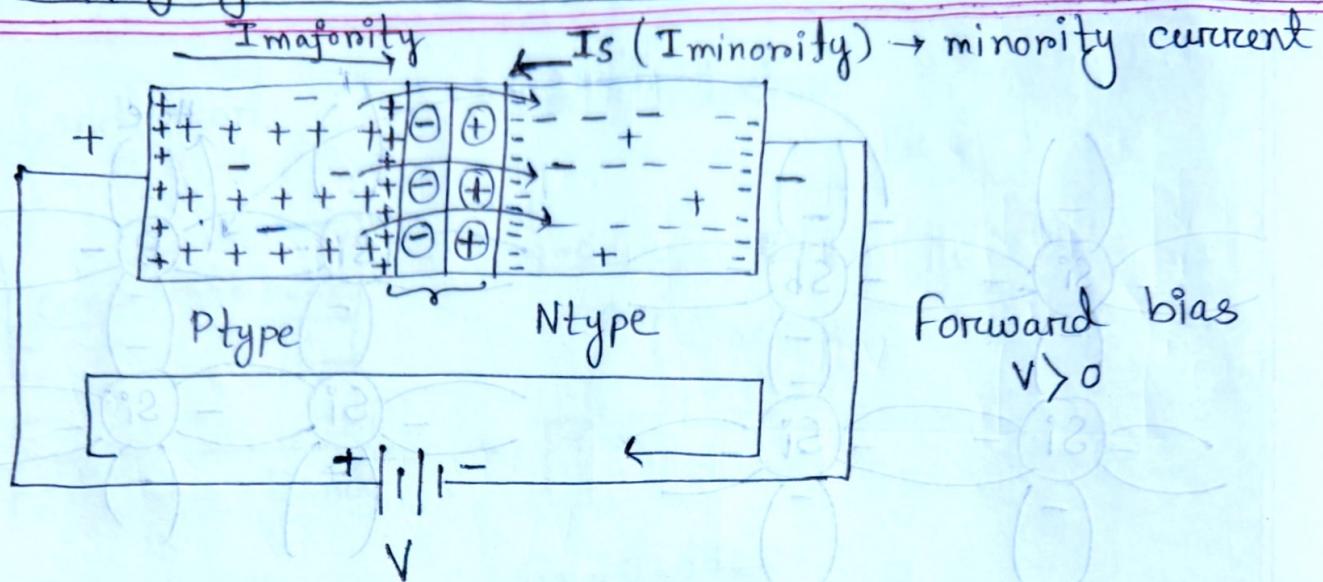
Ntype

Depletion
region
(w)

P-N \rightarrow Diode

Anode \rightarrow cathode

Applying V on P-N Diode :



Depletion region limit I minority तक.

$$I_D = I_{\text{majority}} - I_{\text{minority}}$$

* If $V=0$, P-N Diode is called cut off. Then, Depletion region will be reformed.

□ Reverse bias condition when $V < 0$.

$$\square \text{ Diode current, } I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right)$$

$$I_S \rightarrow \text{Saturation current}$$

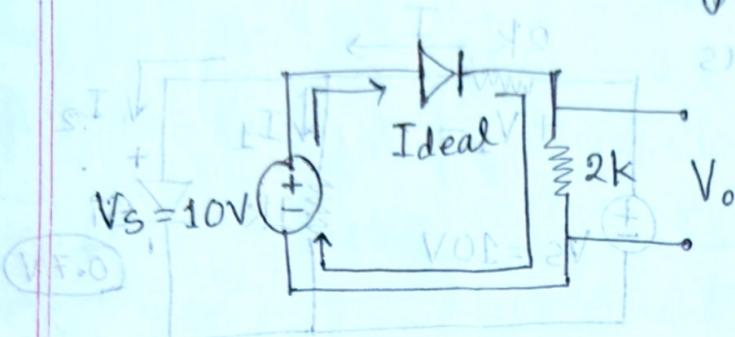
$$\frac{\text{Forward Bias}}{\text{Reverse Bias}} = \left(I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right) \right)$$

$V_D \rightarrow$ Applied Voltage (F-Bias)

$V_T \rightarrow$ Thermal Voltage

$\eta \rightarrow$ Identity factor (1 or 2) } $\eta \rightarrow 1 : \text{Ge}$
 depends on construction } $\eta \rightarrow 2 : \text{Si}$

Determine the voltage V_o



Soln:

Diode \rightarrow forward bias \rightarrow "ON"

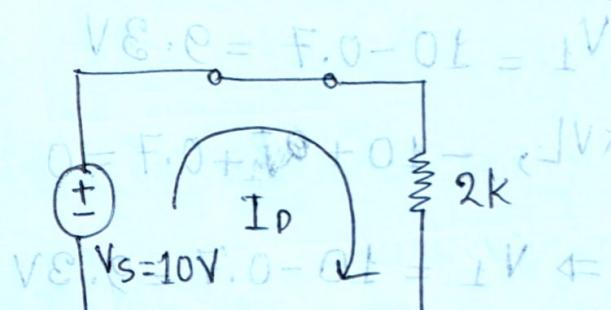
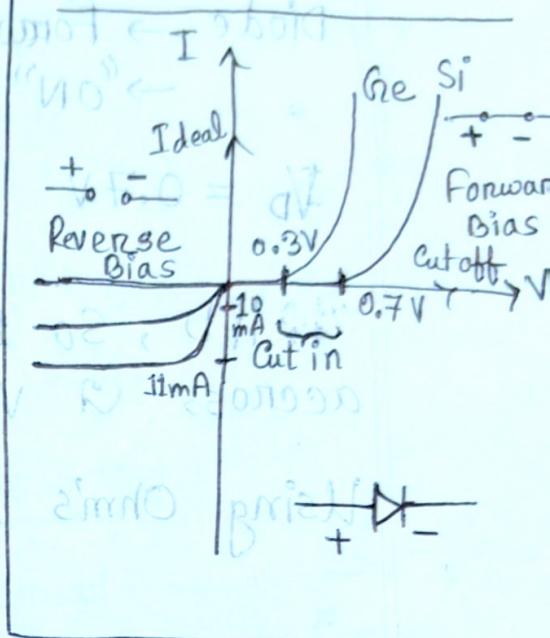
Ideal Diode, $V_D = 0V$

$$I_D = \frac{V_s}{2k} = \frac{10}{2k} \quad [Ohm's\ Law]$$

$$= 5\text{ mA}$$

$$\begin{aligned} V_o &= 2k \times I_D \\ &= 2k \times 5\text{ mA} \\ &= 10V \end{aligned}$$

I-V characteristic curve



$$A.m.e.d.a. P = \frac{V_o}{2k} = \frac{1V}{2k} = I$$

Reverse Diode এর ফেজে,

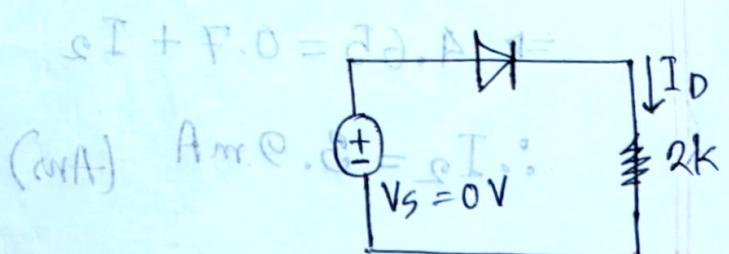
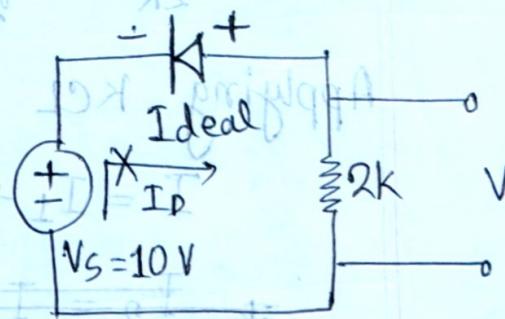
Diode \rightarrow Reverse bias \rightarrow "OFF"

$$I_D = 0A$$

$$V_o = 0V$$

Diode \rightarrow cut off

$$I_D = 0A$$

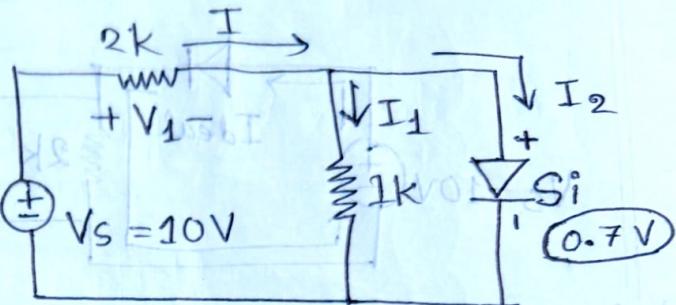


Determine I , I_1 , I_2 & V_1

Diode \rightarrow Forward bias
 \rightarrow "ON"

$$V_D = 0.7V$$

$1k \parallel D$, so $1k$ এর
 across $V = 0.7V$



Using Ohm's law, $I_1 = \frac{0.7}{1k} = 0.7mA$

$$V_1 = 10 - 0.7 = 9.3V$$

OR, KVL, $-10 + V_1 + 0.7 = 0$
 $\Rightarrow V_1 = 10 - 0.7 = 9.3V$

$$I = \frac{V_1}{2k} = \frac{9.3}{2} = 4.65mA$$

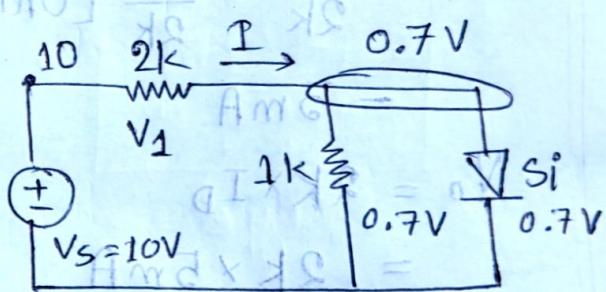
Applying KCL at node A,

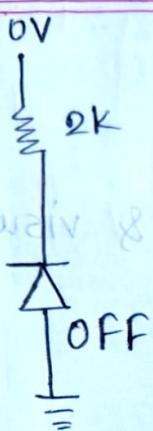
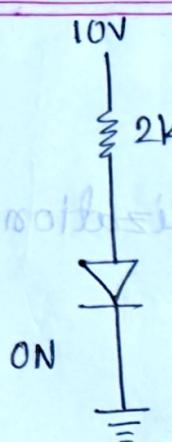
$$I = I_1 + I_2$$

$$\Rightarrow I_2 = I - I_1$$

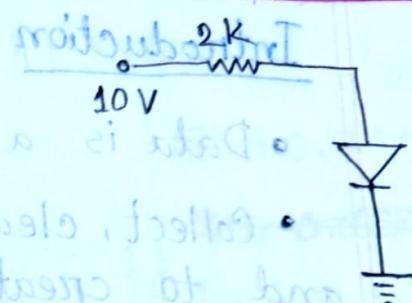
$$\Rightarrow 4.65 = 0.7 + I_2$$

$$\therefore I_2 = 3.9mA \quad (\text{Ans})$$





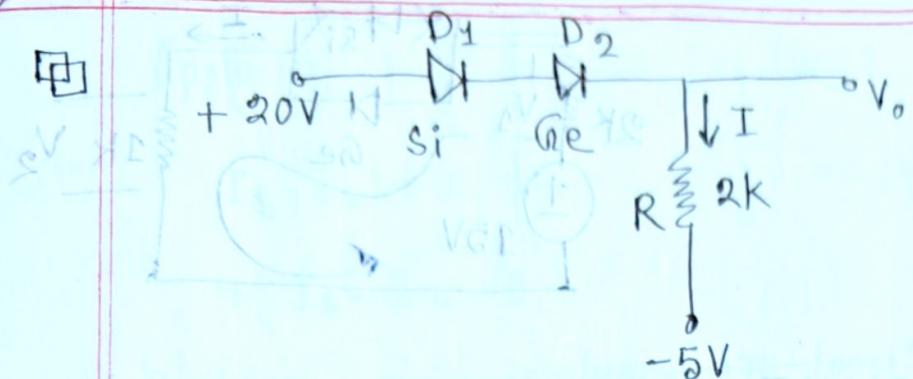
A hand-drawn circuit diagram on a piece of lined paper. It features a rectangular loop. On the left side, there is a battery symbol with '10V' written next to it. Above the top horizontal segment of the rectangle, there is a resistor symbol with '2K' written above it. To the right of the rectangle, there is an inductor symbol.



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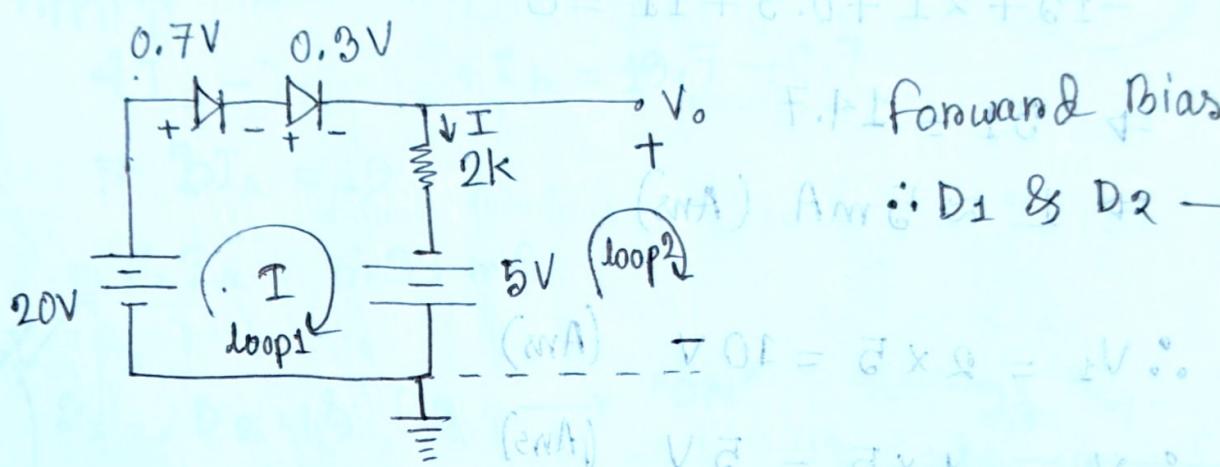
C.W
27/10/2024

Determine the current I & the voltage V_o



$$Si = 0.7V$$

$$Ge = 0.3V$$



KVL,

$$-20 + 0.7 + 0.3 + 2I - 5 = 0$$

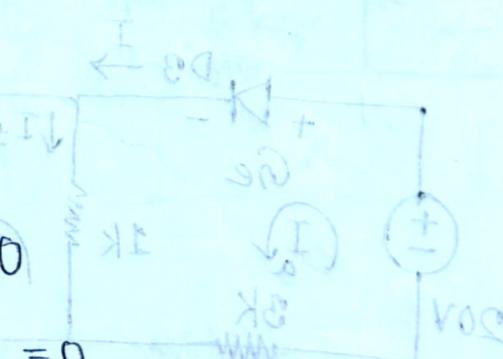
$$\Rightarrow 2I = 24$$

$$\Rightarrow I = 12 \text{ mA} \quad (\text{Ans})$$

$$\text{KVL in loop 2, } +5 - 2I + V_o = 0$$

$$\Rightarrow 5 - 24 + V_o = 0$$

$$\Rightarrow V_o = 19 \text{ V} \quad (\text{Ans})$$



F.C.L = $I_0 R_0 + I R_0 + G R_0 + Q_0$

Determine the current I & the voltage V_1 & V_2

Q) $D_1 \rightarrow \text{"OFF"}$

$D_2 \rightarrow \text{"ON"}$

Applying KVL,

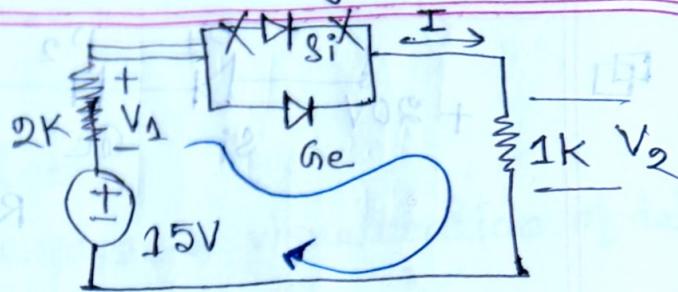
$$-15 + 2I + 0.3 + 1I = 0$$

$$\Rightarrow 3I = 14.7$$

$$\Rightarrow I \approx 5 \text{ mA} \quad (\text{Ans})$$

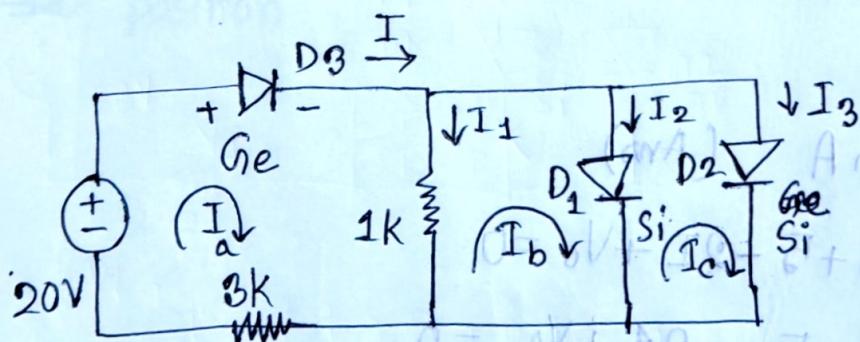
$$\therefore V_1 = 2 \times 5 = 10 \text{ V} \quad (\text{Ans})$$

$$\therefore V_2 = 1 \times 5 = 5 \text{ V} \quad (\text{Ans})$$



Determine the voltage V_1 & the currents I_1, I_2, I_3

Q)



Applying mesh analysis in loop 1,

$$-20 + 0.3 + I_a - I_b + 3I_a = 0$$

$$\Rightarrow 4I_a - I_b = 19.7$$

Applying mesh analysis in loop 2,

$$A_m F.O. \quad I_b - I_a + 0.7 = 0$$

$$\Rightarrow I_a - I_b = 0.7$$

Applying mesh analysis in loop 3,

$$4I_a - I_b - I_a + I_b = 19.7 - 0.7$$

$$\Rightarrow 3I_a = 19$$

$$\therefore I_a = 6.33 \text{ mA}$$

Wrong Answer

Soln:

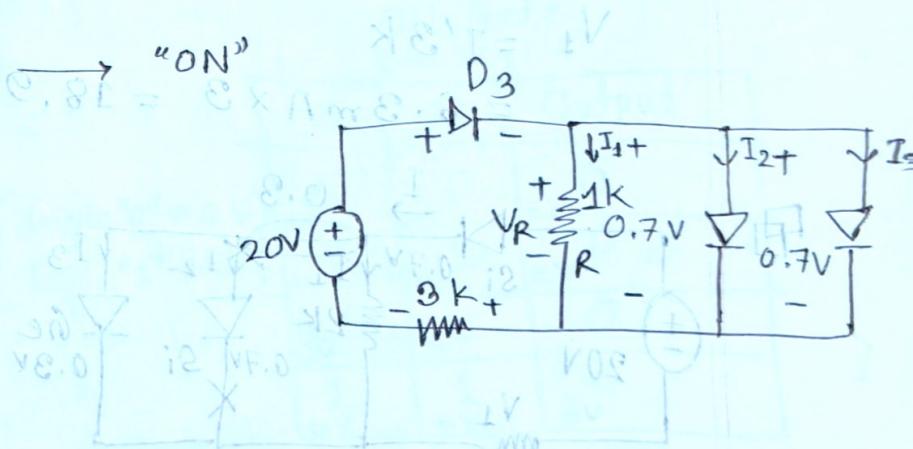
D_1, D_2 (as) D_3 V e.g. \rightarrow "ON"

$$V_{D_3} = 0.3V$$

$$V_{D_1} = V_{D_2} = 0.7V$$

Since, $R \parallel D_1 \parallel D_2$

$$V_R = V_{D_1} = V_{D_2} = 0.7V$$



Applying KVL, $-20 + V_{D_3} + V_R + V_1 = 0$

$$\Rightarrow -20 + 0.3 + 0.7 + I' 3k = 0$$

$$\therefore I' = 6.3 \text{ mA} = I$$

(Ans)

Applying KCL,

$$I = I_1 + I_2 + I_3$$

$$\Rightarrow I_2 + I_3 = I - I_1$$

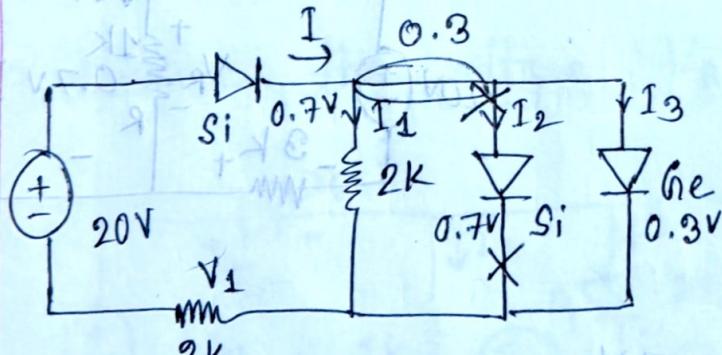
$$= 6.3 \text{ mA} - 0.7 \text{ mA}$$

$$= 5.6 \text{ mA}$$

$$I_2 = I_3 = \frac{5.6}{2} \text{ mA} = 2.8 \text{ mA} \quad (\text{Ans})$$

$$V_1 = I' 3K$$

$$= 6.3 \text{ mA} \times 3 = 18.9 \text{ V} \quad (\text{Ans})$$



KVL,

$$-20 + 0.7 + 0.3 + 2I = 0$$

$$\Rightarrow 2I = 19$$

$$\therefore I = 9.5 \text{ mA}$$

As D_2 = "OFF", $I_2 = 0 \text{ mA}$

Using Ohm's law,

$$0 = F_0, I_1 = \frac{0.7}{2K} = 0.7 \text{ mA}$$

$$F_0 = \alpha I - \nu I$$

$$= 6.3 \text{ mA} - 0.7 \text{ mA}$$

$$= 5.6 \text{ mA}$$

$$I_2 = I_3 = \frac{5.6}{2} \text{ mA} = 2.8 \text{ mA} \quad (\text{Ans})$$

$$A_m C_d = \alpha I$$

$$V_1 = I' 3K$$

$$= 6.3 \text{ mA} \times 3 = 18.9 \text{ V} \quad (\text{Ans})$$

$$\# V_1, I_1, I_2 \& I_3$$

$$VF_0 = 29 \text{ V} = 14 \text{ V}$$

$$29 / 14 = 2.07 \text{ A}$$

$$VF_0 = 29 \text{ V} = 29 \text{ V} = 2 \text{ V}$$

KVL in loop, CDR, $I_1 = \frac{20 \times 0.3}{2} = 0.15 \text{ mA}$

Applying KCL, $I = I_1 + I_3$

$$I_3 = I - I_1$$

$$\therefore I_3 = 0.5 - 0.15 = 0.35 \text{ mA}$$

$\therefore V_1 = 2 \times I = 2 \times 0.5 = 10 \text{ V}$

Slide-11

AND Gate

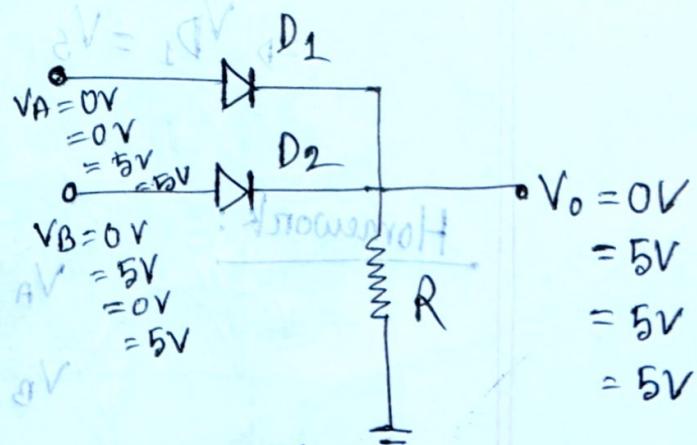
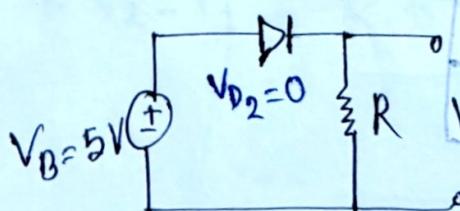
A	B	Output
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

{ logic "0" \rightarrow 0V }
 { logic "1" \rightarrow 5V }

A	B	Output
0V	0V	0V
0V	5V	5V
5V	0V	0V
5V	5V	5V

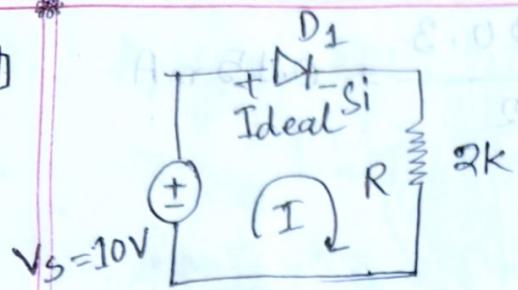
D_1 & $D_2 \rightarrow$ Ideal diode

$$V_{D1} \& V_{D2} \rightarrow 0V$$



This circuit is representing OR gate

Determine the load line for the following circuit and determine the Q-point.



Soln: Applying KVL, $-10 + 0.7 + 2I = 0$
 $\Rightarrow I = 4.65 \text{ mA}$

$$\text{Let } V_{D1} = 0V$$

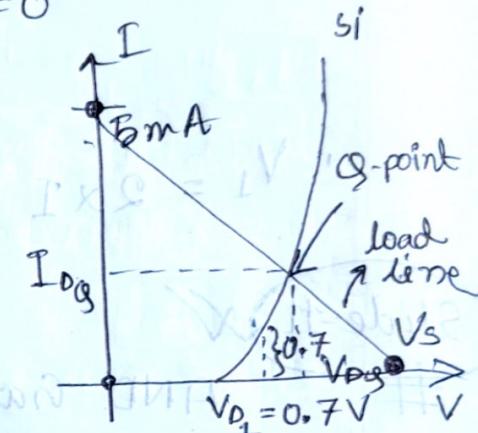
$$-Vs + VR = 0$$

$$\Rightarrow VR = Vs$$

$$\Rightarrow IR = Vs$$

$$\Rightarrow I = \frac{Vs}{R}$$

$$= \frac{10}{2} = 5 \text{ mA}$$



Let, $I = 0A$, From eqn ①

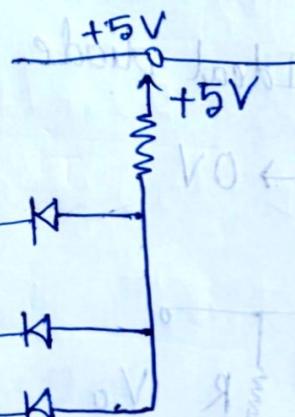
$$-Vs + V_{D1} + IR = 0$$

$$\Rightarrow -Vs + V_{D1} = 0$$

$$[IR = 0]$$

$$\Rightarrow V_{D1} = Vs$$

Homework:

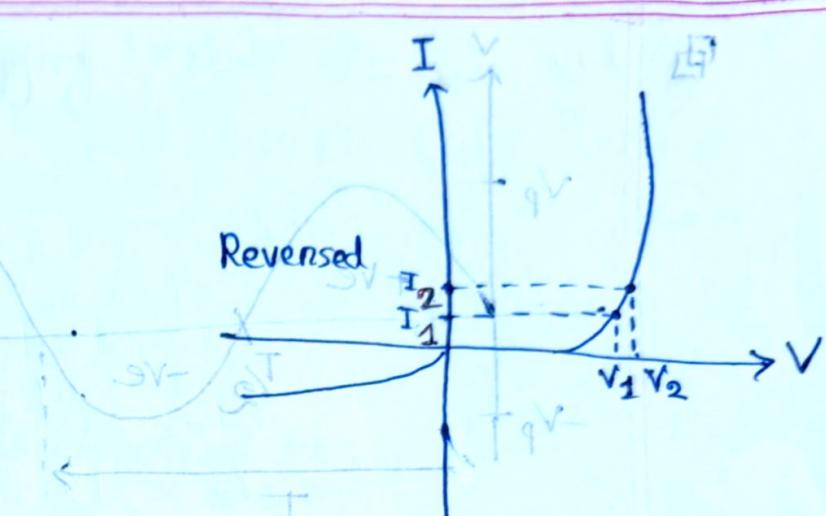


29/10/24

$$I = I_b \left(e^{\frac{V_D}{nV_T}} - 1 \right)$$

$$= I_s e^{\frac{V_D}{nV_T}} - I_s$$

Forward Bias Reverse Bias



V_T = Thermal Voltage

$$\therefore V_T = \frac{kT}{q} = 25.5 \approx 26 \text{ mV}$$

Let, $n = 1$

$$\therefore I_1 = I_s e^{\frac{V_1}{V_T}}$$

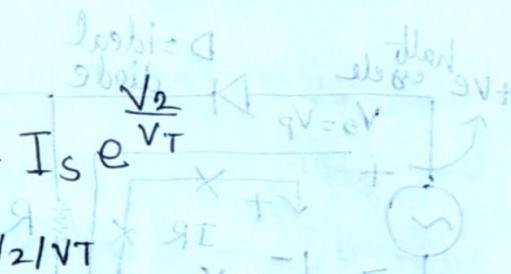
$$\therefore \frac{I_2}{I_1} = \frac{I_s e^{\frac{V_2}{V_T}}}{I_s e^{\frac{V_1}{V_T}}} = \frac{e^{\frac{V_2}{V_T}}}{e^{\frac{V_1}{V_T}}}$$

$$\Rightarrow \frac{I_2}{I_1} = \frac{e^{\frac{V_2}{V_T}}}{e^{\frac{V_1}{V_T}}}$$

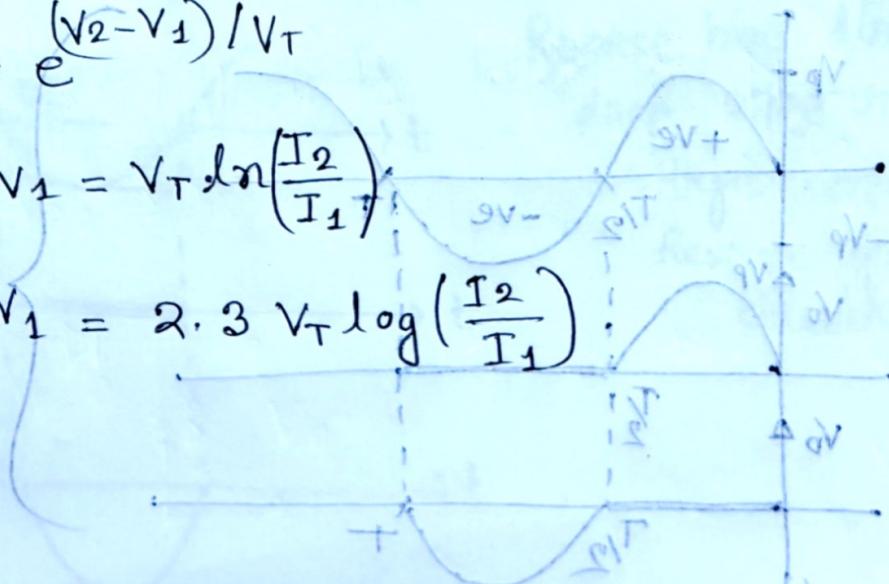
$$\Rightarrow \frac{I_2}{I_1} = e^{\frac{(V_2 - V_1)}{V_T}}$$

$$\Rightarrow V_2 - V_1 = V_T \ln \left(\frac{I_2}{I_1} \right)$$

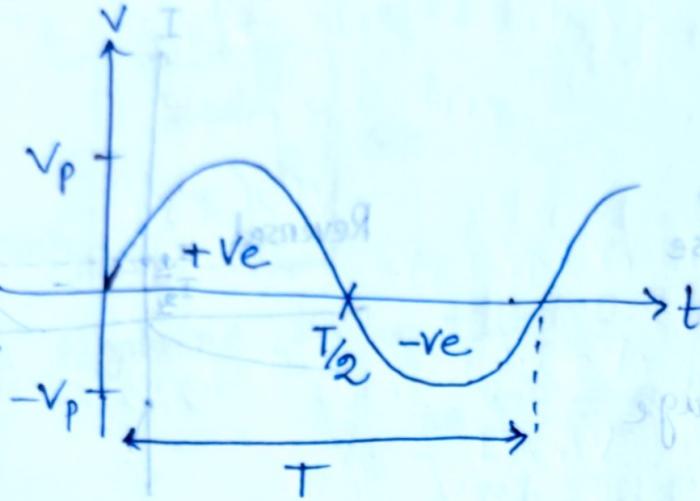
$$\Rightarrow V_2 - V_1 = 2.3 V_T \log \left(\frac{I_2}{I_1} \right)$$



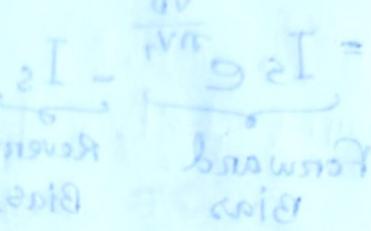
Hence, Reverse Bias



Q

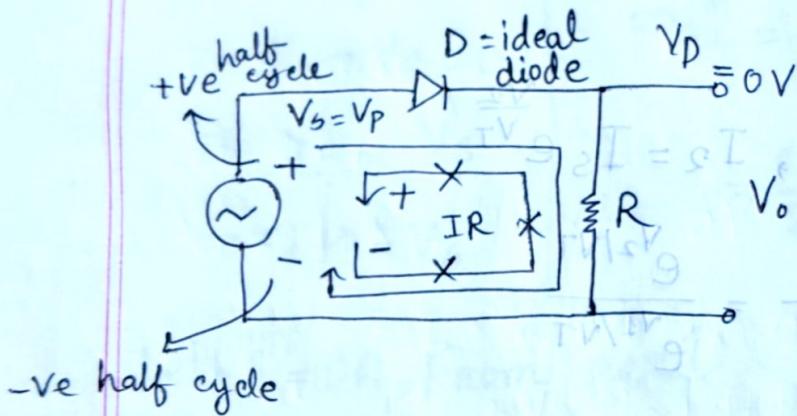


($\omega = \text{angular frequency}$)



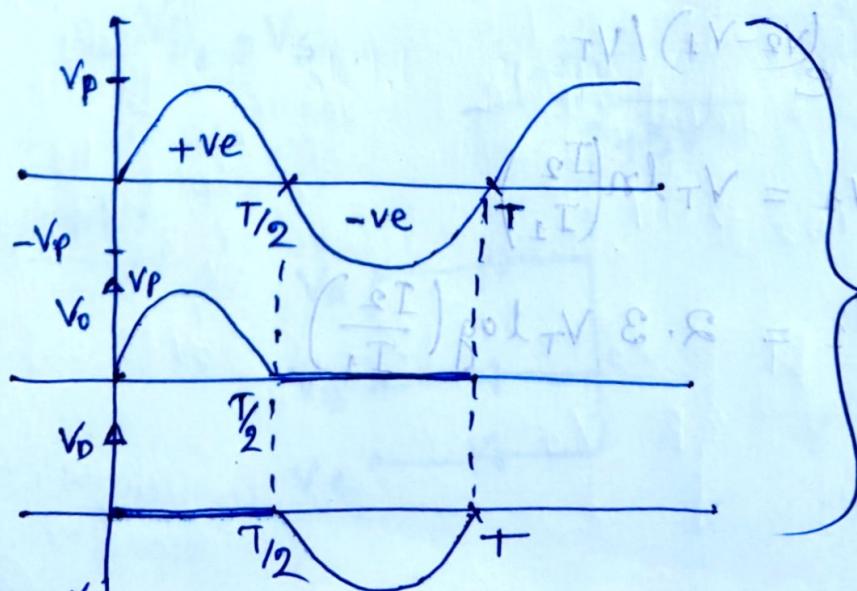
* For +ve half cycle
 $D \Rightarrow$ forward bias

* For -ve half cycle
 $D \Rightarrow$ Reverse bias



Q

Halfwave Rectifier:



halfwave
Rectifier
Circuit

For, +ve half cycle, Applying KVL,

$$-V_p + V_D + V_o = 0$$

$$\Rightarrow V_o = V_p - V_D$$

$$\therefore V_o = V_p$$

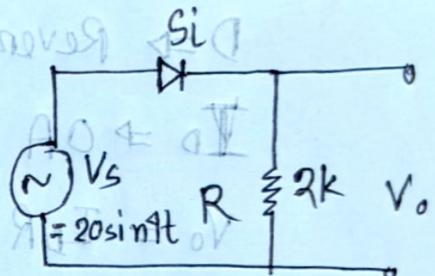
For, negative (-ve) half cycle, Applying KVL,

$$V_S + V_D + V_o = 0$$

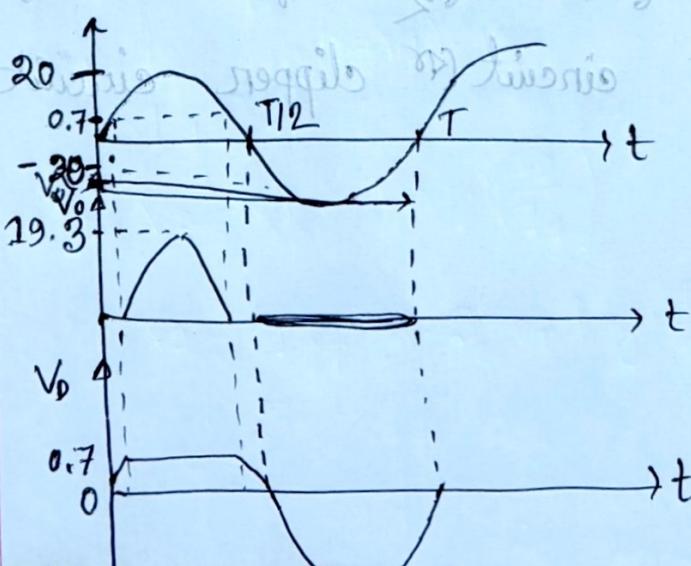
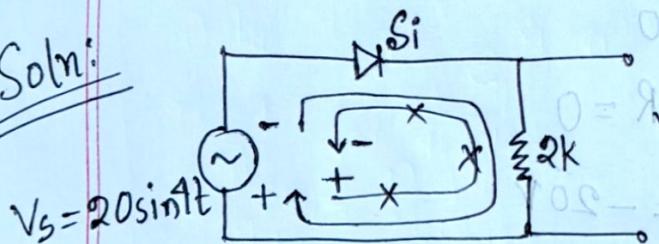
$$\Rightarrow V_o = -V_S = -V_p$$

Hence, $IR = 0, V_o = I$

- # Determine the output voltage V_o and sketch the wave forms across the output resistance and diode



Soln:



Reverse bias fixed voltage drop রিভার্স বিয়েজ টাইমেন্ডেন্স
Voltage রিভার্স বিয়েজ
Reverse bias এ open circuit

For +ve half cycle ($0 - T/2$)

D \Rightarrow Forward bias

$$V_D = 0.7V$$

\therefore Applying KVL, $-V_s + V_D + V_o = 0$

$$\Rightarrow -20 + 0.7 + V_o = 0$$

$$\therefore V_o = 19.3V$$

For (-ve) half cycle ($T/2 - T$)

D \Rightarrow Reverse bias

$$I_D \Rightarrow 0A$$

$$V_o = I_D R = 0 \times 2K = 0V$$

\therefore Applying KVL, $V_s + V_D + V_o = 0$

$$\Rightarrow V_s + V_D + I_D R = 0$$

$$\Rightarrow V_D = -V_s = -20V$$

* Diode দ্বারা অংশ কেটে যাওয়া আর একটা অংশ

যেটো যাওয়া এই ধরনের circuit কে clipper circuit বলে।

পুরো ডায়ড

ব্যবহার করে

বিনাস

