



EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Final Examination, Fall 2021

Course: CSE360 – Computer Architecture, Section 3
Instructor: Md. Nawab Yousuf Ali, PhD, Professor, CSE Department
Full Marks: 25
Exam Time: 1 Hour 20 Minutes **Submission Time:** 10 Minutes

Note: There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin.

1. Convert the expression $(A*B) + ((C-D) * E+F)/G - H$ to postfix notation using Dijkstra's algorithm. Show the sequence of steps in the stack. [CO2, C3, Mark: 3]
2. Compute the following expression using stack. [CO2, C3, Mark: 3]
 $(A*B) + (C+D) * E+F$
3. Analyze and Compare zero-, one-, two-, and three- address machines by writing programs to compute the following expression for each of the four machines. [CO3, C5, Mark: 5]

$$X = \frac{A - B / C}{D + E * F}$$

The instructions available for use are as follows:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOV ($X \leftarrow Y$)	MOVE ($X \leftarrow Y$)
POP M	STORE M	ADD($X \leftarrow X+Y$)	ADD($X \leftarrow Y+Z$)
ADD	ADD M	SUB ($X \leftarrow X-Y$)	SUB($X \leftarrow Y-Z$)
SUB	SUB M	MUL ($X \leftarrow X * Y$)	MUL($X \leftarrow Y * Z$)
MUL	MUL M	DIV($X \leftarrow X/Y$)	DIV($X \leftarrow Y/Z$)
DIV	DIV M		

4. A nonpipelined processor has a clock rate of 2.9 GHz and an average CPI (Clock per instruction) of 5. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays the clock rate of the new processor has to be reduced to 2.3 GHz. [CO3, C3 Mark: 2+2]
 - a. What is the speed up achieved for a program with 200 instructions?
 - b. What is the MIPS rate for each processor?

5. Assume a pipeline with five-stages: fetch instruction (FI), decode instruction (DI), calculate addresses (CA), fetch operand (FO), and execute instruction (EI). Draw a diagram for a sequence of 8 instructions, in which the second instruction is a branch that effects on instruction pipeline operation in which there are no data dependencies. [CO4, C4, Mark: 4]
6. Consider a 16-bit processor in which the following appears in main memory, starting at location 322: [CO4, C4, Mark: 6]

322	Load to AC	Mode
323	631	
324	Next instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R3, which has a value of 399. There is also a base register that contains the value 150. The value of 631 in location 323 may be part of the address calculation. Assume that location 437 contains the value 808, location 438 contains the value 809, and so on. Determine the effective address and the operand to be loaded for the following address modes.

- Immediate
- Direct
- Indirect
- PC relative
- Displacement
- Register
- Register indirect.
- Autoindexing with increment, using R3