



EAST WEST UNIVERSITY

Department of Computer Science and Engineering B.Sc. in Computer Science and Engineering Program Mid Term I Examination, FALL 2020

Course: CSE360 – Computer Architecture, Section-3
Instructor: Md. Nawab Yousuf Ali, PhD, Professor, CSE Department
Full Mark: 25
Time: 1 Hour and 20 Minutes

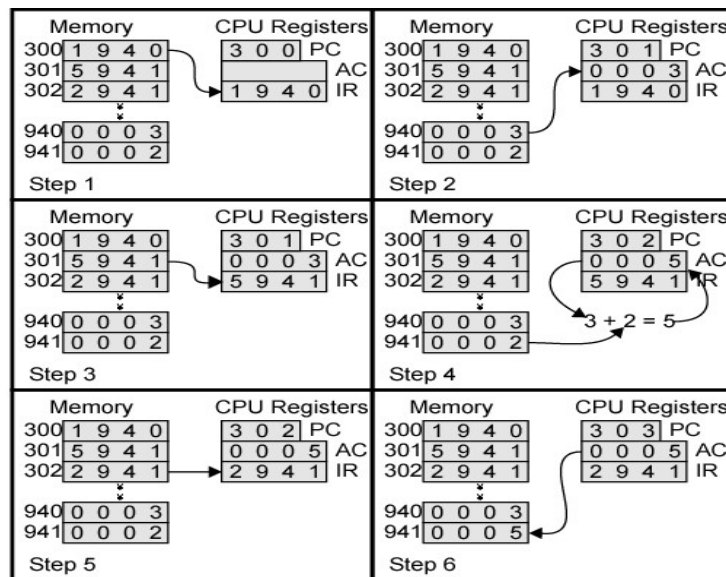
Note: There are FIVE questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

1. The hypothetical machine has two instructions: [CO1, C2, Mark: 7]
 0011 = Load AC from I/O
 0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:

- Load AC from device 7
- Add contents of memory location 940
- Store AC to device 9

Assume that the next value retrieved from device 7 is 3 and that location 940 contains a value of 2



2. Consider a hypothetical microprocessor generating a 32-bit address (for example, assume that the program counter and the address register are 32-bits wide) and having 32-bit data bus. [CO1, C2, Mark: 2+3]
- What is the maximum memory address space that the processor can access directly if it is connected to a “16-bit memory”?
 - If an input and output instruction can specify a 16-bit I/O port number, how many 16-bit I/O port can the microprocessor support? How many 32-bit I/O ports? Explain.

3. When a CPU operates at a clock frequency of 3.5GHz, requires an average of 27 CPI for executing one instruction, **what** is the performance (in MIPS) of the CPU? [CO1, C3, Mark: 3]
4. Consider a 64-bit microprocessor, with a 32-bit external data bus, driven by an 16-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. [CO1, C3, Mark: 2+ 3]
 - a) **What** is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s?
 - b) To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain.
5. Consider a hypothetical 64-bit microprocessor having 64-bit instructions composed of two fields: the first two byte contains the opcode and the remainder the immediate operand or an operand address. [CO2, C3, Mark: 2+3]
 - a. **What** is the maximum directly addressable memory capacity (in bytes)?
 - b. How many bits are needed for the program counter and the instruction register?