May 4, 2021

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Assessment 02, Spring 2021

Course: **CSE360 – Computer Architecture, Section 3**
Instructor: **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department**
Full Marks: **20**
Time: **1 Hour 40 Minutes**

Note: There are FIVE questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin.

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1. Assume that the access time is 35 ns and the recharge time is 55 ns. [CO2, C3, Mark: 2+2]
   a) What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 2-bit output?
   b) Constructing a 64-bit memory system using these chips yields what data transfer rate?

2. Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes six bus clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers two bytes of information between memory and I/O devices. [CO2, C3, Mark: 2+2+3]
   a) Suppose we clock the 8237A at a rate of 3.25 MHz. How long does it take to transfer one byte?
   b) What would be the maximum attainable data transfer rate?
   c) Assume that the memory is not fast enough, and we have to insert four wait states per DMA cycle. What will be the actual data transfer rate?

3. A 62-bit computer has five selector channels and one multiplexor channel. Each selector channel supports four magnetic disk and three magnetic tape units. The multiplexor channel has three-line printers, four card readers, and 11 VDT terminals connected to it. Assume the following transfer rate: [CO2, C5, Mark:3]

   Disk drive: 650 Kbytes/sec
   Magnetic tape drive 176 Kbytes/sec
   Line printer 4.6 Kbytes /sec
   Card reader: 2.1 Kbytes/sec
   VDT: 1.35 Kbytes/sec
   Estimate the minimum aggregate I/O transfer rate in this system.

4. Consider a magnetic disk drive having the following specifications. [CO2, C5, Mark: 3]

Rotational speed	8550 rmp
Transfer rate	33 MB/Sec
Average seek time	45 milliseconds

   What is the average time to read a data block of 2500 bytes?

5. A DMA controller transfers 128-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 9600 characters per second. The CPU is fetching and executing instructions at an average rate of four million instructions per second. By how much will the CPU be slowed down because of the DMA transfer? [CO2, C6, Mark: 3]