

Chapter 2

"Instructions : Language of the Computer"

Exercise Solution

→ 2.1:

Ans: $f = g + (h - 5);$

addi f, h, -5

add f, g, f

→ 2.2:

Ans: add f, g, h

add f, i, f

$f = i + (g + h)$

→ 2.3:

Ans:

$B[8] = A[i - j]$

sub \$t0, \$s3, \$4

sll \$t0, \$t0, 2

add \$t0, \$s6, \$t0

lw \$t1, 0(\$t0)

sw \$t1, 32(\$s7)

→ 2.4:

Ans: 1. $\text{slr } \$t0, \$s0, 2 \quad \# \ \$t0 = f \times 4;$

2. $\text{add } \$t0, \$s6, \$t0 \quad \# \ \$t0 = SA[f];$

3. $\text{slr } \$t1, \$s1, 2 \quad \# \ \$t1 = g \times 4$

4. $\text{add } \$t1, \$s7, \$t1 \quad \# \ \$t1 = SB[g];$

5. $\text{lw } \$s0, 0(\$t0) \quad \# \ f = A[F];$

6. $\text{addi } \$t2, \$t0, 4 \quad \# \ \$t2 = A[f+1];$

7. $\text{lw } \$t0, 0(\$t2) \quad \# \ \$t0 = A[F+1];$

8. $\text{add } \$t0, \$t0, \$s0 \quad \# \ \$t0 = A[F+1] + A[F];$

9. $\text{sw } \$t0, 0(\$t1) \quad \# \ B[g] = A[F+1] + A[F];$

Overall $B[g] = A[F+1] + A[F];$

→ 2.5:

Ans: In the above MIPS code we can only remove the line 6 and modify line 7 by

7. $\text{lw } \$t0, 4(\$t0)$

8. $\text{add } \$t0, \$t0, \$s0$

9. $\text{sw } \$t0, 0(\$t1)$

→ 2.7:

Ans: value → 0xabcdef12

Little Endian	
Address	Data
3	ab
2	cd
1	ef
0	12

Big Endian	
Address	Data
3	12
2	ef
1	cd
0	ab

→ 2.6:

Ans:

0xabcdef12 in decimal → 2862400018

→ 2.5:

Ans:

$$B[8] = A[i] + A[j];$$

$\text{all } \$t0, \$s3, 2 \quad \# \$t0 = i \times 4$
 $\text{add } \$t0, \$t0, \$s6 \quad \# \$t0 = 8A[i]$
 $\text{lw } \$t0, 0(\$t0) \quad \# \$t0 = A[i]$
 $\text{seel } \$t1, \$s4, 2 \quad \# \$t1 = j \times 4$
 $\text{add } \$t1, \$t1, \$s6 \quad \# \$t1 = A[j]$
 $\text{lw } \$t1, 0(\$t1) \quad \# \$t1 = A[j]$

add \$t0, \$t0, \$t1 # $t0 = A[i] + A[j]$
 sw \$t0, 32(\$t7) # $B[8] = A[i] + A[j]$.

→ 2.10:

Ans:

addi \$t0, \$s6, 4 # $t0 = A[i]$
 add \$t1, \$s6, \$0 # $t1 = A[0]$
 sw \$t1, 0(\$t0) # $t0 = A[0]$
 lw \$t0, 0(\$t0) # $t0 = A[0]$
 add \$s0, \$t1, \$t0 # $f = A[0] + A[0]$
 $f = A[0] + A[0]$

→ 2.11:

Ans:

	type	opcode	reg	rd	rd	immed
addi \$t0, \$s6, 4	I-type	8	22	8		4
add \$t1, \$s6, \$0	R-type	0	22	0	9	
sw \$t1, 0(\$t0)	I-type	43	8	9		0
lw \$t0, 0(\$t0)	I-type	35	8	8		0
add \$s0, \$t1, \$t0	R-type	0	9	8	16	

→ 2.12.1:

Ans:

\$50 → 0x80000000

\$61 → 0xD0000000

∴ add \$t0, \$50, \$61

value of \$t0 → 0x150000000

→ 2.12.2:

Ans:

the result in \$t0 is overflow

→ 2.12.3:

Ans:

sub \$t0, \$50, \$61

0xB0000000

→ 2.12.4:

Ans:

~~the~~ No overflow

→ 2.12.5:

Ans:

0x1D0000000.

→ 2.13.6:

Ans: Overflow.

→ 2.13.1:

Ans:

add \$t0, \$s0, \$s1

The memory allocated to one instruction is 4 bytes

The range of numbers can be calculated as 2^{n-1}

$$n = 32$$

$$\therefore \text{The range is } 2^{31} \text{ to } -2^{31} \\ = 2,147,483,647 \text{ to } -2,147,483,647$$

$$\therefore \text{Range of } \$s1 = 2,147,483,647 - 128 \\ = 2,147,483,519$$

→ 2.13.2

Ans:

sub \$t0, \$s0, \$s1

$$\text{Range of } \$s1 = 128 - 2,147,483,647 \\ = -2,147,483,519$$

→ 2.13.3:

Ans:

sub \$t0, \$s1, \$s0

$$\text{range of } \$s1 = -2147483648 + 128 \\ = -2147483520$$

→ 2.16:

Ans: sub \$t3, \$s3, \$v0
 $op = 0$, $rs = 3$, $rd = 2$, $rd = 3$, $shamt = 0$, $func = 34$

$$\begin{array}{r} 000000 \\ \hline 0 \end{array} \quad \begin{array}{r} 00011 \\ \hline 3 \end{array} \quad \begin{array}{r} 00010 \\ \hline 2 \end{array} \quad \begin{array}{r} 00011 \\ \hline 3 \end{array} \quad \begin{array}{r} 00000 \\ \hline 0 \end{array} \quad \begin{array}{r} 100010 \\ \hline 34 \end{array}$$

$op = 6bit$ $rs = 5bit$ $rd = 5bit$ $rd = 5bit$ $shamt = 5bit$ $func = 6bit$

→ 2.17:

Ans:

lw \$v0, 4(\$v1)

$$op = 0x23, rs = 1, rd = 2, const = 0x4$$

$$\begin{array}{r} \overset{32}{1} \overset{16}{0} \overset{8}{0} \overset{4}{0} \overset{2}{0} \overset{1}{1} \\ 100011 \\ \hline 0x23 \end{array} \quad \begin{array}{r} 00001 \\ \hline 1 \end{array} \quad \begin{array}{r} 00010 \\ \hline 2 \end{array} \quad \begin{array}{r} 0000 \quad 0000 \quad 0000 \quad 0100 \\ \hline 0x4 \end{array}$$

→ 2.18.1:

Ans: In R type instructions, opcode would be 8 bits, rs, rt, rd, fields would be 7 bits each.

→ 2.18.2:

Ans: In the I type instructions, opcode would be 8 bits, rs, rt would be 7 bits each.

→ 2.19:

Ans: slt \$t2, \$t0, 41

The instructions performs the logical left shift on \$t0. but shift 41 not reg. ligible because we can ^{use} only 32 registers in this case shift 30 and 14. The value of \$t2

$\$t2 = 0xAAAAAAAA$

or

\$t2, \$t2, \$t1

Now the value of \$t2 and \$t2 perform the logical operation OR and store in \$t2

AAAAAAAA OR 12345678

$\$t2 = 0xBABEFFFF$

→ 2.19.2:

Ans: srl \$t2, \$t0, 4

The ins srl will make the logical right shift on \$t0. Then the value of \$t2

$$\$t2 = 0xAAAAAAAA0$$

andi \$t2, \$t2, -1

The value of \$t2 will perform the logical operations

AND with immediate -1

$$\$t2 = AAAAAAAAA0$$

→ 2.19.3:

Ans: srl \$t2, \$t0, 3

The ins srl will make the logical right shift on \$t0. Then the value of \$t2

$$\$t2 = 0x15555555$$

andi \$t2, \$t2, 0xFFFF

Now the value of \$t2 will perform the logical AND with 0xFFFF ; 0x15555555 AND 0xFFFF

$$\$t2 = 00005515$$

→ 2.25.1:

Ans: if type.

→ 2.25.2:

Ans: addi \$t2, \$t2, -1

beq \$t2, \$0, loop

→ 2.26.1:

Ans: 20

→ 2.26.2:

Ans:

i = 20;

do {

B += 2;

i = i - 1;

} while (i > 0)

→ 2.26.3:

Ans: $B * N$

→ 2.20:

Ans:

strl \$t0, \$t0, 11

strl \$t0, \$t0, 26

ori \$t2, \$0, 0x03ff

sll \$t2, \$t2, 16

ori \$t2, \$t2, 0xffff

and \$t1, \$t1, \$t2

or \$t1, \$t1, \$t0

→ 2.21:

Ans:

nor \$t1, \$t2, \$t2

→ 2.22:

Ans:

lw \$t3, 0(\$s1)

sll \$t1, \$t3, 4

→ 2.23:

Ans:

\$t2 = 3

→ 2.24:

Ans:

Jump! no, beg: no

→ 2.29:

Ans:

```
for(i=0; i<100; i++) {  
    result += MemArray[50];  
    50 = 50 + 4;  
}
```

→ 2.30:

Ans:

```
addi $t1, $50, 400  
Loop: lw $s1, 0($t1)  
      add $s2, $s2, $s1  
      addi $t1, $t1, -4  
      bne $t1, $50, Loop.
```

→ 2.32:

Ans: Due to the recursive nature of the code,
it is not possible for the compiler to in line
the function call.

→ 2.27:

addi \$t0, \$0, 0

beq \$0, \$0, TEST1

LOOP1: addi \$t1, \$0, 0

beq \$0, \$0, TEST2

LOOP2: add \$t3, \$t0, \$t1

sll \$t2, \$t1, 4

add \$t2, \$t2, \$t3

sw \$t3, (\$t2)

addi \$t1, \$t1, 1

TEST2: sll \$t2, \$t1, \$t1

bne \$t2, \$0, LOOP2

addi \$t0, \$t0, 1

TEST1: sll \$t2, \$t0, \$t0

bne \$t2, \$0, LOOP1

→ 2.28:

Ans: 14 instructions to implement and 158 instructions executed

→ 2.35:

Ans: We can use the tail-call optimization for the second call to func. but then we must restore $\$ra$, $\$s0$, $\$s1$ and $\$bp$ before that call. We save only one instructions ($\$ra$, $\$s0$)

→ 2.38:

Ans: 0×00000011

→ 2.39:

Ans: Generally all solutions are similar:

lui $\$t1$, top-16-bits:

ori $\$t1$, $\$t1$, bottom 16-bits.

→ 2.40:

Ans: No jump can go up to $0 \times 0FFFFFFFC$

→ 2.41:

Ans: No, range is $0 \times 604 + 0 \times 1FFFC = 0 \times 00020604$
to $0 \times 604 - 0 \times 20000 = 0 \times FFFE0604$.

→ 2.42:

Ans: Yes range is $0x1FFFF004 + 0x1FFFC$

$$= 0x2001F000 \text{ to } 0x1FFFF004$$

$$- 0x20000 = 1FFDF004.$$

→ 2.45:

Ans: It is possible for one or both processors to complete this code without ever reaching the SC instructions. If only one executes SC, it completes successfully. If both reach SC, they do so in the same cycle, but one SC completes first and then the other selects this and fails.

→ 2.46.2:

Ans: 167.64%, 1113.43%

→ 2.47.1:

Ans: 2.6

→ 2.47.2:

Ans: 0.88

→ 2.47.3:

Ans: 0.5333333333.