December 6, 2020

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term II Examination, Fall 2020

Course: **CSE360 – Computer Architecture, Section 3**
Instructor: **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department**
Full Marks: **25**
Time: **1 Hour 20 Minutes**

Note: There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin.

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1. A two-way set-associative cache has lines of 64 bytes and a total size of 16 Kbytes. The 128-Mbyte main memory is byte addressable. Show the format of main memory addresses. [CO2, C3, Mark: 3]

2. Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes four bus clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers one byte of information between memory and I/O devices [CO2, C3, Mark: 2+2+3]
   a. Suppose we clock the 8237A at a rate of 3.5 MHz. How long does it take to transfer one byte?
   b. What would be the maximum attainable data transfer rate?
   c. Assume that the memory is not fast enough and we have to insert three wait states per DMA cycle. What will be the actual data transfer rate?

3. Consider a hard disk drive having the following specifications [CO2, C5, Mark:2+3]

Rotational speed	5000 RPM
Transfer rate	50 MB/sec
Average seek time	35 milliseconds
Controller overhead	2.5ms

   a) Calculate the average rotational latency.
   b) `What is the average time to read 2.5 KB of data?

4. Consider a memory system with the following parameters: [CO2, C3, Mark: 1+1+3]
   Tc = 150 ns Cc = 10^-6 $/ bit
   Tm = 1500 ns Cm = 10^-7 $/ bit
   a. What is the cost of 2 MByte of main memory?
   b. What is the cost of 2.5 MByte of main memory using cache memory technology?
   c. If the effective access time is 25% greater than the main memory access time, what is the hit ratio H?

5. Assume that the access time is 120ns and the recharge time is 80ns. [CO2, C6, Mark: 1+2+2]
   a. What is the memory cycle time?
   b. What is the maximum data rate this DRAM can sustain, assuming a 2-bit output?
   c. Constructing a 64-bit memory system using these chips yields what data transfer rate?

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