UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Fall 1404
Computer Assignment 2
Gate Structures and Expressions in SystemVerilog
Week 6

Name:
Date:

1. Using the NAND gates of Problem 1 of Computer Assignment 1, generate a 2-to-1 MUX with a select input, *s*, two data inputs *a* and *b*, and an enable input, *e*. Use the expression *y = e ? (a&~s) | (b&s) : 1'b0* for the multiplexer *y* output. Use inverters as needed with delay values that are based on the transistors of Assignment 1. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making *To1* and *To0*. Make sure the time distance between your input changes is much larger than the gate delay values. As part of your test data apply a situation where a single change causes a glitch on the output.

2. Take the worst-case delay values from the above problem and back-annotate the delay values into the multiplexer expression of the above problem using an **assign** statement. In a testbench simulate the structure of the previous problem alongside with the **assign** statement of this problem and report the differences. Be able to explain the delay values that you are getting.

3. Using the three-state NAND gate of Problem 2 of Computer Assignment 1, and NAND gates from Problem 1, generate a 2-to-1 MUX with a select input, *s*, data inputs *a* and *b*., and an output-enable input, *oe*. Use the expression *y = oe ? (a&~s) | (b&s) : 1'bZ* for the multiplexer *y* output. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making *To1* and *To0* transitions. Make sure the time distance between your input changes is much larger than the gate delay values. As part of your test data apply a situation where a single change causes a glitch on the output.

4. Take the worst-case delay values from the above problem and back-annotate the delay values into a multiplexer expression using an **assign** statement. In a testbench simulate the structure of the previous problem alongside with the **assign** statement of this problem and report the differences. Be able to explain the delay values that you are getting.

5. In a testbench, instantiate the MUX circuits of Part 1 and Part 3 and compare the timing and output values of these circuits. Explain the differences between these two circuits as far as the number of transistors and other physical parameters such as power consumption.

Deliverables:

Generate a report that includes item discussed below for each of the five parts of this CA.

A. Show the circuit diagram that you are analyzing. Show gates and/or transistors according to the specified delays.
B. Hand-simulate the circuit you have shown in Part A and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show your SystemVerilog description of the design you are simulating and the testbench for it. Best is to use the Snip tools to get the image from Notepad++. This way you see all keywords and indentations. Make sure your SV codes are properly indented and all line-up rules are followed.
D. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
E. When simulation is complete, or even if you have a partial simulation, include an image of the output waveform showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.