UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Fall 1404
Computer Assignment 5
Mealy/Moore State Machines, Pre- and Post-Synthesis
Week 24

Name:	Date:

A sequenced detector circuit searches on its *serIn* input for a start sequence of **10110**. When the start sequence is received, the detected output (*detOut*) is asserted. The initial state of this circuit is where the search begins for the next sequence.

a. Write a complete behavioral SystemVerilog description of a Moore machine that detects the **10110** sequence. Use an asynchronous reset and positive edge of the clock. This is your pre-synthesis design of the Moore **10110** detector.
   i. Using a SystemVerilog testbench in ModelSim completely simulate your circuit. This is your pre-synthesis description.
   ii. Import your Moore design in Quartus and build a symbol for it. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of your Moore **10110** detector. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
   iii. Instantiate the pre- and post-synthesis descriptions of the Moore machine in a SystemVerilog testbench and compare the timing of the two descriptions.

b. Write a complete behavioral SystemVerilog description of a Mealy machine that detects the **10110** sequence. Use an asynchronous reset and positive edge of the clock. This is your pre-synthesis design of the Mealy **10110** detector.
   i. Using a SystemVerilog testbench in ModelSim completely simulate your circuit. This is your pre-synthesis description.
   ii. Import your Moore design in Quartus and build a symbol for it. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of your Moore **10110** detector. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
   iii. Instantiate the pre- and post-synthesis descriptions of the Mealy machine in a SystemVerilog testbench and compare the timing of the two descriptions.

c. Write a SystemVerilog testbench to simultaneously test the post-synthesis descriptions of the Mealy and Moore machines.
   i. Instantiate the post-synthesis descriptions of the Moore machine alongside with that of the Mealy machine in a SystemVerilog testbench and compare the timing of the two descriptions.
   ii. Use input sequences that will create pulses on the output of the Mealy machine and not on the Moore machine output.

Deliverables:

Generate a report that includes all the items below:

A. Prior to coming to the lab, for all the above problems hand-drawn schematic diagrams and partial timing diagrams are required. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA.

B. Document your Quartus projects of Parts a and b. Make sure you understand the synthesis outputs and their corresponding timings.

C. For Part a and Part b, you should look at the FPGA layouts, device view and RTL view. Be able to explain the details of various views. In the layout, be able to identify FPGA cells that use a memory element versus those that are purely combinational.

D. For Part c, show waveforms and explain the differences between the output of the Moore machine and that of the Mealy machine.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.