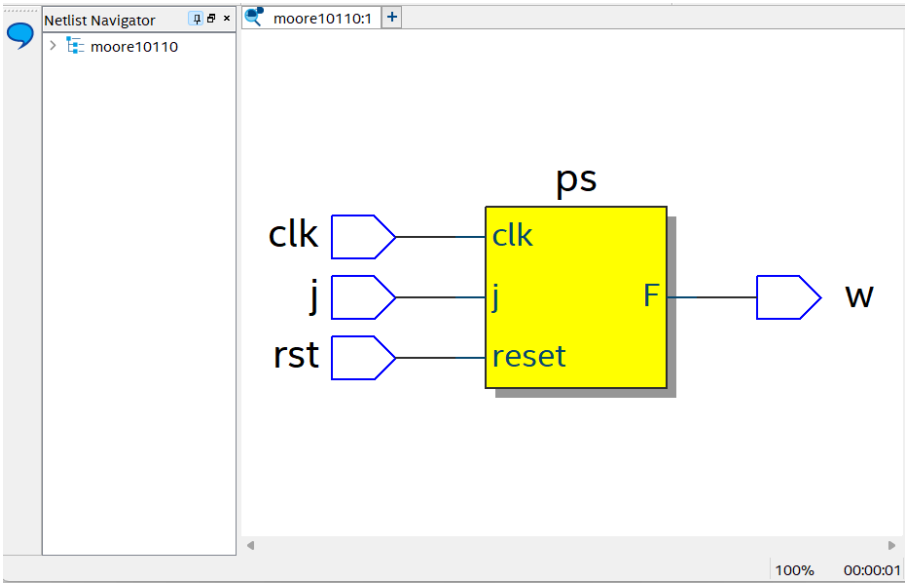
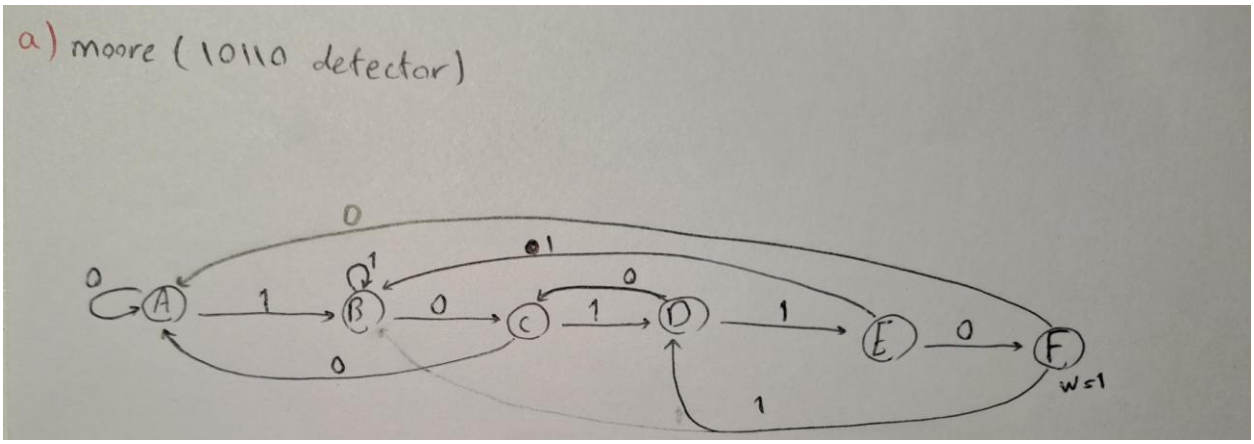
Amirali Mokhtarian CA5

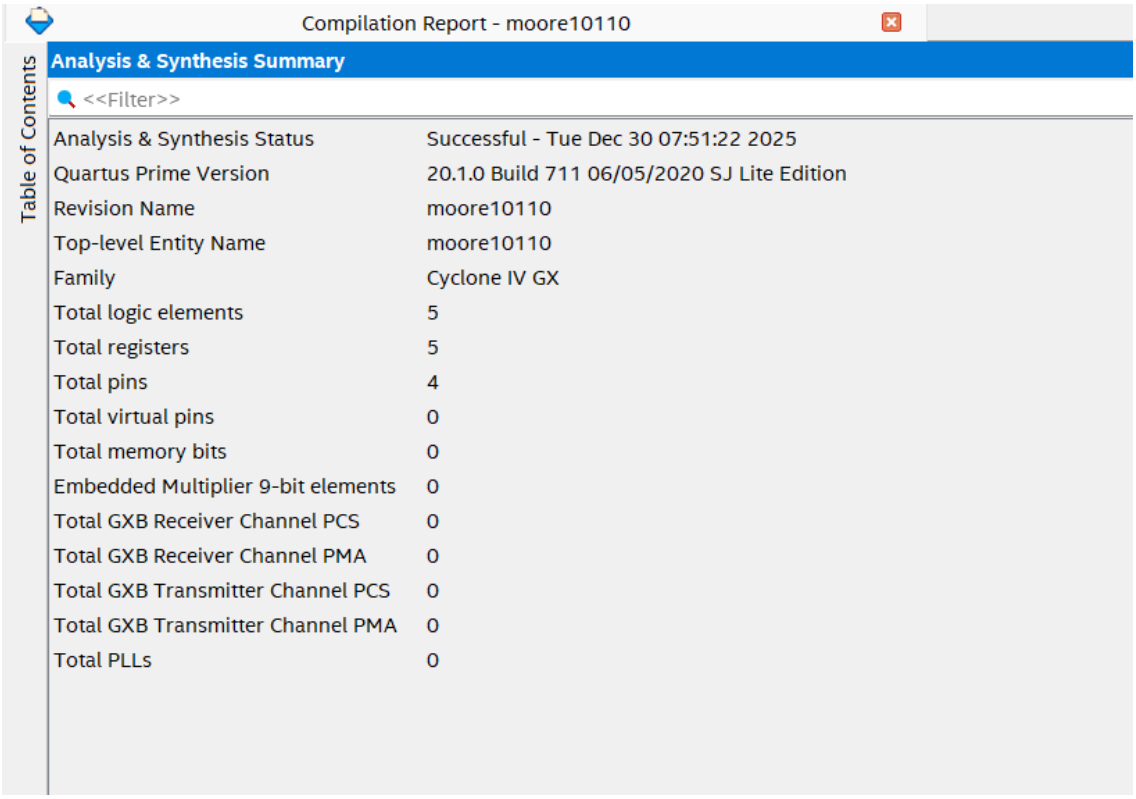
810803088

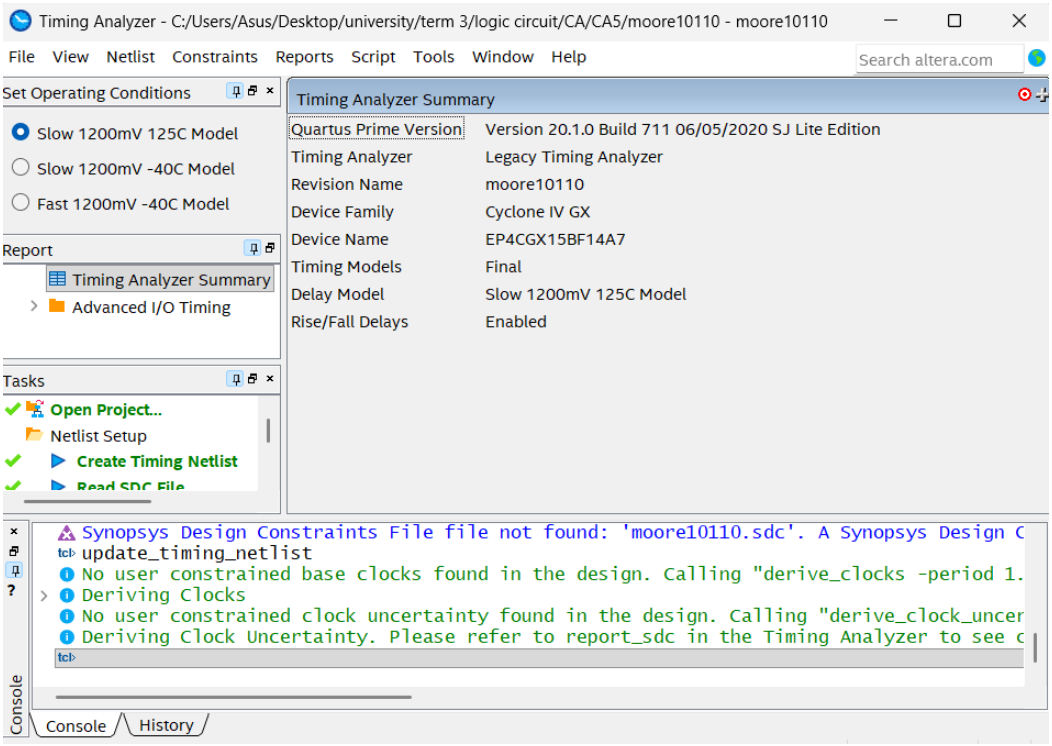
P1



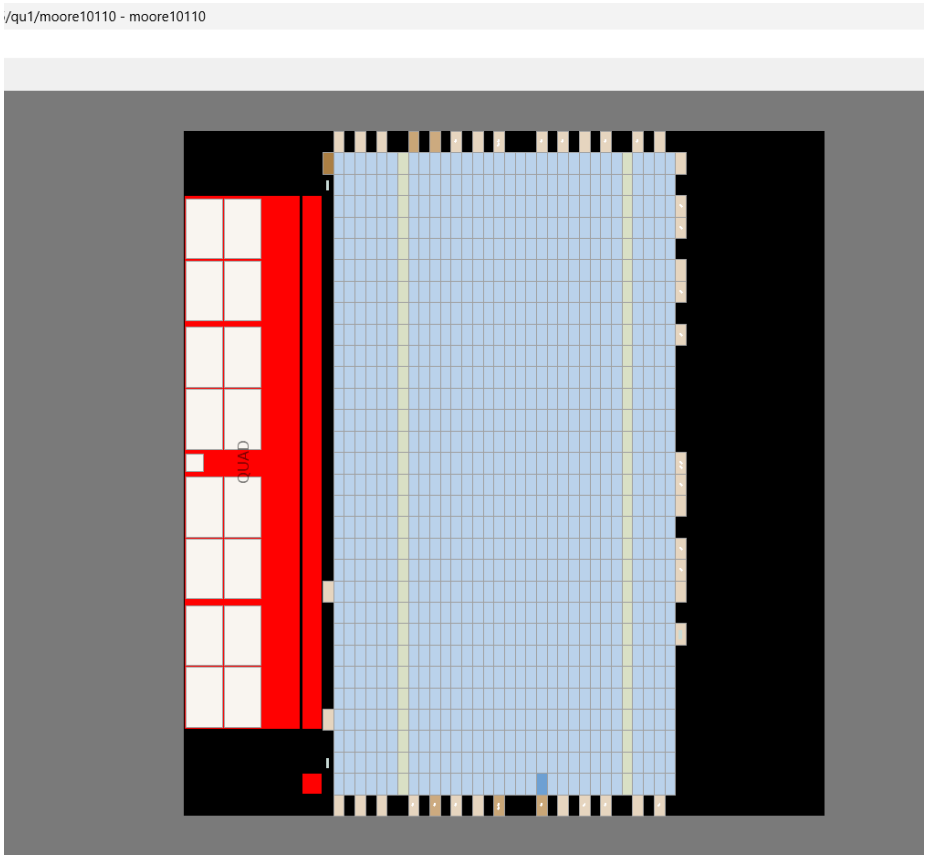


```
module moore10110 (input clk, rst, j , output w);
    reg [2:0] ns,ps;

    parameter [2:0] A=3'b000 , B=3'b001 , C=3'b010 ,
    D=3'b011, E=3'b100 , F=3'b101;

    always @(j,ps) begin
        ns=A;
        case (ps)
            A: ns= j ? B : A;
            B: ns= j ? B : C;
            C: ns= j ? D : A;
            D: ns= j ? E : C;
            E: ns= j ? B : F;
            F: ns= j ? D : A;
            default: ns=A;
        endcase
    end

     assign w = (ps==F) ? 1'b1 : 1'b0;

     always @(posedge clk , posedge rst) begin
        if(rst) ps<=3'b000;
        else ps<=ns;
     end
endmodule
```

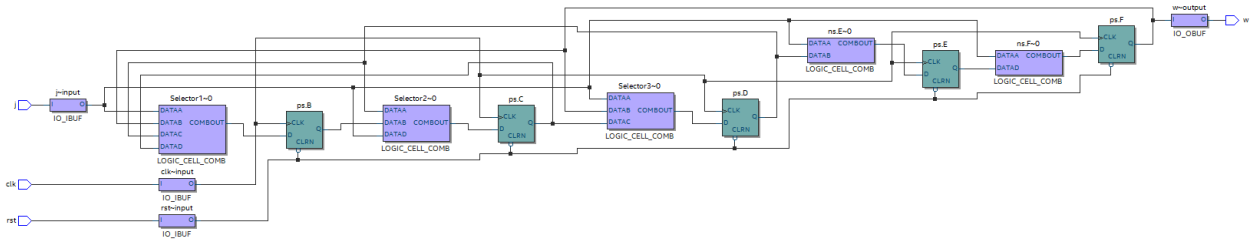

Compilation Report - moore10110
Table of Contents
Analysis & Synthesis Summary
<<Filter>>
Analysis & Synthesis Status | Successful - Tue Dec 30 07:51:22 2025
Quartus Prime Version | 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name | moore10110
Top-level Entity Name | moore10110
Family | Cyclone IV GX
Total logic elements | 5
Total registers | 5
Total pins | 4
Total virtual pins | 0
Total memory bits | 0
Embedded Multiplier 9-bit elements | 0
Total GXB Receiver Channel PCS | 0
Total GXB Receiver Channel PMA | 0
Total GXB Transmitter Channel PCS | 0
Total GXB Transmitter Channel PMA | 0
Total PLLs | 0


Timing Analyzer - C:/Users/Asus/Desktop/university/term 3/logic circuit/CA/CA5/moore10110 - moore10110
File View Netlist Constraints Reports Script Tools Window Help
Search altera.com
Set Operating Conditions
Slow 1200mV 125C Model
Slow 1200mV -40C Model
Fast 1200mV -40C Model
Report
Timing Analyzer Summary
Advanced I/O Timing
Tasks
Open Project...
Netlist Setup
Create Timing Netlist
Timing Analyzer Summary
Quartus Prime Version | Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Timing Analyzer | Legacy Timing Analyzer
Revision Name | moore10110
Device Family | Cyclone IV GX
Device Name | EP4CGX15BF14A7
Timing Models | Final
Delay Model | Slow 1200mV 125C Model
Rise/Fall Delays | Enabled
Synopsys Design Constraints File file not found: 'moore10110.sdc'. A Synopsys Design C
update_timing_netlist
No user constrained base clocks found in the design. Calling "derive_clocks -period 1.
Deriving Clocks
No user constrained clock uncertainty found in the design. Calling "derive_clock_uncer
Deriving Clock Uncertainty. Please refer to report_sdc in the Timing Analyzer to see c
Console
Console History

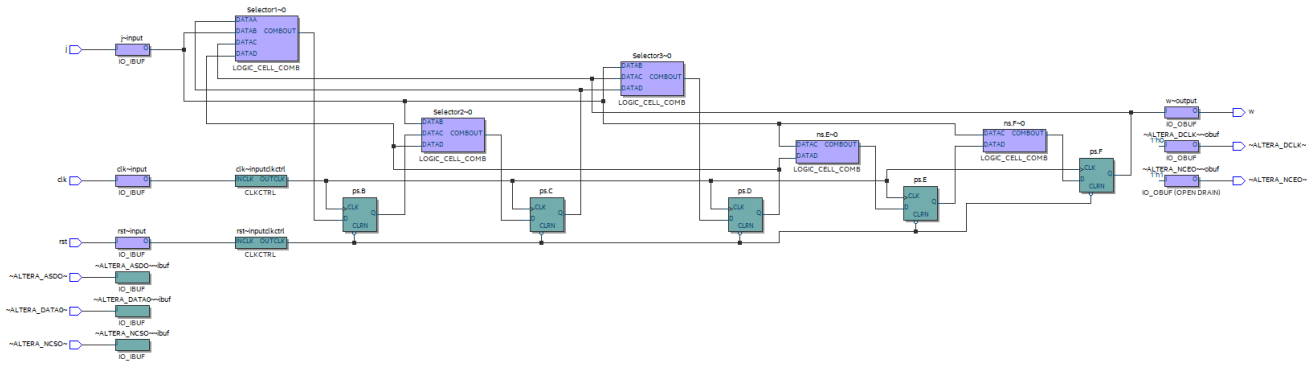
Floorplan



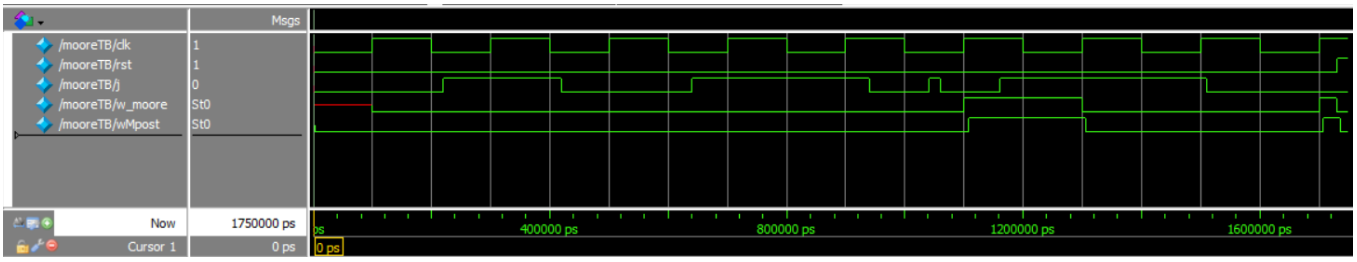
Post mapping

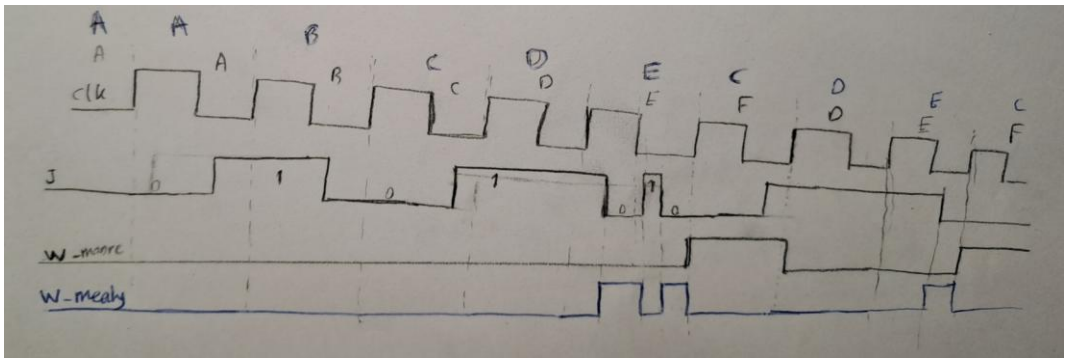


Post fitting

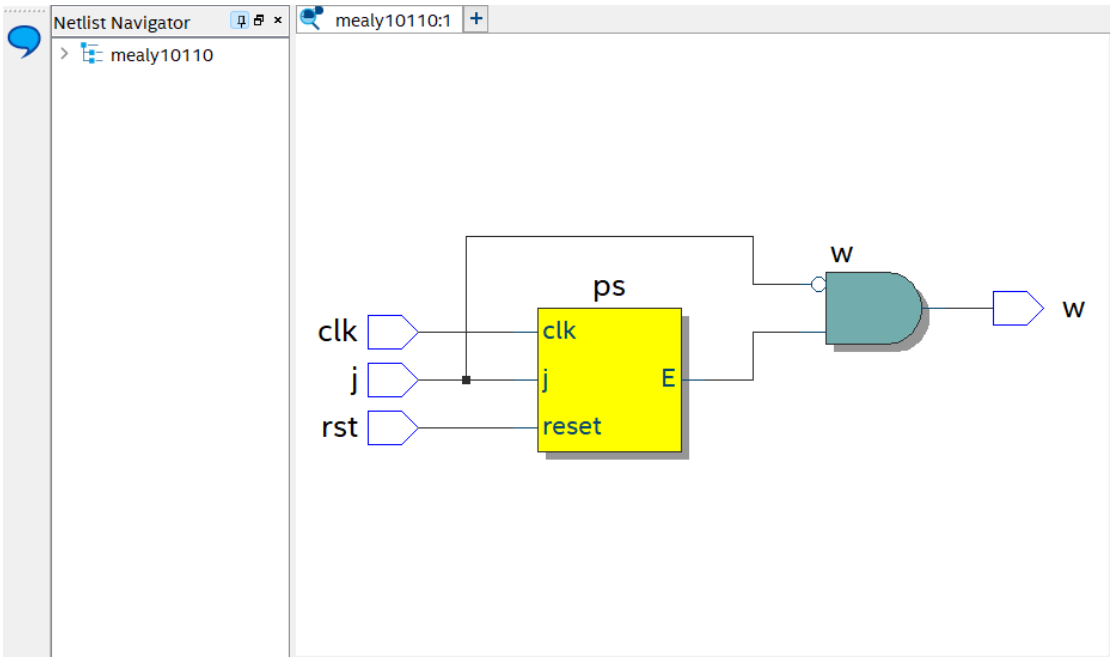


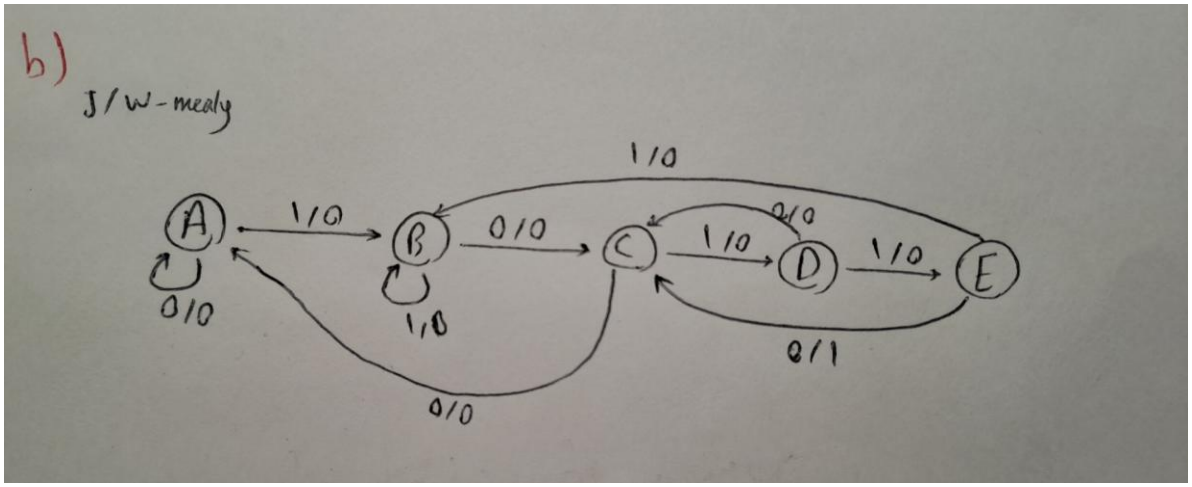
Waveforms of pre&post synthesize moore machine



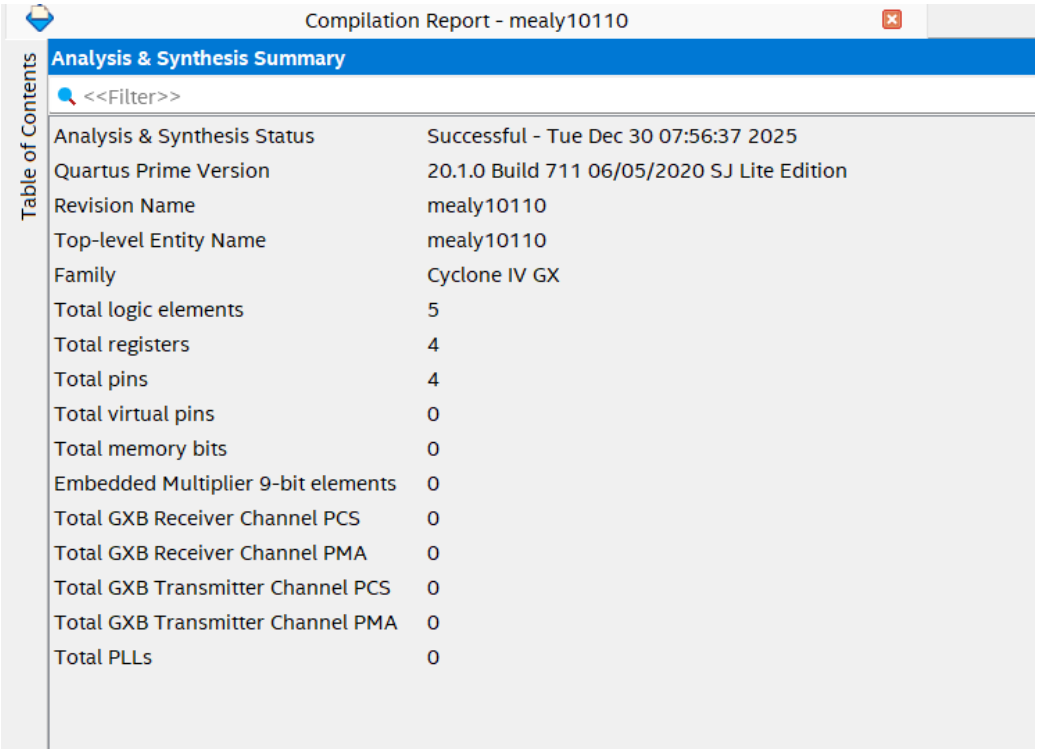


P2

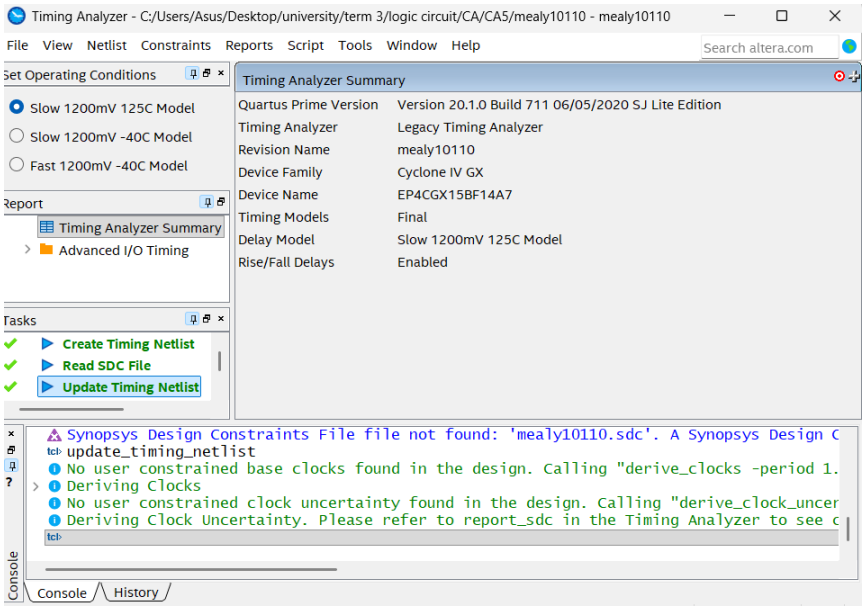

Netlist Navigator
mealy10110
mealy10110:1
ps
clk
j
rst
E
reset
w
w


b)
J/W - mealy
A
B
C
D
E
1/0
0/0
0/1

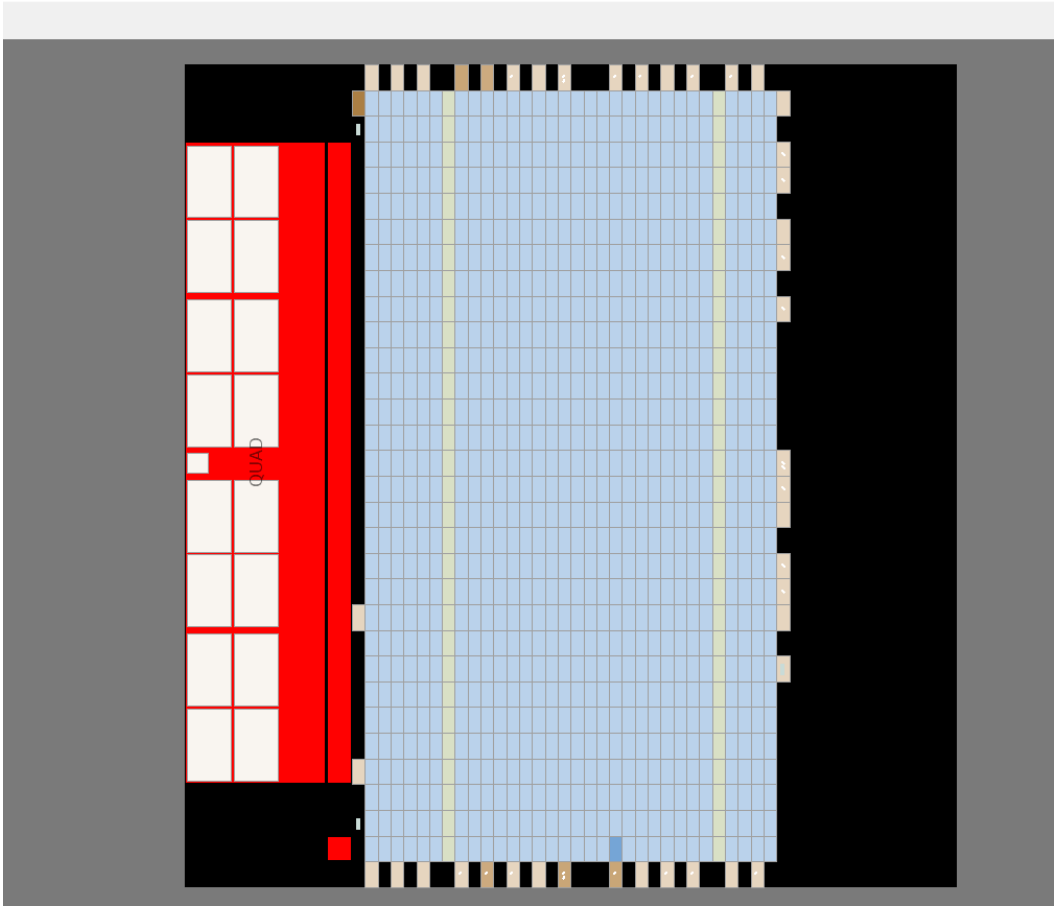
```
module mealy10110(input clk, rst, j , output w);
    reg [2:0]ns,ps;
    parameter [2:0] A=3'b000, B=3'b001, C=3'b010,
    D=3'b011 , E=3'b100;

    always @(ps, j) begin
        ns=A;
        case (ps)
            A: ns= j ? B : A;
            B: ns= j ? B : C;
            C: ns= j ? D : A;
            D: ns= j ? E : C;
            E: ns= j ? B : C;
            default: ns=A;
        endcase
    end

    assign w = (ps==E && j==1'b0) ? 1'b1 : 1'b0;

    always @(posedge clk, posedge rst) begin
        if(rst) ps<=A;
        else ps<=ns;
    end

endmodule
```



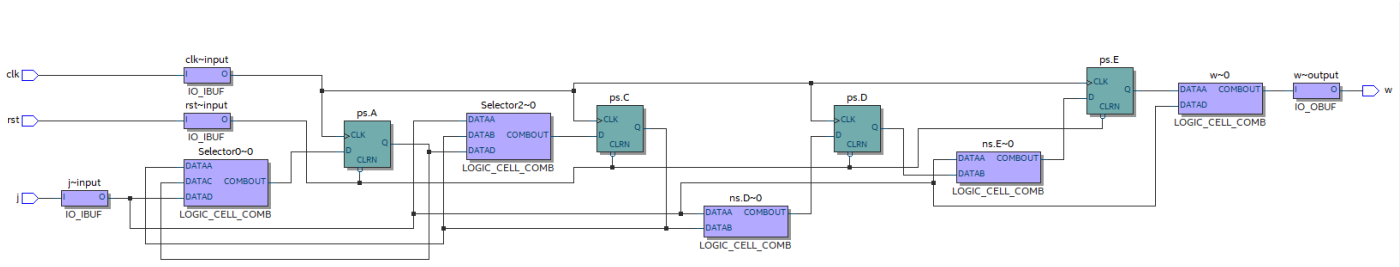
As we can see the Mealy machine uses four registers while the Moore machine uses five. This is because a Moore machine requires an additional state to represent the detection of the sequence, since its output depends only on the current state. In contrast, the Mealy machine output depends on both the present state and the current input. Therefore, instead of the last register in moore we can use an AND gate between the state condition and the input.



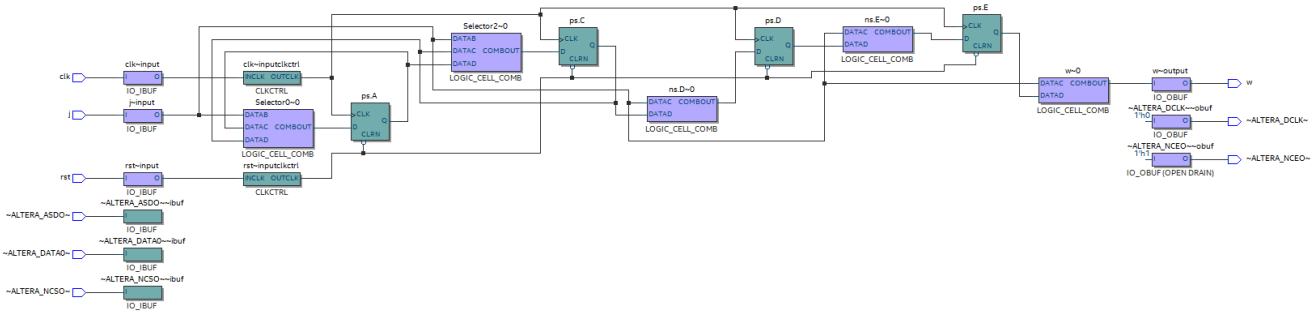
/qu2/mealy10110 - mealy10110



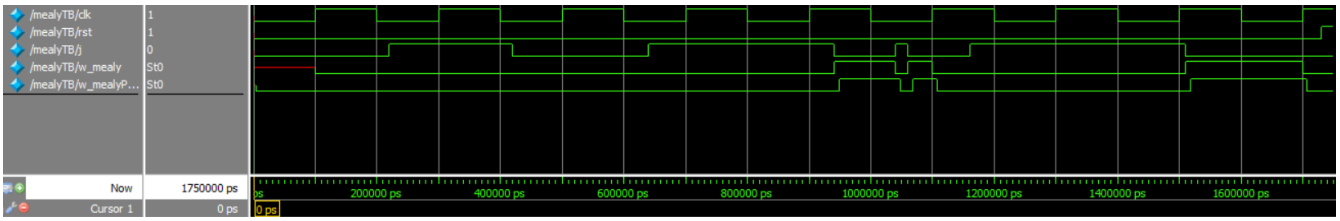
Post mapping



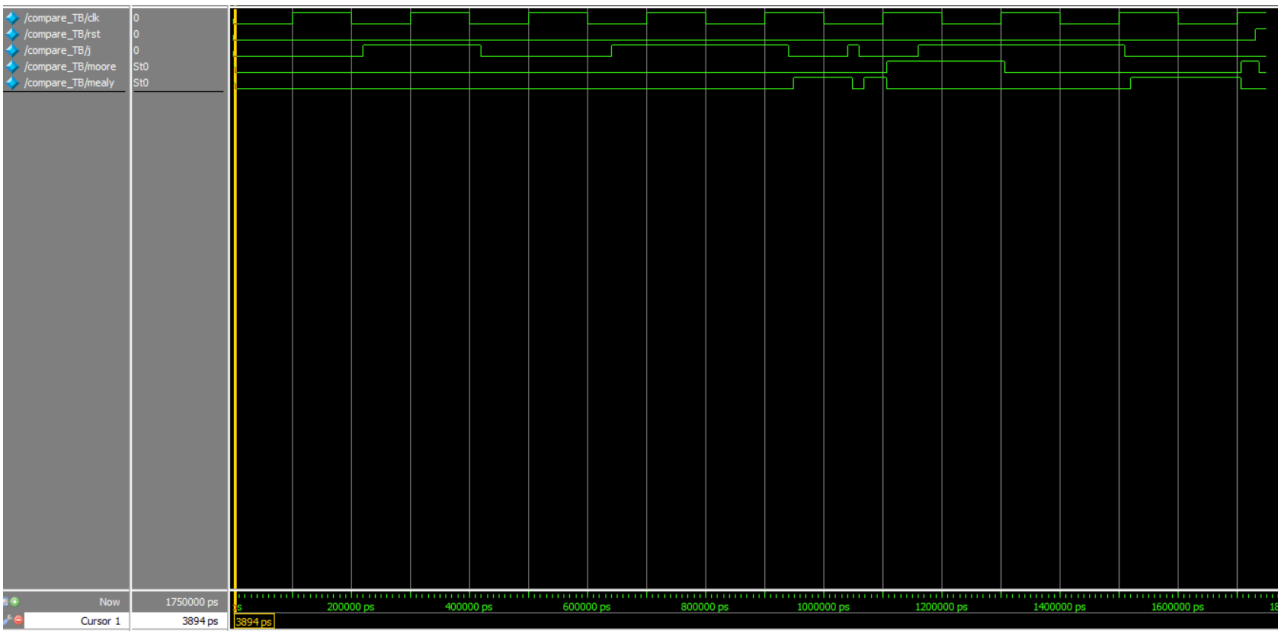
Post fitting



Waveforms of pre&post synthesize mealy machine



P3


/compare_TB/clk
/compare_TB/rst
/compare_TB/j
/compare_TB/moore
/compare_TB/mealy
0
0
0
St0
St0
Now
1750000 ps
Cursor 1
3894 ps
200000 ps
400000 ps
600000 ps
800000 ps
1000000 ps
1200000 ps
1400000 ps
1600000 ps
3894 ps

Testbench (which apply to all parts)

```
`timescale 1ns/1ns
module compare_TB ();
    reg clk, rst, j;
    wire moore,mealy;
    moore10110_post instant(.clk(clk) , .rst(rst) , .j(j) , .w(moore));
    mealy10110_post instantt(.clk(clk) , .rst(rst) , .j(j) , .w(mealy));
    initial begin
        clk=1'b0; #100;
        forever begin
            clk = ~clk; #100;
        end
    end

    initial begin
       rst = 1'b0;
       j=1'b0; #220;
       j=1'b1; #200;
       j=1'b0; #220;
       j=1'b1; #300;
       j=1'b0; #100;
       j=1'b1; #20;//for mealy
       j=1'b0; #100;
       j=1'b1; #350;
       j=1'b0; #220;
       rst=1'b1; #20;
       $finish;
    end
endmodule
```