

SHIH-HAO TSENG

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EDUCATION

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- Cornell University (CU)**, Ithaca, NY, U.S.A. Aug. 2013 - Dec. 2018
PhD in Electrical and Computer Engineering (Advisor: Dr. A. Tang)
- Relevant Coursework:
Practicum in Operating Systems, Advanced Computer Networking, Approximation Algorithm, Convex Analysis, Functional Analysis, Statistical Inference and Decision, Stochastic Systems: Estimation and Control.
- National Taiwan University (NTU)**, Taipei, Taiwan Sept. 2008 - June 2012
Bachelor of Science in Engineering (minor in Economics)
- GPA: 92.20/100.00; ranking 2nd in a class of 226

RESEARCH INTERESTS

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- Networked systems, in-network processing, edge computing, Internet of Things, scheduling algorithms.
 - Control theory, deployment architecture, controller synthesis, stability and optimization.
 - Network simulation and emulation, controller performance evaluation.

SELECTED PUBLICATIONS

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- **S.-H. Tseng**, S. Agarwal, R. Agarwal, H. Ballani, and A. Tang, “Inter-Datacenter Bulk Transfers with Coded-Bulk,” in *Proc. USENIX NSDI*, 2021.
 - **S.-H. Tseng** and J. Anderson, “Deployment Architectures for Cyber-Physical Control Systems,” in *Proc. IEEE ACC*, 2020.
 - **S.-H. Tseng**, A. Tang, G. Choudury, and S. Tse, “Routing Stability in Hybrid Software-Defined Networks,” in *IEEE/ACM Trans. Netw.*, 2019.
 - **S.-H. Tseng**, “Perseverance-Aware Traffic Engineering in Rate-Adaptive Networks with Reconfiguration Delay,” in *Proc. IEEE ICNP*, 2019.
 - **S.-H. Tseng**, B. Bai, and J. C. S. Lui, “Hybrid Circuit/Packet Network Scheduling with Multiple Composite Paths,” in *Proc. IEEE INFOCOM*, 2018.
 - **S.-H. Tseng**, E. Bitar, and A. Tang, “Random Convex Approximations of Ambiguous Chance Constrained Programs,” in *Proc. IEEE CDC*, 2016.
 - A. Gushchin, **S.-H. Tseng**, and A. Tang, “Optimization-Based Network Flow Deadline Scheduling,” in *Proc. IEEE ICNP*, 2016.

EXPERIENCE

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- California Institute of Technology**, Pasadena, CA, U.S.A. Oct. 2018 - Present
Postdoctoral Scholar Research Associate
- Lead the project of freshness-driven network control.
 - Mentor graduate students on parallel model predictive control and formal test-case generation.
 - Derived realization-stability lemma that unifies existing controller synthesis methods.
 - Investigated the controller deployment architecture for cyber-physical systems.
- Cornell University**, Ithaca, NY, U.S.A. Aug. 2014 - Aug. 2018
Graduate Research Assistant/Teaching Assistant
- Built CodedBulk to boost the throughput of inter-datacenter bulk transfers using network coding.
 - Studied time-aware network management under software-defined networking.
 - Helped teach Introduction to Probability and Inference for Random Signals and Systems.
- The Chinese University of Hong Kong**, Shatin, NT, Hong Kong June 2017 - Aug. 2017
Research Assistant
- Developed efficient scheduling algorithms for hybrid packet/circuit networks.
- AT&T**, Middletown, NJ, U.S.A. June 2016 - Aug. 2016
Student Intern - Technical II
- Developed routing algorithms to stabilize carrier-grade hybrid software-defined networks.

SKILLS

Programming Languages: Proficient in C++, Python and Verilog.

Programming Skills: Working knowledge of linux based C++ socket and multithreaded programming.

Simulation Tools: Proficient in PSpice, MATLAB, and NS-3.

Languages: Fluent in English; native in Mandarin Chinese and Taiwanese Hokkien.

HONORS AND AWARDS

Winner of the AT&T SDN Network Design Challenge 2016

- Awarded to the top team providing the most efficient and cost effective routing solution to carrier-grade networks.

Jacobs Fellowship (CU) 2014

Studying Abroad Scholarship (Ministry of Education, Taiwan(R.O.C.)) 2013

Honorary Member of the Phi Tau Phi Scholastic Honor Society 2012

- Presented to seniors from each college in Taiwan ranking within top 1% of their department.

President's Awards (NTU) 2009, 2010, 2011, 2012

- Four-time recipient; awarded to students ranking within top 5% of their department.

Outstanding Project Award 2011

- Awarded to the top 10 teams of Cross-Strait Finals of 2011 Innovate Asia Competition (FPGA design).